LAB 6

1. Design a combinational circuit that multiplies two signals A and B (4-bit each).

2. Design a 8 x 4 memory with asynchronous read. Ports are CLK (Clock), WE (write enable), DIN (Data input), Dout (Data output), W_ADDR (Write address), R_ADDR (Read address).

3. Design a 4 x 8 memory with asynchronous read and Output Enable (OE). Output is available when OE='1' and set to "00000000" when OE='0'.

4. Design a 4 x 5 memory with synchronous read. Ports are CLK (Clock), WE (Write enable), ADDR (Address), DIN (Data input) and Dout (Data output).

5. Design a 8 x 5 bidirectional memory with asynchronous read. Ports are CLK (Clock), WE/RE (Write / Read enable), ADDR (Address) and DIN/DOUT (Data in / Data out).

6. Design a 6 x 3 memory with synchronous read. Ports are CLK (Clock), Write Enable (WE), Output Enable (OE), Write address/Read address1 (WADDR/RADDR1), Read address 2 (RADDR2), Data in (DIN), Data out 1 (DOUT1) and Data out 2 (DOUT2).