LAB 4

1. Design (8x1) multiplexer using process.

2. Multiplexer(4 x 1) using Tri-state buffer
   (i) 6 Tri-State Buffers.
   (ii) 8 Tri-State Buffers.

3. Design the following counters and demonstrate their use in frequency divider
   (i) MOD 5 Counter
   (ii) MOD 7 Counter

4. Design 4-bit counter with asynchronous reset and Synchronous Load

5. Design a 4-bit Up/Down counter with asynchronous reset. Use assert statement to ensure that two consecutive count differs by 1.

6. Design a 5-bit even counter with asynchronous reset and synchronous load. If counter is loaded with invalid data, it should go to "00000". Use assert statement to make sure that counter is coming back to valid state if loaded with invalid state.

7. Design a Sequence generator that generates sequence 01101001. The order of output is from right to left (i.e. first bit is '1', second is '0', third is '0' and so on). The circuit should be capable of repeating this sequence. Make sure that your design is not going into unstable state if reset is pressed.

8. Design a Sequence generator that generates sequence 1010011011. The order of output is from right to left (i.e. first bit is '1', second is '1', third is '0' and so on). The circuit should be capable of repeating this sequence. Make sure that your design is not going into unstable state if reset is pressed.