LAB 3

1. 8 x 3 Priority Encoder using concurrent statements

2. Use concept of array and with select statement to design ROM which implements the

    following functions:

    F1= A'BC + AB + A'BC'
    F2= ABC' + A'B'C' + A'C
    F3= ABC + AB'C' + A'B'C
    F4= AB + BC + CA

3. Design a T latch using
    (i) Concurrent Statement
    (ii) Sequential Statements
    Note: First design without any delay and simulate design (Identify the problem) then
    add delay of 3ns and verify the simulation results

4. Design D Flip Flop with
    (i) Asynchronous Reset
    (ii) Synchronous Reset
    (iii) Asynchronous Reset and Preset.
    (iv) Asynchronous Reset and Preset with Enable.

5. Ring Counter (6-bits) using Schematic. Verify following frequency dividers f/6, f/3
    and **f/2** using concept of generic.