LAB 7

1. Design a sequence detector for 1101 using
   (i) Mealy Non Overlapping
   (ii) Mealy Overlapping

2. Design a sequence detector for 11011 using
   (i) Moore Non Overlapping
   (ii) Moore Overlapping

3. Design a Traffic Light controller using state machine. Inputs of traffic light controller are reset and Pass. Outputs are Red, Yellow and Green.

   The controller follows the following steps
   1. Initially Red Light is ON.
   2. Red and Yellow both are ON.
   3. Only Green is ON.
   4. Green and Yellow both are ON.
   5. Returns to 1 step.

   When pass button is pressed, green light turns on irrespective of the current state.

4. Design ALU which accepts two inputs A and B each of 4-bit. One input cin of 1-bit, 5-bit output Y and selection lines for selecting one out of many operations.

   Separate arithmetic and Logic Unit operations. Write functions for logical unit and Procedures for Arithmetic unit in a package and call them in code as per requirement.

Operations
Complement A (Y=/A)
Complement B (Y=/B)
AND (Y=AB)
OR (Y=A+B)
NAND (Y=/(AB))
NOR (Y=/(A+B))
XOR (Y=/A.B +A/B)
XNOR (Y=/A./B +AB)
Transfer A (Y= A)
Transfer B (Y= B)
Increment A (Y= A + 1)
Increment B (Y= B + 1)
Decrement A (Y= A - 1)
Decrement B (Y= B - 1)
ADD (Y= A + B)
ADD with carry (Y= A + B + Cin)

5. Use “TEXTIO” based verification to test Universal Shift Register designed in Lab 5. Inputs will be in form of strings i.e. LOAD to perform Loading operation, RSHIFT to perform right shift LSHIFT to perform Left Shift.