Lab 8

1. Design UDP for 8: 1 Multiplexer

2. Design UDP for positive edge triggered D Flip Flop with asynchronous reset (clear) and asynchronous set (preset).

3. Design a Priority resolver. The resolver receives four requests req_a, req_b, req_c, req_d and generates four grants **gnt_a**, **gnt_b**, **gnt_c**, **gnt_d**. At initial stage A has higher priority over B, B has higher priority over C and D has the least priority. Requests are sampled only if **busy** is low. At the later stages, resolver uses Least Recently Used Algorithm for generating grants based on requests received. On transcript display the devices that are generating request and the device that is provided grant.