Multilevel Paging

Consider an 8-bit logical address.

Page size = 16 bytes (ie; 4 bits). ∴ 8 - 4 = 4 bits for page no. (2^4 = 16 pages)
offset.

Let Page Table size be restricted by Page size.

Size of PTE = 4 bytes.

∴ 1st level PT

no of PTEs in one PT in 1st level = $\frac{16}{4} = 4$ entries.
(16 → Page size; 4 → size of one PTE)

∴ No of PTs in 1st level = $\frac{16}{4} = 4$
(16 → no of pages for process; 4 → no of entries in one PT)

ie; 4 PTs, each with 4 entries (in 1st level).

∴ needs 2nd level:

no of PTEs in one 2nd level PT = $\frac{16}{4} = 4$ entries.

∴ No of PTs in 2nd level = $\frac{4}{4} = 1$.
(4 → no of PTs in 1st level; 4 → no of entries in one PT)

ie; 1 PT with 4 entries in 2nd level.

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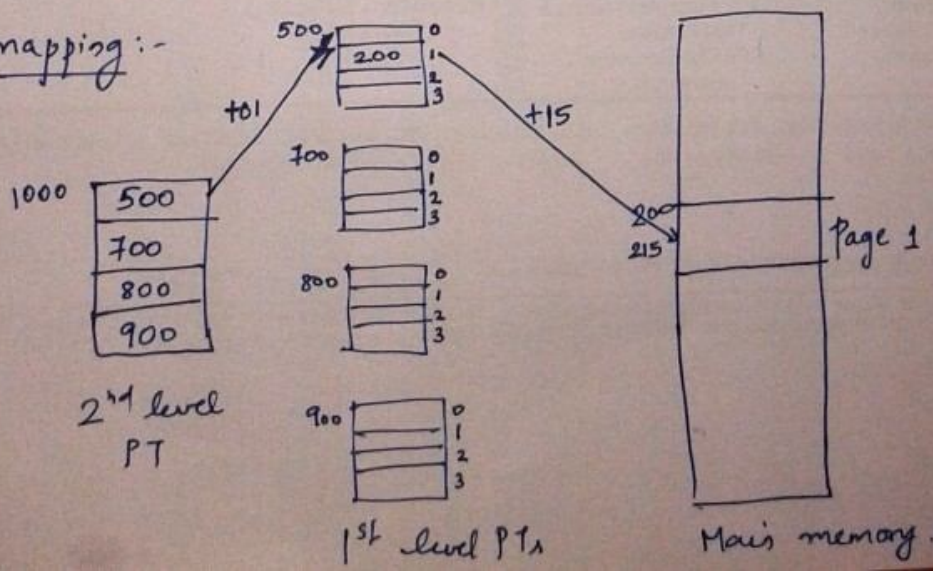
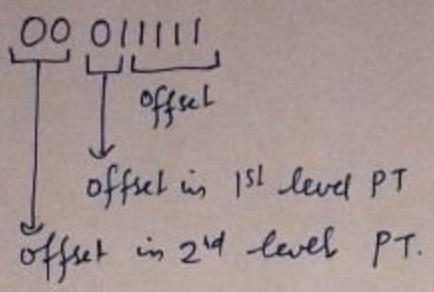
eg mapping:-



Consider a logical address



Root PT pointer (Pointer to 2nd level PT) → 1000.

1000 + 0 → 1000. (has entry 500). ie; Pointer to 1st PT in 1st level

500 + 1 → 501 (has entry 200) ie; address of Page 1 of process

200 + 15 → 215 (Word to be accessed in memory).

00011111 → 31

logical address 31 is in 31 % 16 = 1 (page 1).

page size