Platformio ASSIGNMENT

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1. Neglecting the delays due to the logic gates in the circuit shown in figure, the decimal equivalent of the binary sequence [ABCD] of initial logic states, which will not change with clock, is

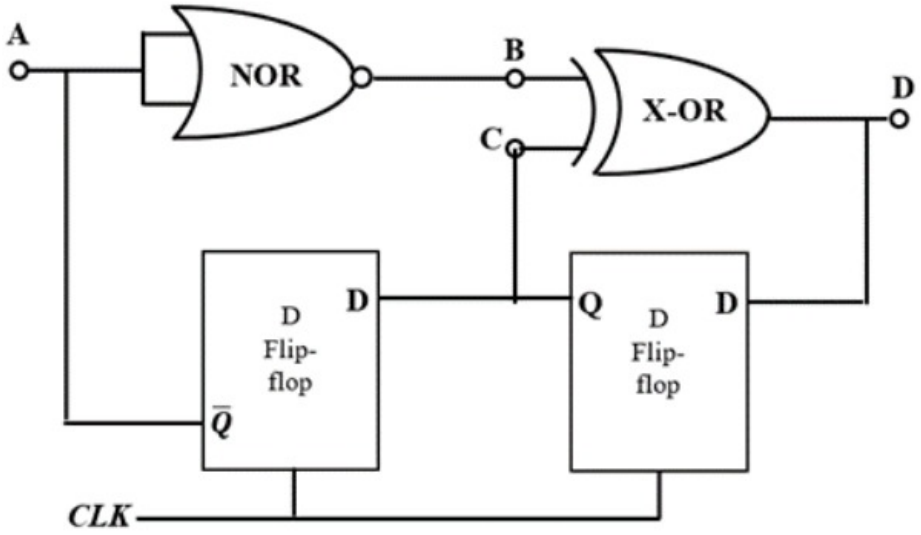

Figure 1: D-Flip-flop

Fig. 1