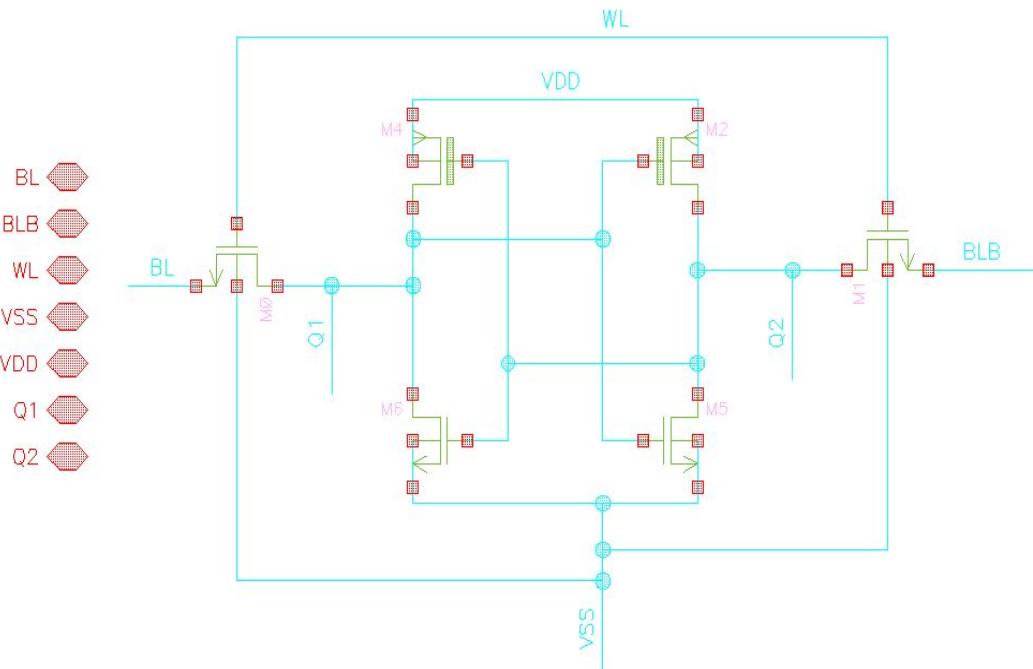


SRAM ARRAY

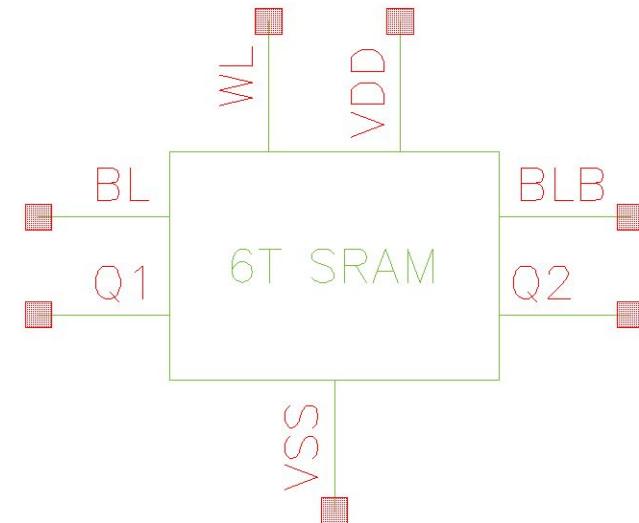
PREPARED BY: CHANDRAHAAS

6T SRAM BITCELL

Schematic

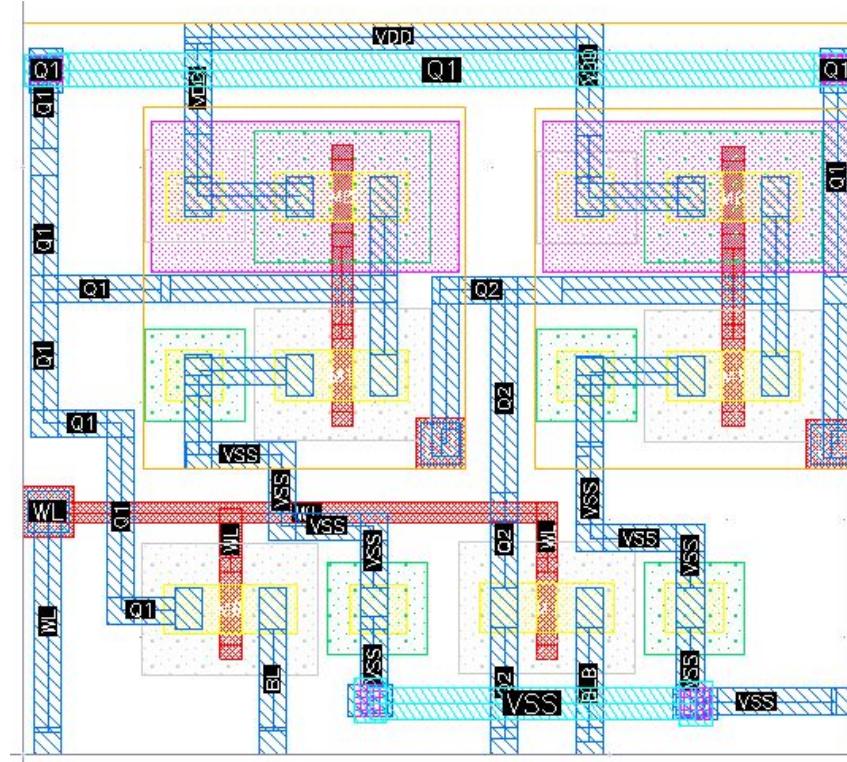


Symbol



6T SRAM BITCELL

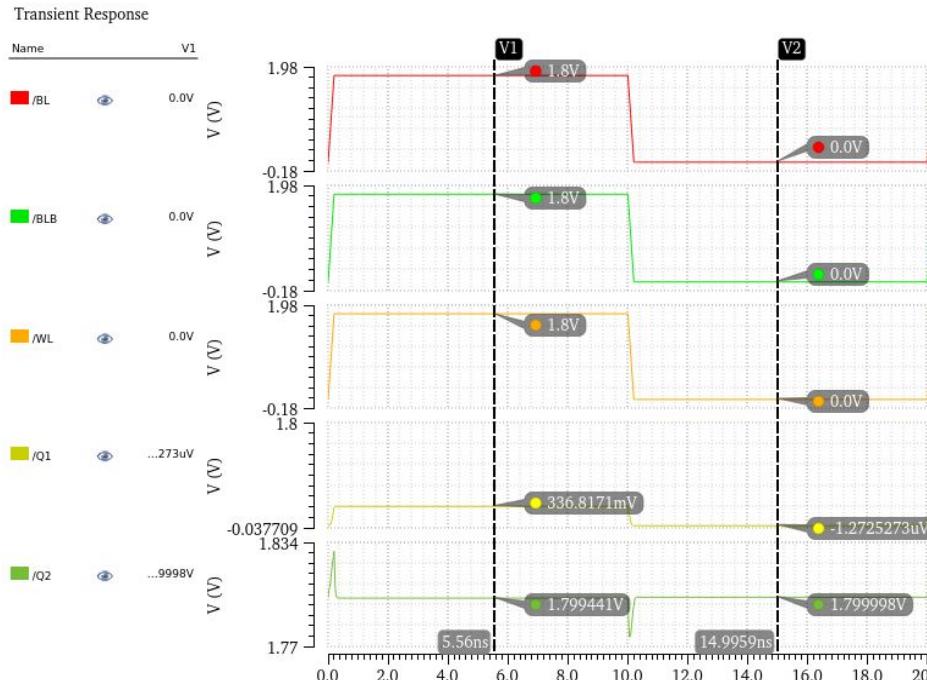
Layout



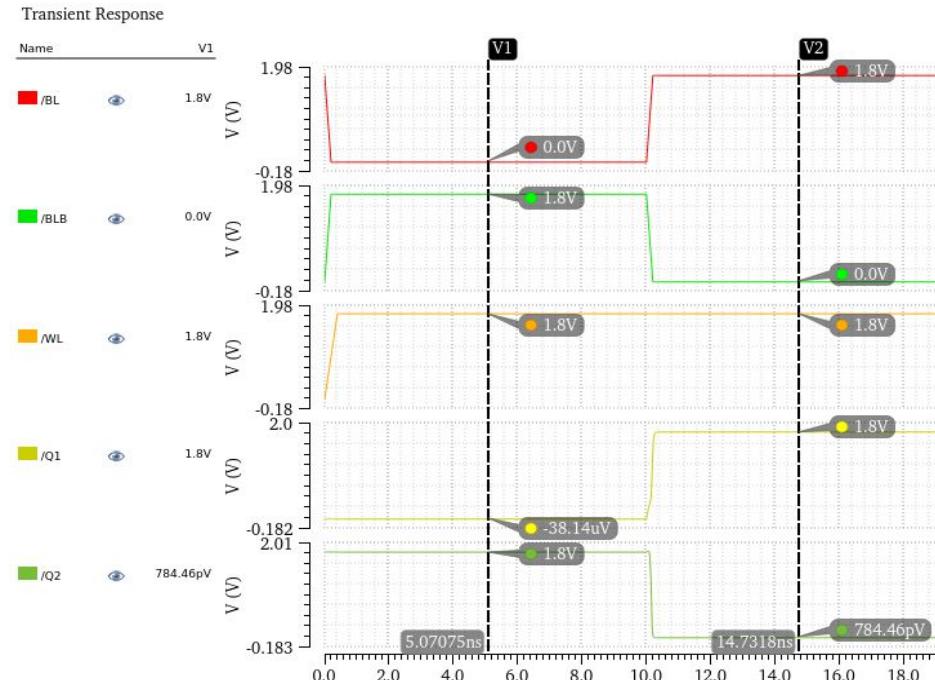
$$\begin{aligned} \text{Area} &= 6.23 \times 7.12 \\ &= 44.36 \mu\text{m}^2 \end{aligned}$$

6T SRAM BITCELL

Transient Response (READ)



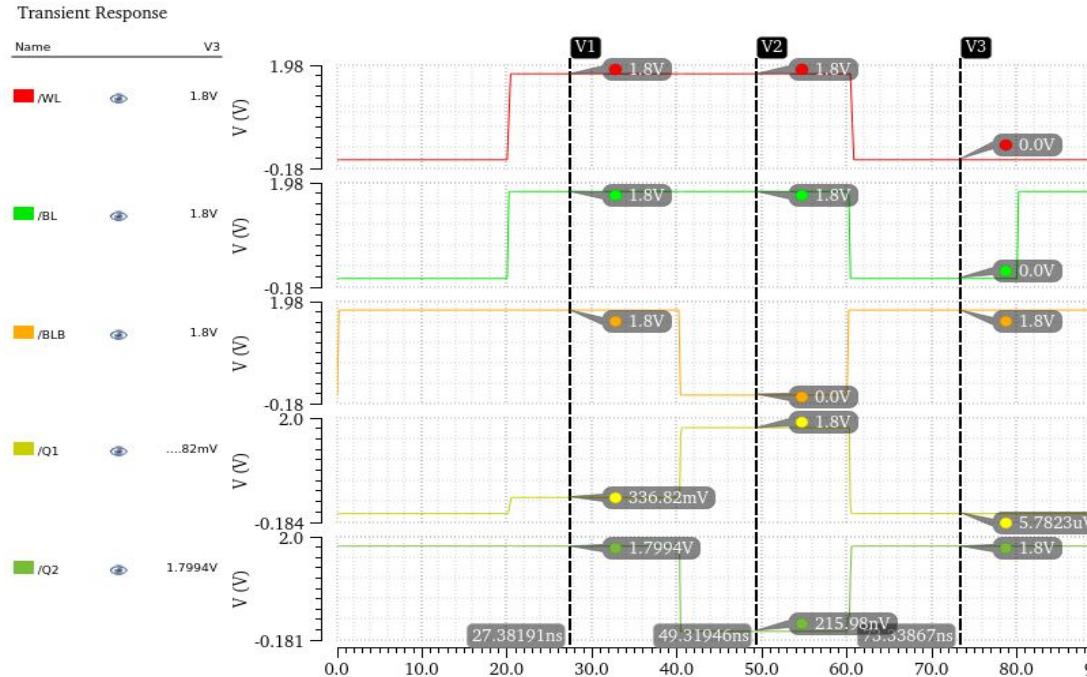
Transient Response (WRITE)



*with initial conditions (Q1=0 , Q2=1.8)

6T SRAM BITCELL

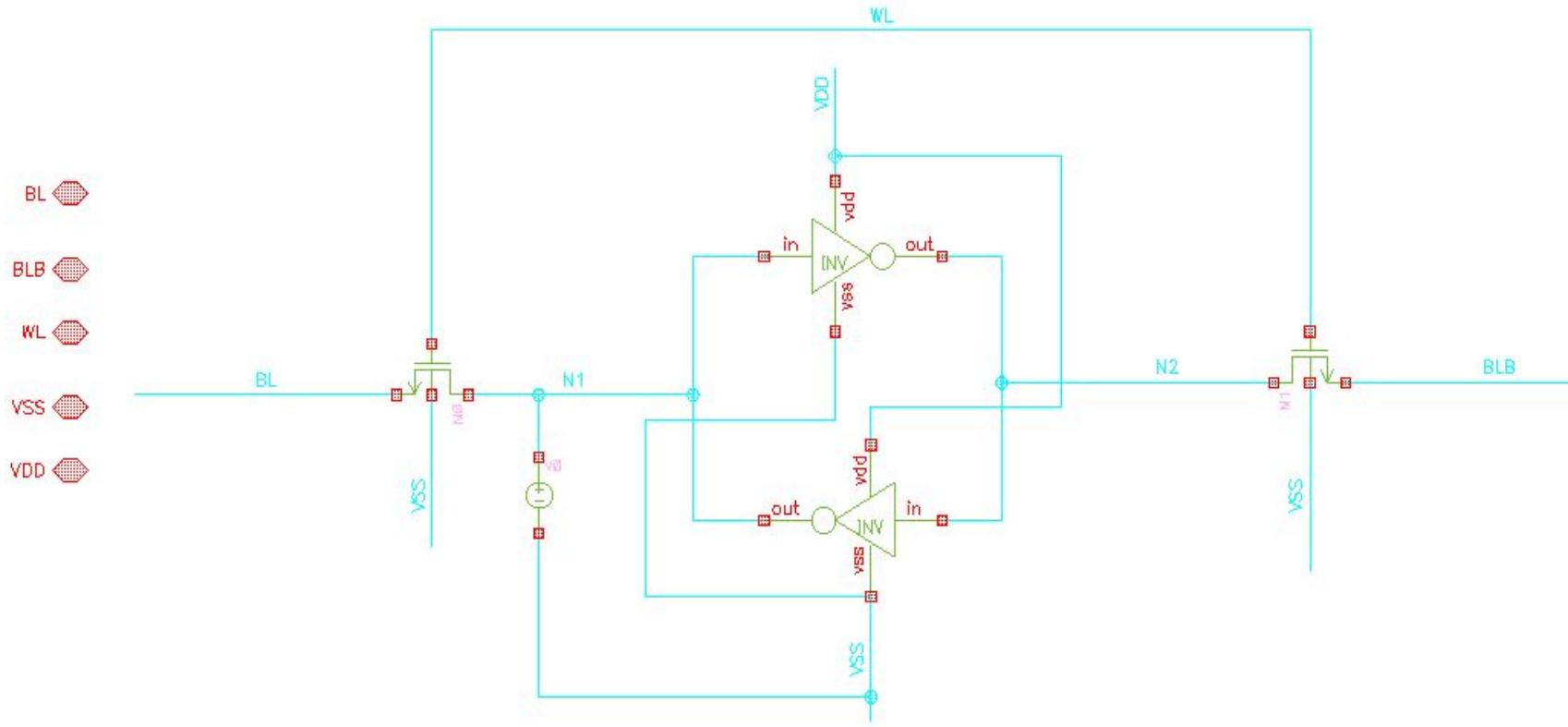
Transient Response(READ, WRITE and HOLD)



*with initial conditions (Q1=0 , Q2=1.8)

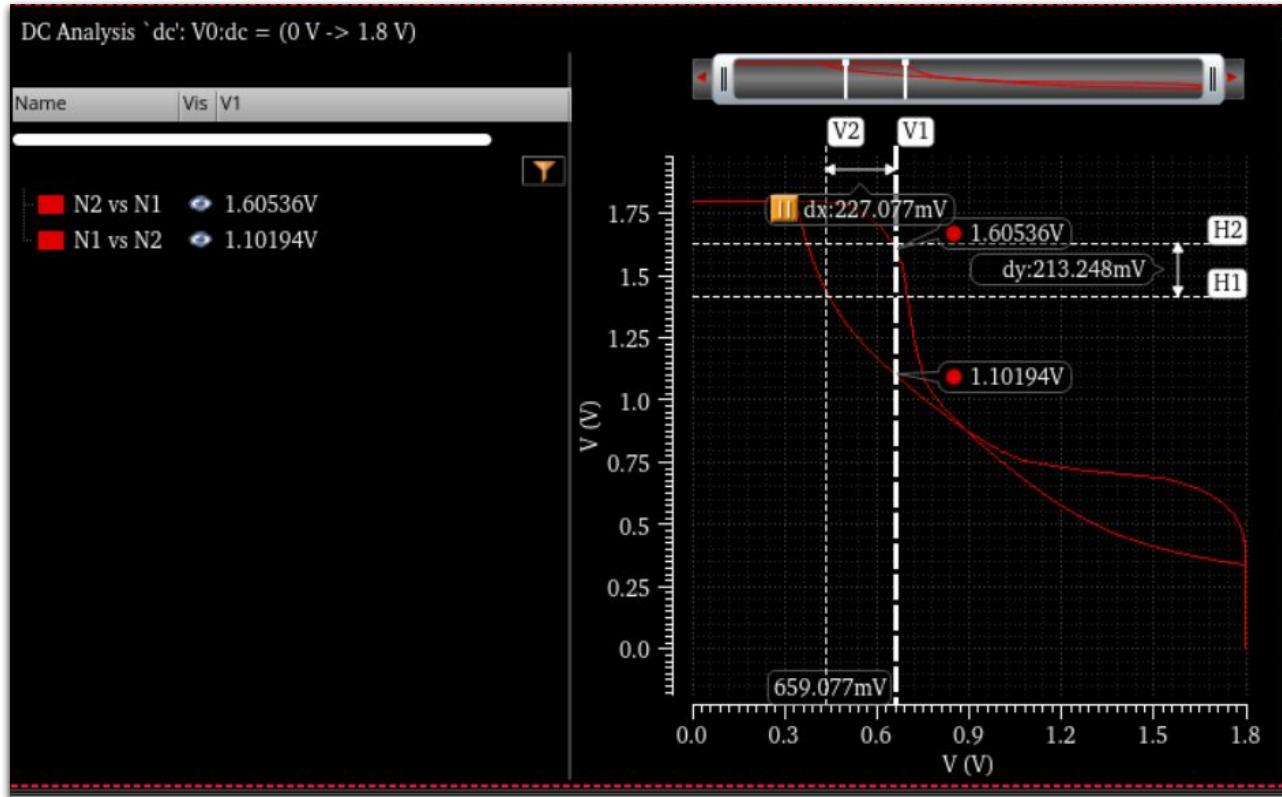
6T SRAM BITCELL

Noise Margin



6T SRAM BITCELL

Noise Margin



$$\begin{aligned}\text{Noise margin} &= 1.414 \cdot (a) \\ &= 1.414 \cdot 220 \\ &= 311.08 \text{ mV}\end{aligned}$$

where $a = \text{side of square}$

6T SRAM BITCELL

Conclusion

After trying Gated Vdd technique we got less Power Consumption but less accuracy and stability.

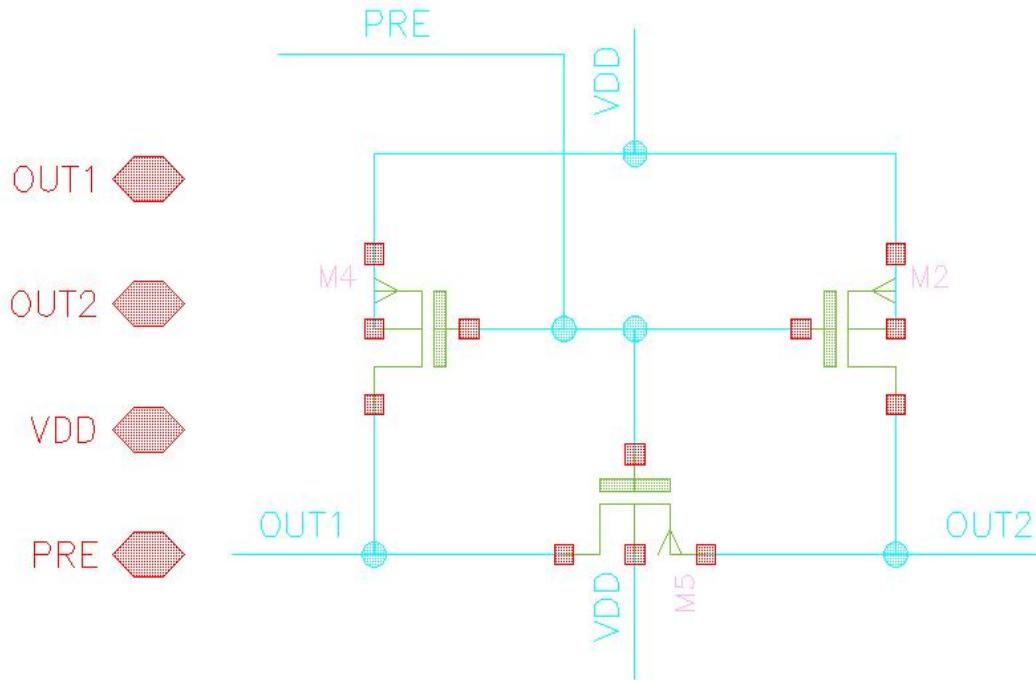
References

IEEE Paper

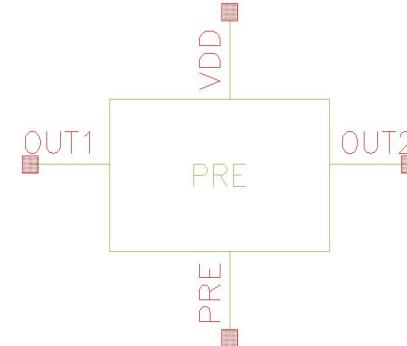
- 1) Design and Analysis of Low Power SRAM Cells Akshay Bhaskar School of Electronics Engineering
VIT University, Vellore, India

PRECHARGE

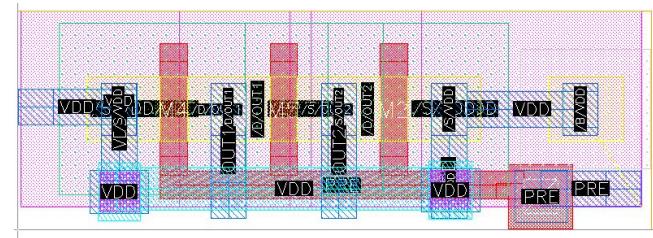
Schematic



Symbol



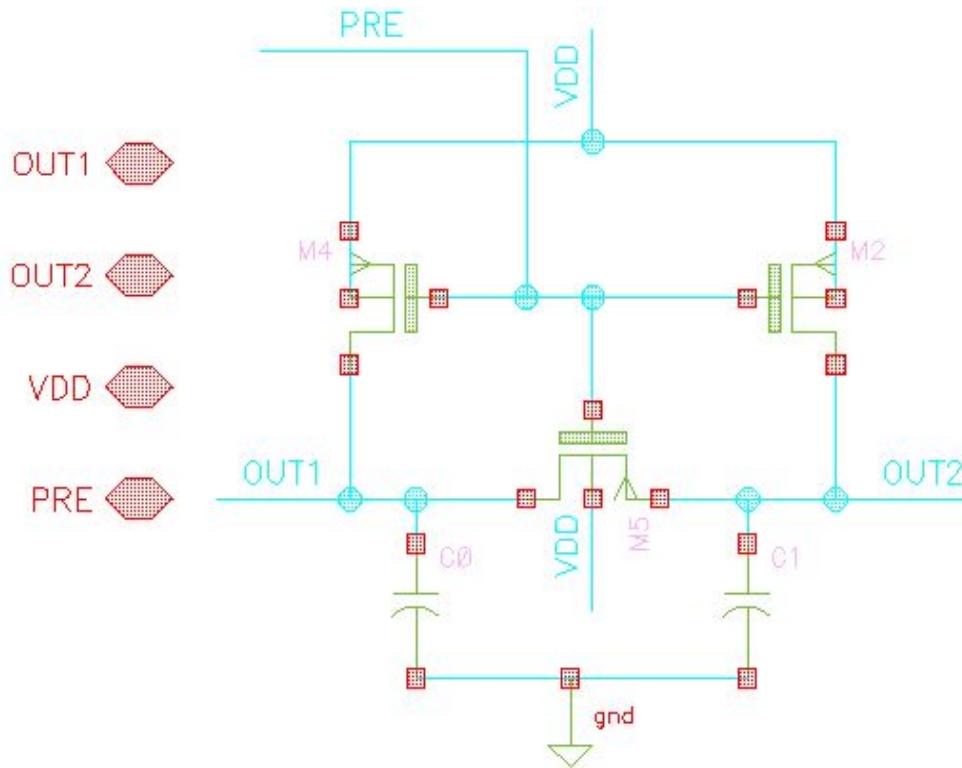
Layout



$$\text{Area} = 4.145 \times 1.425 = 5.9 \mu\text{m}^2$$

PRECHARGE (WITH CAPACITORS)

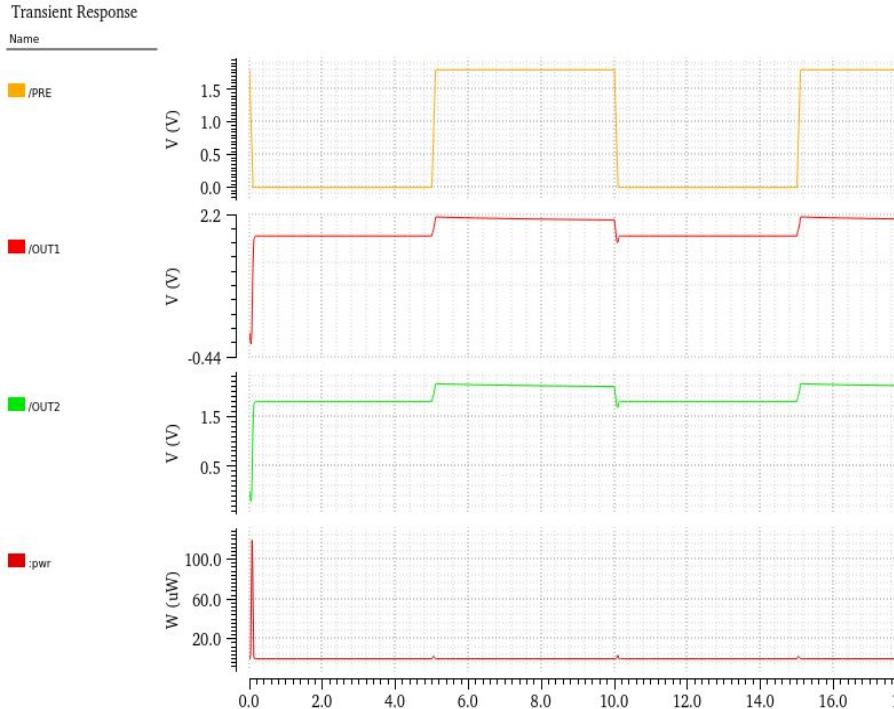
Schematic



- Adding Capacitors to the output terminals of the precharge helps to stabilize the bitline voltages around 1.8V.
- A comparison has been shown in the upcoming slide.
- Here we have used a capacitor of 20 femto Farad.

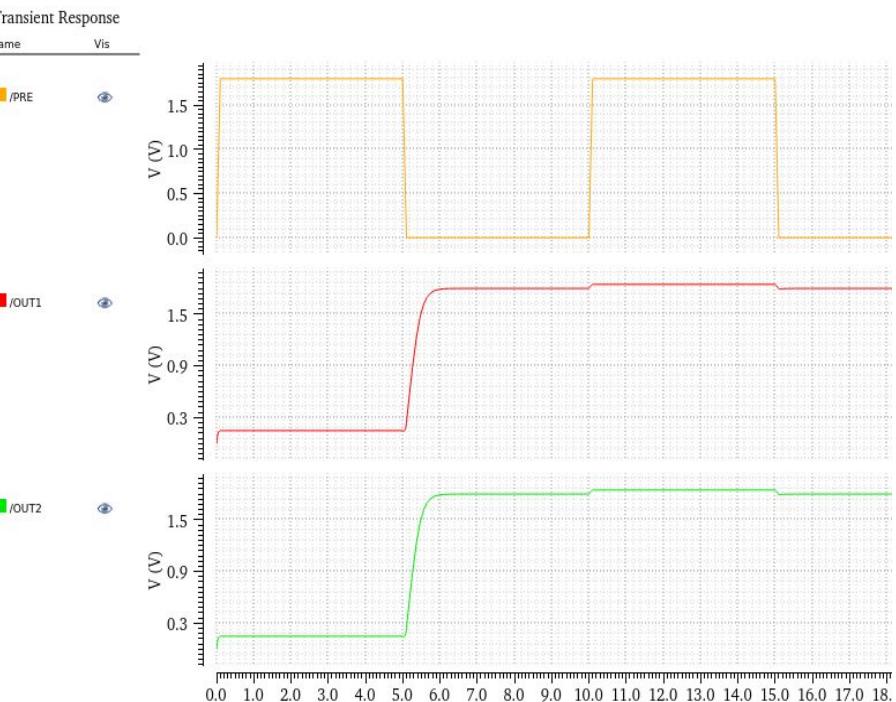
PRECHARGE (TRANSIENT RESPONSE)

Without Capacitor



Avg. Power Consumed = **0.165 uW**

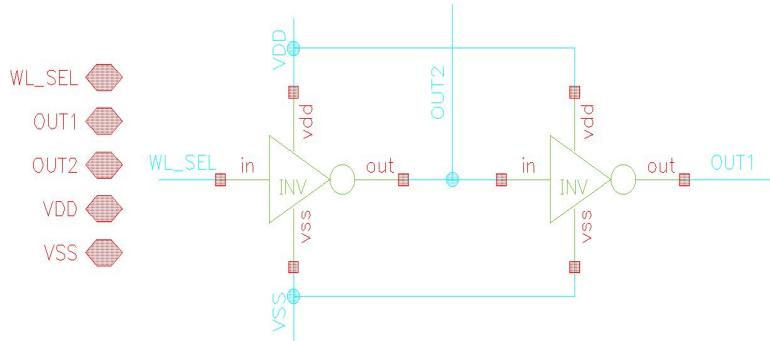
With Capacitor



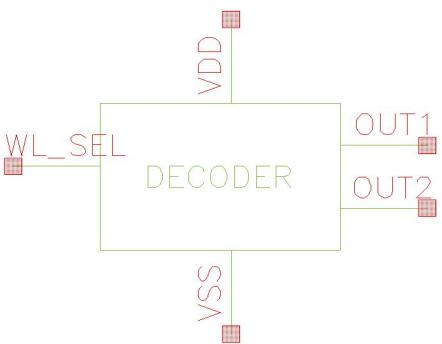
Avg. Power Consumed = **1.729 uW**

1x2 DECODER

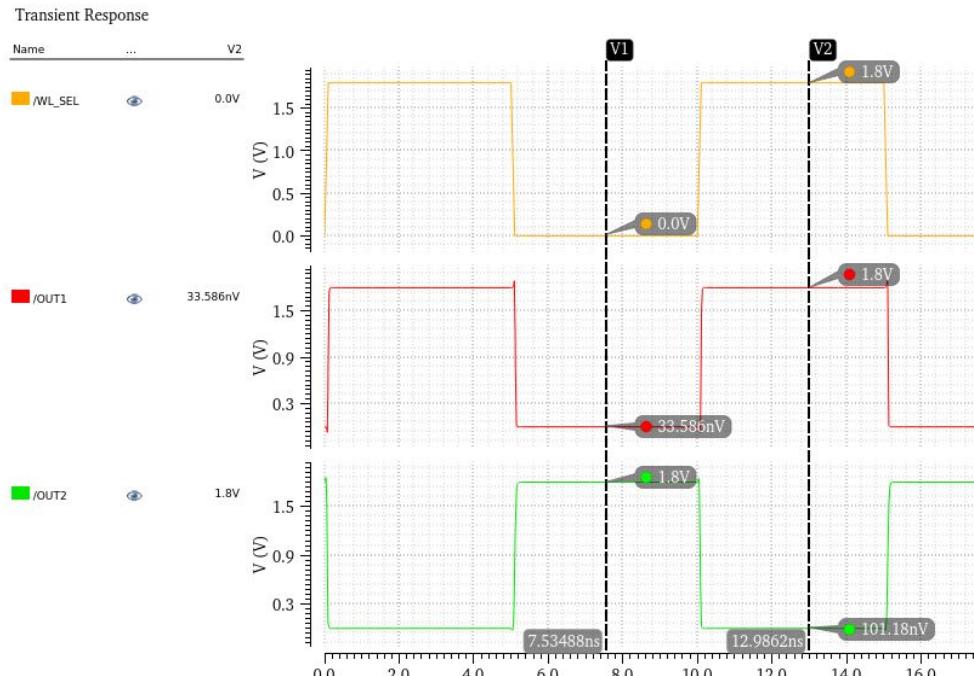
Schematic



Symbol



Transient Response

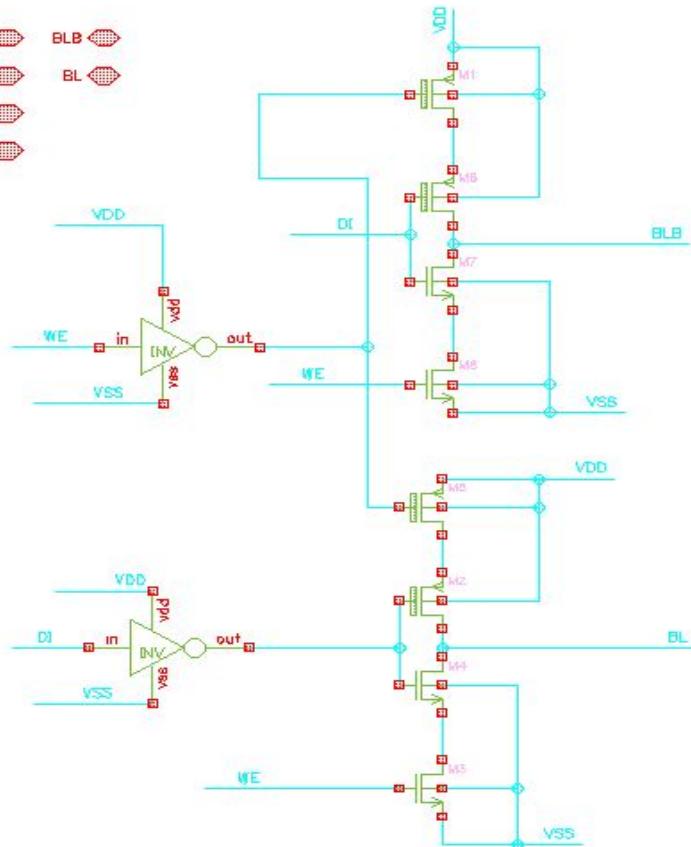


Avg. Power Consumed = 1.435 uW

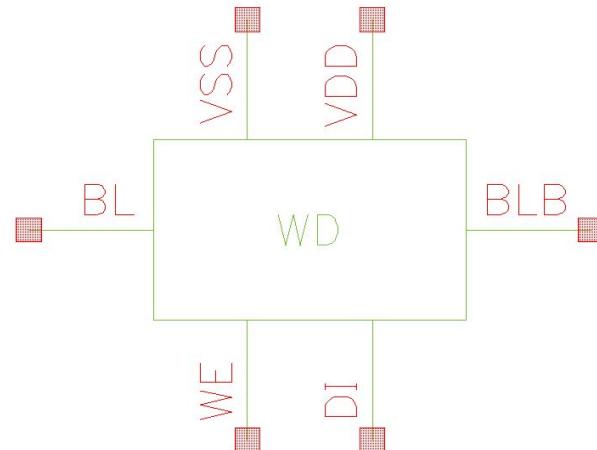
WRITE DRIVER

Schematic

VSS ◊ BLB ◊
VDD ◊ BL ◊
WE ◊
DI ◊

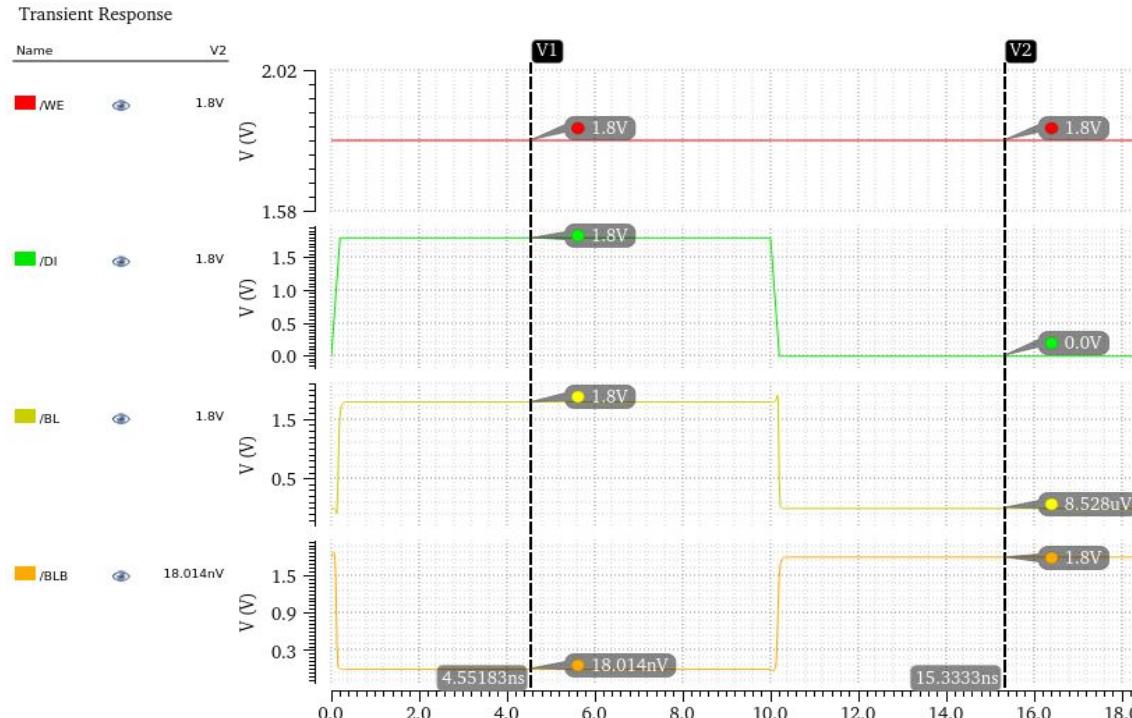


Symbol



WRITE DRIVER

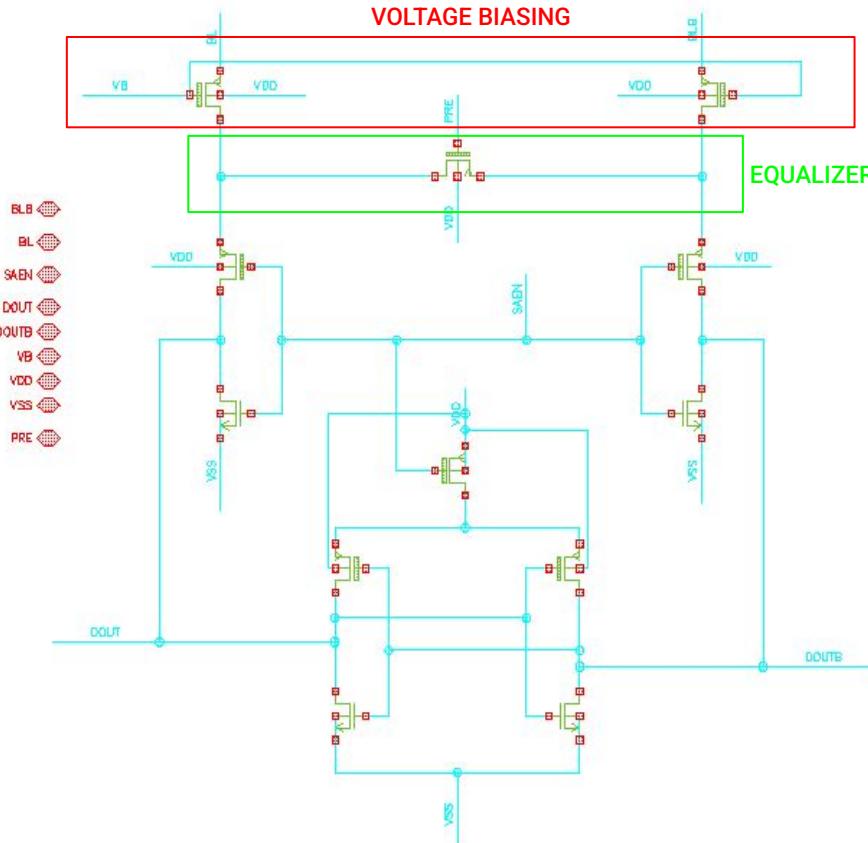
Transient Response



Avg. Power Consumed = **1.037 uW**

SENSE AMPLIFIER

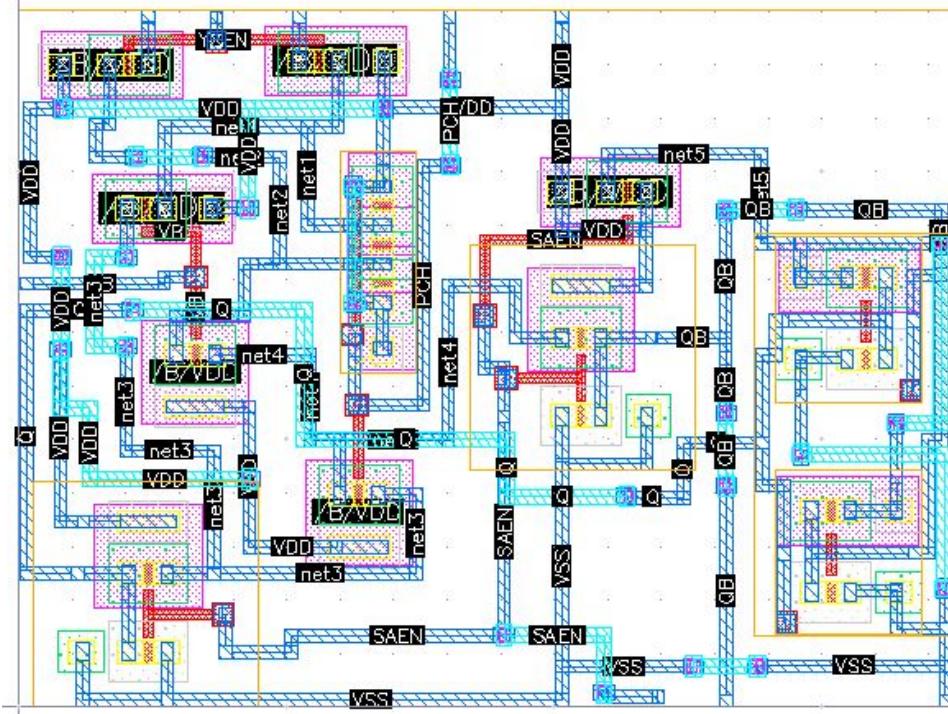
Schematic



- This is the schematic of a Charge Transfer Sense Amplifier (CTSA) which works on charge redistribution mechanism between very high bit-line capacitance and low output capacitance of the sense amplifier.
- This is more power efficient than the conventional Voltage Mode Sense Amplifier (VMSA); with Avg. Power being 2.06 uW rather than 8 uW of VMSA.
- We tried reducing its circuitry so as to reduce power which is shown in the subsequent slides.

SENSE AMPLIFIER

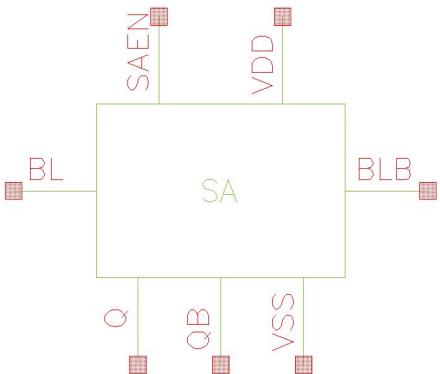
CTSA Layout along with Precharge



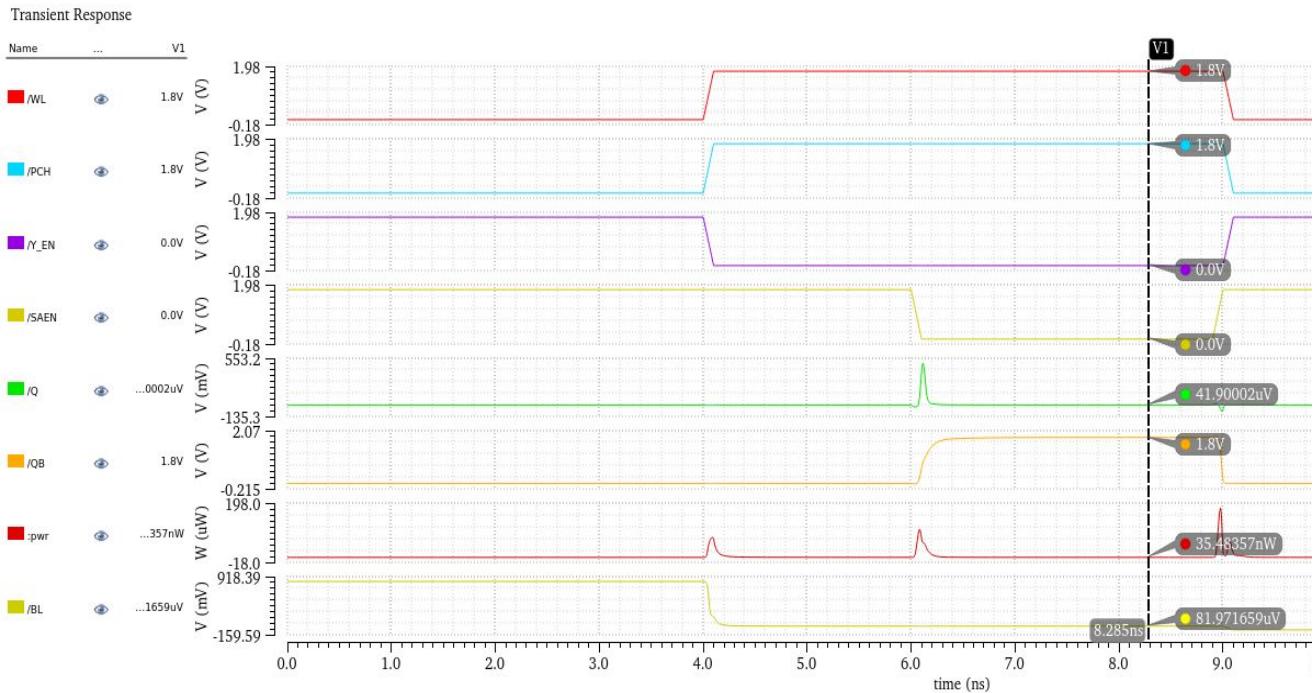
**Area= 13.015*17.51
= 227.89 μm^2**

SENSE AMPLIFIER

Symbol

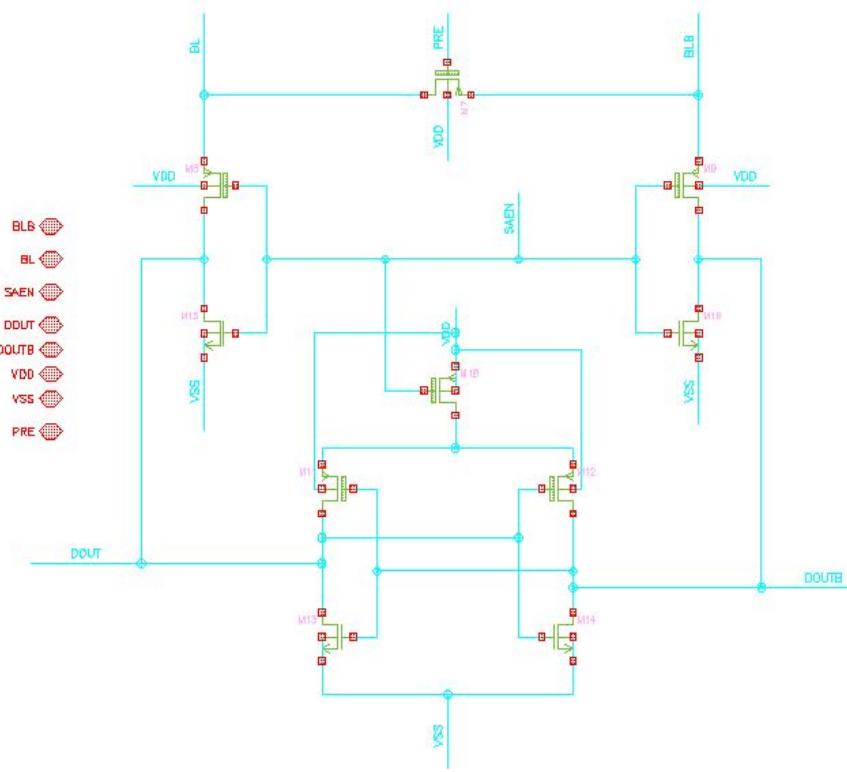


Transient Response

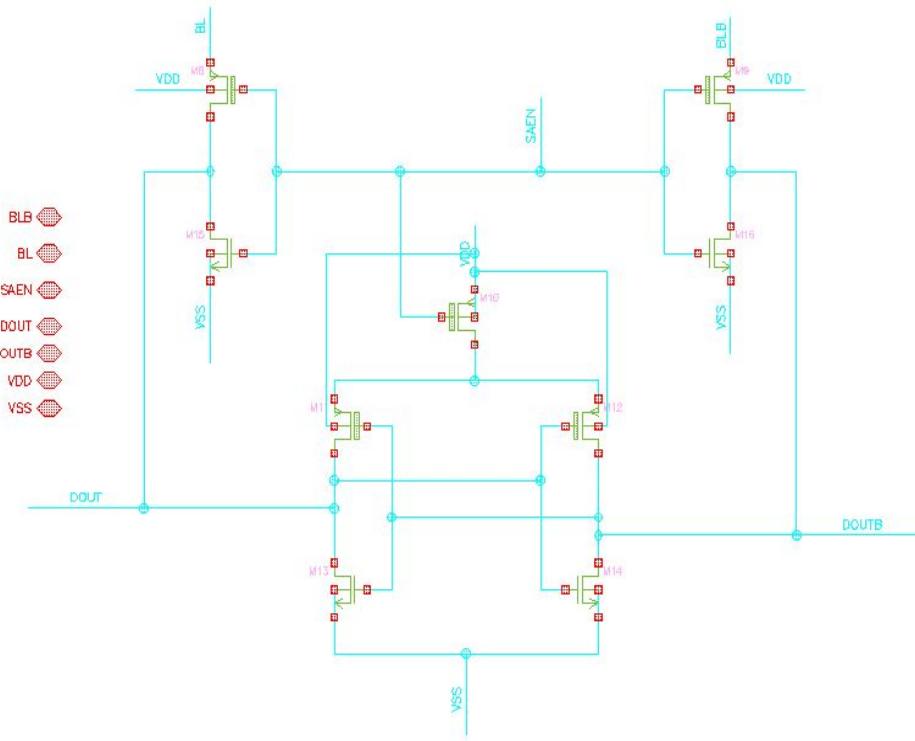


SENSE AMPLIFIER

CTSA without Voltage Biasing



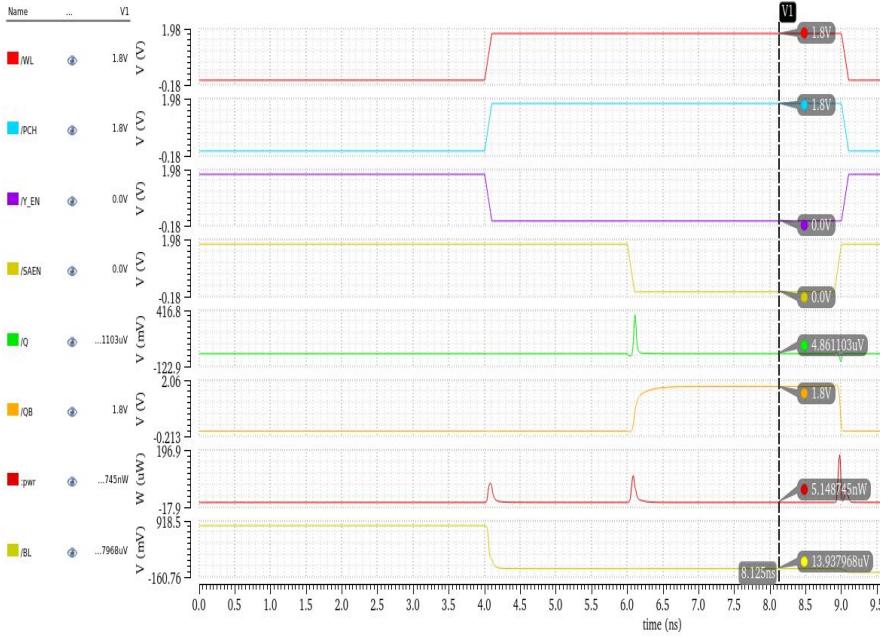
CTSA without Voltage Biasing & Equalizer



SENSE AMPLIFIER

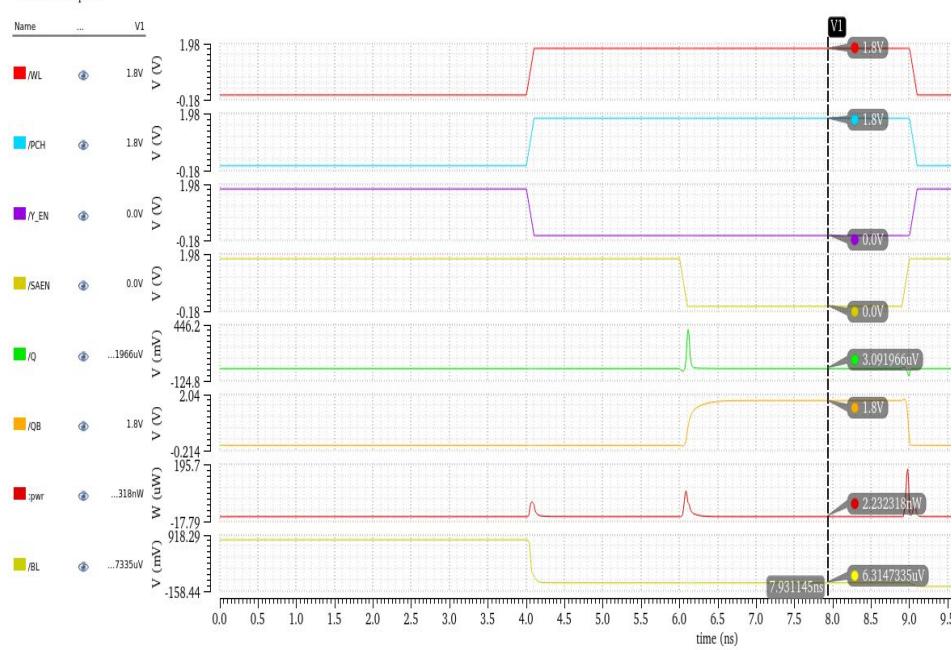
Transient Response

Transient Response



CTSA without Voltage Biasing

Transient Response



CTSA without Voltage Biasing + Equalizer

SENSE AMPLIFIER

- Comparing the two reduced circuitry of the CTSA with the original one, we found that:

CTSA	CTSA (without Voltage Biasing)	CTSA (without Voltage Biasing & Equalizer)
Avg. Power Consumed: 2.065 uW	Avg. Power Consumed: 1.856 uW	Avg. Power Consumed: 1.686 uW

- Clearly, the power has come down as we removed the biasing & equalizing circuitry.
- Also the transient response of all the three circuits were almost the same.
- So, we can conclude from here that we can use the CTSA even after removing the biasing & equalizing circuitry, which gives the same result at lower power consumption.

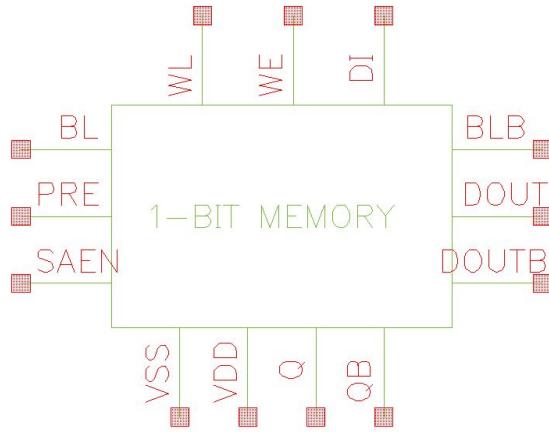
SENSE AMPLIFIER

References

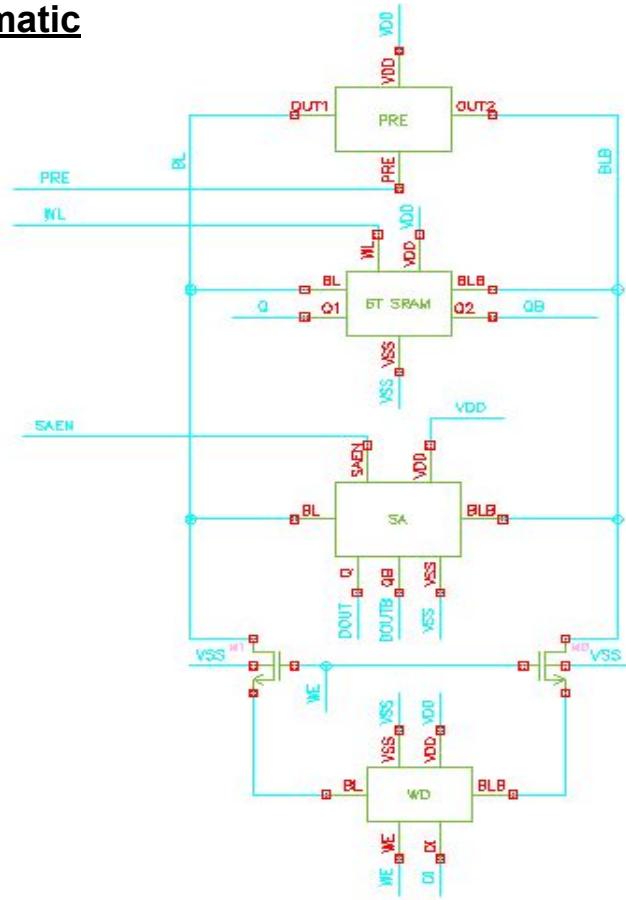
- **IEEE Transactions:** A Self-Biased Charge-Transfer Sense Amplifier Sandeep Patil, Michael Wieckowski, and Martin Margala University of Rochester Department of Electrical and Computer Engineering Rochester, NY, United States
- High-Performance and Low-Voltage Sense-Amplifier Techniques for sub-90nm SRAM Manoj Sinha*, Steven Hsu, Atila Alvandpour, Wayne Burleson*, Ram Krishnamurthy, Shekhar Borkar Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, USA* Microprocessor Research Labs, Intel Corporation, Hillsboro, OR 97124, USA
- Comparative Study of Sense Amplifiers for SRAM Mohammed Shafique, M. Tech Scholar Vivekananda Global University, Jaipur; Ruchi Sharma Associate Professor, Department of Electronics & Communication, Vivekananda Global University, Jaipur

1-BIT MEMORY ARCHITECTURE

Symbol

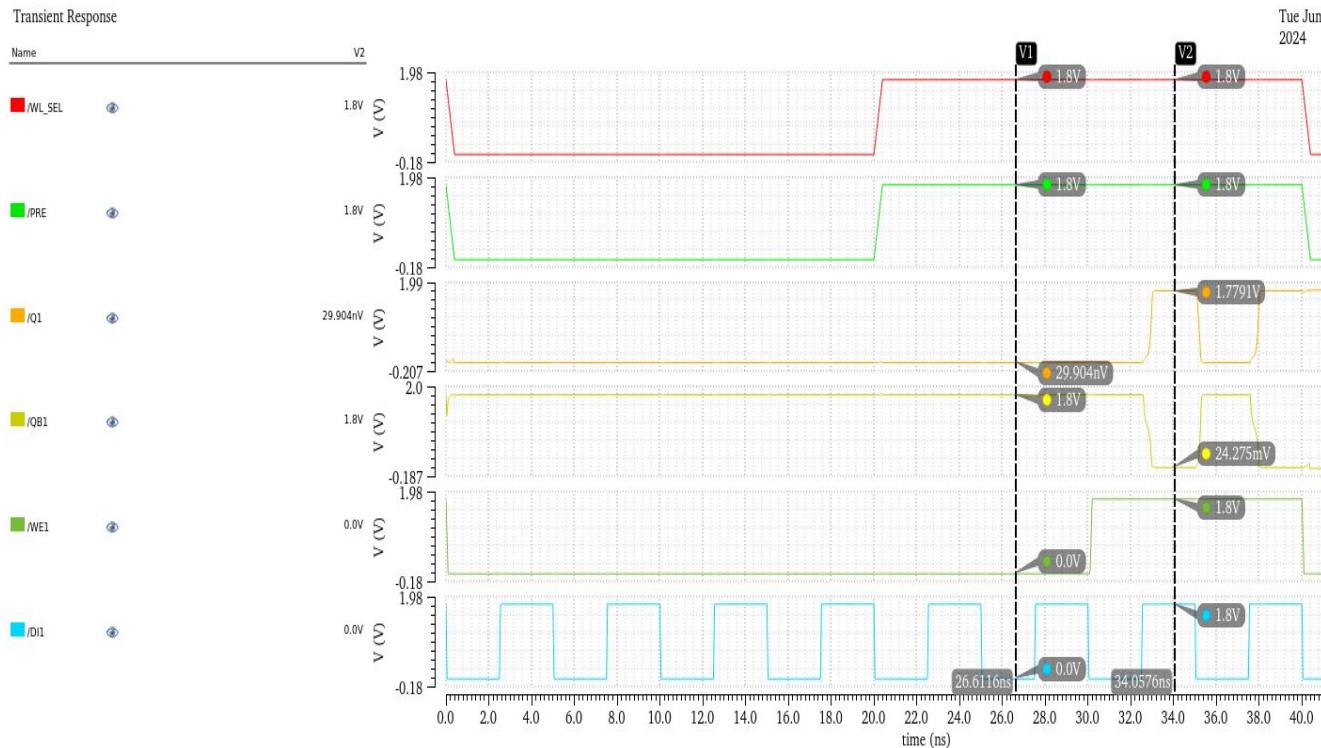


Schematic



1-BIT MEMORY ARCHITECTURE

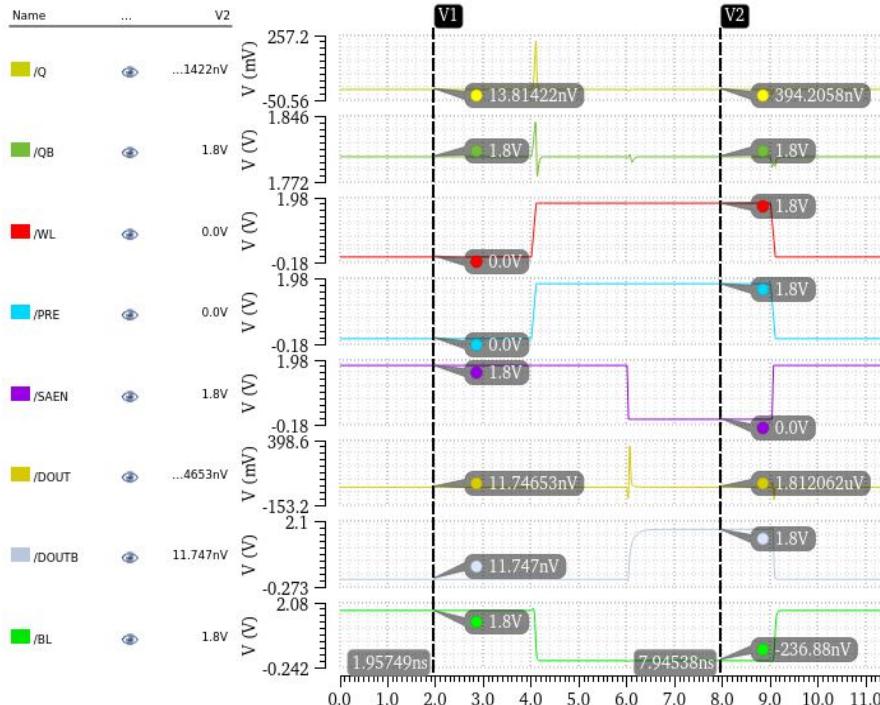
Transient Response(WRITE)



1-BIT MEMORY ARCHITECTURE

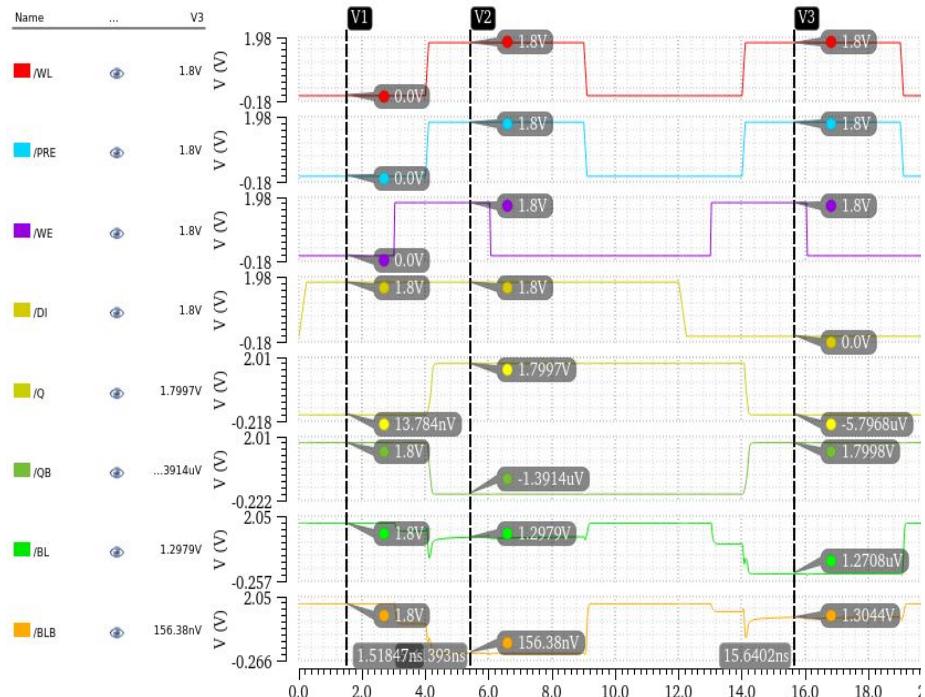
Transient Response(READ)

Transient Response



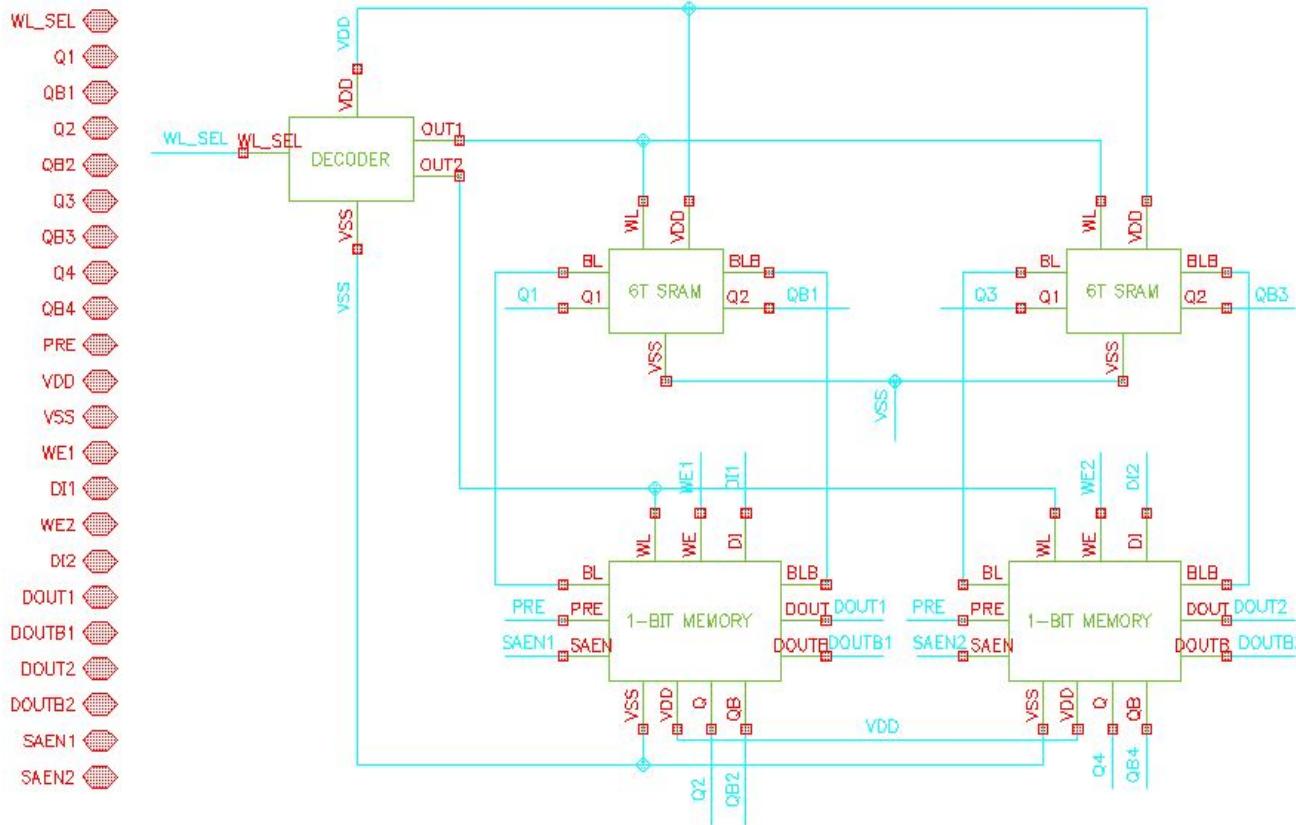
Transient Response(WRITE)

Transient Response



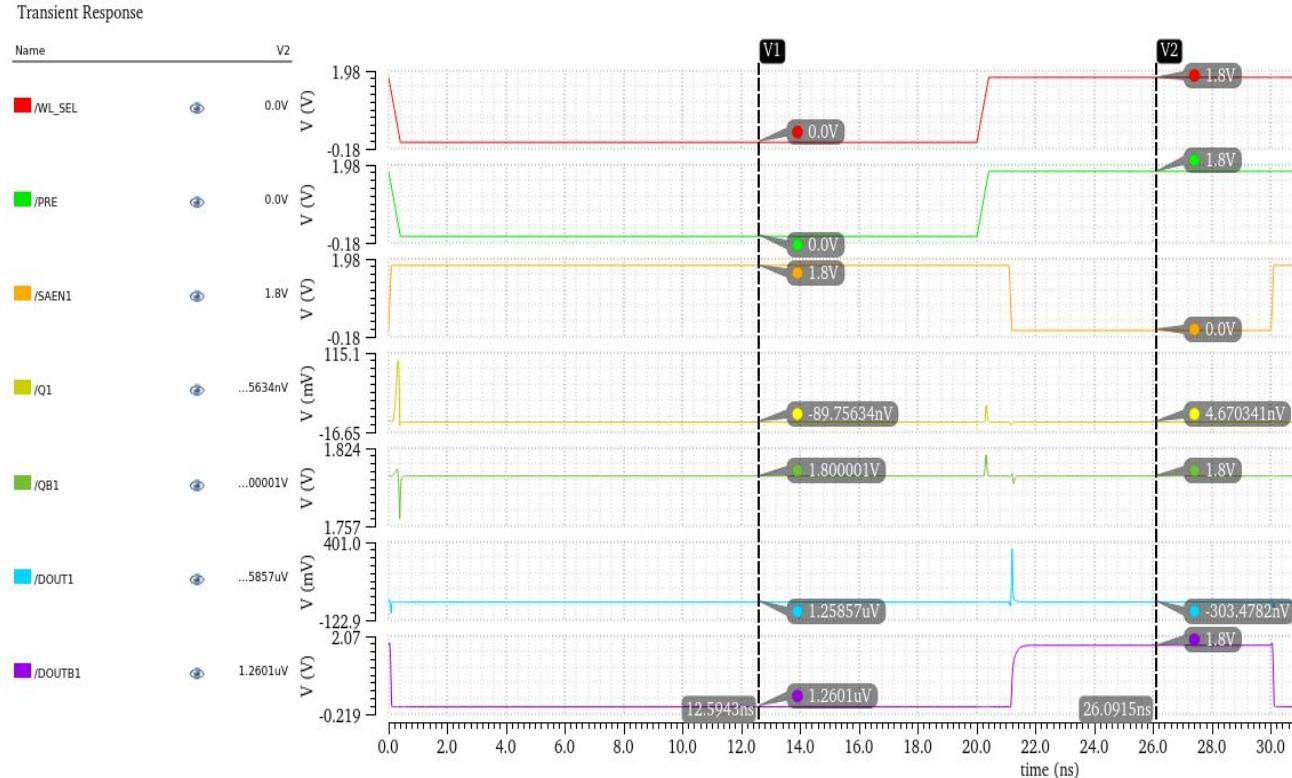
4-BIT MEMORY ARCHITECTURE

Schematic



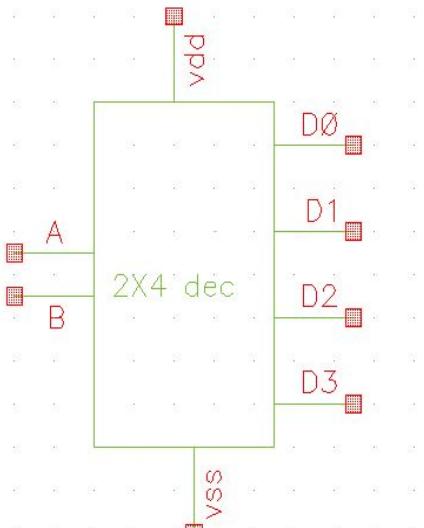
4-BIT MEMORY ARCHITECTURE

Transient Response(READ)

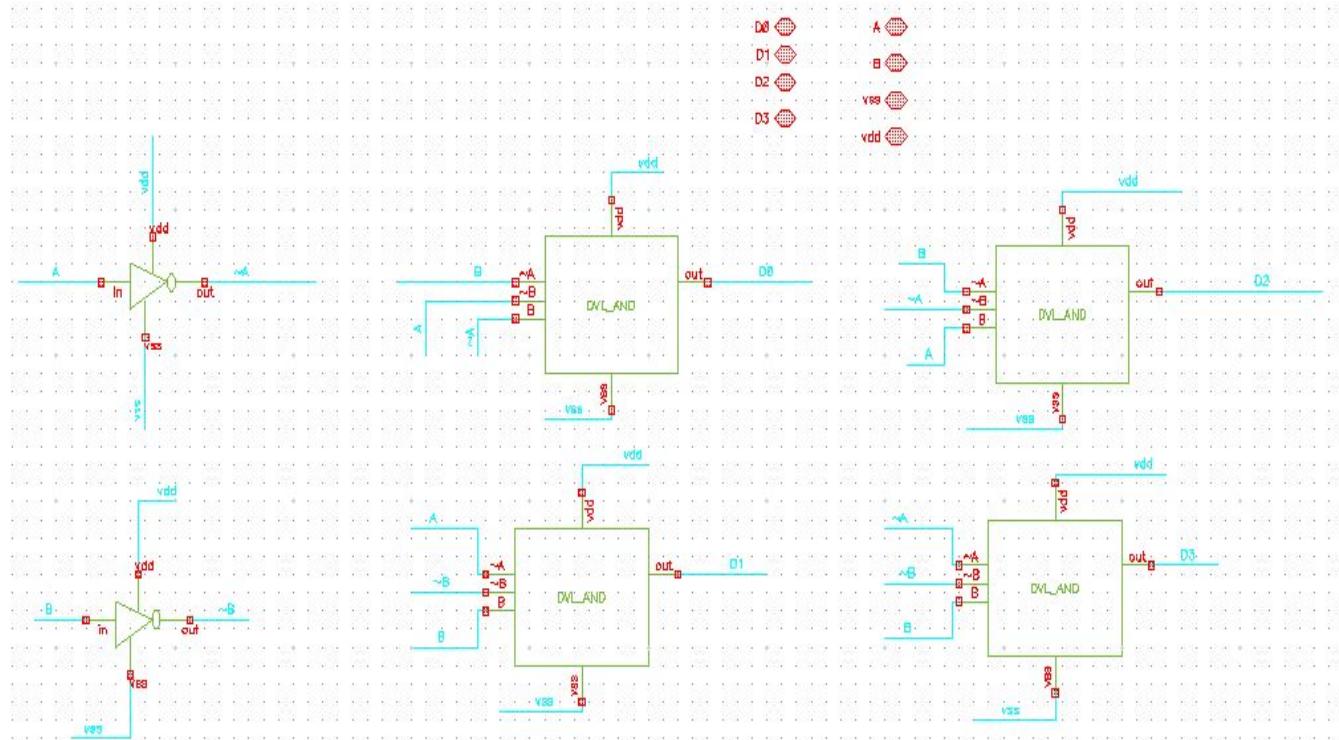


2x4 ROW DECODER

Symbol

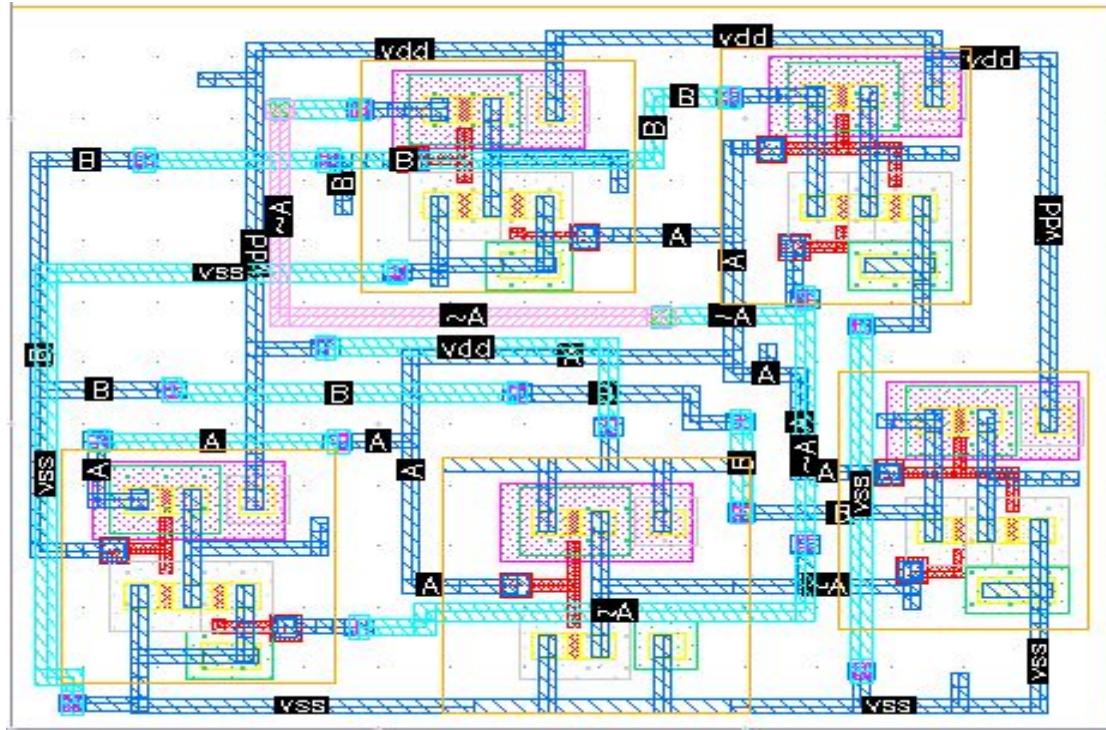


Schematic



2x4 ROW DECODER

Layout



$$\begin{aligned} \text{Area} &= 15.1 * 11.8 \\ &= 178.18 \mu\text{m}^2 \end{aligned}$$

2x4 ROW DECODER

Conclusion

Conventional Decoder Power Consumption = **3.799 uW**;

New Decoder Power Consumption = **1.286 uW**

Compared to a conventional decoder design , our approach **consumes 66% less power** due to the fewer number of gates and the efficient handling of static and dynamic power dissipation through DVL techniques.

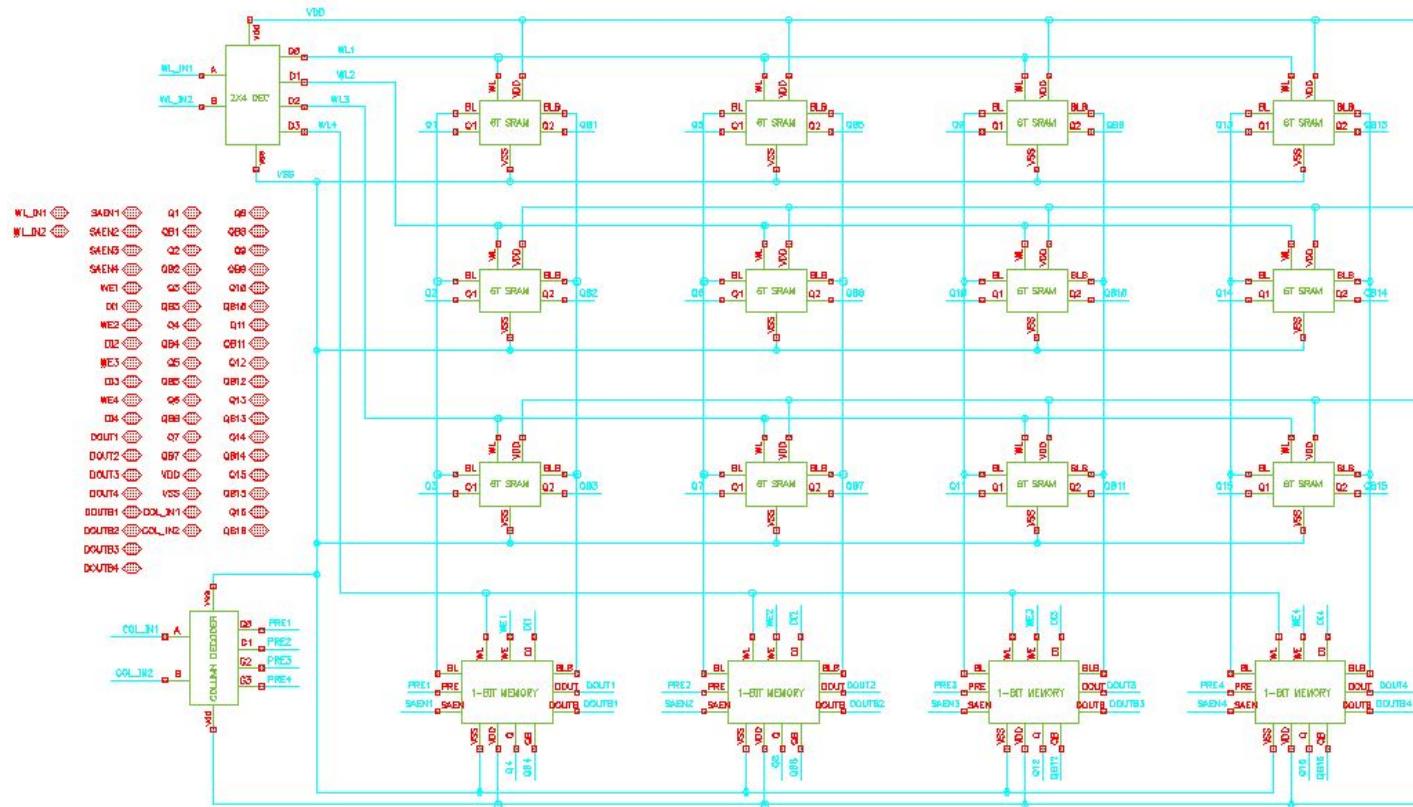
References

IEEE Paper

- 1)Design of Low-Power High-Performance 2–4 and 4–16 Mixed-Logic Line Decoders Dimitrios Balobas and Nikos Konofaos

4X4 MEMORY ARRAY

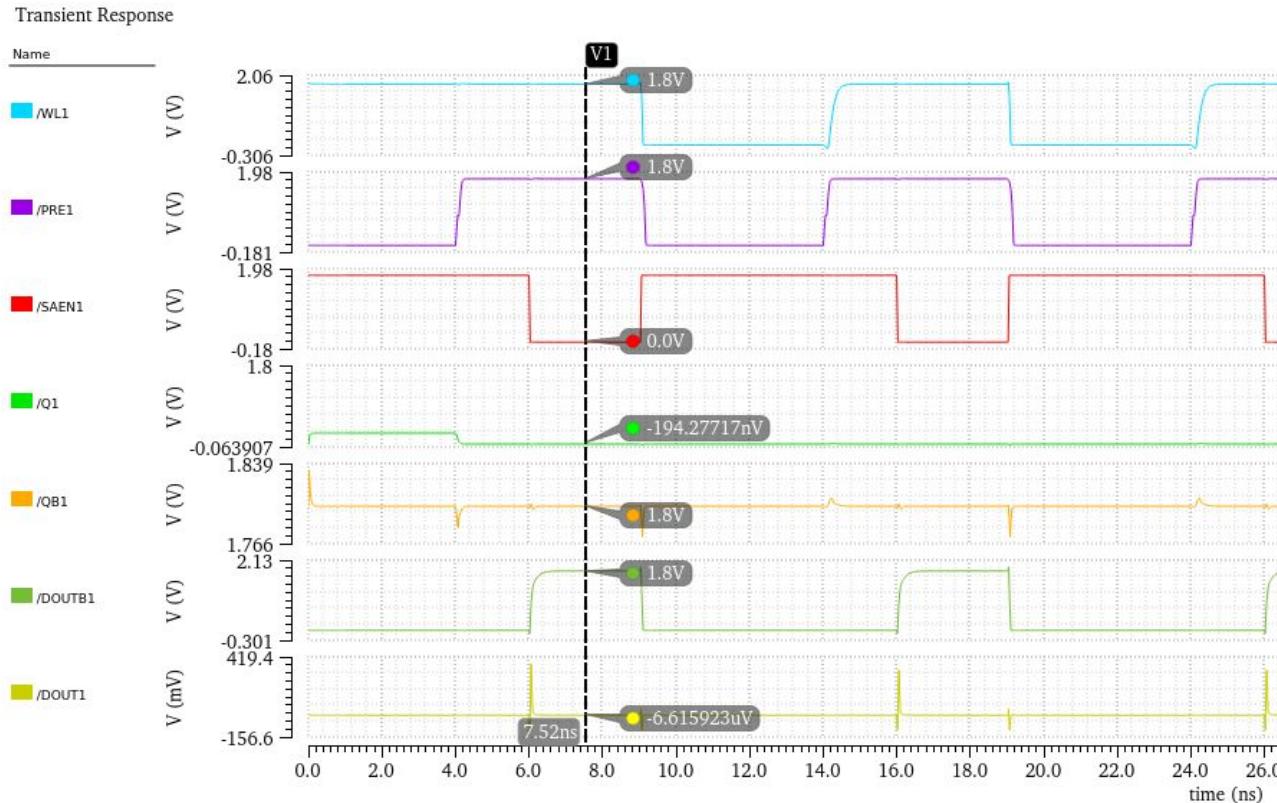
Schematic



4X4 MEMORY ARRAY

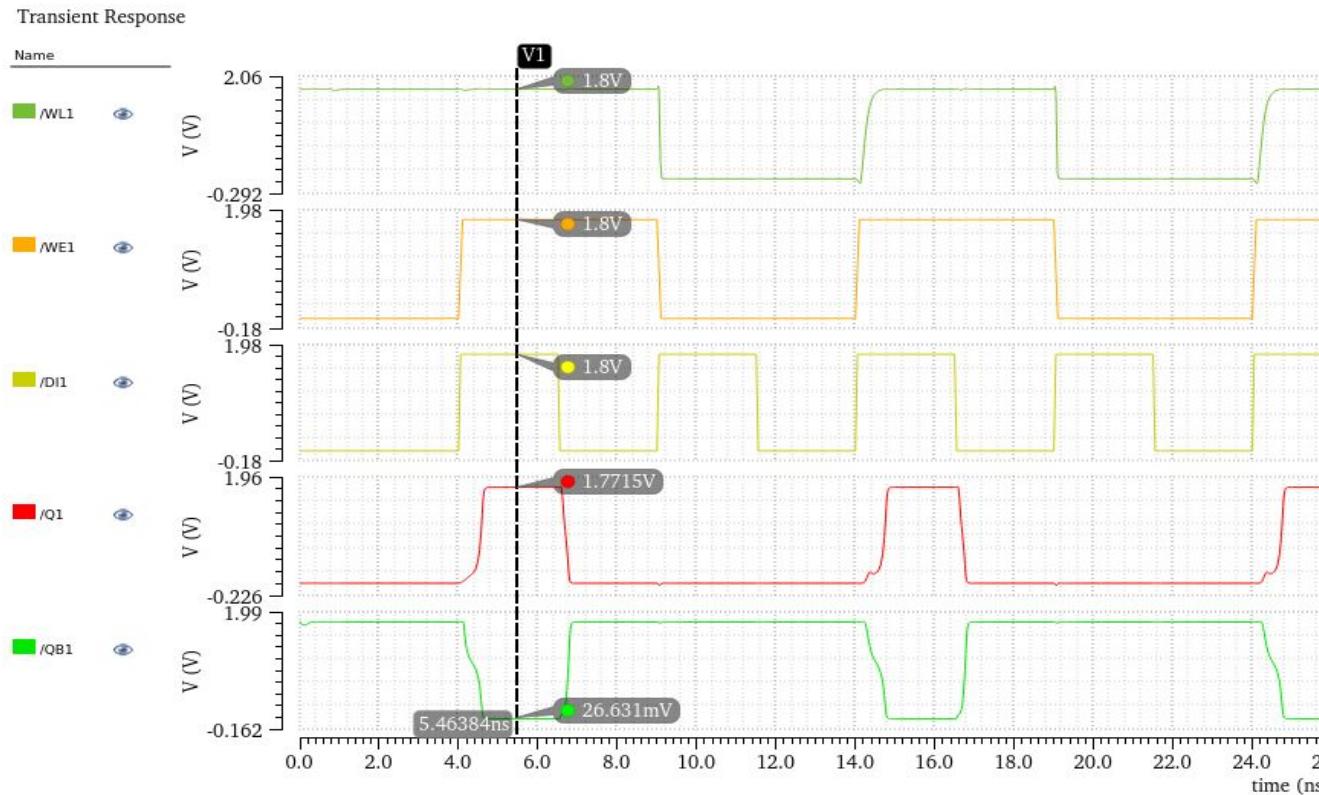
Transient Response(READ)

Avg. Power Consumed = 298.3 uW



4X4 MEMORY ARRAY

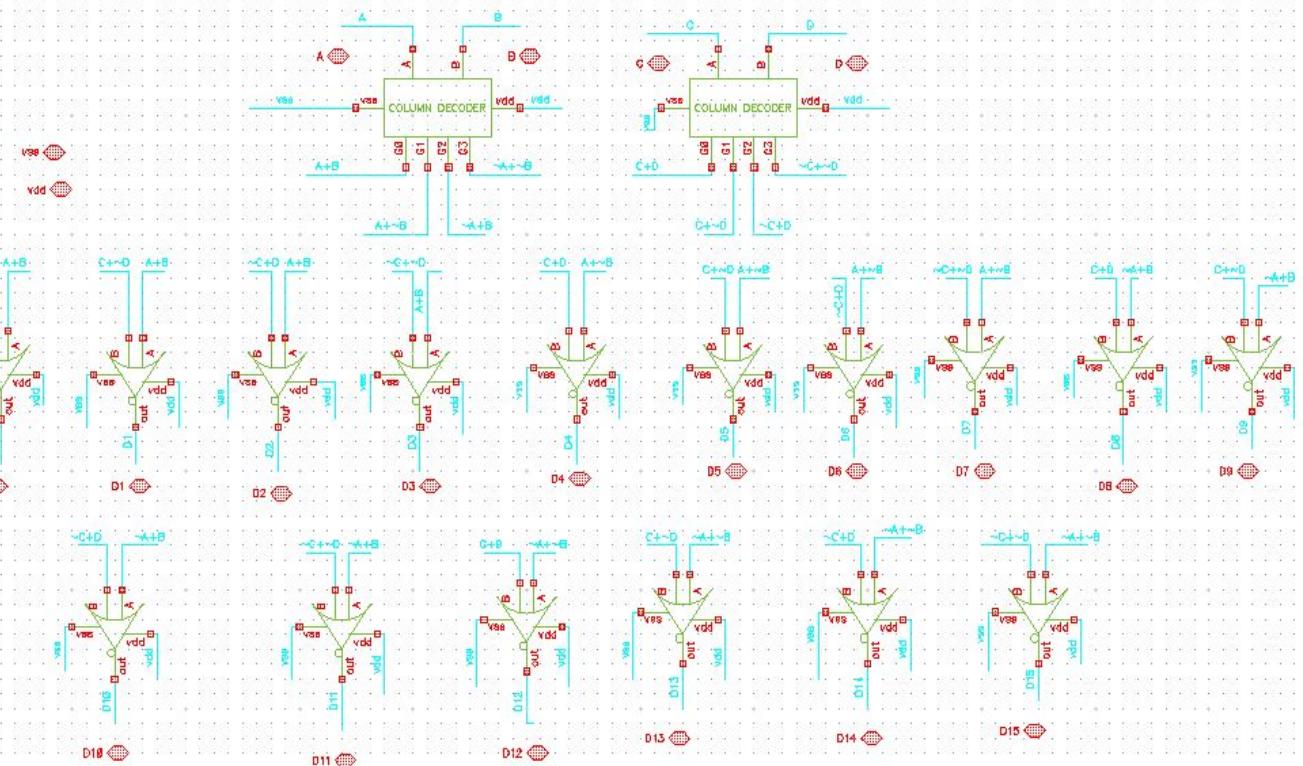
Transient Response(WRITE)



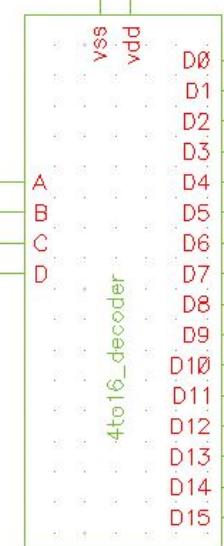
1-Kb MEMORY

4x16 DECODER

Schematic

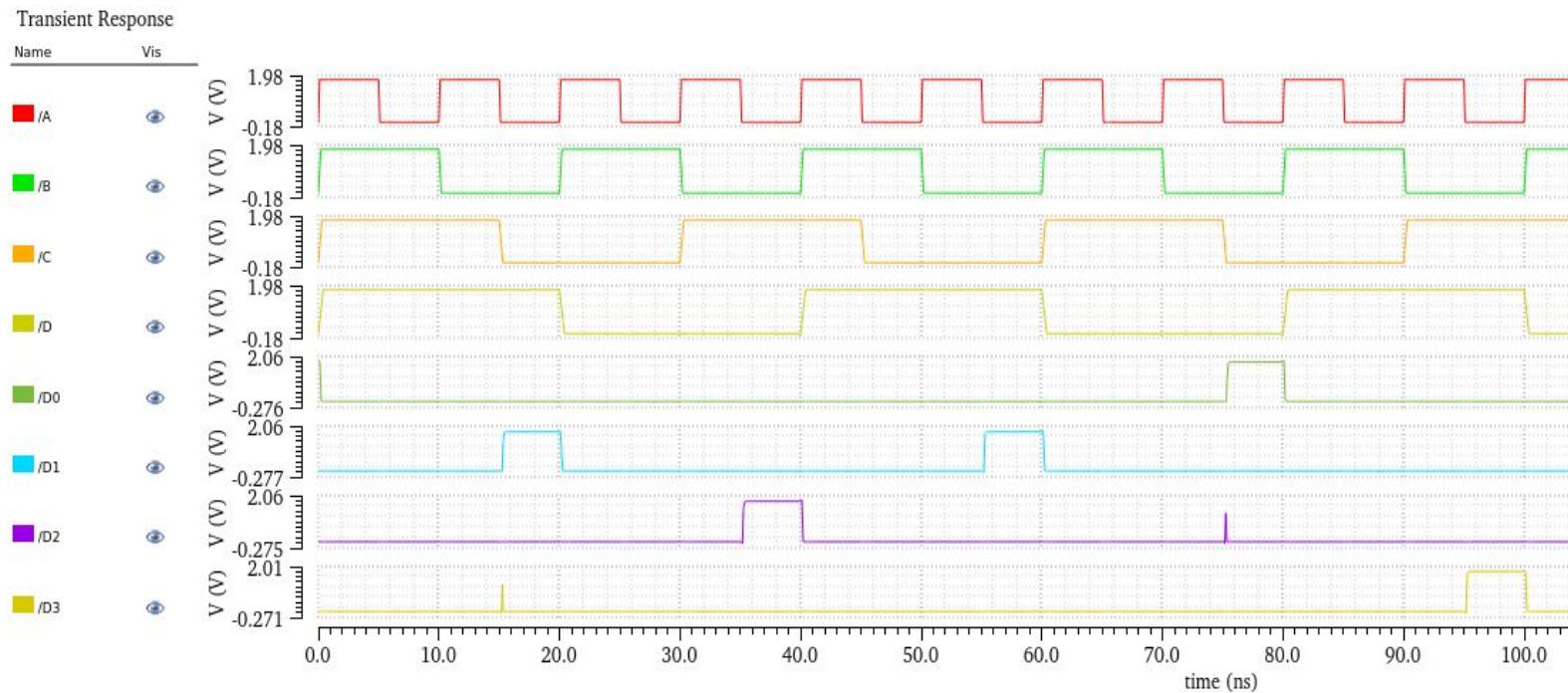


Symbol



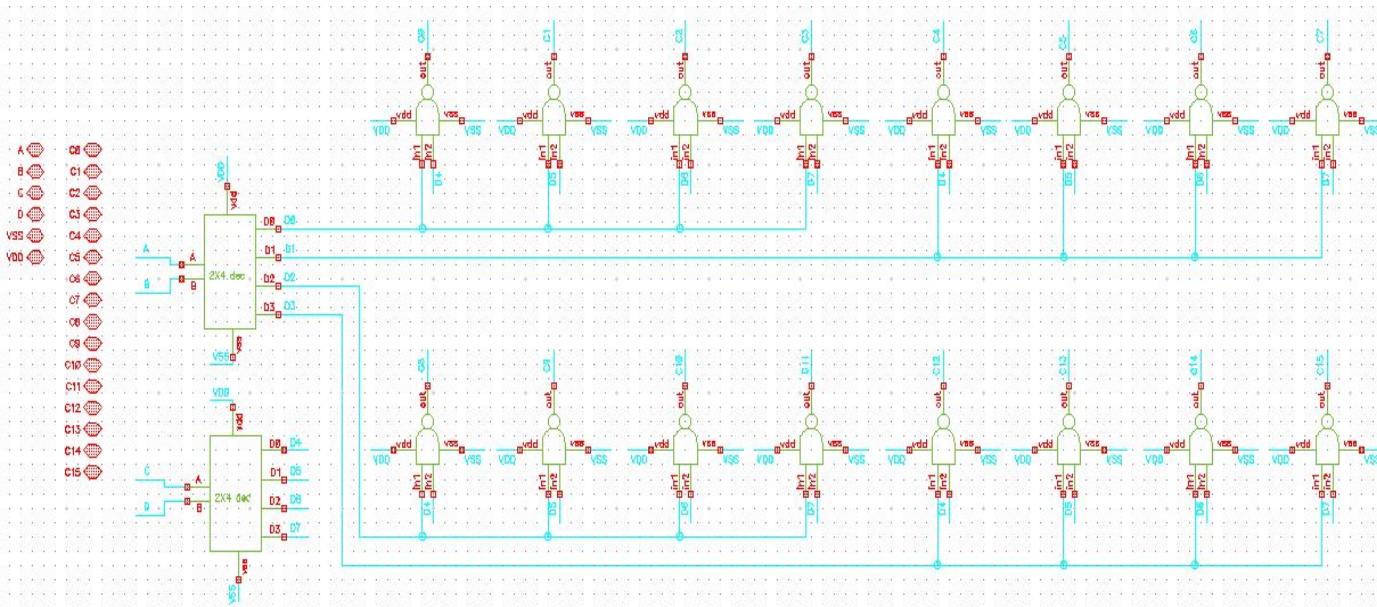
4x16 DECODER

Transient Response



4x16 COLUMN DECODER (LOGIC LOW)

Schematic



Symbol

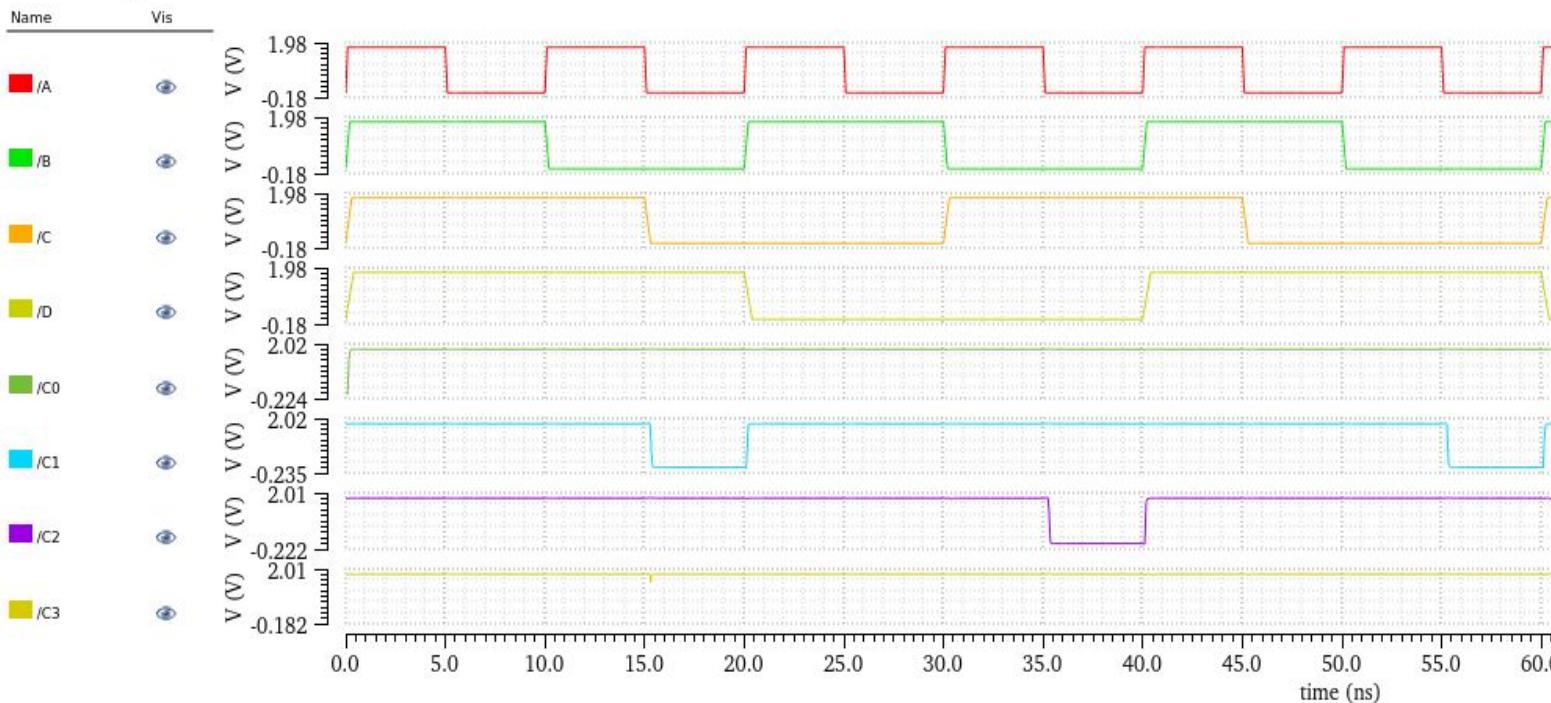


4x16 COLUMN DECODER (LOGIC LOW)

Transient Response

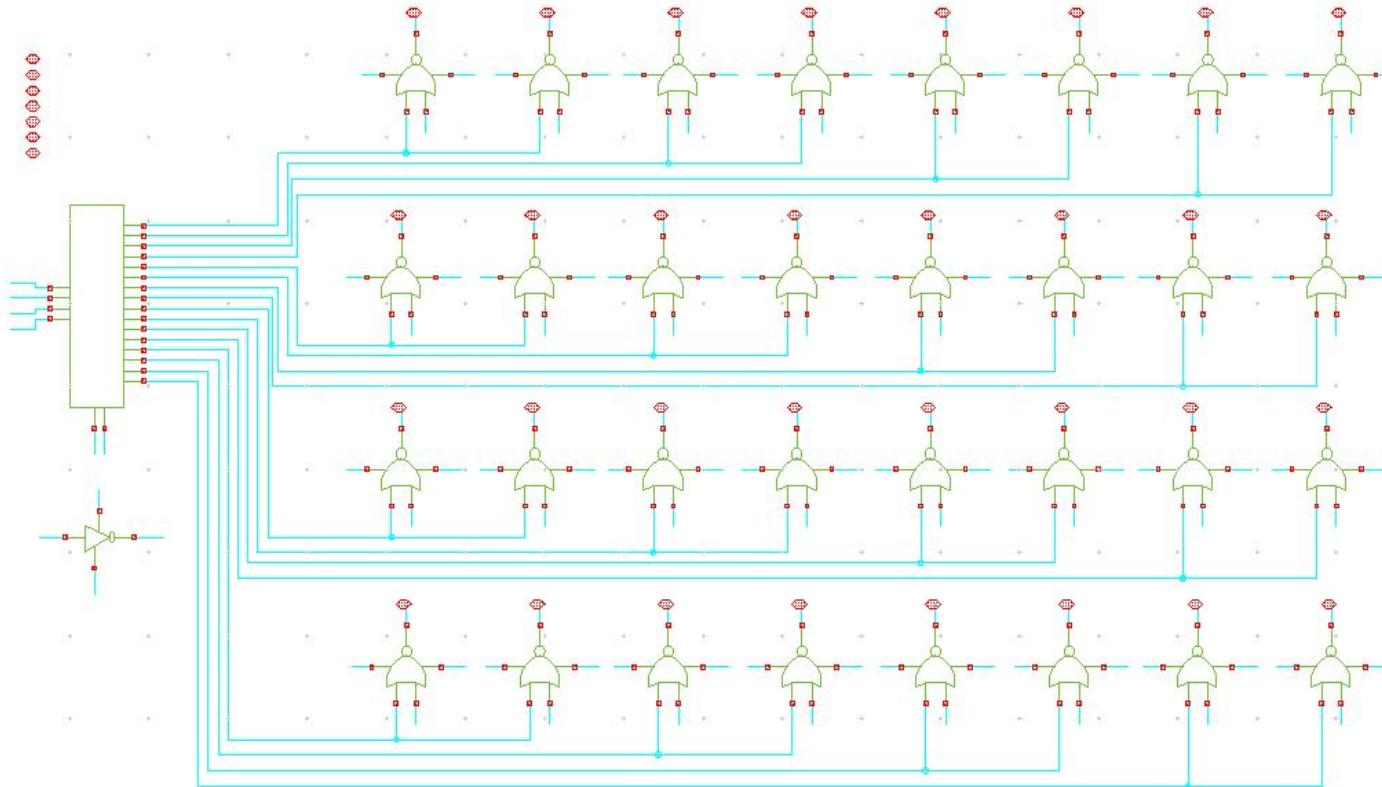
Avg. Power consumed
=10.92 uW

Transient Response

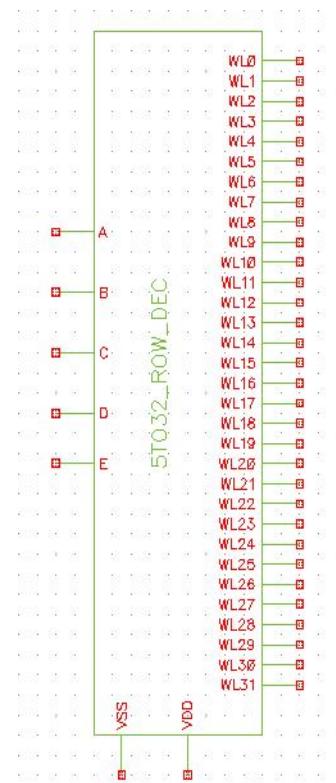


5x32 ROW DECODER

Schematic



Symbol

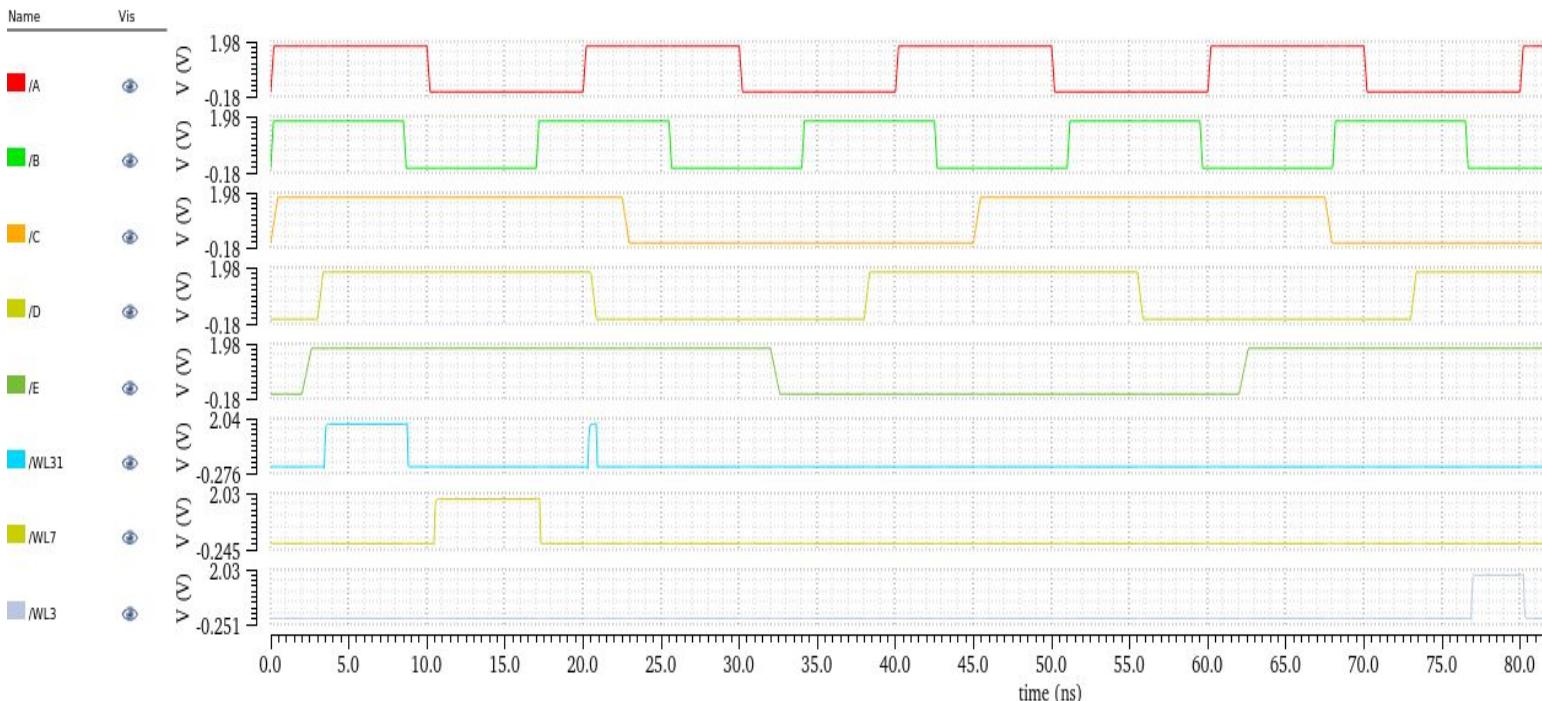


5x32 ROW DECODER

Transient

Avg. Power Consumed
=1.191 uW

Transient Response



5x32 ROW DECODER

Conclusion

Traditional 5-32 decoder : **No. of transistor used= 370**

Proposed 5-32 decoder:

Power consumption = 295 uW

Power consumption = 1.191 uW

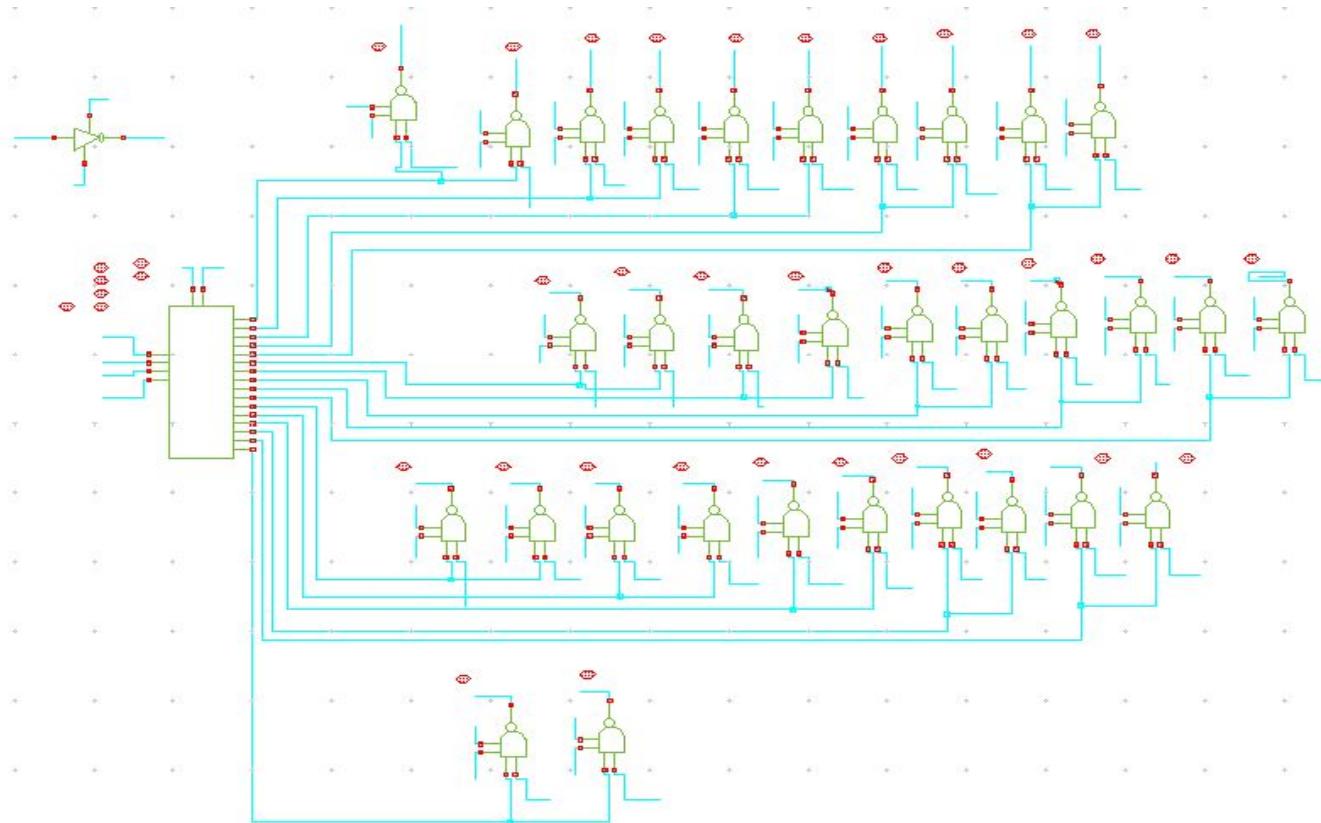
References

- 1) www.jetir.org (ISSN-2349-5162)

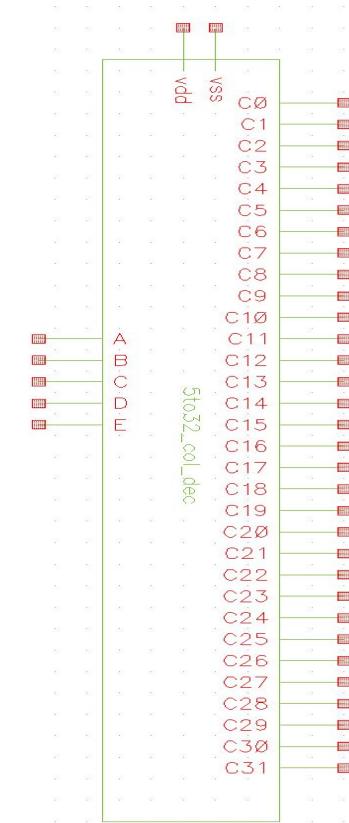
Design and analysis of a 5:32 Address decoder for a high speed SRAM based

5x32 COLUMN DECODER (LOGIC LOW)

Schematic



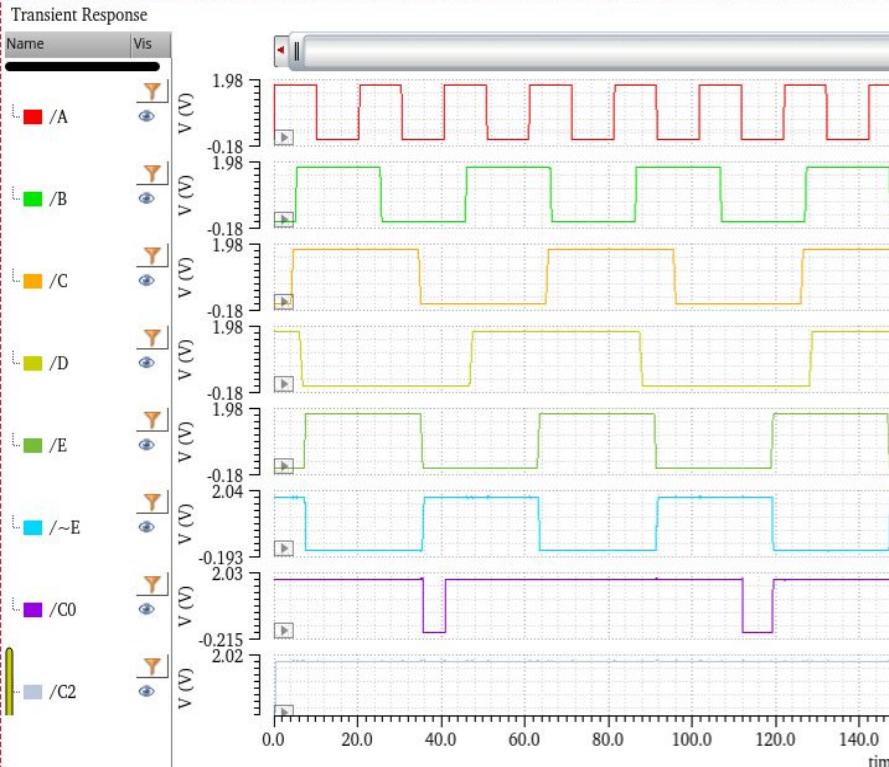
Symbol



5x32 COLUMN DECODER (LOGIC LOW)

Transient

Avg. Power Consumed: 13.26 uW

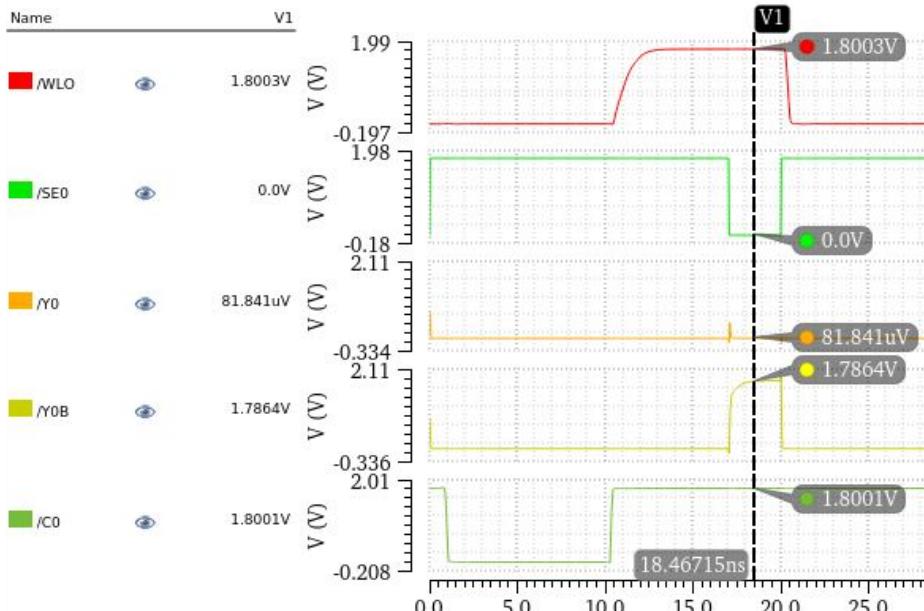


1-KB MEMORY ARCHITECTURE (TRANSIENT RESPONSE)

Read (Initial Condition Q=0)

Avg. Power Consumed
=1.251 mW

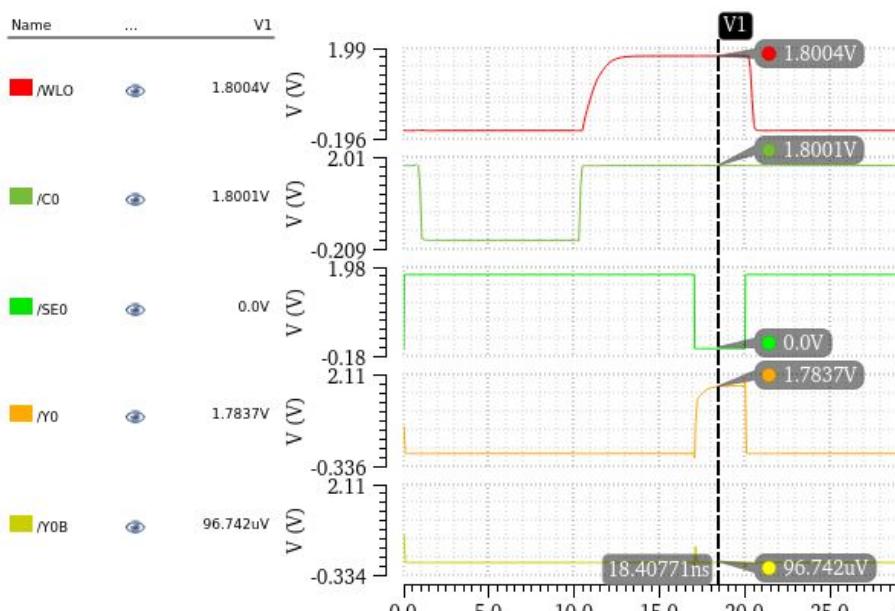
Transient Response



Read (Initial Condition QB=0)

Avg. Power Consumed
=1.377 mW

Transient Response

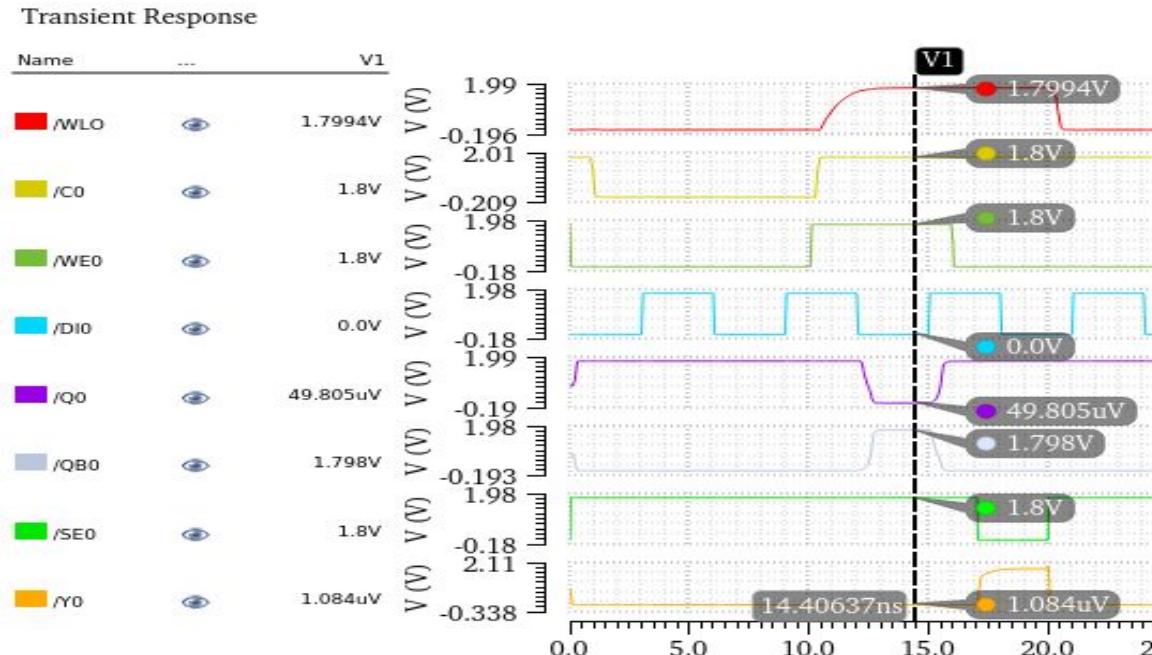


1-KB MEMORY ARCHITECTURE (SCHEMATIC)



1-Kb MEMORY ARCHITECTURE (TRANSIENT RESPONSE)

Read-Write-Hold in Cell 0



Avg. Power Consumed = 1.515 mW

POWER COMPARISON

- This slide contains a power comparison between the conventional and the modified circuits that we have used in the memory architecture.

CIRCUITS	CONVENTIONAL	MODIFIED
PRECHARGE	0.165 uW	1.729 uW
SENSE AMPLIFIER	2.065 uW	1.686 uW
2x4 ROW DECODER	3.799 uW	1.286 uW
5x32 ROW DECODER	-	1.191 uW
5x32 COLUMN DECODER	-	13.26uW

REFERENCES

IEEE Paper*

- 1) *Design and Analysis of Low Power SRAM Cells Akshay Bhaskar School of Electronics Engineering VIT University, Vellore, India
- 2) *Design of Low-Power High-Performance 2–4 and 4–16 Mixed-Logic Line Decoders Dimitrios Balobas and Nikos Konofaos
- 3) Design and analysis of a 5:32 Address decoder for a high speed SRAM based
- 4) Design and Performance Analysis of 32 32 Memory Array SRAM for Low-Power Applications