CHANDRA KIRAN NARALA

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OBJECTIVE

Electrical Engineering graduate student with academic experience on hardware design seeking full-time role in Hardware Design.

EDUCATION

Master of Science in Electrical Engineering | NYU Tandon December 2023

- Relevant Courses: Advanced Very Large-Scale Integrated Circuits, Analog Systems and Circuits, Advanced Hardware Design, Computer System Architecture, Digital Signal Processing.

Bachelors in Electronics and Communications Engineering | GVPCOE, India September 2020

- Courses: Digital Logic Design, VLSI Design, Microprocessors and Microcontrollers, Digital Signal Processing, Linear and Digital IC's.

SKILLS

Language skills: C, Python, Verilog, VHDL, x86 Assembly Level Programming

Tools and technologies: Cadence Virtuoso, Innovus, Genus, Xilinx Vivado, Vitis HLS, Matlab, NI Labview, Mutlisim, VS Code

Area of Expertise: RTL ASIC Design, Digital & Analog Design, STA, Communication Protocols, CNN

PROFESSIONAL EXPERIENCE

Programmer Analyst, Cognizant Technology Solutions, India November 2020 - December 2021

- Optimized Python modules, featuring iterative processes to execute UNIX queries and commands. Triggered job start-ups for regression, and actively monitored and analyzed outcomes. Modified selenium automation suites for a web application, implementing a data-driven framework with Maven dependencies.

Research Assistant, S. Sagar Krishna, GVPCOE, India January 2019 - March 2020

- Implemented a YOLOv2 object detection model on an FPGA platform, optimizing for high-speed processing and power efficiency.
- Successfully integrated CNN using Vitis HLS and Vivado on a Zynq-7000 SoC, achieving real-time detection with a 3.2 Tbps throughput.
- Demonstrated 82% reduction in hardware usage and a 2% decrease in error rate, outperforming CPU implementations with 26.62 GOP/s performance and power consumption of just 2.6W.

CASE STUDY/PROJECTS

MBIST engine for 256x4b SRAM Memory array using 7nm Technology

- Developed a behavioral Verilog description for each component, incorporating a BIST engine at SRAM speed.
- Enabled testing with 4 test patterns: Blanket 0 & 1, Checkerboard and reverse Checkerboard, March C, and March LR.

8b ALU using 7nm Technology

- Fabricated hardware of 8b ALU to synthesize and build a physical layout using Genus and Cadence Innovus using ASAP 7nm library and programmed a behavioral Verilog description of 8b ALU and conducted synthesis to determine component dependencies on area power and cycle time and finalized the physical layout.

RISC-V RV32I 32-bit Processor | GitHub

- Architected a 32-bit a processor which executes a subset of the open-source RISC-V RV32I instruction set.
- Interfaced this design on an FPGA basys3 board, conducted power, area, and timing analysis, with the design operating at 100MHz, reporting negative slack in timing constraints, allowing operation at even higher frequencies.

256x32 SRAM Memory Array using 7nm Technology

- Designed and simulated 8Kbits 6T SRAM memory cell, comprising essential peripherals such as row and column decoders, sense amplifiers, pre-charge circuits, and write drivers to support non-destructive read and reliable write operations.
- With HSPICE memory array circuit is simulated and performed simulations to evaluate functionality, timing, and performance for read and write operations.

Folded Cascode Operational Transconductance Amplifier using 45nm Technology

- Architected a folded cascode operational transconductance amplifier with a voltage biasing circuit, meeting design specifications with a 71dB gain, 180uW power consumption, and a 65^{o} phase margin using a 45nm CMOS design.
- Evaluated transistor sizing in OTA circuitry, leveraging overdrive voltage estimations to optimize voltage biasing and examined different transistor scales. Optimized phase margin and bandwidth performance through analysis and testing.

Fingerprint Matcher with GUI | GitHub

- Developed a Python-based fingerprint matching application using OpenCV and tkinter, achieving a 95% accuracy rate through the implementation of the Scale-Invariant Feature Transform (SIFT) algorithm.
- Improved matching efficiency by 20% via advanced preprocessing techniques, resulting in faster results for users.