CHANDRA KIRAN NARALA

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SUMMARY

Aspiring FPGA Engineer with a strong foundation in RTL design, FPGA synthesis, and hardware acceleration. Proficient in Verilog, VHDL, FPGA synthesis, and static timing analysis for low-latency, high-speed applications.

EDUCATION

NYU Tandon | MS in Electrical Engineering | USA Jan 2022 - Dec 2023

Courses: Advanced VLSI, Advanced Hardware Design (FPGA/ASIC Verification), Computer System Architecture, DSP.

GVPCOE | Bachelors in Electronics and Communications Engineering | India Jul 2016 - Sept 2020

Courses: Digital Logic Design, VLSI, FPGA Design, Digital Signal Processing, Linear and Digital IC's.

SKILLS

HDL & Programming: Verilog, SystemVerilog, VHDL, x86 Assembly Level Programming, Python, C, CSS, HTML
FPGA & ASIC Tools: Cadence Virtuoso, Xilinx Vivado, Altera Quartus Prime, Verdi, Matlab, NI Labview, Cadence Innovus,
Hardware & Prototyping: Digilent Basys3, STM32f429I Discovery Board,
Area of Expertise: Ultra-Low Latency FPGA Design, RTL Coding, FPGA Synthesis, Static Timing Analysis, DSP

PROJECTS

Low Latency Pong Game on Artix-7 FPGA July 2024

- Designed and implemented a Pong game on Artix-7 FPGA using Verilog and VGA controller (640x480 resolution at 60Hz).
- Developed a custom finite state machines for low-latency paddle control, ball movement, and score tracking.
- Optimized timing synchronization using hSync/vSync signals and a 25MHz clock divider, ensuring smooth frame rendering.

MBIST engine for 256x4b SRAM array using (7nm) Dec 2023

- Designed and implemented a Built-In Self-Test engine for 256x4b SRAM using Verilog, achieving reliable 100MHz operation.
- Executed SRAM validation using industry-standard test patterns including Blanket 0,1, Checkerboard, March C, and March LR, ensuring robust fault coverage.

RISC-V RV32I 32-bit Processor Nov 2022

- Architected a 32-bit RISC-V RV32I processor in Verilog, integrating a 5-stage pipeline for efficient instruction execution.
- Deployed an FPGA Basys3 board, achieving 100MHz operation with optimized timing constraints and logic utilization.
- Performed power, area, and timing analysis, identifying and resolving negative slack to enhance performance and efficiency.

High-performance 256x32 SRAM Array (7nm) Nov 2022

- Designed and simulated a 256x32 SRAM array in HSPICE, optimizing read/write stability, power efficiency, and timing accuracy.
- Conducted HSPICE simulations, resolved 12+ critical timing violations, improving data integrity and reducing access latency.

Real-Time Heart Rate and Blood Pressure Monitor (STM32 +MPR Sensor) May 2022

- Developed a real-time heart rate & blood pressure monitor on STM32F429I, Implemented SPI protocol for reliable and low-latency signal acquisition from the MPR sensor.
- Implemented the Maximum Amplitude Algorithm to extract systolic and diastolic pressure with 98% accuracy from Oscillometric waveform data. Derived an Oscillometric Waveform Envelope graph, optimizing signal processing for accurate pressure detection.

PROFESSIONAL EXPERIENCE

Research Assistant | High-Density Memory Design and Optimization in 7nm FinFET Technology
NYU, USA Jan 2024 - Present

- Designed & optimized 256x4b SRAM array, improving read/write speed and reducing power consumption by 20% to 6T.
- Executed synthesis & Static Timing Analysis, for timing closure and optimal performance, area, and power trade-offs.
- Extracted and debugged netlists to meet with design specifications, identifying and resolving design bugs through iterative testing.
- Developed custom testbenches and simulation scripts in Python and TCL, automating critical stages of the verification process.

Programmer Analyst | Network Optimization and Automation
Cognizant Technology Solutions, India Nov 2020 - Dec 2021

- Optimized low-latency data transmission and real-time processing pipelines, reducing packet delay by 20% and increasing throughput by 15%, ensuring efficient data flow for high-speed applications.
- Performed performance profiling and bottleneck analysis on high-speed data processing workflows, optimizing execution latency and processing overhead for real-time embedded systems.
- Automated system validation, test case generation, and debugging workflow using Python, reducing manual effort by 40%.