**Name: S Dinesh**

**Roll no: 317126510170**

**Section: CSE-C**

**CA Assignment - 2**

**Exploiting ILP in Intel Core i7:**

Pipelining: An implementation technique in which multiple instructions are overlapped in execution, much like an assembly line.

• Superscalar: Dynamic multiple-issue processors are also known as superscalar

Processors

1. Multiple Issue: launch multiple instructions in every pipeline stage. (Patterson and Hennessy, 2014, p 332)
2. Dynamic pipeline scheduling: Many superscalars extend the basic framework of dynamic issue decisions to include dynamic pipeline scheduling... [which] chooses which instructions to execute next, possibly reordering them to avoid stalls

• Out-of-order execution: A situation in pipelined execution when an instruction blocked from executing does not cause the following instructions to wait.

1. In-order commit: A commit in which the results of pipelined execution are written to the programmer visible state in the same order that instructions are fetched.

• Register renaming: The renaming of registers by the compiler or hardware to remove anti-dependences.

• Speculation: An approach whereby the compiler or processor guesses the outcome

of an instruction to remove it as a dependence in executing other instructions.

1. Branch prediction: A method of resolving a branch hazard that assumes a given outcome for the branch and proceeds from that assumption rather than waiting to ascertain the actual outcome.

**ARM Cortex A8 :**

* ARM refers to Cortex-A8 as application processors
* Embedded processor running complex operating system
  + Wireless, consumer and imaging applications
  + Mobile phones, set-top boxes, gaming consoles automotive navigation/entertainment systems
* Three functional units
* Dual, in-order-issue, 13-stage pipeline
  + Keep power required to a minimum
  + Out-of-order issue needs extra logic consuming extra power
* Figure 14.11 shows the details of the main Cortex-A8 pipeline
* Separate SIMD (single-instruction-multiple-data) unit

10-stage pipeline

The A8 is a dual issue, statically scheduled with dynamic issue detection which allows the processor to issue one or two instructions per clock.

the pipeline uses a simple two-issue statically scheduled superscalar to allow reasonably high clock rate with low power

the A8 uses a dynamic branch predictor and incorrect prediction results in 13 cycle penalty as the pipeline is flushed.

**ILP in ARM Cortex A8 :**

**Deeper Pipeline**: For pipeline, the speed is limited by the length of the longest stage, and the longest stage is set to be the standard one cycle time. For the deeper pipeline, the time of the new sub-stage is small. The smaller time resolution therefore leads to less time to complete one instruction.

**Output dependency**: An output dependency occurs if two paralleled instructions are writing into the same location. An error occurs if the second instruction implement before the first one.

**Anti-dependency**: An anti-dependency exists if an instruction uses a location as an operand while a following one is writing into that location; if the first one is still using the location when the second one writes into it, an error occurs.