
National Institute of Technology Karnataka, Surathkal
Department of Electronics and Communication Engineering

# RF Mini Project

## Analog Front end for Passive UHF RFID tag

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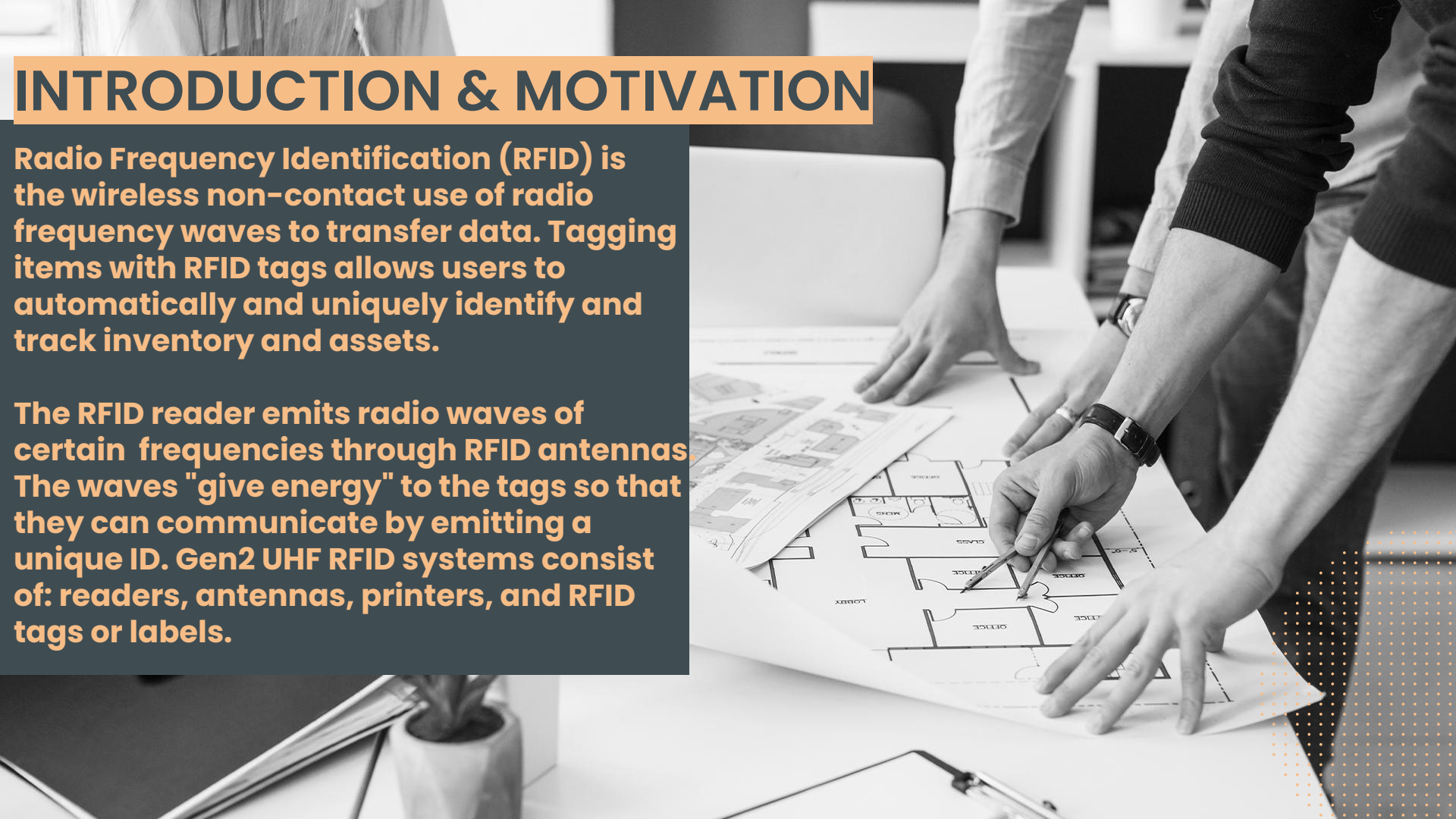
# INTRODUCTION & MOTIVATION

Radio Frequency Identification (RFID) is the wireless non-contact use of radio frequency waves to transfer data. Tagging items with RFID tags allows users to automatically and uniquely identify and track inventory and assets.

The RFID reader emits radio waves of certain frequencies through RFID antennas. The waves "give energy" to the tags so that they can communicate by emitting a unique ID. Gen2 UHF RFID systems consist of: readers, antennas, printers, and RFID tags or labels.

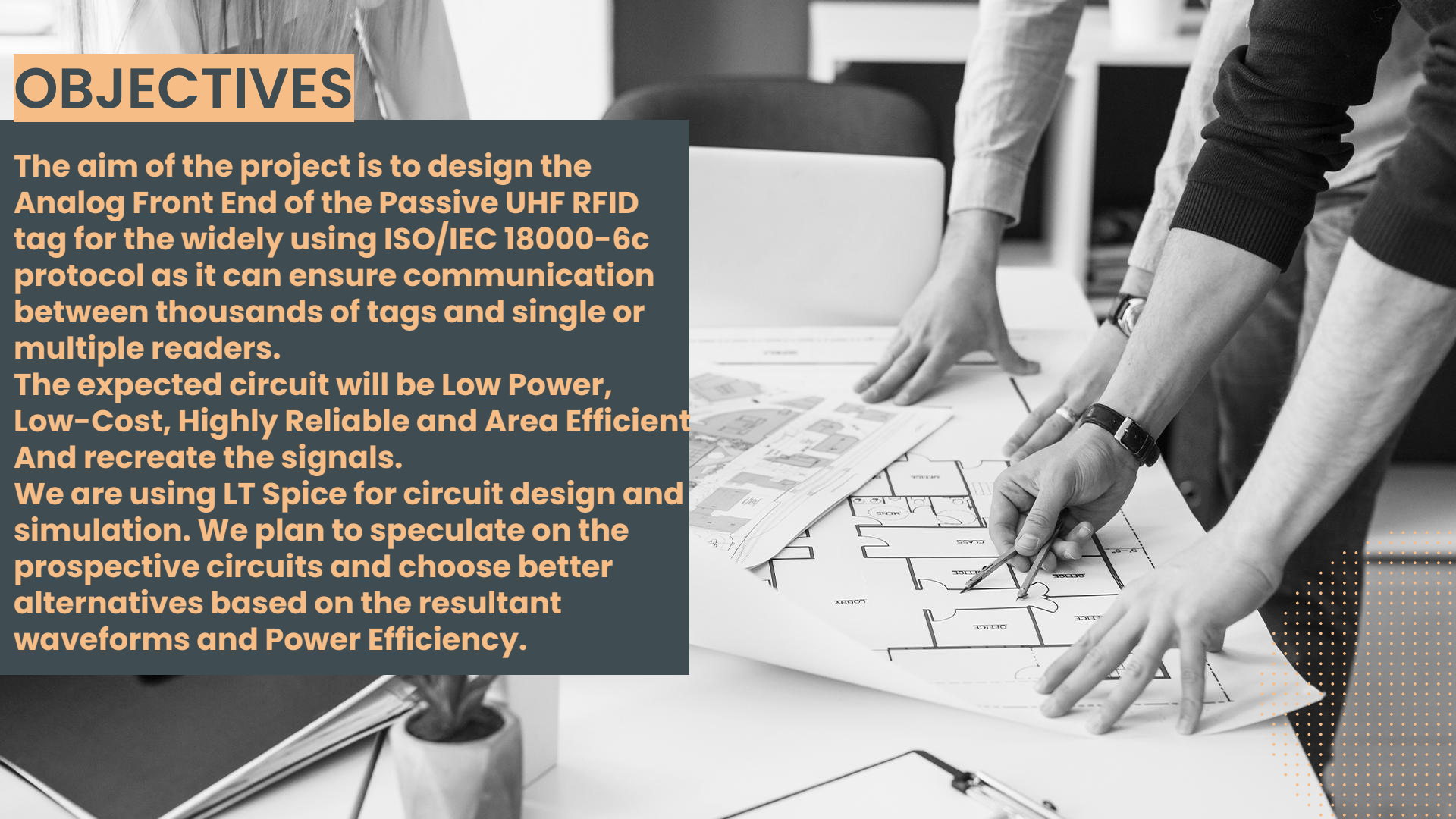


# OBJECTIVES

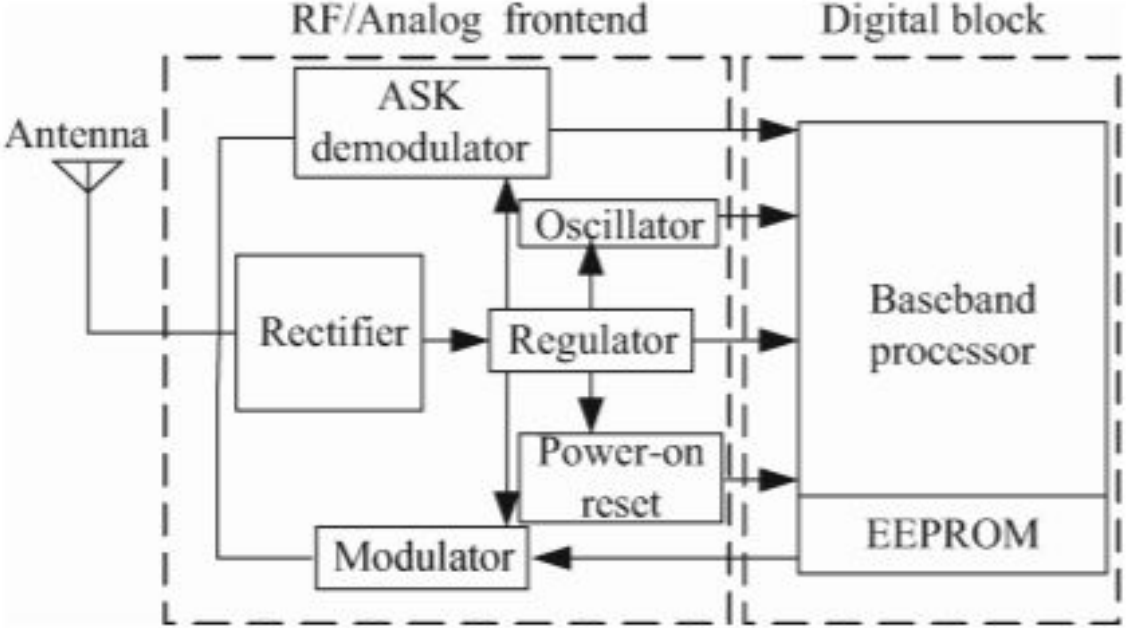
The aim of the project is to design the Analog Front End of the Passive UHF RFID tag for the widely using ISO/IEC 18000-6c protocol as it can ensure communication between thousands of tags and single or multiple readers.

The expected circuit will be Low Power, Low-Cost, Highly Reliable and Area Efficient And recreate the signals.

We are using LT Spice for circuit design and simulation. We plan to speculate on the prospective circuits and choose better alternatives based on the resultant waveforms and Power Efficiency.



# Block Diagram of the proposed UHF RFID Tag



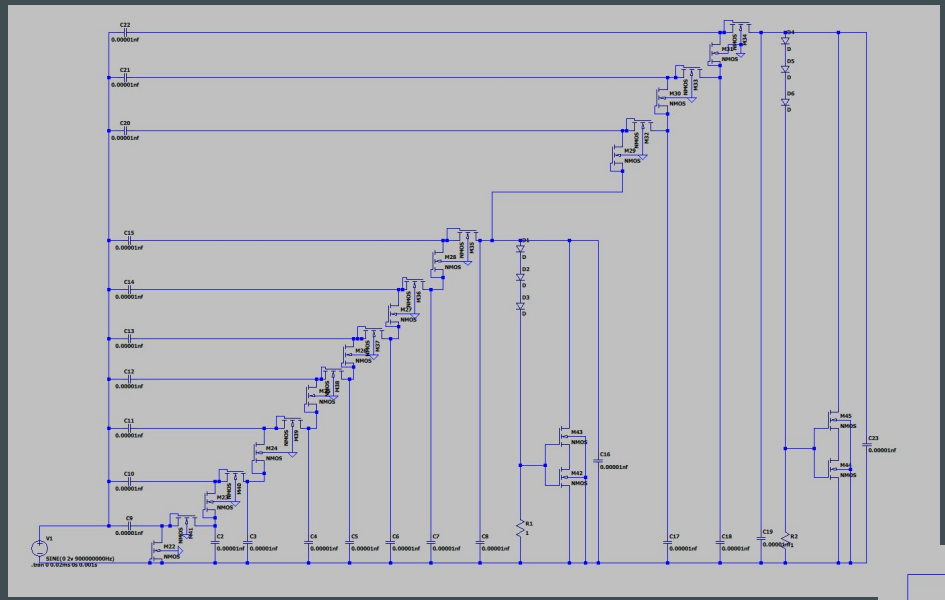
# CIRCUIT DESIGN IN LT SPICE, SIMULATION & EXPLANATION

## Voltage Rectifier

The rectifier circuit uses the traditional Dickson rectifier structure. The original circuit is a diode-connected rectifier the diodes used are a Schottky barrier diode. In the circuit we are using, NMOSFET which is adopted to replace the Schottky barrier diode, as shown in Fig. This way, the chip's manufacturing cost is reduced, and even power consumption is reduced. In the case of the Schottky diode, we need a cutoff voltage of 0.5v, while in the case of NMOSFET, we will require 0.2v. This is because the Schottky diode is higher than NMOSFET. The rectifier circuit consists of a multi-stage full-wave voltage cascade, discharge circuits and energy storage capacitors. The discharge circuit is added at the output of the rectifier to avoid voltage overdrive. Based on the below circuit the number of stages was decided

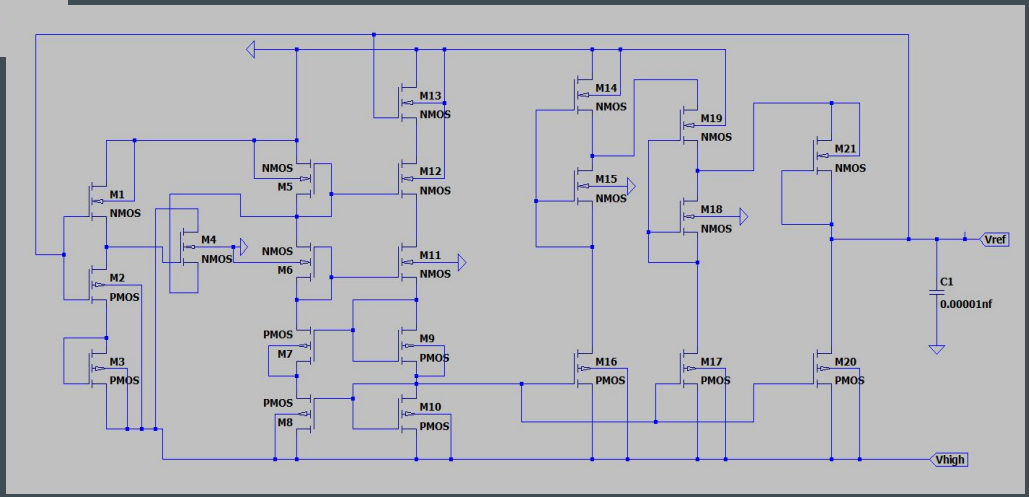
## Voltage Reference

It generates two voltages with opposite temperature coefficients and adds them to produce an output voltage with a near-zero temperature coefficient. The voltage reference consists of MOSFET circuits operated without resistors in the subthreshold region. The Input to the circuit is the v_HIGH of the rectifier, the way the voltage is taken from the ground and in between the voltage divider circuit of M14, M15 and M19 and M18 and the voltage across M21 is added after simplification of the equation and after sizing the mosfets appropriately we can get a non variant V_ref voltage value, The only mosfet that operates in the strong inversion, deep triode region while the rest operate in sub-threshold region



# Voltage Reference

# RECTIFIER



# Voltage Regulator

The voltage regulator helps us provide a stable power supply for the analog front-end as well as other components of the circuit. The rectifier output voltage will vary widely when changing the distance between tag and reader as we increase the distance the value will decrease, As a result, an excellent power supply rejection ratio is needed in the voltage regulator design so that the electronics components can work correctly. The regulator circuit generates two outputs. One is the about 1.8V voltage required for the EEPROM which is the digital backend,and the other is a 1V voltage for other circuits of the analog front end. The error amplifiers are used so that a constant value can be supplied, as it samples values from one stage before the output of the circuit and this value will be below 1v so the error amplifier will be in high, we have also changed the number of mosfets that need to be used as there internal resistance is different as compared to the one used in the research paper

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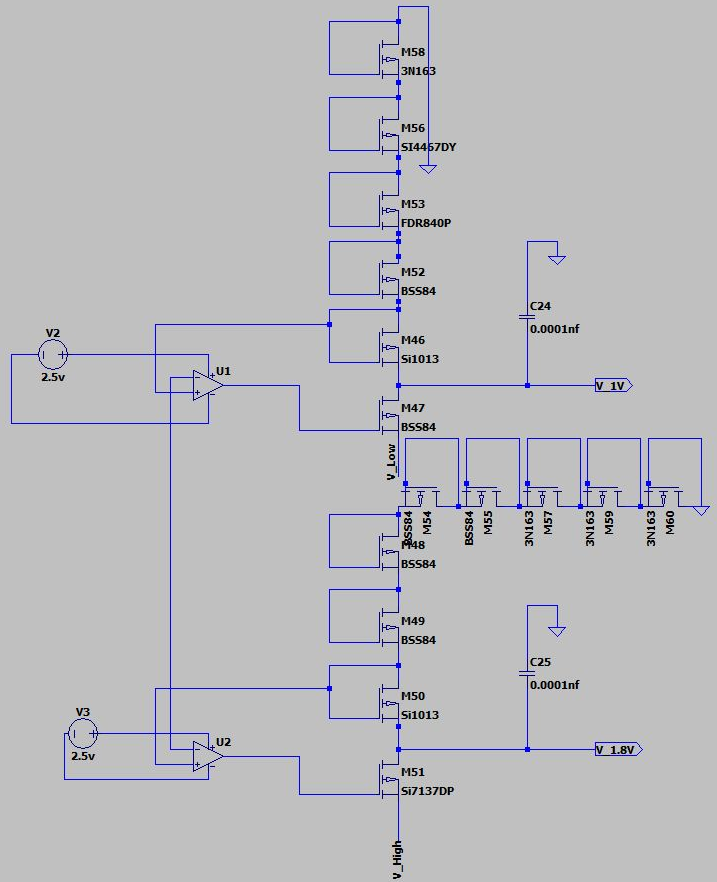

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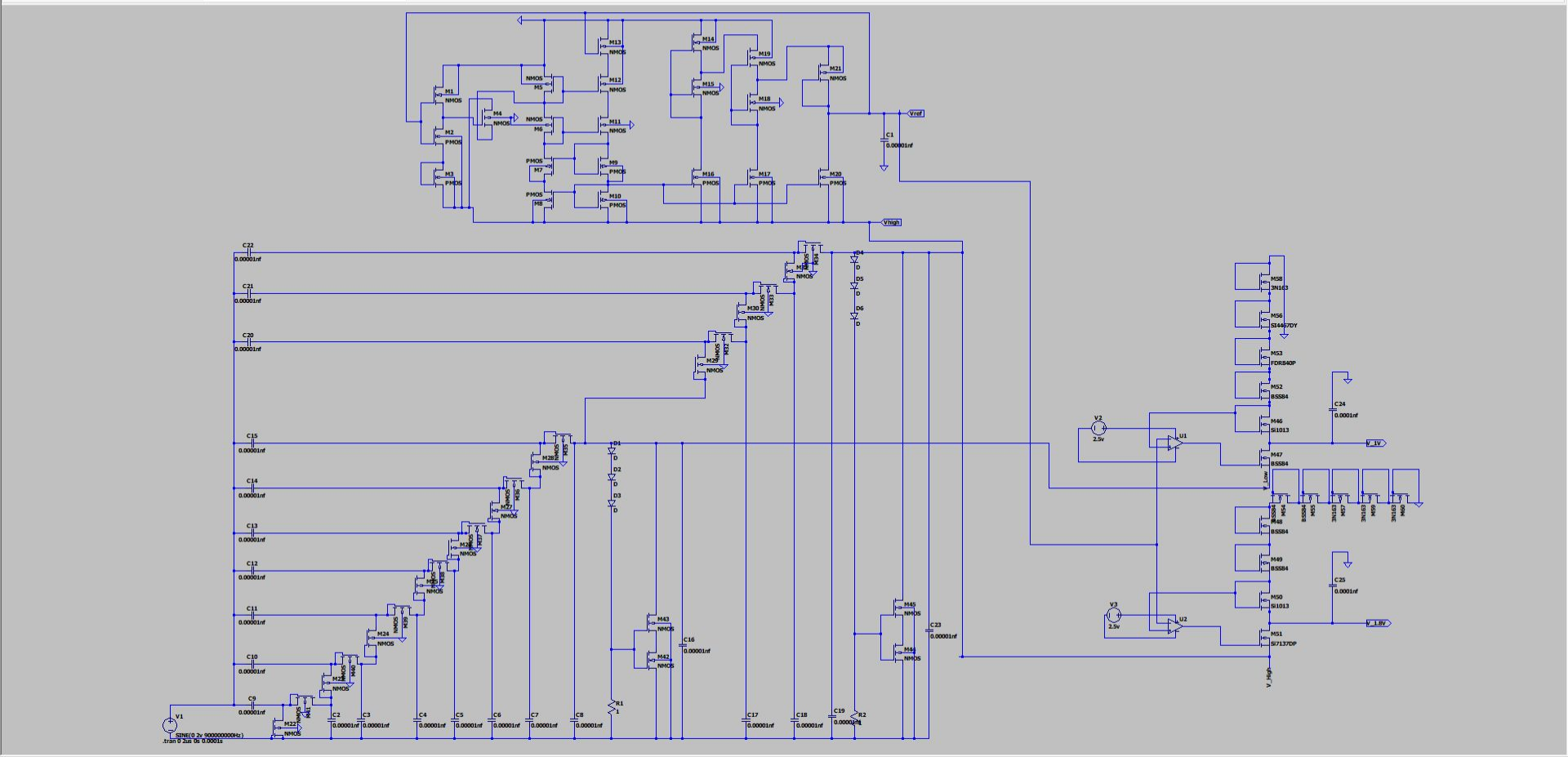
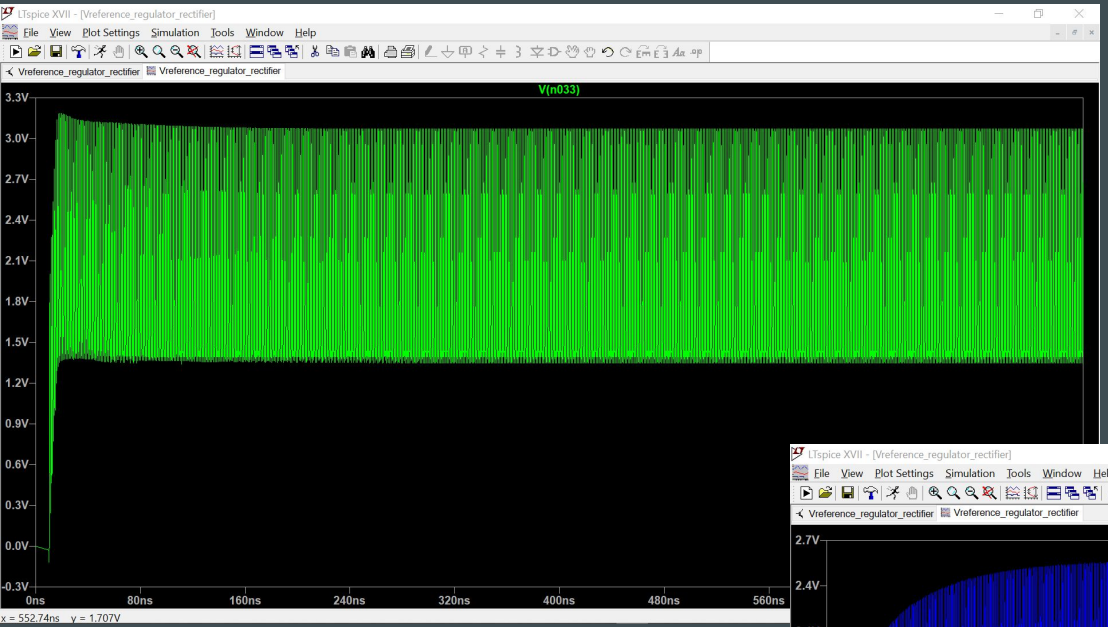


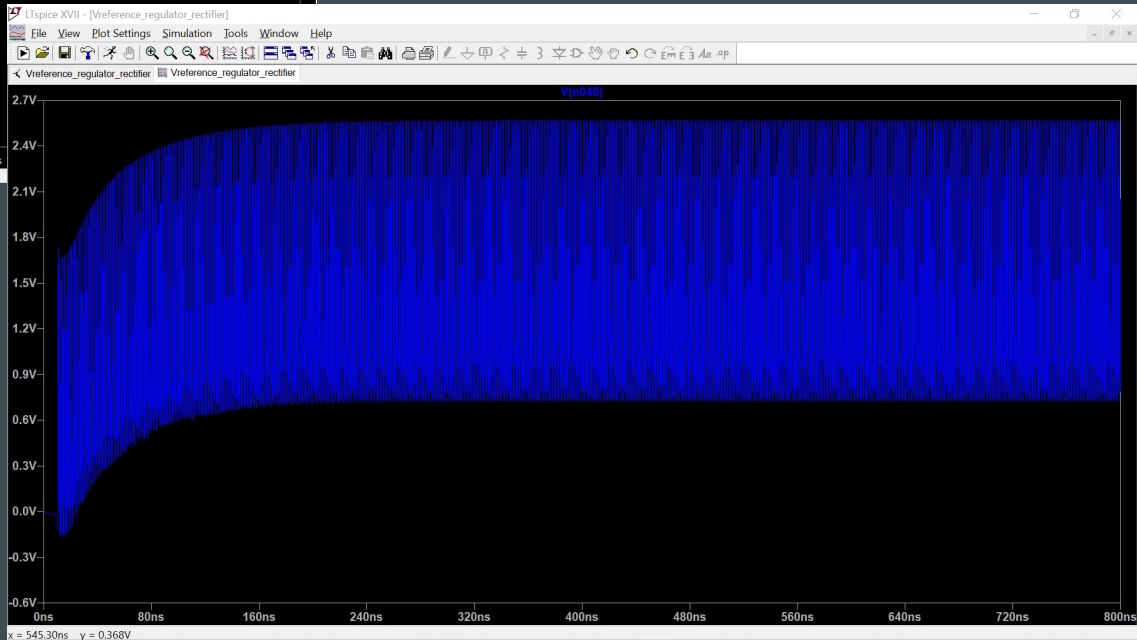
# V_Low Simulation

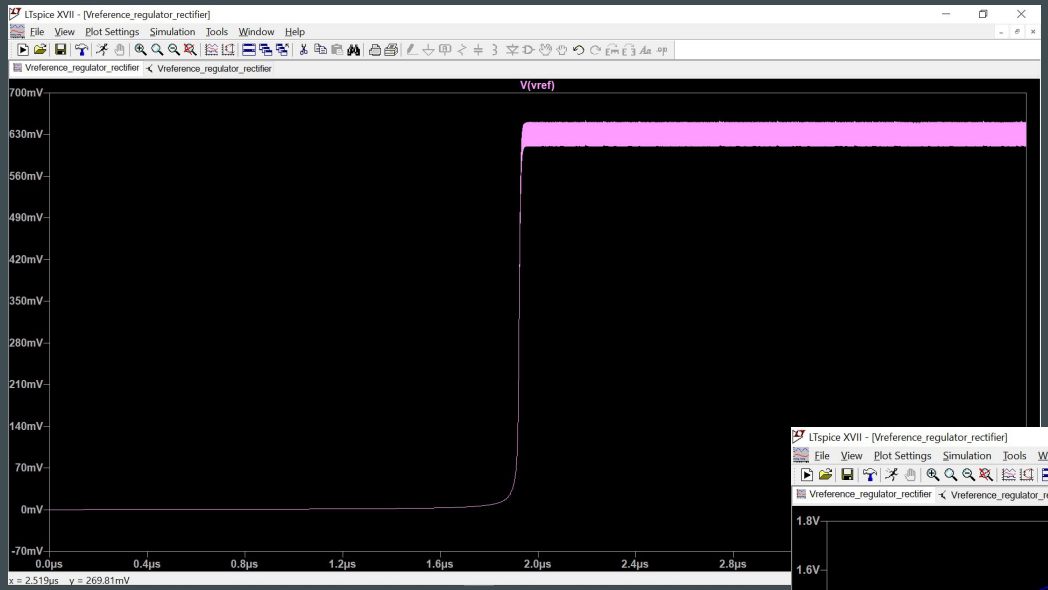
The graph below us shows the V_LOW output after the RF signal has been sent through the rectifier, the circuit basically clamps the signal and averages it at 1.4 volts.And even though we are applying only 0.2 volts the voltage swing is almost 3v and this is due to the high frequence




# V_High Simulation

The graph below us shows the V_HIGH output after the RF signal has been sent through the rectifier, the circuit basically clamps the value and averages it at 2.4 volts. And even though we are applying only 0.2 volts the voltage swing is almost 3v and this is due to the high frequence



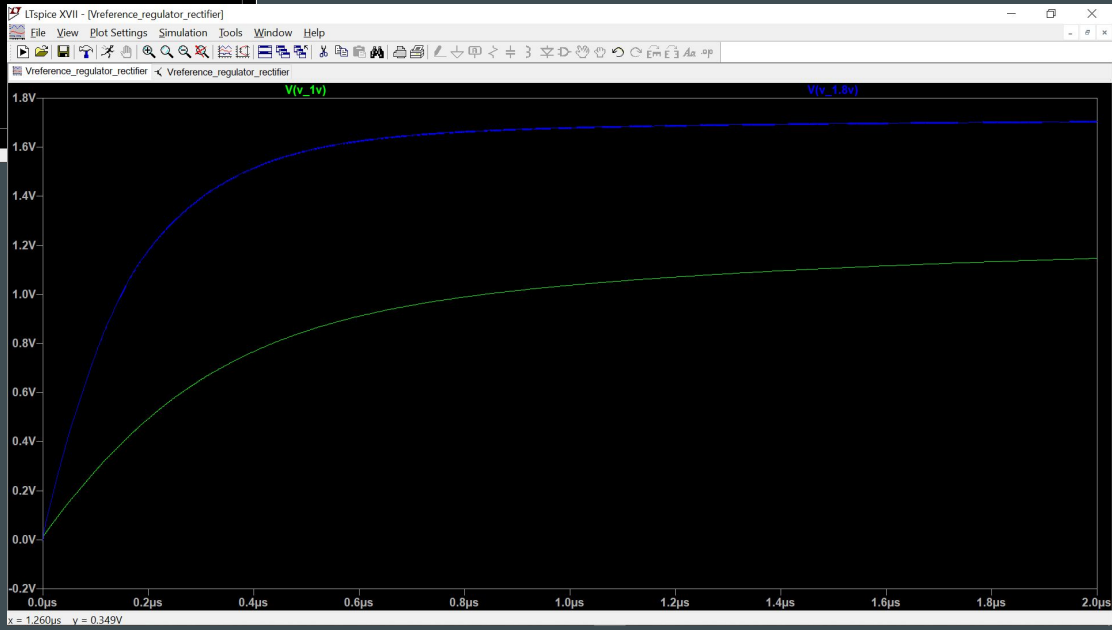



# Combined Simulation

The graph below us shows the V_1.8 & V_1 output after obtaining the V_ref, V_HIGH and V_Low signals they are passed through the comparator as it removes all ac components of the circuit and gives us an almost pure dc output after using the voltage divider NMOSFET circuit.

# V_Ref Simulation

The graph below us shows the V_Ref output after the V_HIGH signal has been sent through the V_ref circuit, we can see that initially the values increases very slowly and when it crossed to the saturation region of the mosfets the output voltage increased till 0.630v which there was a small voltage swing across this value but it can be considered as a dc signal

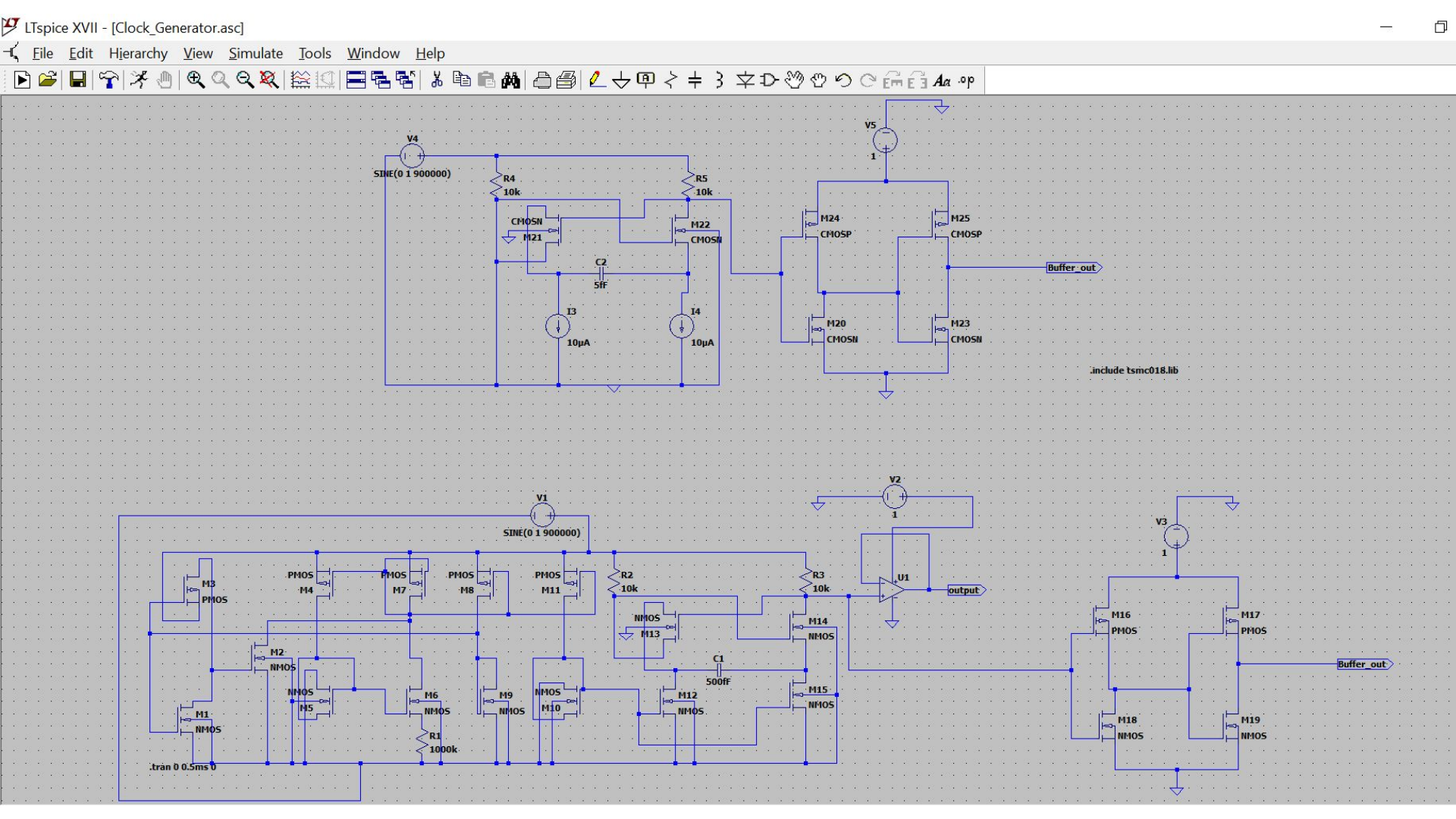


## Clock Generator

We used a relaxation oscillator (OSC), which is not sensitive to the process variation and supply voltage used. The oscillator, shown in Fig  includes a start-up circuit, a bias current generating circuit, an oscillation circuit and a buffer. The oscillator output frequency is closely related to the C, I , delta V .

## Ask Demodulator

The circuit diagram shows the architecture of the ASK demodulator. A single stage rectifier doubler is used to obtain the envelope of the input signal. Following the rectifier is a limiter that provides attenuation at high RF power levels. Finally, the hysteresis comparator compares the data envelope with an average of the data envelope to determine if the data is a “1” or a “0”.


LTspice XVII - [Clock_Generator.asc]
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V4
SINE(0 1 900000)
R4
10k
R5
10k
CMOSN
M21
M22
CMOSN
C2
5fF
I3
10µA
I4
10µA
V5
1
M24
CMOSP
M25
CMOSP
Buffer_out
M20
CMOSN
M23
CMOSN
.include tsmc018.lib
V1
SINE(0 1 900000)
V2
1
V3
1
PMOS
M3
PMOS
M4
PMOS
M7
PMOS
M8
PMOS
M11
R2
10k
R3
10k
U1
output
NMOS
M13
M14
NMOS
C1
500fF
M2
NMOS
NMOS
M5
M6
NMOS
M9
NMOS
NMOS
M10
M12
NMOS
M15
NMOS
M1
NMOS
R1
1000k
.tran 0 0.5ms 0
M16
PMOS
M17
PMOS
Buffer_out
M18
NMOS
M19
NMOS

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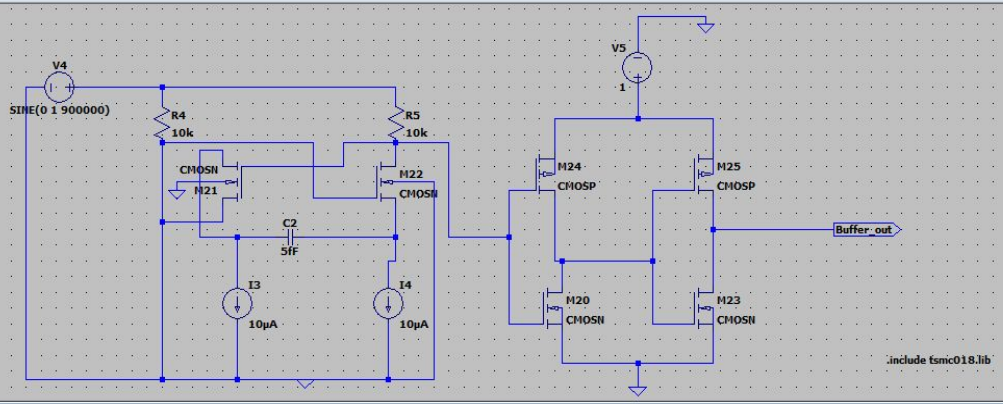
Clock_Generator.asc

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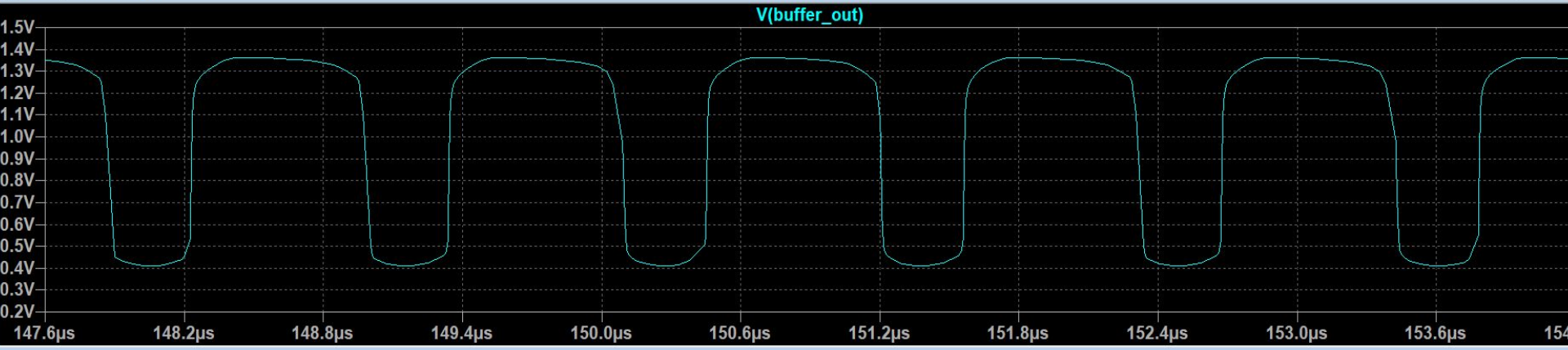

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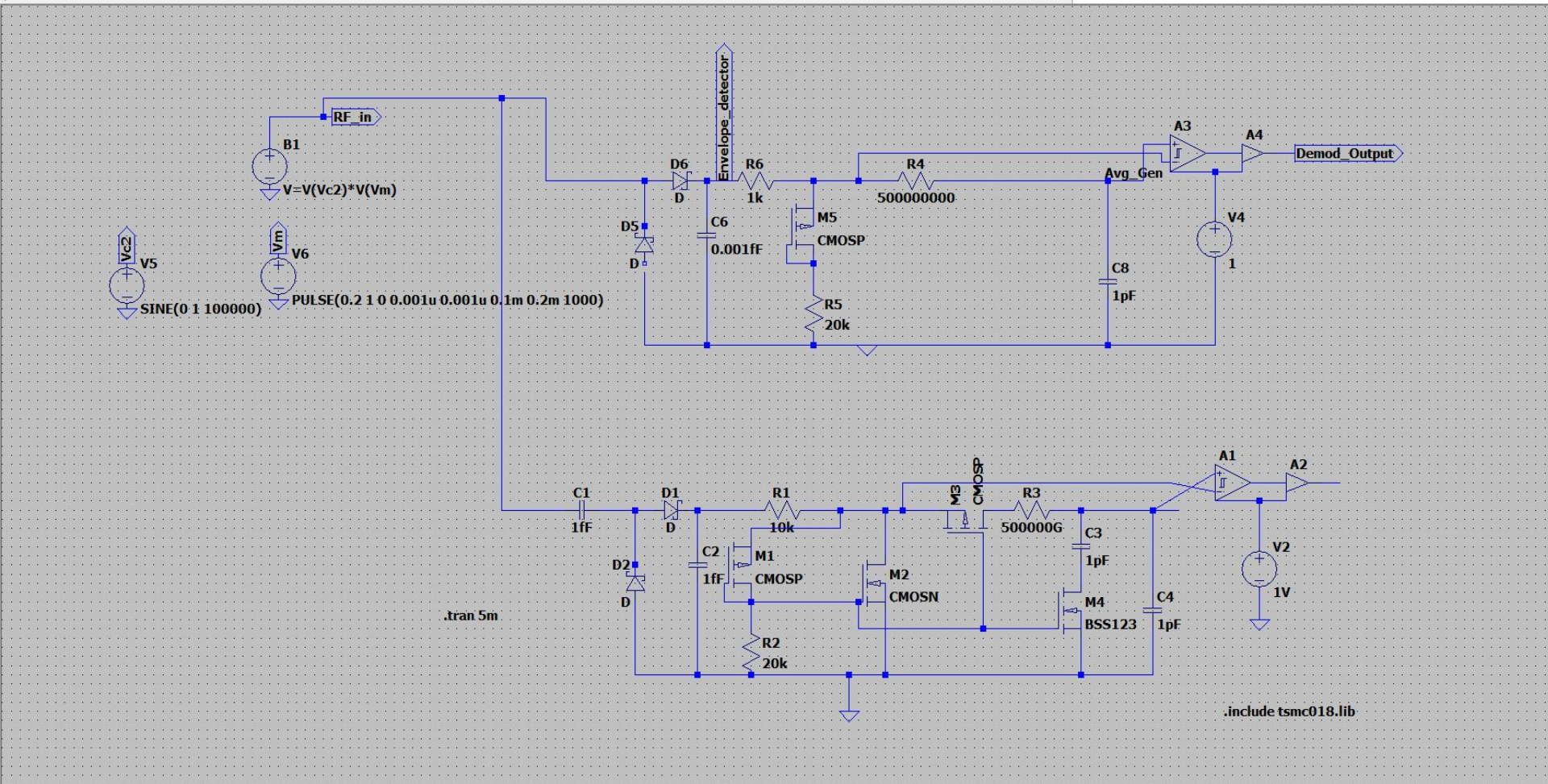

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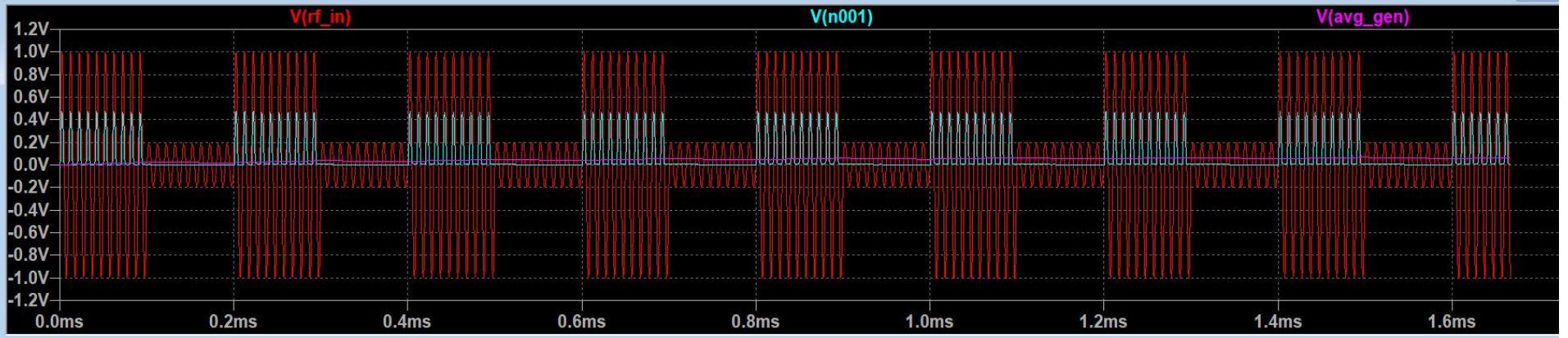
Demodulator.raw

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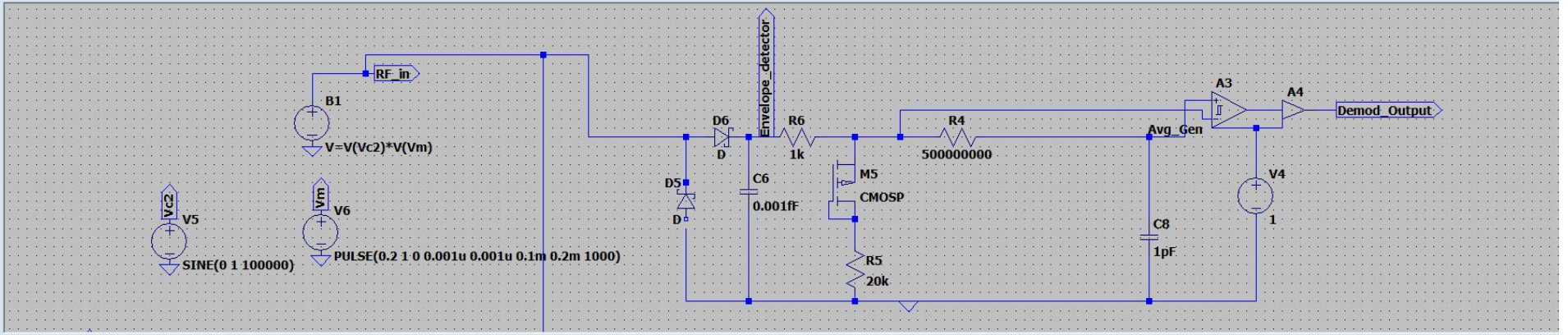

# CONCLUSION & FUTURE WORK

Through our project, we have designed a passive UHF RFID Tag Chip's Analog Front-end, for which we have used several components - The Voltage Regulator (consisting of only MOSFETs- i.e. low power, area efficient & Cost effective), a stable Clock Generator, a novel area-efficient ASK demodulator, and a Voltage Rectifier. These components when put together result in a low cost, area efficient, low power, cost effective and highly reliable Analog Front end.

The future work includes designing the Digital Block of the RFID Tag as given in the Block Diagram.
Another goal can be, to embed a sensor that will be interfaced with our Frontend to retrieve meaningful real life values with our RFID Tag.

# REFERENCES

Wang Yao, Wen Guangjun, Mao Wei, He Yanli, Zhu Xueyong, et al. Design of a passive UHF RFID tag for the ISO18000-6C protocol. IEEE J Solid-State Circuits, 2011

Jianqin Qian, Chun Zhang, Liji Wu, Xijin Zhao, Dingguo Wei, Zhihao Jiang, Yuhui He, et al. A Passive UHF Tag for RFID-based Train Axle Temperature Measurement System

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https://ieeexplore.ieee.org/document/6911276