A Project Report on:

"Design of a Analog Front end for a Passive UHF RFID Tag"

Submitted by:

Chandravaran K (181EC156)

Shruti Masand (181EC245)

V SEM BTECH (ECE)

Under the guidance of

Prof T. Laxminidhi

Department of ECE, NITK Surathkal

in partial fulfilment for the award of the degree
of
Bachelor of Technology
in
Electronics and Communications
at

National Institute of Technology Karnataka, Surathkal

November 2020

TABLE OF CONTENTS

INTRODUCTION **2**
RECTIFIER 3
VOLTAGE REFERENCE 4
REGULATOR 4
CLOCK GENERATOR 5
ASK DEMODULATOR 5

OBJECTIVES **6**

LT SPICE CIRCUIT DESIGN AND EXPLANATION **7**
RECTIFIER 7
VOLTAGE REFERENCE 9
VOLTAGE REGULATOR 10
CLOCK GENERATOR 11
ASK DEMODULATOR 12

SIMULATION/RESULTS **13**
Full Circuit 13
V_HIGH 14
V_LOW 14
V_REFERENCE 15
V_1V and V_1.8V 15
CLOCK GENERATOR 16
ASK DEMODULATOR 16

CONCLUSION & FUTURE SCOPE **17**

REFERENCES **18**

Introduction

Radio Frequency Identification (RFID) is the wireless non-contact use of radio frequency waves to transfer data. Tagging items with RFID tags allows users to automatically and uniquely identify and track inventory and assets.
The RFID reader emits radio waves of certain frequencies through RFID antennas. The waves "give energy" to the tags so that they can communicate by emitting a unique ID. Gen2 UHF RFID systems consist of: readers, antennas, printers, and RFID
tags or labels.

A brief description of the circuits that we have used and modified for obtaining better results for the Analog Front End of our passive UHF RFID Tag Chip is given below.

RECTIFIER

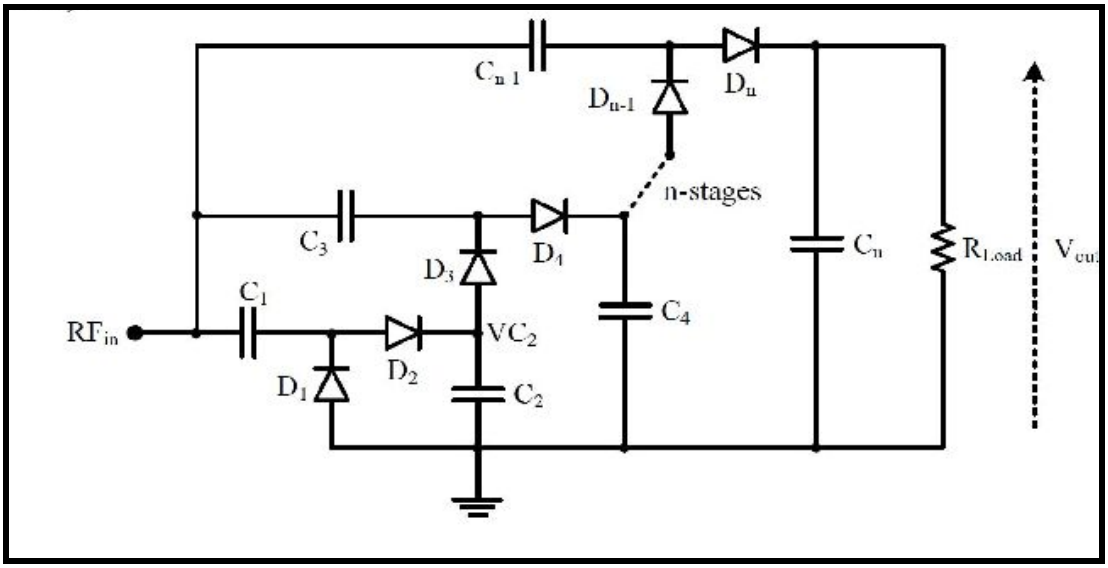


Fig: Dicksons Rectifier Circuit

This is the conventional rectifier that is used in RF systems and it uses Schottky diodes due to the low forward voltage and high switching speed switching, but due to manufacturing difficulties mosfets or other special diodes can be used. The main job of the circuit is to convert the ambient RF signal to a DC value. The capacitors used here are in femto farads as the frequency of input is MHz. The circuit has been taken from [1]. Where we have used 180nm CMOS technology for the circuit which has very low threshold value for the simulation purpose of the project. As mentioned in the paper we have added a discharge circuit so that the switching can occur fast across the capacitor.

VOLTAGE REFERENCE

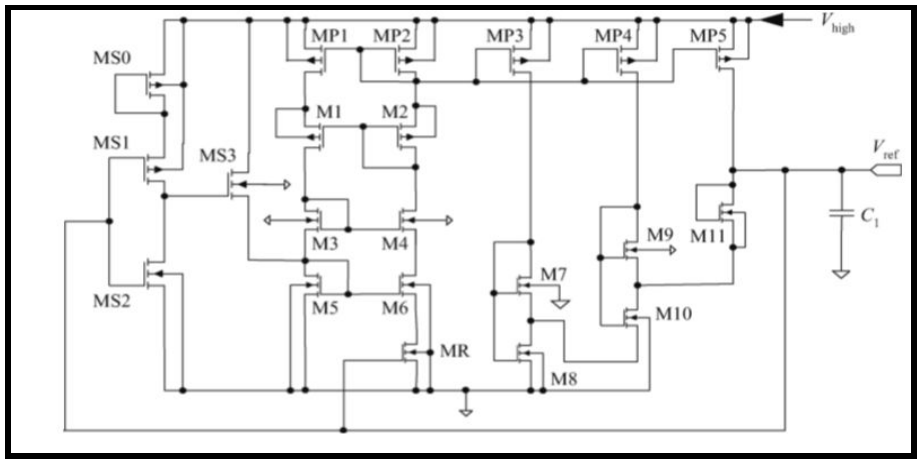


Fig : Voltage Reference Circuit[1]

This is the proposed layout for the V_{Ref} circuit that we are going to use which uses a startup circuit on the left side which has a feedback from output which used to make the system stable and we can see it is being fed into an inverter and those it is a negative feedback. After which we have a set of MOSFETS under MP1 and MP2 which help in creating a constant current source and into the right hand part of the circuit which is the voltage dividing circuit which helps us get the required output.

REGULATOR

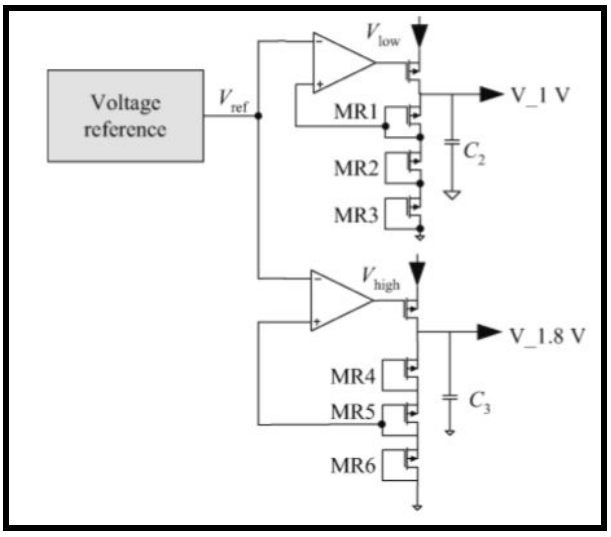


Fig: Voltage Regulator[1]

This is the proposed regulator circuit; the comparators are the main components that help us remove the voltage swings. As from the rectifier shifts the average value of the signal the comparator can use a fixed V_{Ref} to give a study output voltage to the voltage dividing circuit which in our case uses mosfets rather resistance so that manufacturing becomes easy and will have less power consumption as mosfets have very low forward resistance. The number of the MOFETs varies based on the application and the amount of voltage output. This circuit had been taken from the research paper [1].

CLOCK GENERATOR

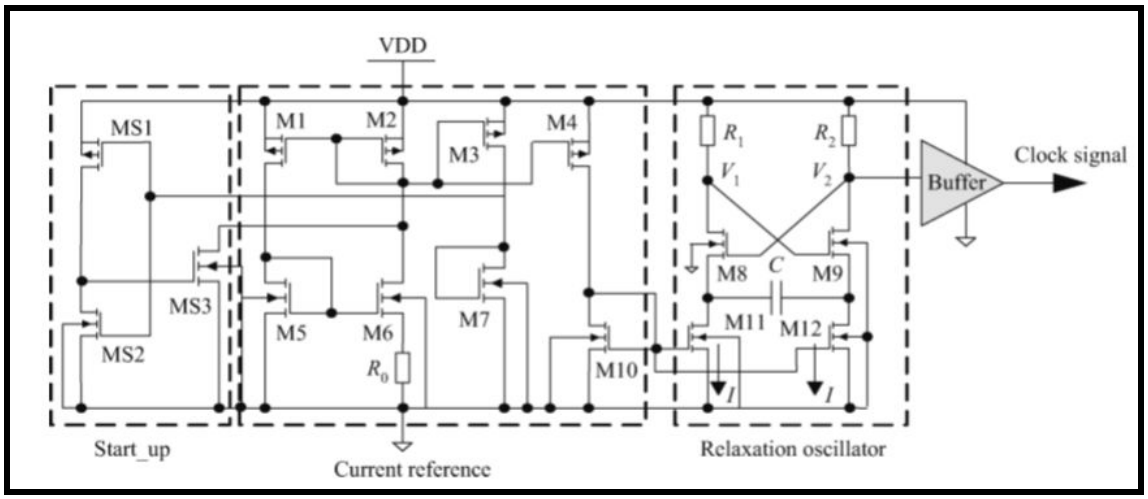


Fig: Clock Generator Circuit[1]

This is the proposed circuit for the Clock generator. It has three parts which are the startup segment necessary to initiate the current flow, the Current reference which employs current mirroring action in order to provide M11 and M12 the current that we desire. This is followed by a relaxation oscillator and a simple buffer. This circuit had been taken from the research paper [1].

ASK DEMODULATOR

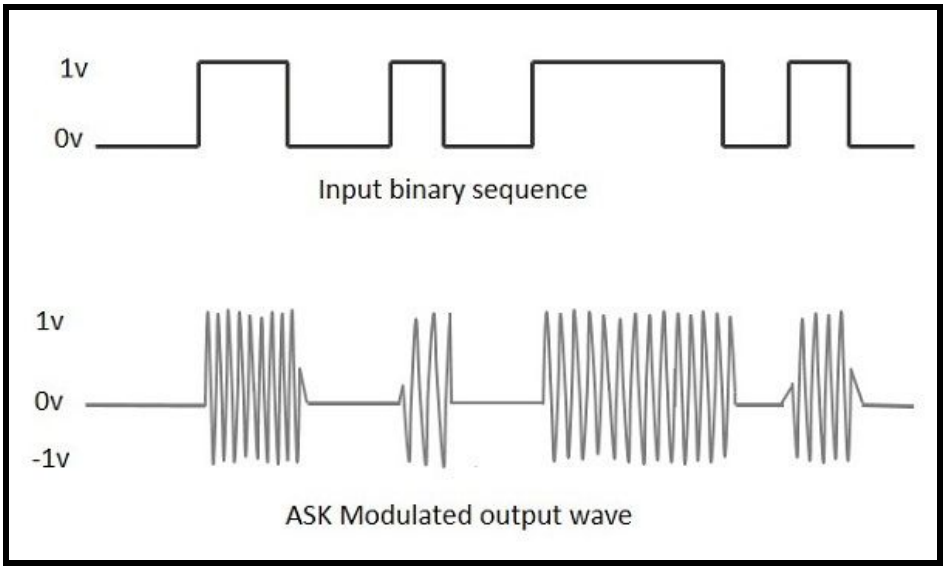


Fig: ASK Modulation

To understand an ASK Demodulator we need to understand the ASK signal and the wave form can be seen in the above picture. And we can see that we have a higher ASK signal wherever there is data and Lower value when there is a zero, this is how the data is modulated and can be transmitted over the medium.

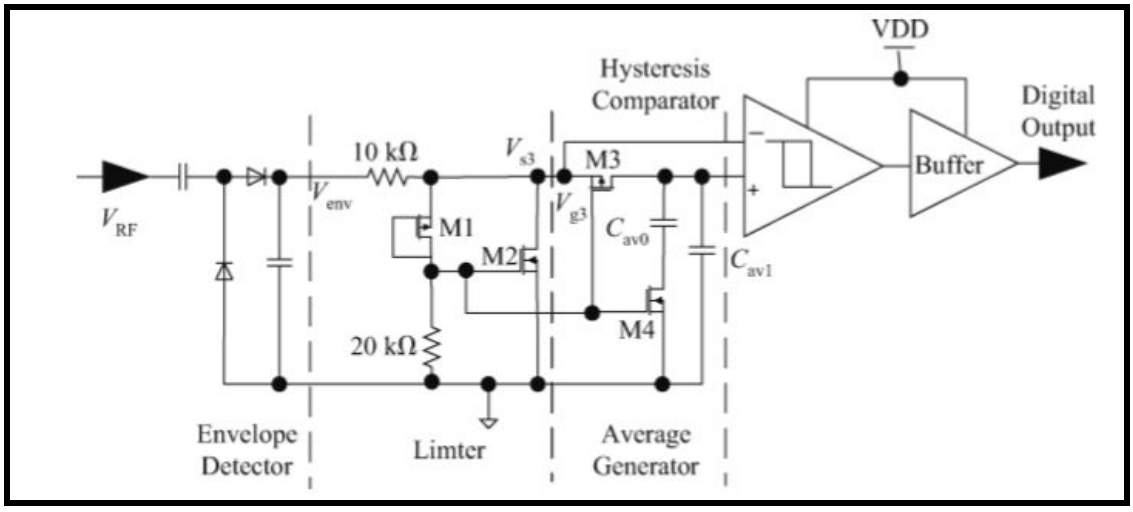


Fig: ASK Demodulator Circuit[1]

This is the proposed circuit for the ASK Demodulator. The Vrf signal is supposed to be a RF modulated wave that is received at the antenna of our RFID Tag. This is followed by the envelope detector and the limiter which provide the noise free message signal extracted from the Vrf signal.This is then compared to the average of the message signal generated through the average generator using a hysteresis comparator, buffered to give the desired output. This circuit had been taken from the research paper [1].

OBJECTIVES

The aim of the project is to design the Analog Front End of the Passive UHF RFID tag for the widely used ISO/IEC 18000-6c protocol as it can ensure communication between thousands of tags and single or multiple readers.

Our aim is to make the final circuit such that it is not only Low Power, Low-Cost and Highly Reliable but also, Area Efficient.
We are using LT Spice for circuit design and simulation. We plan to speculate on the prospective circuits and choose better alternatives based on the resultant waveforms and Power Efficiency.

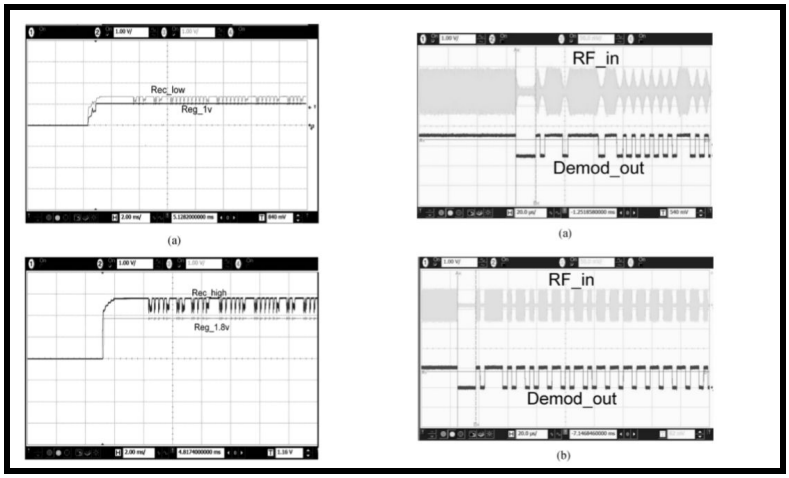


Fig: Required output of Rectifier, Regulator & ASK Demodulator[1]

BLOCK DIAGRAM OF THE PROPOSED UHF RFID

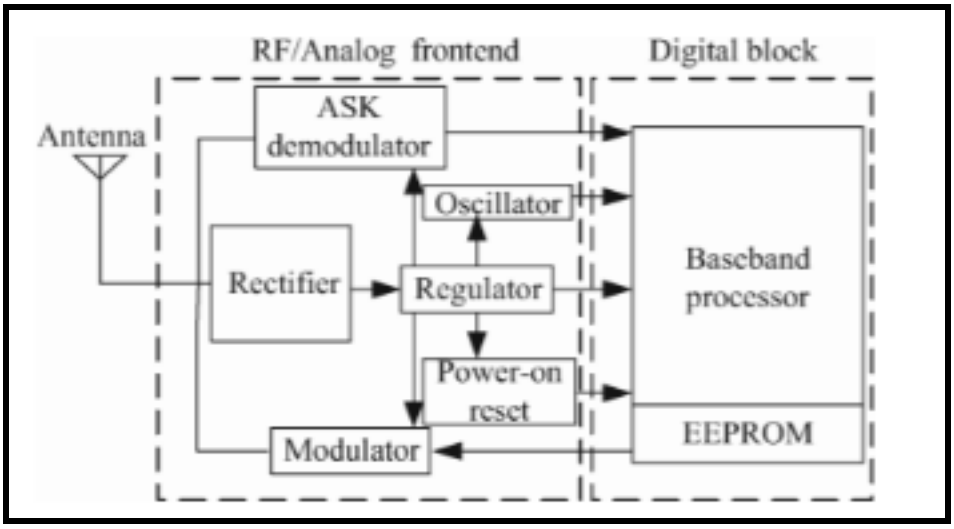
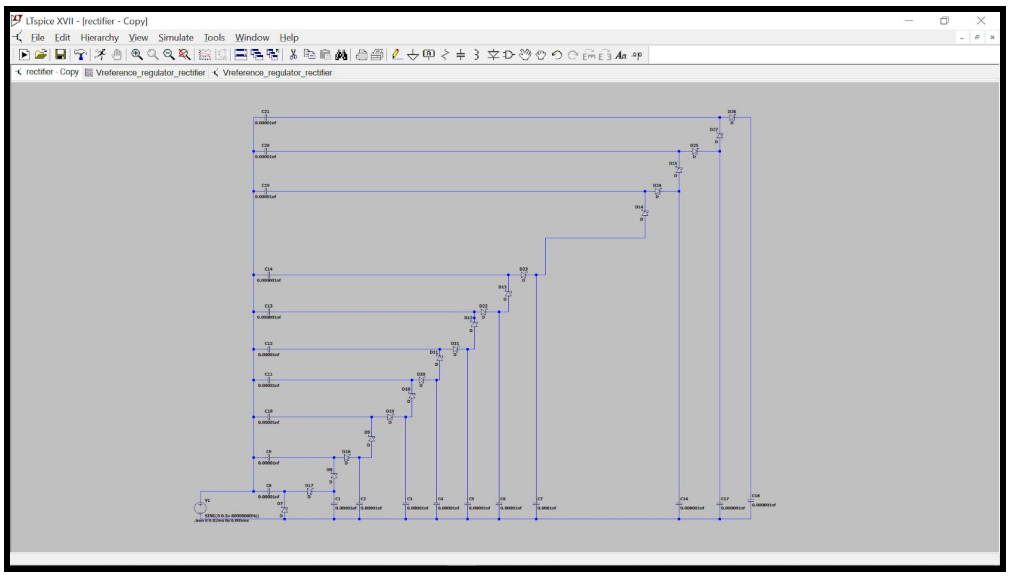


Fig: Block Diagram of Analog Front end[1]

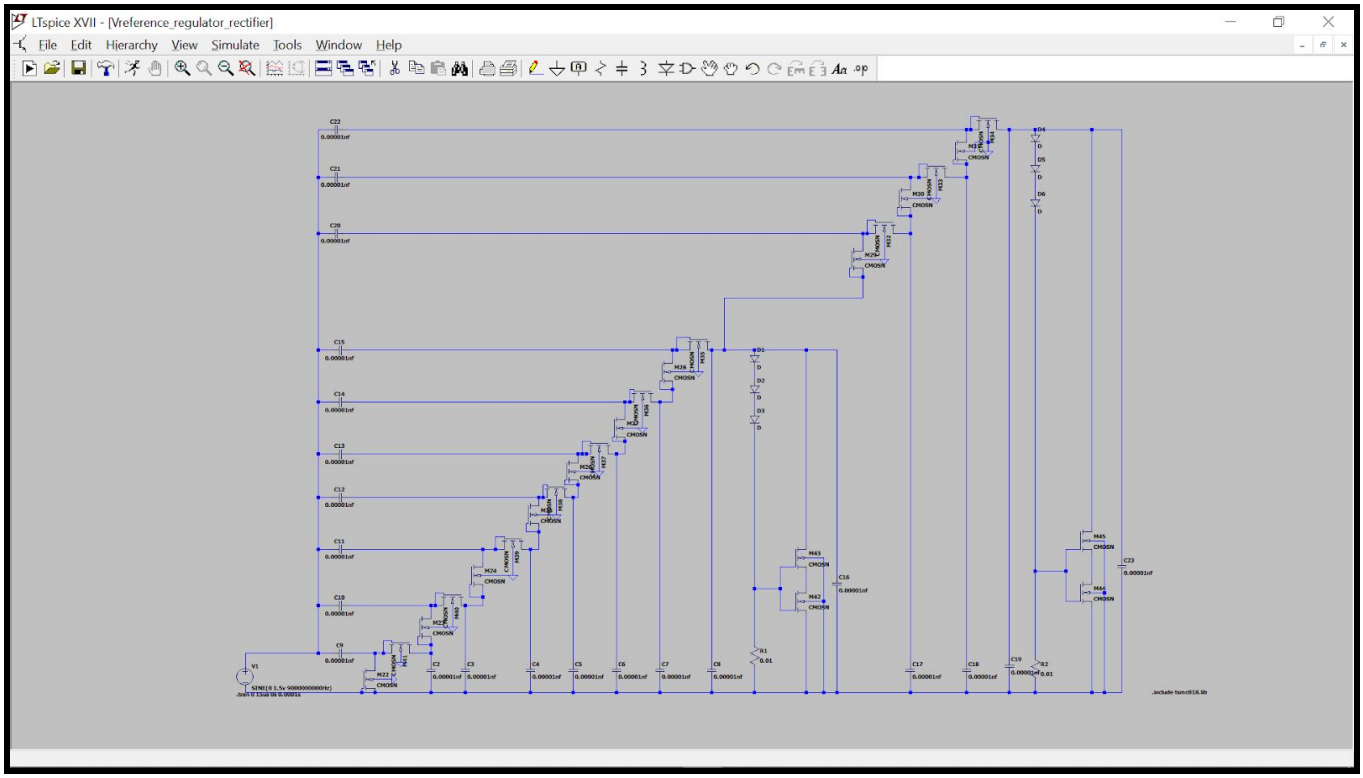
We made the RF analog frontend for the RFID, which includes the Rectifier, Regulator, Oscillator, ASK Demodulator, and Voltage reference; these circuits will basically make up the receiver part of the RFID, and there connection can be shown in the above block diagram, the voltage reference is not shown as it considered a part of the Rectifier, and as we are not making the transmitter circuit therefore we have not designed the modulator circuit and the digital block which is used for the processing of the data.

LT SPICE CIRCUIT DESIGN AND EXPLANATION

RECTIFIER



Fig(1): Rectifier Circuit with Diode



Fig(2): Rectifier Circuit with NMOSFET

The rectifier circuit uses the traditional Dickson rectifier structure. The original circuit is a diode-connected rectifier shown in Fig(1), the diode used as a Schottky barrier diode. In the circuit we are using, NMOSFET is adopted to replace the Schottky barrier diode, as shown in Fig(2). In this way, the chip's manufacturing cost is reduced, and even power consumption is reduced.

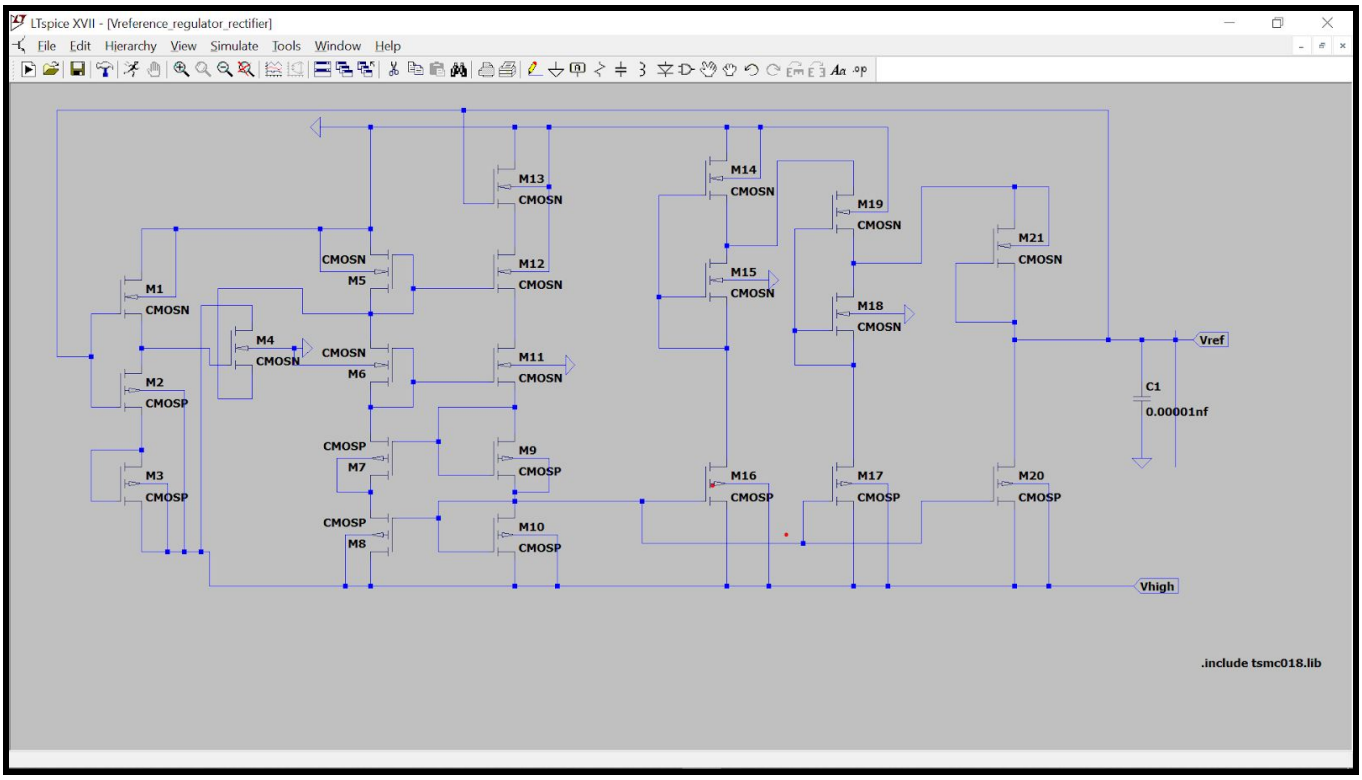
In the case of the Schottky diode, we need a cutoff voltage of 0.5v, while in the case of NMOSFET, we will require 0.2v. This is because the Schottky diode is higher than NMOSFET. The rectifier circuit consists of a multi-stage full-wave voltage cascade, discharge circuits and energy storage capacitors.

The discharge circuit is added at the output of the rectifier to avoid voltage overdrive. Based on the below circuit the number of stages was decided

$$V_{DC} = 2*N*(V_{RF}-V_{MOS})$$

The V_{DC} , V_{RF} and V_{MOS} are known and on back calculations we have a 7 stage for V_{LOW} and 10 stages for V_{HIGH}. We are using 180nm technology with a very low V_{MOS}

1) VOLTAGE REFERENCE



Fig(3): Voltage Reference Circuit

The above circuit takes two generated voltages with opposite temperature coefficients and adds them to produce an output voltage with a near-zero temperature coefficient, this is very important for the circuit as there will always be changes in the surrounding temperature so it is important we do this for a V_{ref} generation. The input of the circuit is the V_{HIGH} which is generated by a rectifier shown before. The voltage reference consists of MOSFET circuits operated without resistors in the subthreshold region. This circuit's output is directly fed to the Voltage Regulator. The equation of V_{ref} can be given as follows

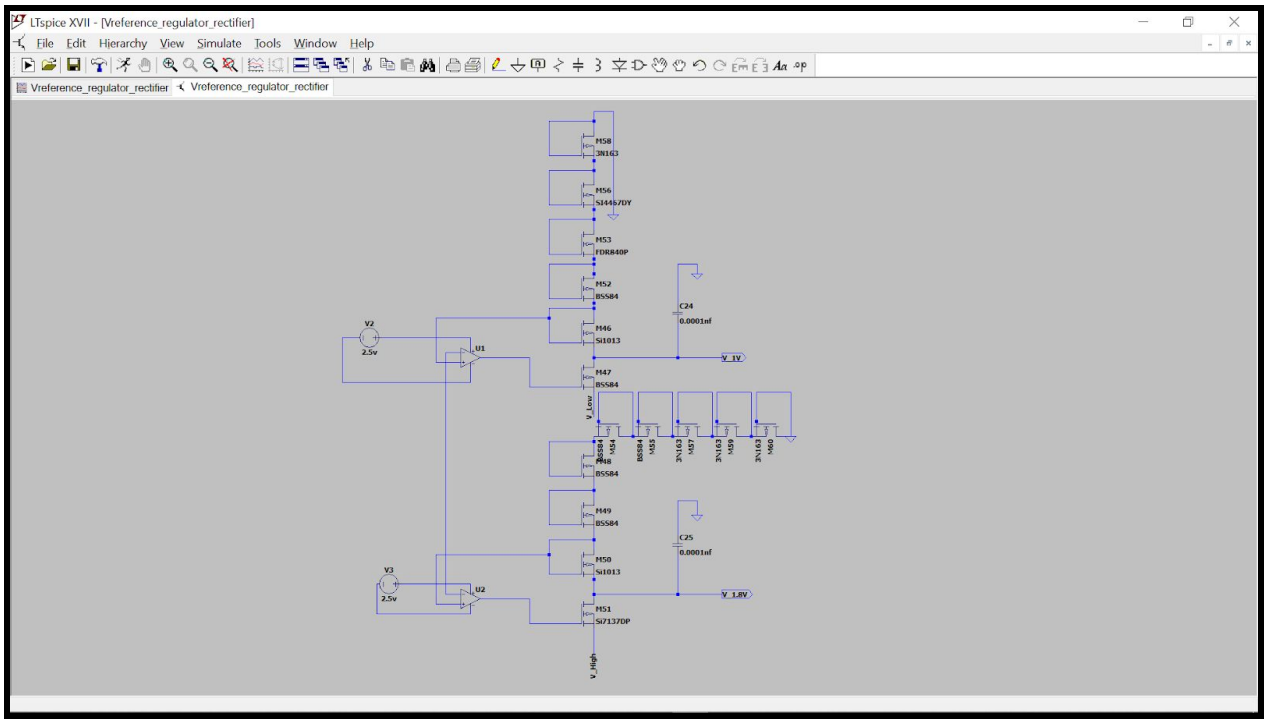
$$V_{ref} = V_{M14} - V_{M15} + V_{M19} - V_{M18} + V_{M21}$$

The above equations can be simplified to

$$V_{ref} = V_{THO} + T[(kn/q)*\ln(2I_b/(K_{14}*I_0) + (kn/q)*\ln(2K_{14}K_{18}/K_{19}K_{21})]$$

Where k is boltzmann constant, V_{tho} is the threshold voltage at 0K, T is the absolute temperature and q is the elementary charge the V_{ref} with 0 temperature can be obtained by adjusting the dimensions of the transistors that are present.

2) VOLTAGE REGULATOR



Fig(4): Voltage Regulator Circuit

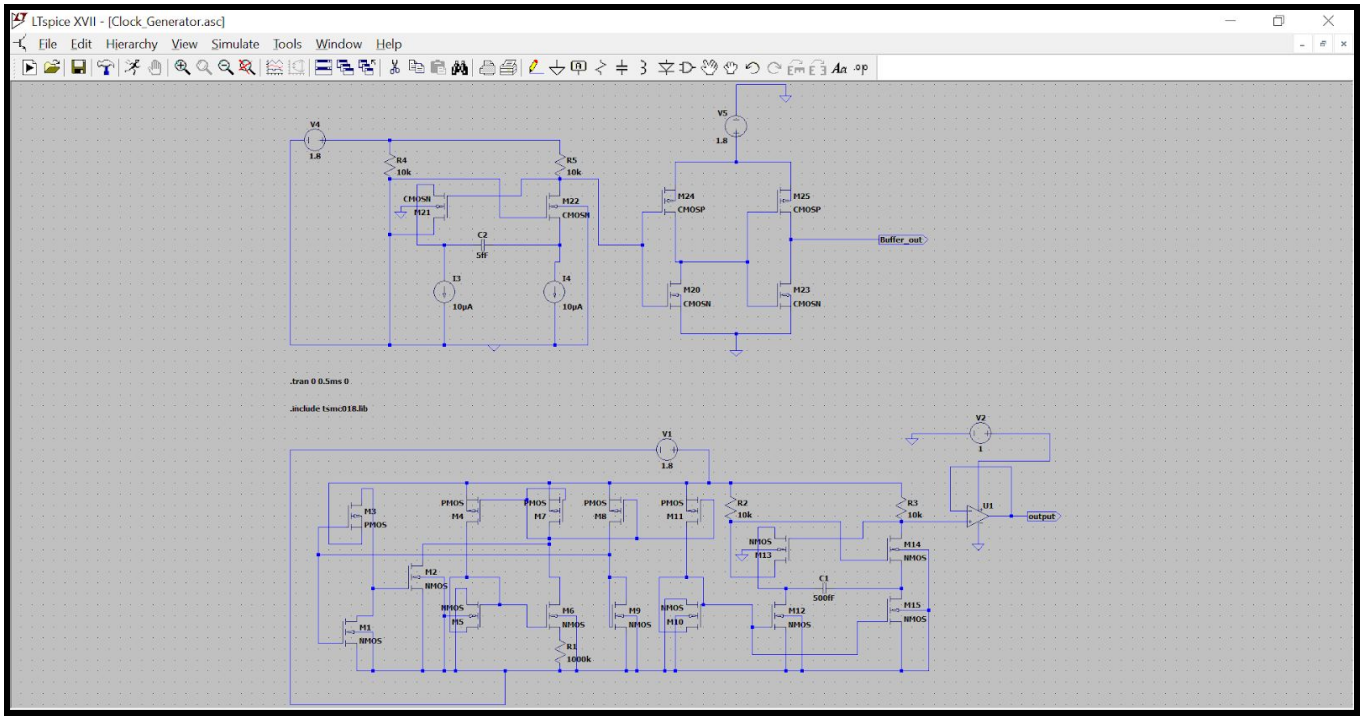
The voltage regulator provides a stable power supply for the front-end and the other circuits. The rectifier output voltage will vary widely when changing the distance between tag and reader. As a result, an excellent power supply rejection ratio is needed in the voltage regulator design. The regulator circuit generates two outputs.

One is the 1.8V voltage required for the EEPROM, and the other is a 1V voltage for other circuits. The error amplifiers are used so that a constant value can be supplied, as it samples values from one stage before the output of the circuit and this value will be below 1v so the error amplifier will be high.

To save on chip area, several diode-connected PMOS transistors play the role of a potential divider and the V_{HIGH} has 9 transistors that are used and we are tapping after one transistor and even V_{LOW} has 6 transistors that are used and similarly the V_{1V} is tapped from the second position.

We are using capacitors at very low values as we are working with frequencies of Mhz. The above 3 circuits are combined together to get an output.

3) CLOCK GENERATOR



Fig(5): Clock Generator Circuit

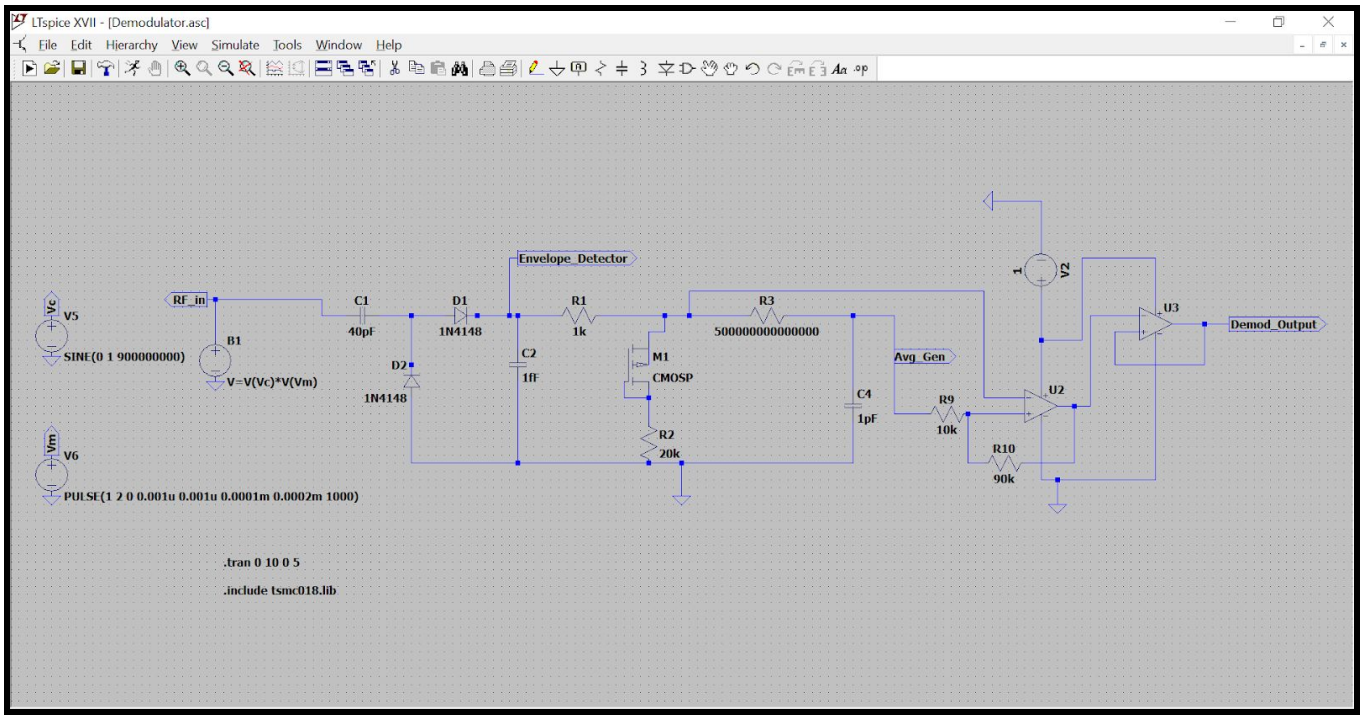
The above shown circuits are 2 interpretations of a Clock Generator.

The lower circuit includes a start-up segment, a bias current reference generating segment, a relaxation oscillator (OSC), which is not sensitive to the process variation and supply voltage used and a buffer. The oscillator output frequency is closely related to the C, I , delta V. The basic requirements for the circuit to function properly are that the MOSFETs, M12 and M15 should be in saturation and M13 and M14 should be in the triode region for effectively receiving and utilising the mirrored current from the current reference segment of the circuit.

The upper circuit is a simpler interpretation of the lower one, where M12 and M15 have been substituted with a constant and ideal current source (as they were expected to be in saturation). It has been made sure with the circuit connections that the other two MOSFETs do operate positively in the triode region for correct functioning. The relaxation oscillator part is then followed by a pair of CMOS inverters back to back in order to supply a more efficient and less area occupying buffer action to our output.

According to the ISO 18000-6c, it is recommended that the clock frequency to be supplied to the digital block needs to be around 1.28Mhz. As can be seen in the simulation figure given later, the frequency of our clock is close to 1.2Mhz. Hence, our circuit operates correctly.

ASK DEMODULATOR



Fig(6): ASK Demodulator Circuit

The circuit diagram shows the architecture of the ASK demodulator.

The circuit design most abundantly used contains a single stage rectifier doubler which is used to obtain the envelope of the input signal. Following the rectifier is a limiter that provides attenuation at high RF power levels. In this circuit, we have not included the Limiter as here, we are providing an ideal RF modulated signal free of any unwanted high noise.

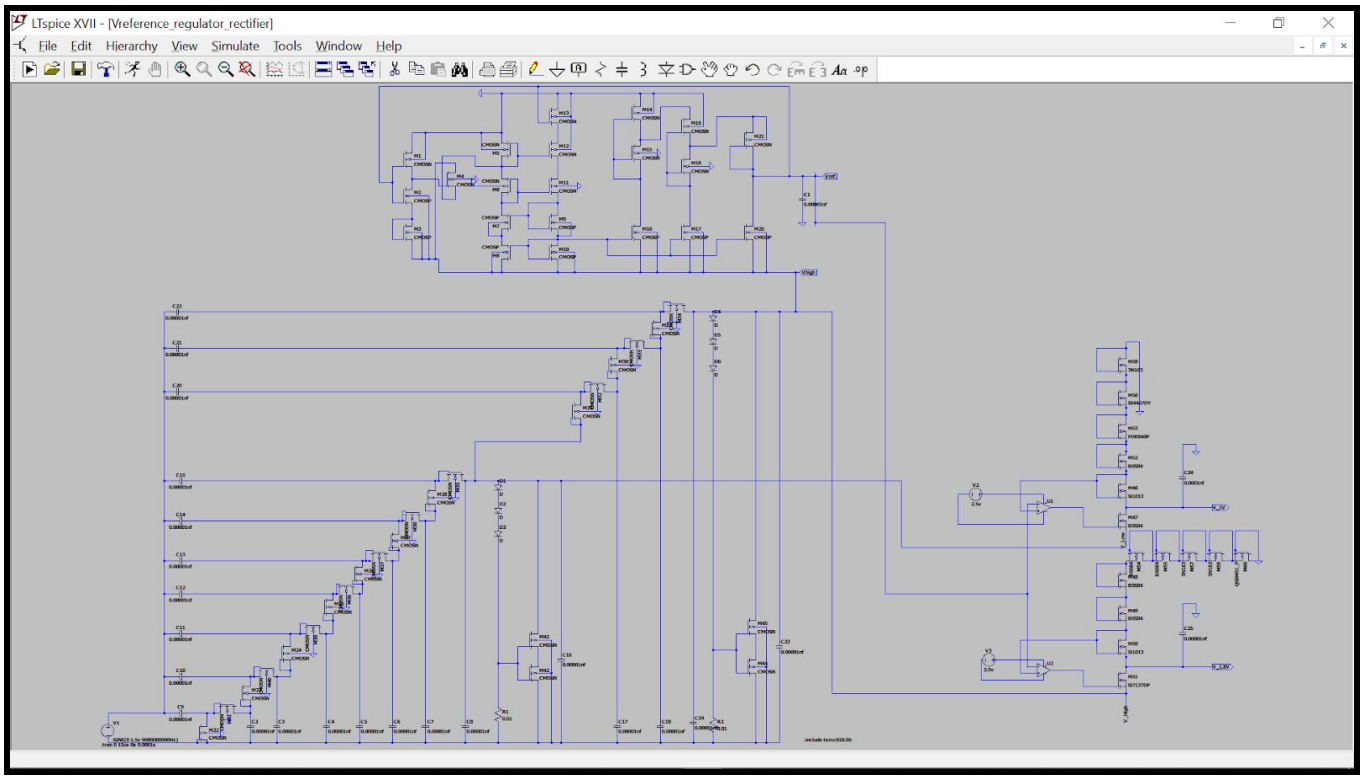
This is followed by the Average generator segment, which in our case employs a Low Pass Filter made using a resistor and a capacitor, whose values have been calculated as per the required period of the signal and keeping in mind that their values depend on the frequency of the message signal that the envelope was carrying. Similarly, the values of the Capacitances in the envelope detector depend on the frequency of the RF modulated signal envelope i.e. the carrier.

Finally, the hysteresis comparator, that has been designed using an opamp, compares the message signal extracted through the envelope detector with the average of the message signal extracted through the average generator to determine if the digital output should be a logical “1” or a “0”. The output of the comparator is then inverted using an opamp which also provides a kind of a buffering action to our output signal.

The resulting waveforms have been shown in the simulation section.

SIMULATION/RESULTS

Full Circuit

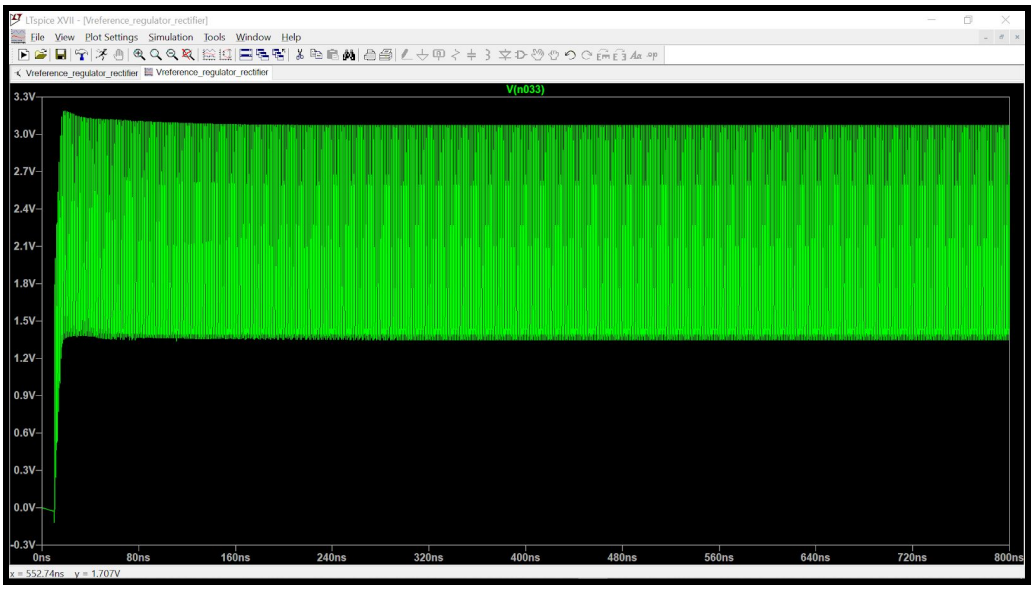


Fig(7): Voltage Regulator, Rectifier & Reference

The above picture is the circuit design of the initial 3 circuits together Rectifier, Voltage Reference and Voltage regulator. The V_{high} is fed to the V_{Ref} and the voltage regulator at once and the We used a relaxation oscillator (OSC), which is not sensitive to the process variation and supply voltage used.

The oscillator, shown in Fig includes a start-up circuit, a bias current generating circuit, an oscillation circuit and a buffer. The oscillator output frequency is closely related to the C, I , delta V_{LOW} is only fed into the Regulator which will give an output of V_{1V} and $V_{1.8V}$.

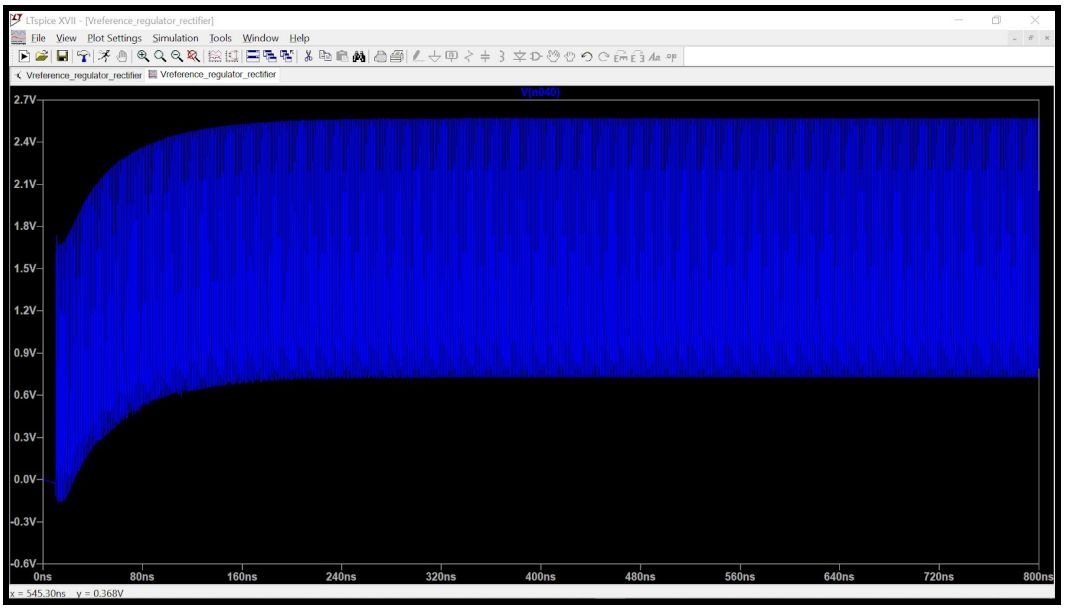
V_HIGH



Fig(8): Simulation output for V_{HIGH}

This is the output of the V_{HIGH} from the Rectifier we can see how the voltage is clamped to a high level due to the NMOSFET and we can see the voltage swing to be very high even though the initial voltage swing is 0.2V this is because of the Rectifier, what is important for us in this circuit is the average value Which comes around 2.4v which is kept as input to the Regulator which removes the voltage swings.

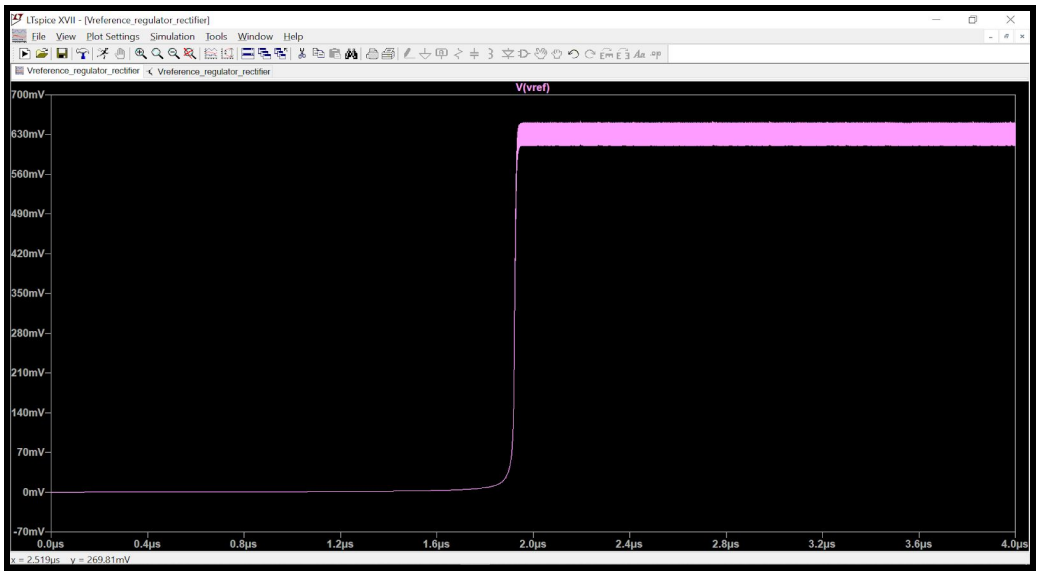
V_LOW



Fig(9): Simulation Output of V_{LOW}

This is the output of the V_{LOW} from the Rectifier we can see how the voltage is clamped to a high level due to the NMOSFET and we can see the voltage swing to be very high even though the initial voltage swing is 0.2V this is because of the Rectifier, what is important for us in this circuit is the average value Which comes around 1.5v which is kept as input to the Regulator which removes the voltage swings.

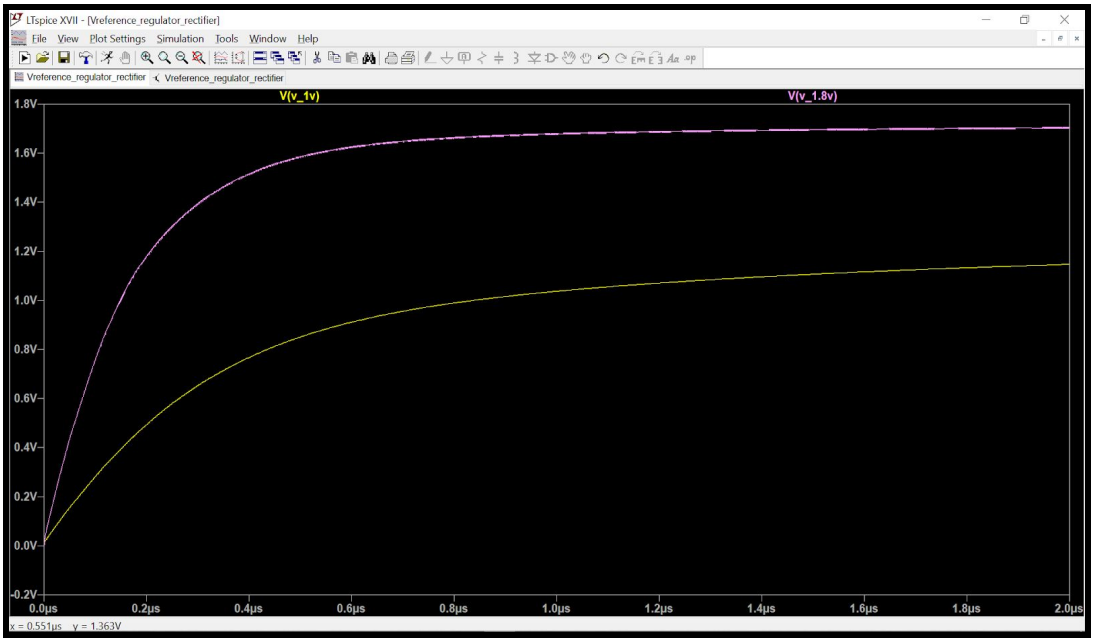
V_REFERENCE



Fig(10): Simulation Output for V_Reference

This waveform is the output of the V_{ref} and we can see that there is no voltage output when the the voltage across the MOSFETS doesn't cross the V_{th} of the MOSFET & as soon as the voltage is crossed the 5 MOSFETS explained in the circuit explanation will start conducting and we'll get the required output from the circuit. There will be small voltage swings due the ac component of the input V_{HIGH}.

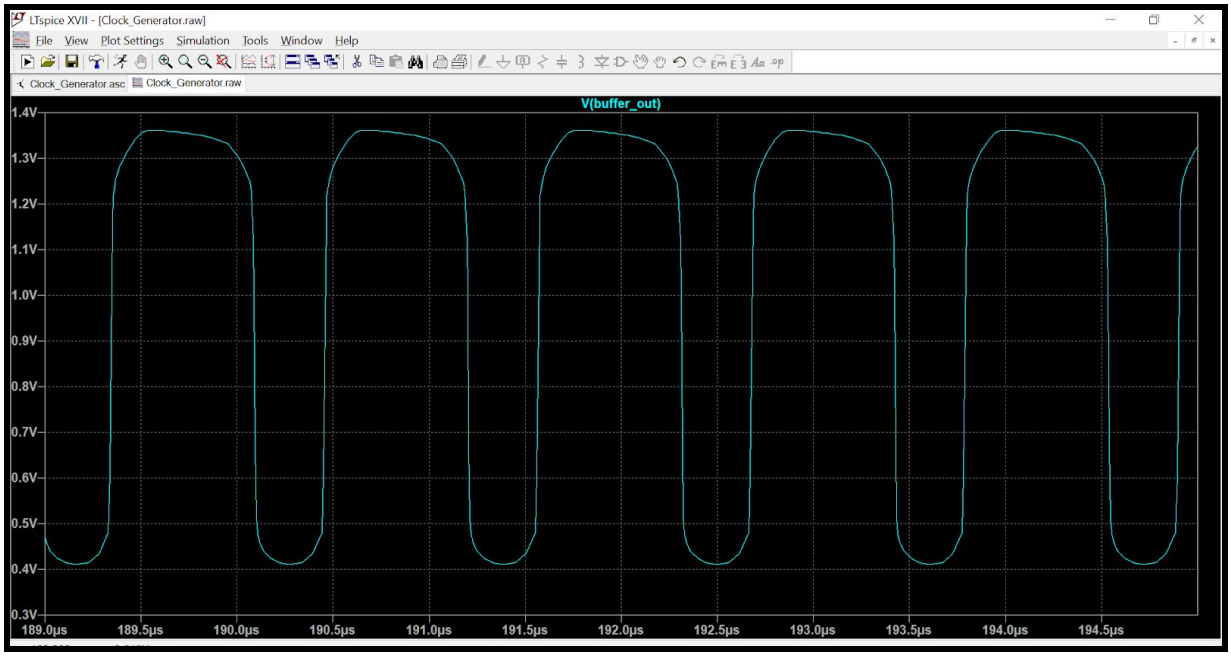
V_1V and V_1.8V



Fig(11): Simulation Output V_1V & V_1.8V

This is the simulation results of the Regulator where the outputs are close to the required values of 1.8V used for the digital block and 1V which is used for the other circuits of the analog front end. We can see now the voltage swings have been removed as we have used a comparator to give a constant voltage which will influence the circuit whenever it is high.

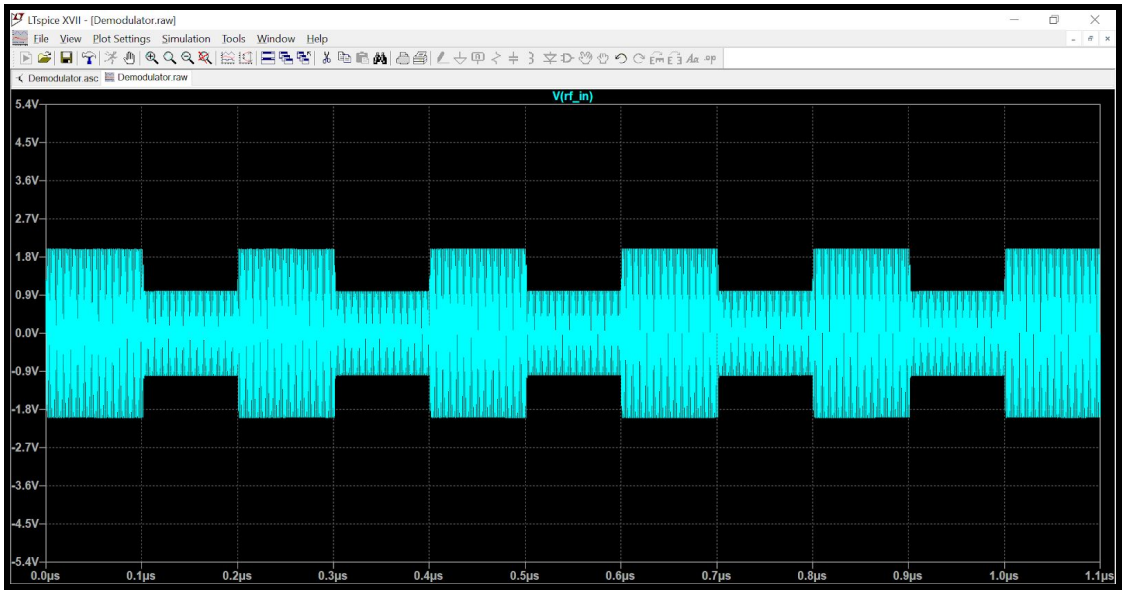
CLOCK GENERATOR



Fig(12): Simulation Output for Clock Generation

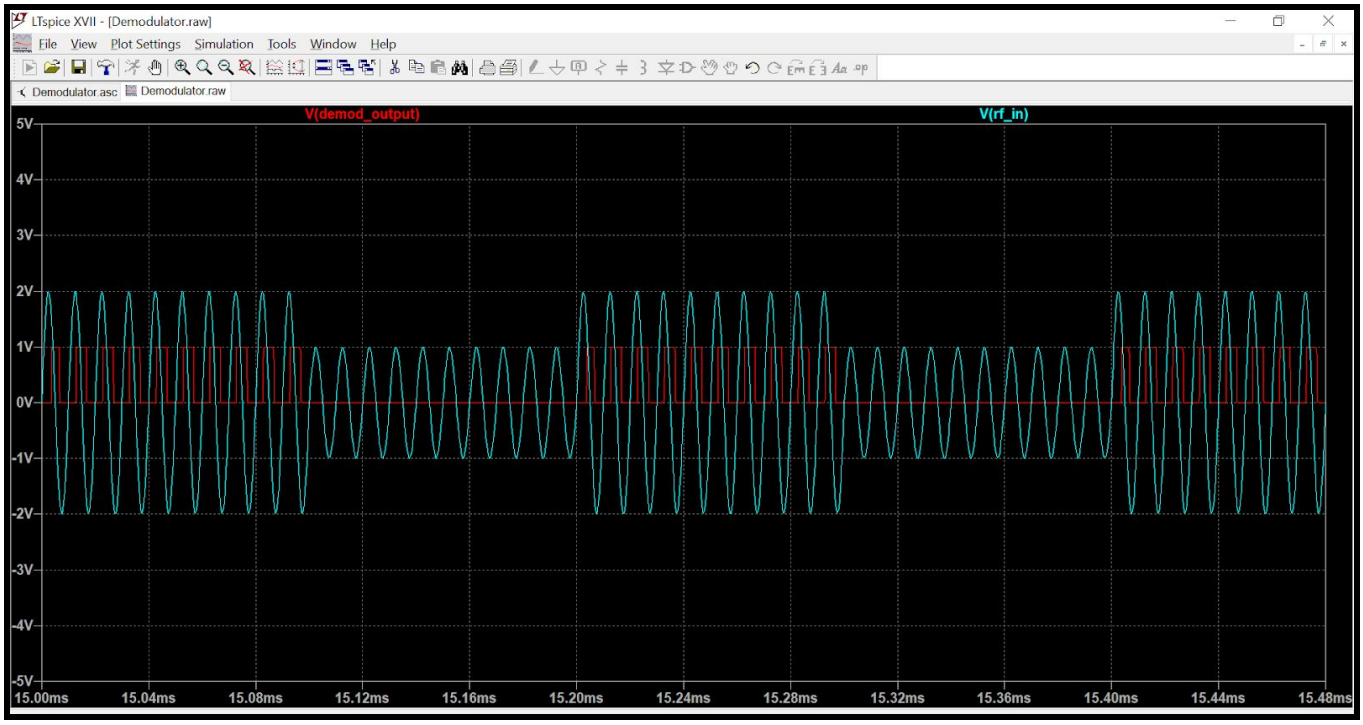
As described in the explanation of the circuit, according to the ISO 18000-6c, it is recommended that the clock frequency to be supplied to the digital block needs to be around 1.28Mhz. As can be seen in the simulation figure, the frequency of our clock is close to 1.2Mhz. Hence, our circuit operates correctly. Also note that the peak to peak voltage is equal to 1V as per our requirements (0.4V to 1.4V).

ASK DEMODULATOR



Fig(13): Simulation Output for ASK Input Signal

The above waveform is a RF Modulated envelope generated artificially using LT SPICE, in order to get proper results from the Demodulator. The frequency of the Carrier wave is 900MHz.



Fig(12) Simulation Output for ASK Demodulation (Red Waveform)

As can be seen in the simulation figure shown, the Blue signal is the RF modulated wave that we have artificially generated in our circuit design to depict the signal received through the antenna of our tag and the Red signal is our final output, which is the demodulator output.

As explained previously, the output matches the requirement. As the frequency of the signal is very high, we have used a carrier of 10000Hz frequency instead of 900MHz just for depicting a clear output.

CONCLUSION & FUTURE SCOPE

Through our project, we have designed a passive UHF RFID Tag Chip's Analog Front-end, for which we have used several components - The Voltage Regulator (consisting of only MOSFETs- i.e. low power, area efficient & Cost effective), a stable Clock Generator, a novel area-efficient ASK demodulator, and a Voltage Rectifier. These components when put together result in a low cost, area efficient, low power, cost effective and highly reliable Analog Front end.

The future work includes :

a) Designing the Digital Block of the RFID Tag as suggested in the Block Diagram.
b) We have used 180nm technology MOSFETs throughout our design, which can be transformed in accordance with the latest technology in order to improve the efficiency of our circuits.
c) Embed a sensor that will be interfaced with our Analog Front end to retrieve meaningful real life values from wherever our RFID Tag is attached.

REFERENCES

[1] Wang Yao, Wen Guangjun, Mao Wei, He Yanli, Zhu Xueyong, et al. Design of a passive UHF RFID tag for the ISO18000-6C protocol. IEEE J Solid-State Circuits, 2011

[2] Jianqin Qian, Chun Zhang, Liji Wu, Xijin Zhao, Dingguo Wei, Zhihao Jiang, Yuhui He, et al. A Passive UHF Tag for RFID-based Train Axle
Temperature Measurement System

https://www.abr.com/what-is-rfid-how-does-rfid-work/
https://www.youtube.com/watch?v=PwCqKvHWRNk
https://www.youtube.com/watch?v=EZcqMf2Nhh4
https://www.atlasrfidstore.com/rfid-insider/active-rfid-vs-passive-rfid
https://ieeexplore.ieee.org/document/6911276
https://electronics.stackexchange.com/questions/375803/how-can-am-modulation-be-performed-in-ltspice-by-built-in-modulator-function