

**NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA,  
SURATHKAL**

**EC302**

**VLSI DESIGN LAB REPORT**

Under the guidance of

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Submitted by

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Oct 22, 2020

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This is the code that is used to calculate the various parameters in few of the questions I have not included it in the main documentation as it will make it too big.

```
*Mos with load
.include ../../t14y_tsmc_025_level3.txt
*mosfet dec
ml vdd vdd out 0 cmosn l=1u w=1u
md out in 0 0 cmosn l=1u w=1u

*netlist
v_in in 0 dc 2 pulse(0 5 1n 0.1n 0.1n 2n 4n)
v_dd vdd 0 dc 5
c1 out 2 0.02p
vdum 2 0 dc 0

*dc analysis
.control
foreach i 0.5u 1u 10u
alter ml l=$i
dc vin 0 5 0.01
run
*find voh,vol
meas dc voh MAX d2
meas dc vol MIN d2
let slope=deriv(d2)
let v90=voh-0.1*(voh-vol)
let v10=vol+0.1*(voh-vol)
let v50=0.5*(vol+voh)
*find vil,vih
meas dc vil find in when slope=-1 cross=1
meas dc vih find in when slope=-1 cross=2
let nml=vil-vol
let nmh=voh-vih
print nml nmh
.endc

*transient analysis
.control
foreach i 0.5u 1u 10u
alter md l=$i
tran 0.001 4n
run
let vi50=0.5*(dc.vil + dc.vih)
*find trise,tfall
meas tran trise trig out val=dc.v10 rise=1 targ d2 val=dc.v90 rise=1
meas tran tfall trig out val=dc.v90 fall=1 targ d2 val=dc.v10 fall=1
print trise tfall

.endc
```

# 1. Study characteristics of NMOS

## Objectives:-

Study the Input and output characteristics of NMOS Transistor, effect of L, W, VTO, LAMBDA, VSB and Temperature on the behaviour of the Transistor

I have written in the whole analysis in one code but will be explaining each part of the code with its respective graphs

## Introduction:-

An NMOS Short for negative-channel metal-oxide semiconductor, and pronounced en-moss, a type of semiconductor that is negatively charged so that transistors are turned on or off by the movement of electrons.

## Circuit Diagram:

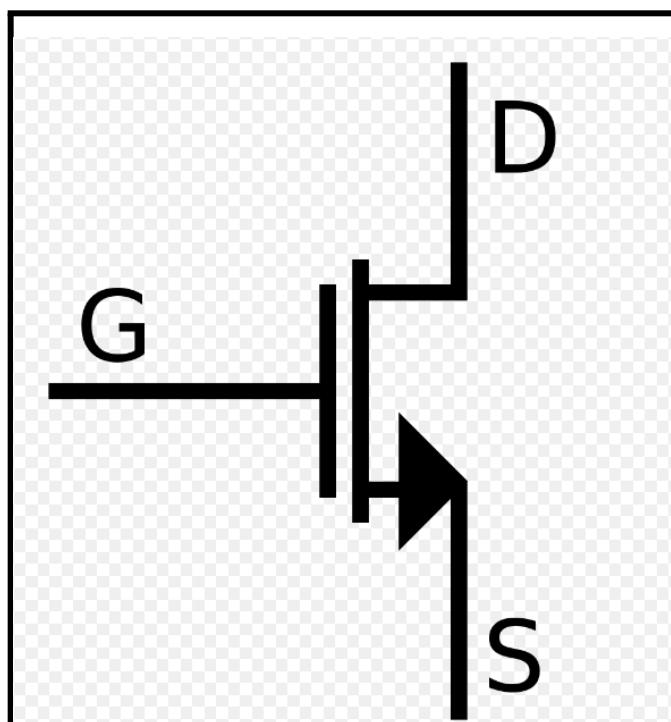


Fig: NMOS

## Input and output characteristics:

```
.include ./t14y_tsmc_025_level3.txt
```

```
m1 vdd in 0 vsb cmosn l=1u w=0.5u
```

```
* power sources excitation etc.
```

```
v_dd vdd 0 3.3
```

```
v_in in 0 3.3
```

```
v_sb 0 vsb 3.3
```

\* PART A\*

\*Input characteristics\*

```
.control
```

```
dc v_in 0 3.3 0.1 v_dd 0 3.3 1
```

```
plot -dc1.v_dd#branch
```

```
.endc
```

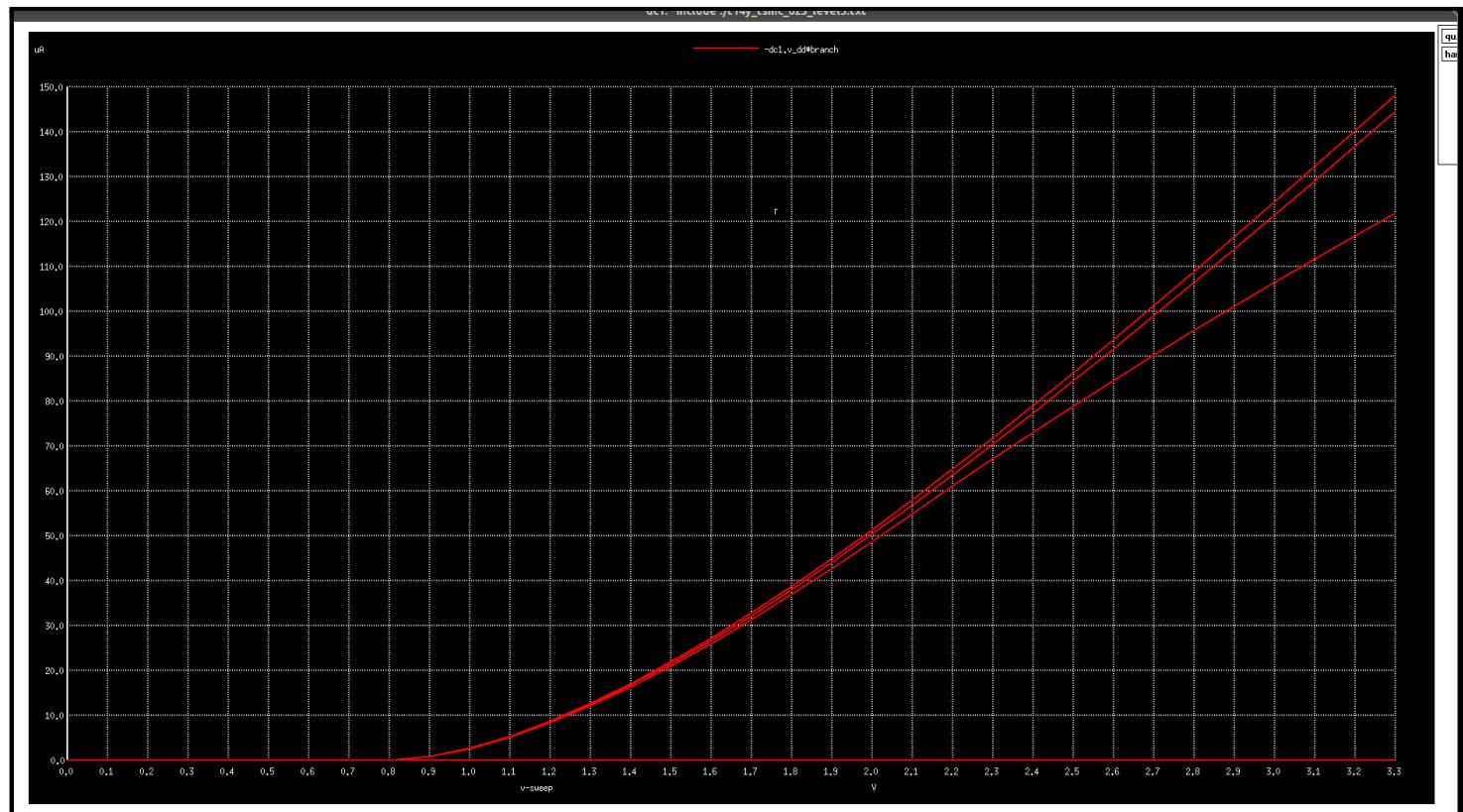
\*Output characteristics\*

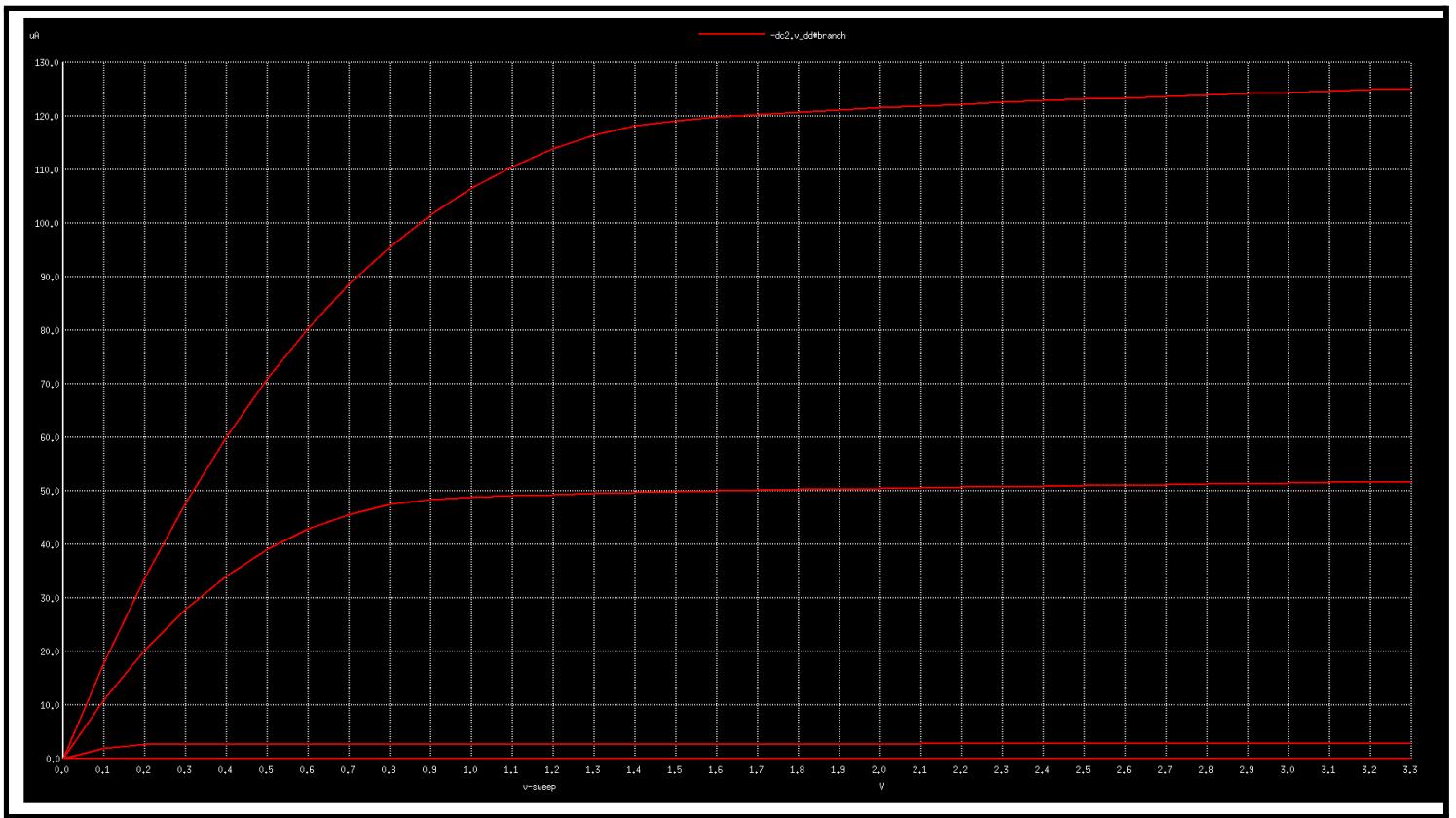
```
.control
```

```
dc v_dd 0 3.3 0.1 v_in 0 3.3 1
```

```
plot -dc2.v_dd#branch
```

```
.endc
```





The above 2 graphs are the input and the output characteristics of an NMos, The first graph is the input characteristics we can observe that the V<sub>to</sub> stays the same and that as we increase the drain voltage the graph shifts up, it behaves just as expected. The second graph is the output characteristics and we can see that lambda is a very low value and that with increase in the v<sub>in</sub> the graph shifts up as it is supposed to behave like this.

## Varying the Width and Length:

```
*PART B*
*Input to Output characteristics by varing the WIDTH*
.control
foreach wid 0.25u 0.5u 5u
    alter m1 w=$wid
    dc v_in 0 3.3 0.1
    dc v_dd 0 3.3 0.1
end
alter m1 w=0.5u
.endc

*Input characteristics
.control
plot dc3.v_dd#branch*(-1) dc5.v_dd#branch*(-1) dc7.v_dd#branch*(-1)
.endc

*Output characteristics
.control
plot dc4.v_dd#branch*(-1) dc6.v_dd#branch*(-1) dc8.v_dd#branch*(-1)
.end
```

\*Part C\*

\*Input to Output characteristics by varying the LENGTH\*

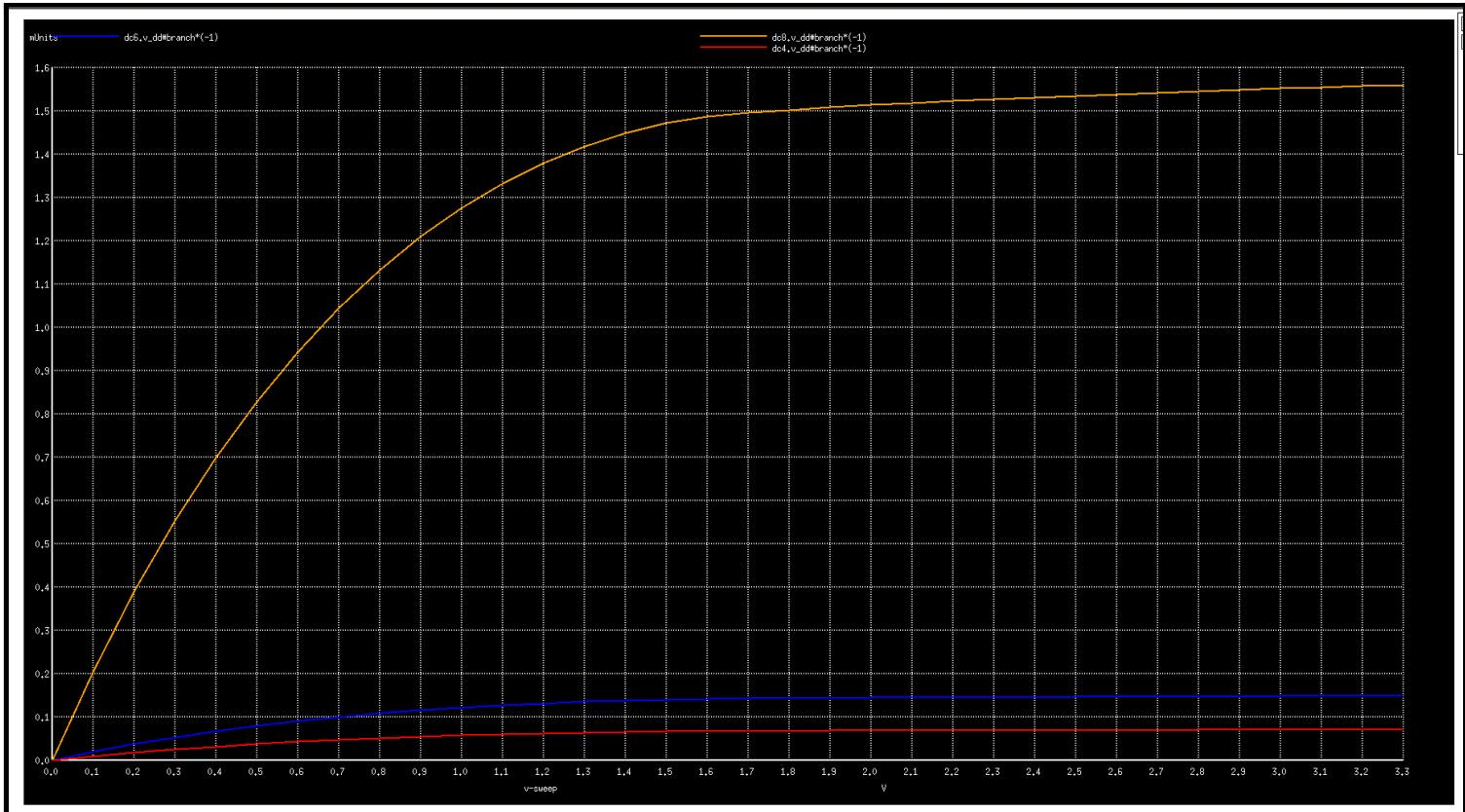
```
.control
foreach len 0.5u 1u 10u
    alter m1 l=$len
    dc v_in 0 3.3 0.1
    dc v_dd 0 3.3 0.1
end
alter m1 l=1u
.endc
```

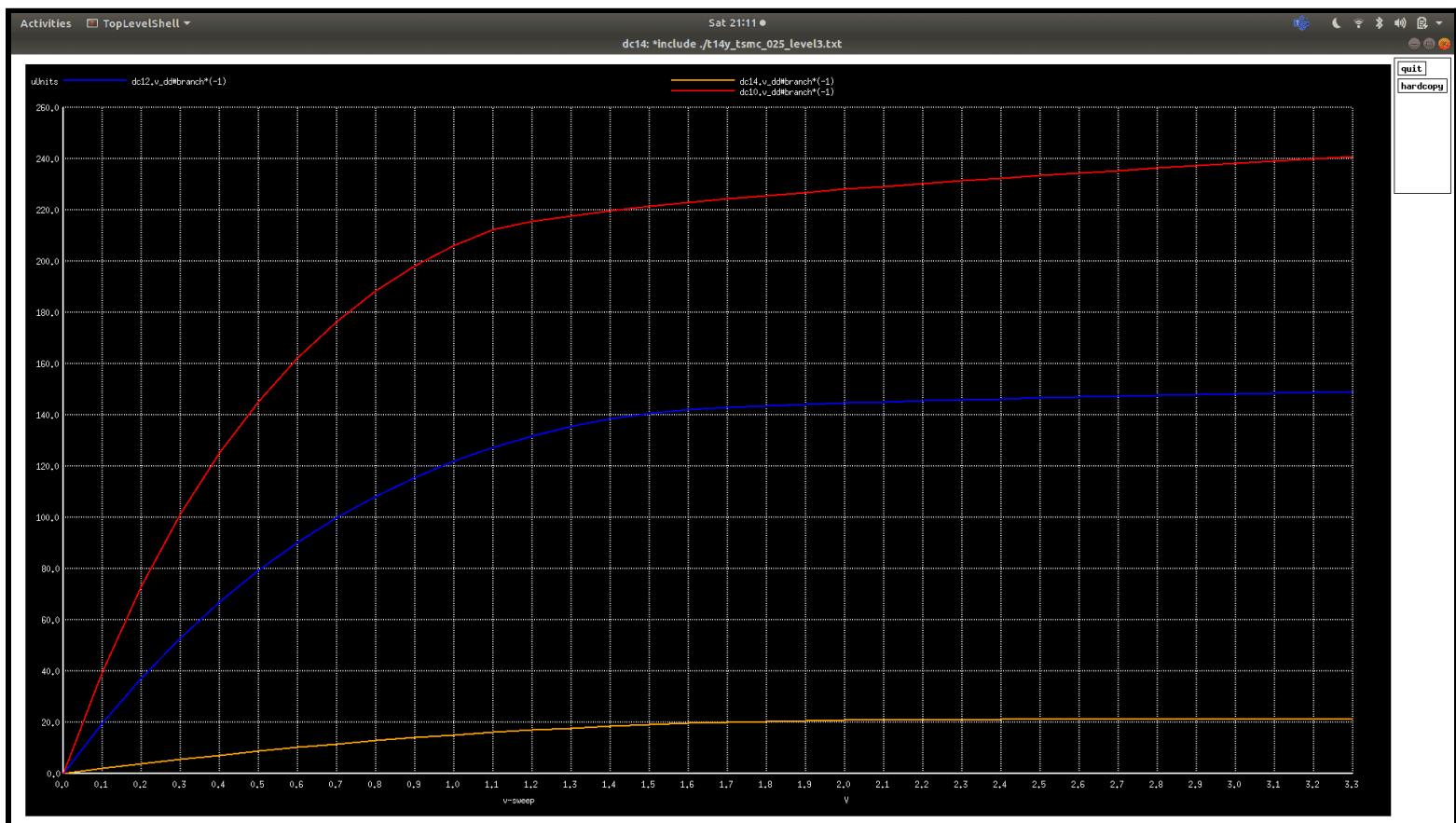
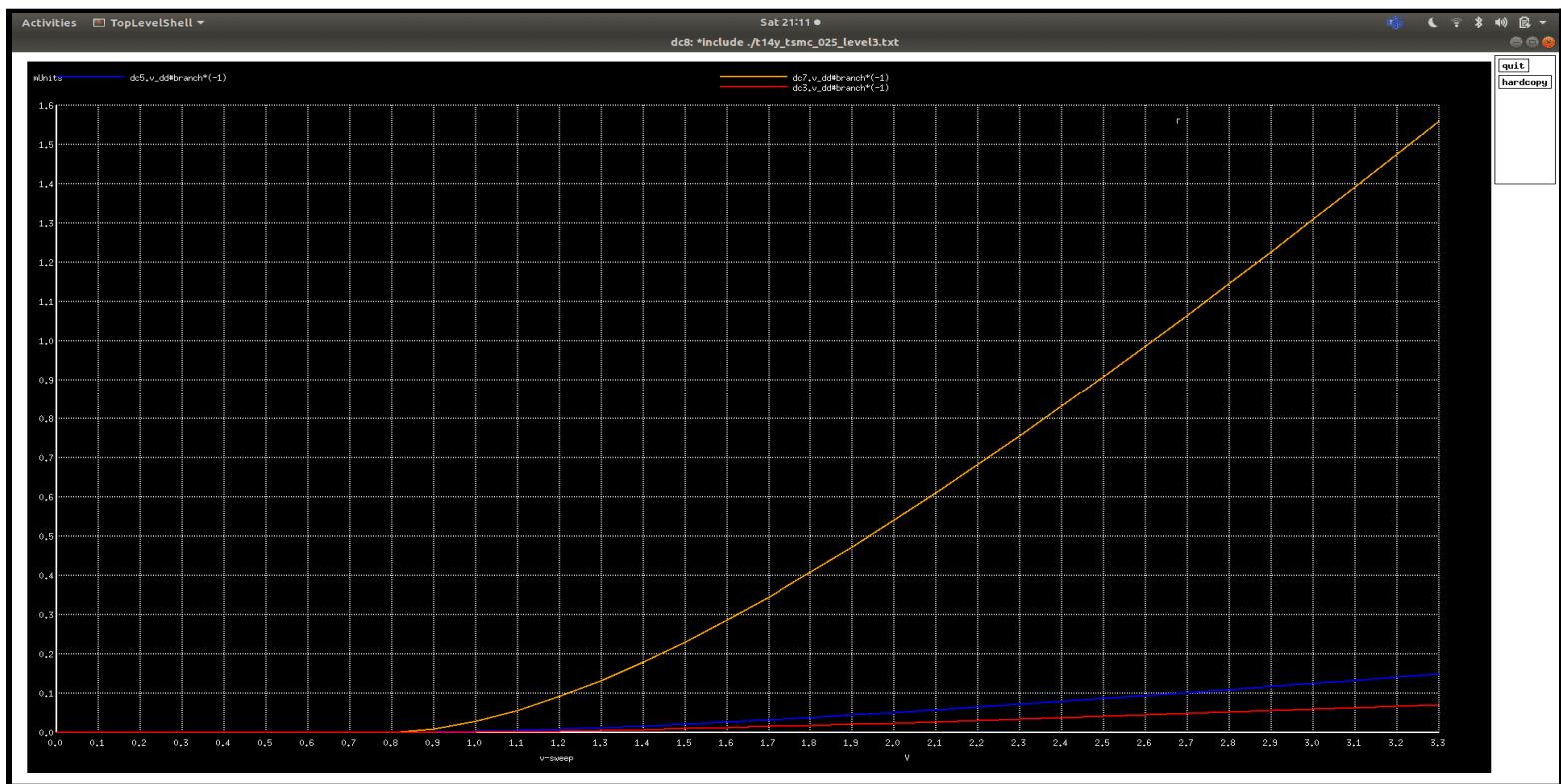
\*Input characteristics

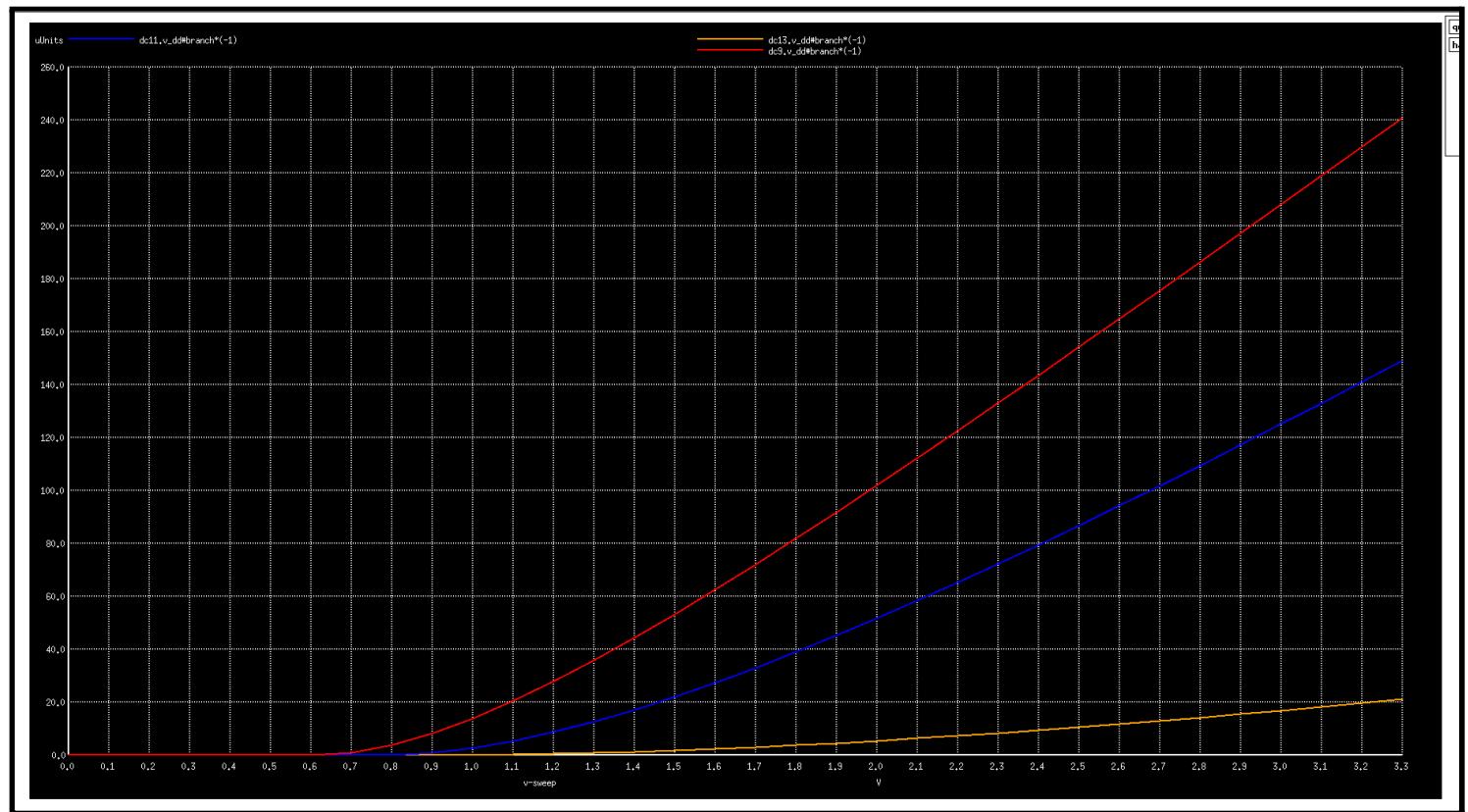
```
.control
plot dc9.v_dd#branch*(-1) dc11.v_dd#branch*(-1) dc13.v_dd#branch*(-1)
.endc
```

\*Output characteristics

```
.control
plot dc10.v_dd#branch*(-1) dc12.v_dd#branch*(-1) dc14.v_dd#branch*(-1)
.endc
```







The above code and graphs are the simulation results of the Input and Output characteristics of the Nmos.

First we change the **width** and plot the input and output characteristics, as we increase the width we can see the output characteristics moving up as the resistance decreases so more current can flow through the mosfet, and the input characteristics the Vto decreases for the same reason.(first 2 graphs)

Second we change the **length** of the transistor and plot the input and output characteristics, here we can see the output characteristics decreases as the resistance increases and we can see that less current flows, similarly the vto also increases for the same reasons(last 2 graphs)

## Varying the Threshold Voltage and Temperature:

\*PART D\*

\*input to Output characteristics by varying the THRESHOLD VOLTAGE\*

```
.control
foreach vol 0.1 0.25 0.5
    altermod m1 VTO=$vol
    dc v_in 0 3.3 0.1
    dc v_dd 0 3.3 0.1
end
alter m1 VTO=0.4238252
.endc
*Input characteristics
.control
plot dc15.v_dd#branch*(-1) dc17.v_dd#branch*(-1) dc19.v_dd#branch*(-1)
.endc
*Output characteristics
.control
plot dc16.v_dd#branch*(-1) dc18.v_dd#branch*(-1) dc20.v_dd#branch*(-1)
.endc
```

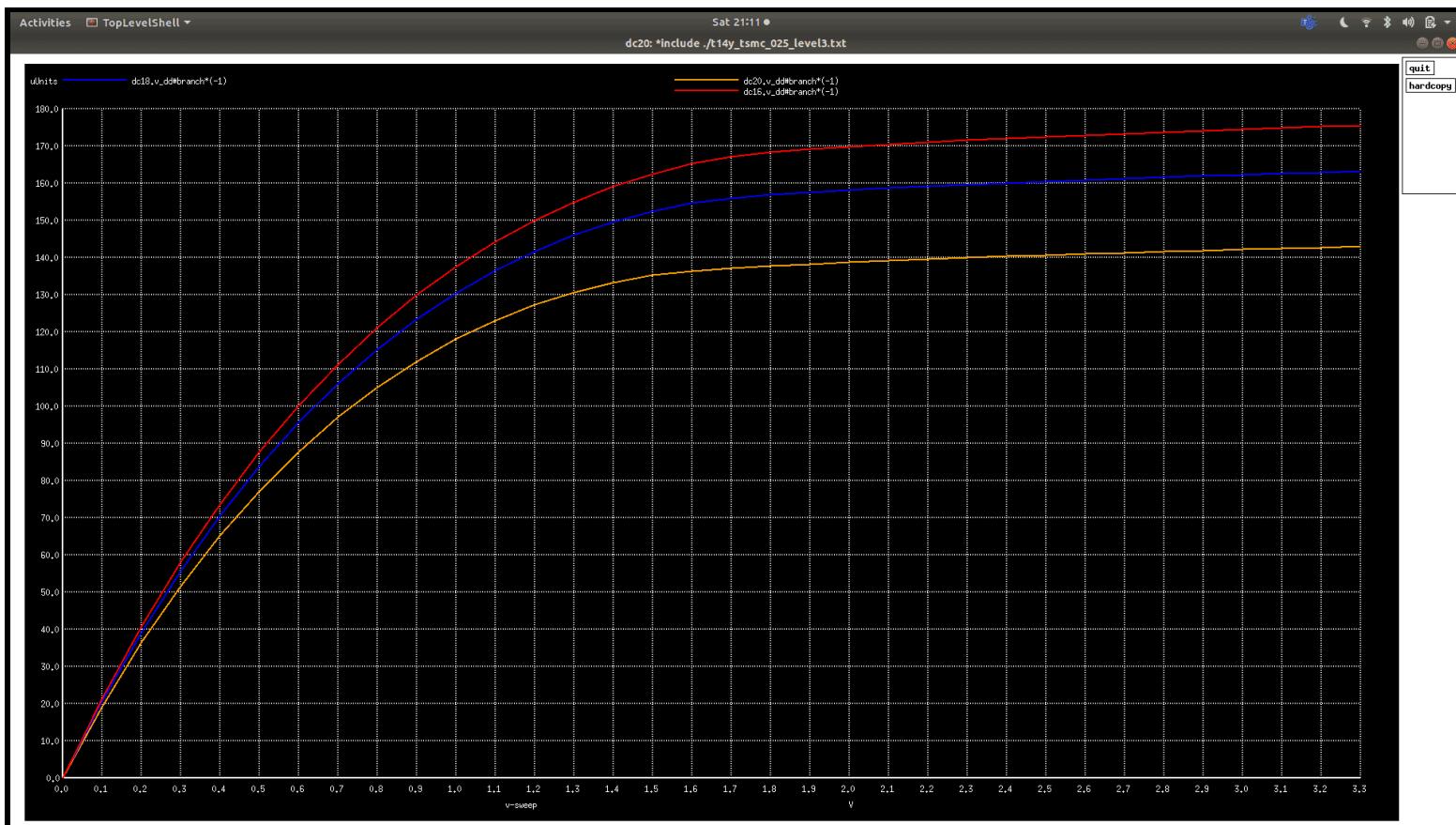
```

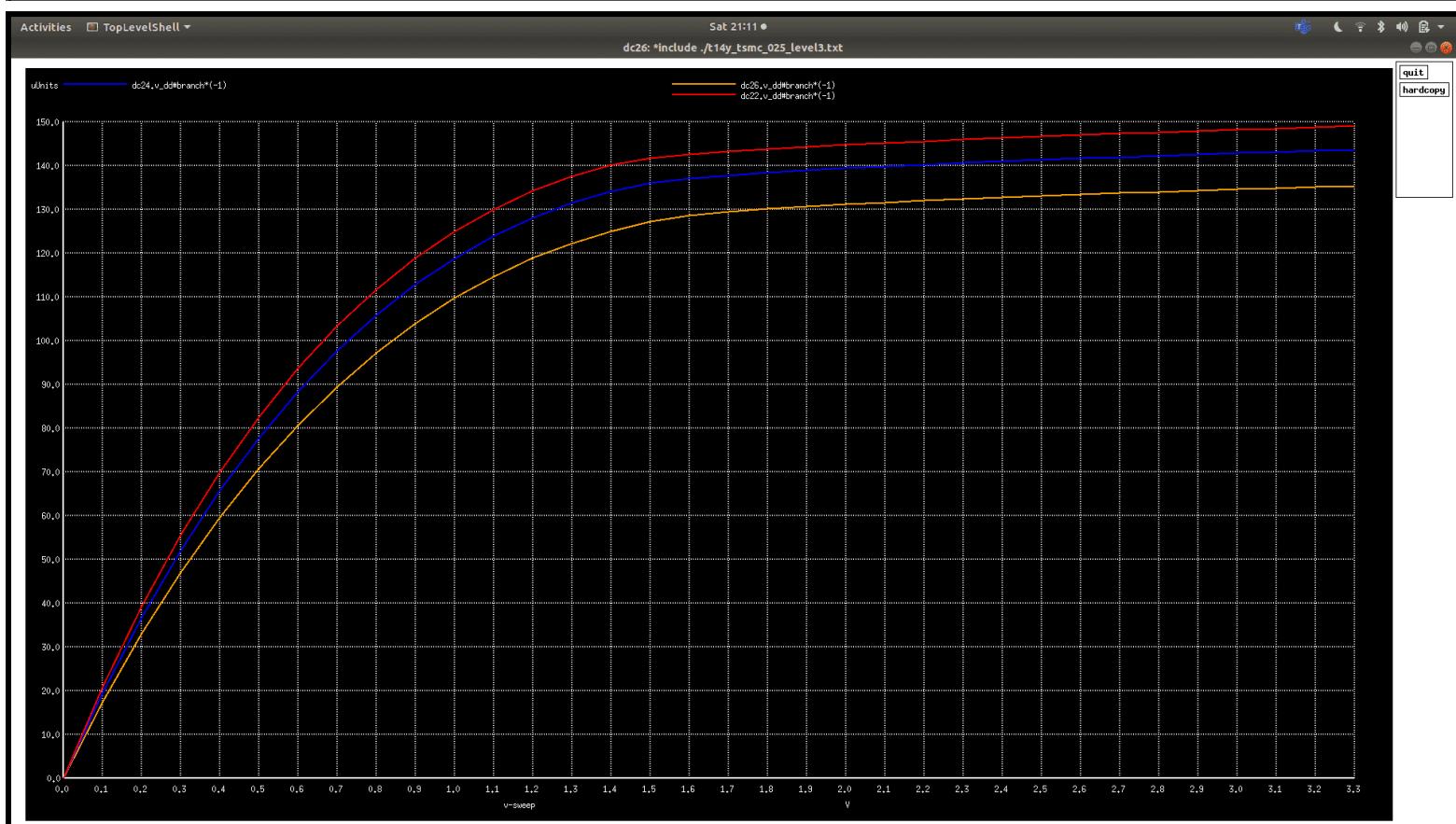
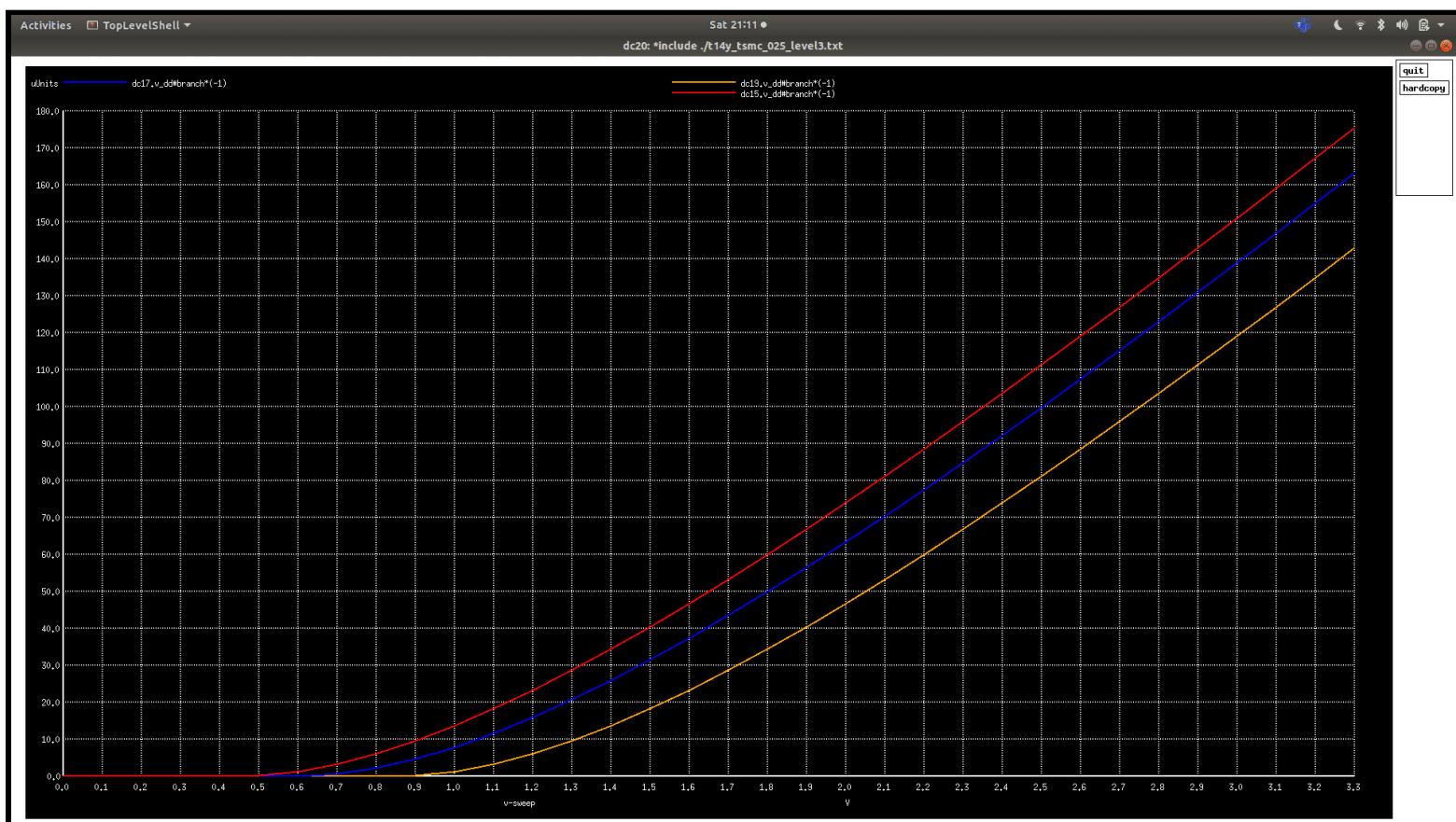
*PART E*
*Input to Output characteristics by varying the TEMPERATURE*
.control
foreach tem 10 25 50
    alter m1 TEMP=$tem
    dc v_in 0 3.3 0.1
    dc v_dd 0 3.3 0.1
end
alter m1 TEMP=27
.endc

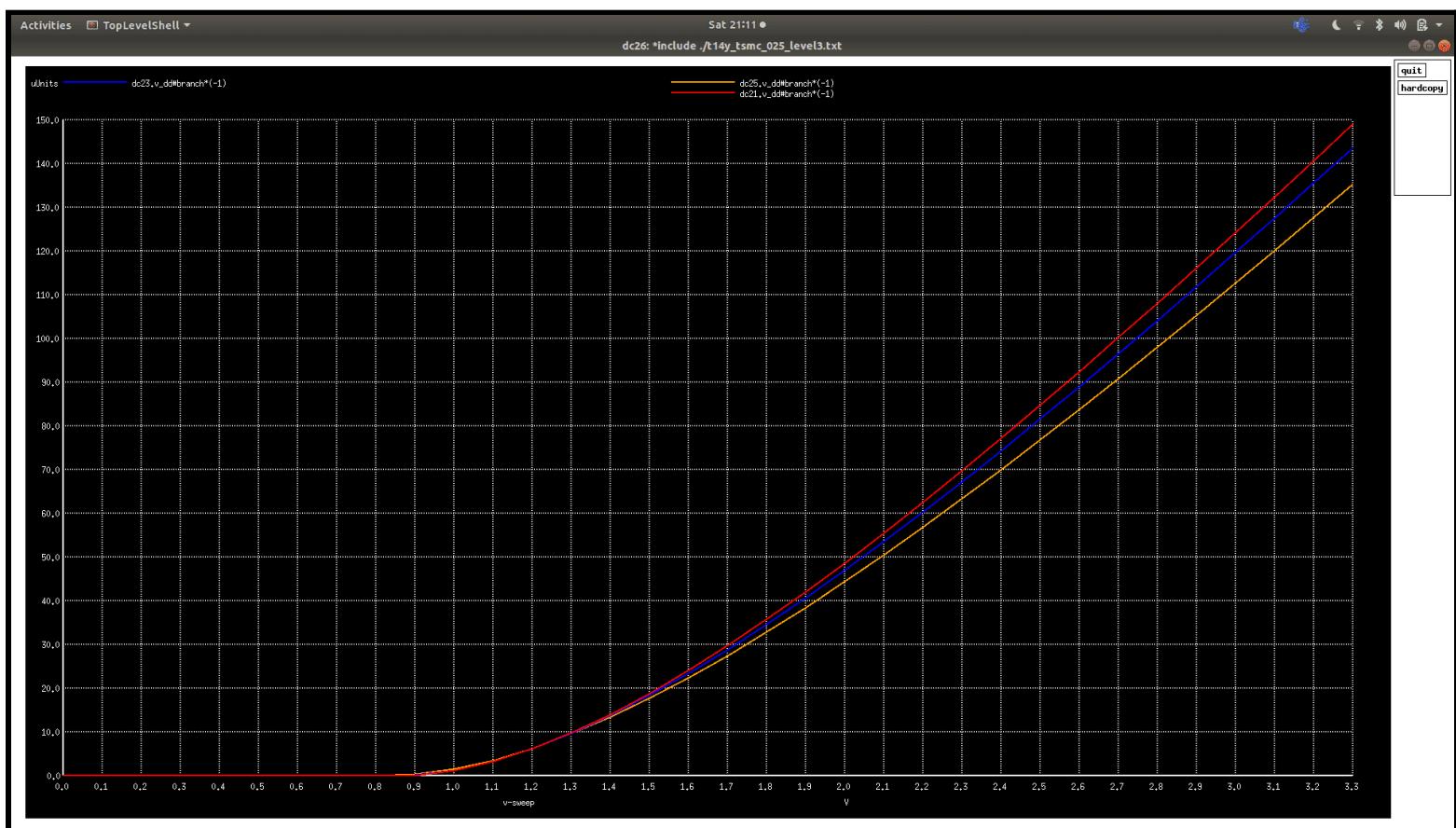
*Input characteristics
.control
plot dc21.v_dd#branch*(-1) dc23.v_dd#branch*(-1) dc25.v_dd#branch*(-1)
.endc

*Output characteristics
.control
plot dc22.v_dd#branch*(-1) dc24.v_dd#branch*(-1) dc26.v_dd#branch*(-1)
.endc

```







The above code and graphs are the simulation results of the Input and Output characteristics of the transistor.

First we change the **VTO** and plot the input and output characteristics, in the Output characteristics we can see there is a small decrease in the current flowing as Vto increases the net current flowing will be lower, and we can see a clear shift of the graph to the right as the Vto increases.(first 2 graphs)

Second we change the **Temperature** of the transistor and plot the input and output characteristics, in the output characteristics we can see a small decrease in the current flowing as the mosfet have negative effect of temperature this is opposite to that of a transistor and due to which we can see a slight change in the graphs.(last 2 graphs)

## Varying the VSB and Lambda:

```
*PART F*
*Input to Output characteristics by varying the VSB
.control
dc v_dd 0 3.3 0.1 v_sb 0 3.3 1
dc v_in 0 3.3 0.1 v_sb 0 3.3 1
.endc
*Input characteristics
.control
plot dc28.v_dd#branch*(-1)
.endc
*Output characteristics
.control
plot dc27.v_dd#branch*(-1)
*.endc
```

```
.include ./t14y_tsmc_025_level3.txt

.MODEL nfet1 NMOS LEVEL=1 LAMBDA=0.5

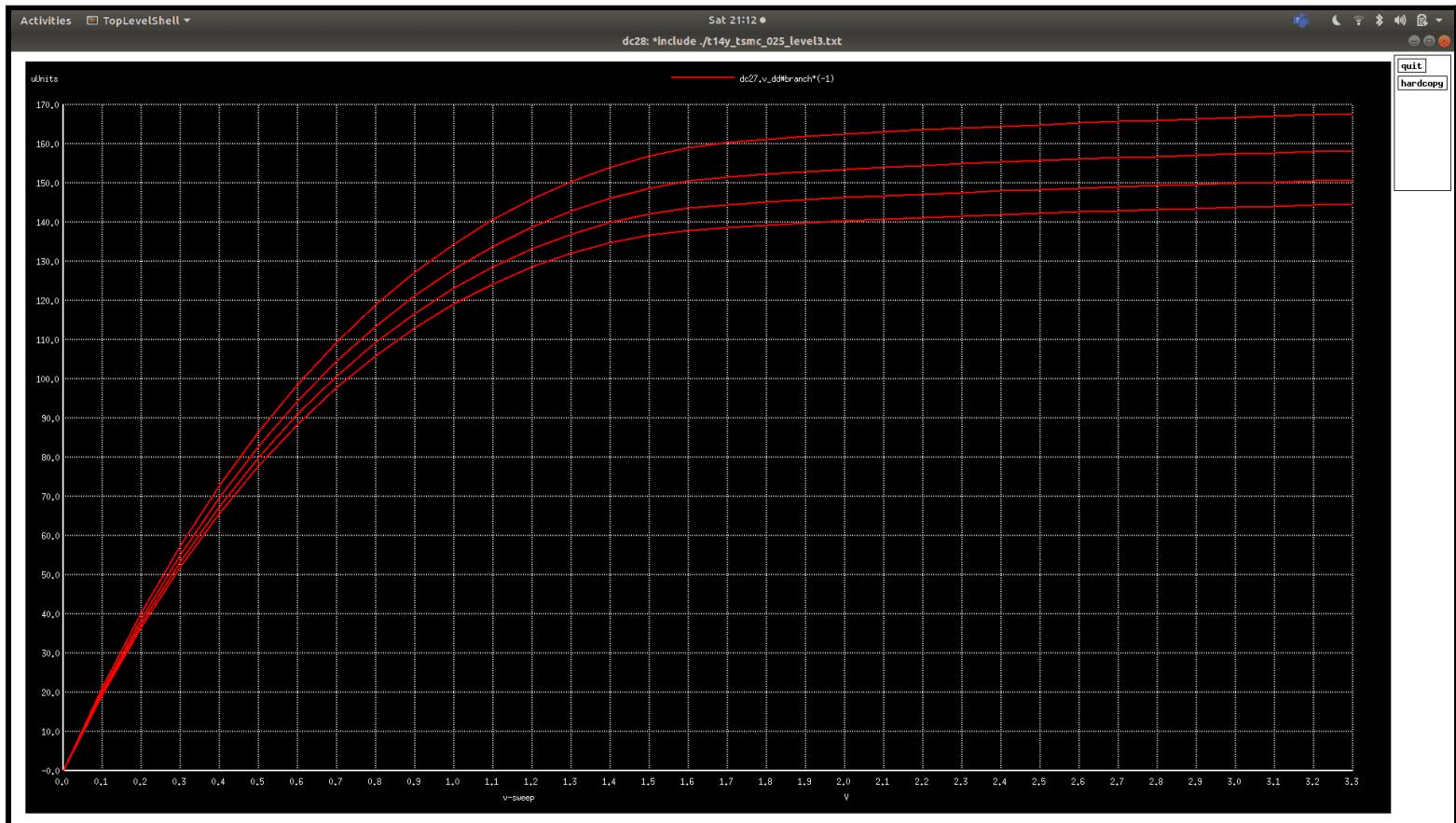
m3 vdd in 0 0 nfet1 l=2u w=1u

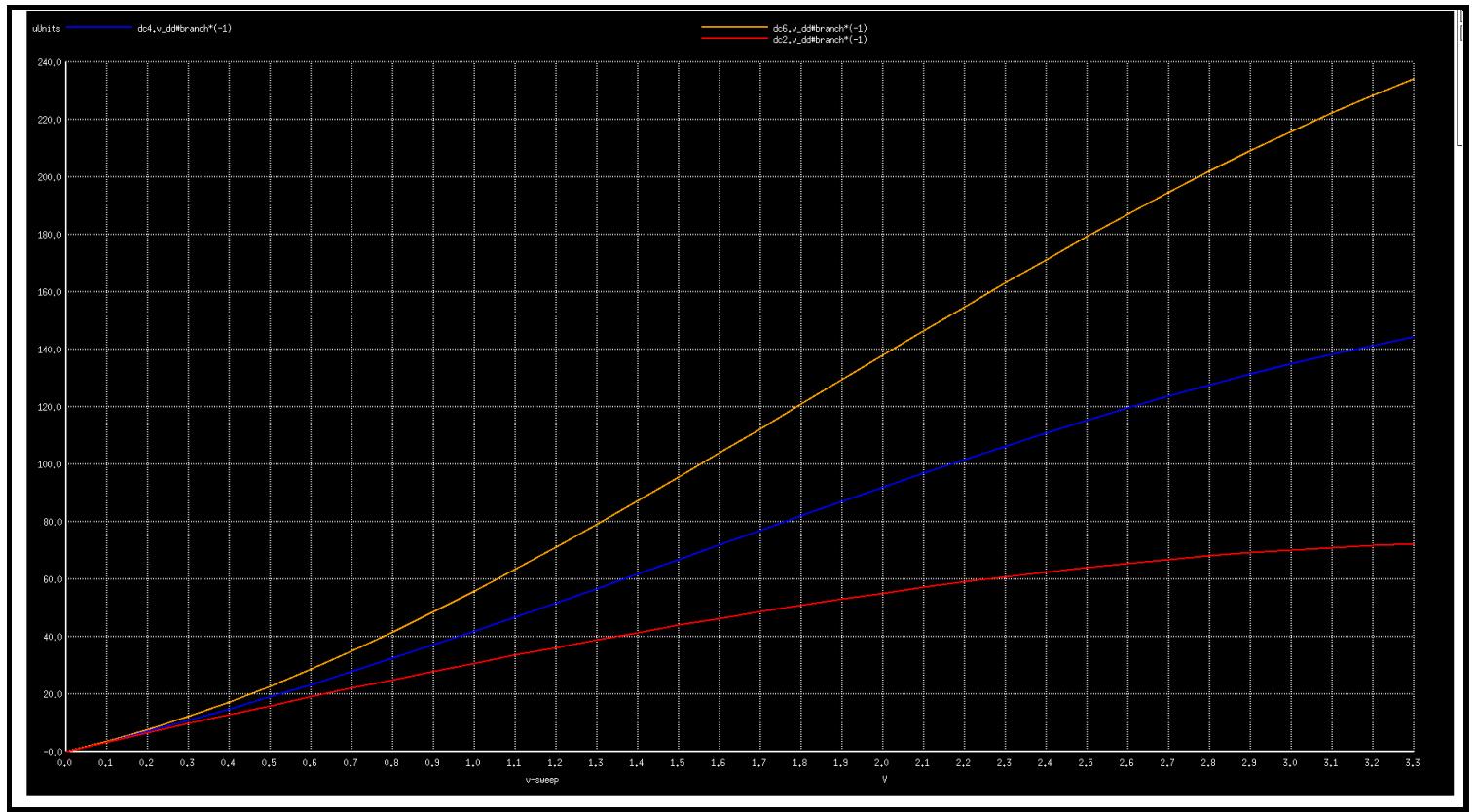
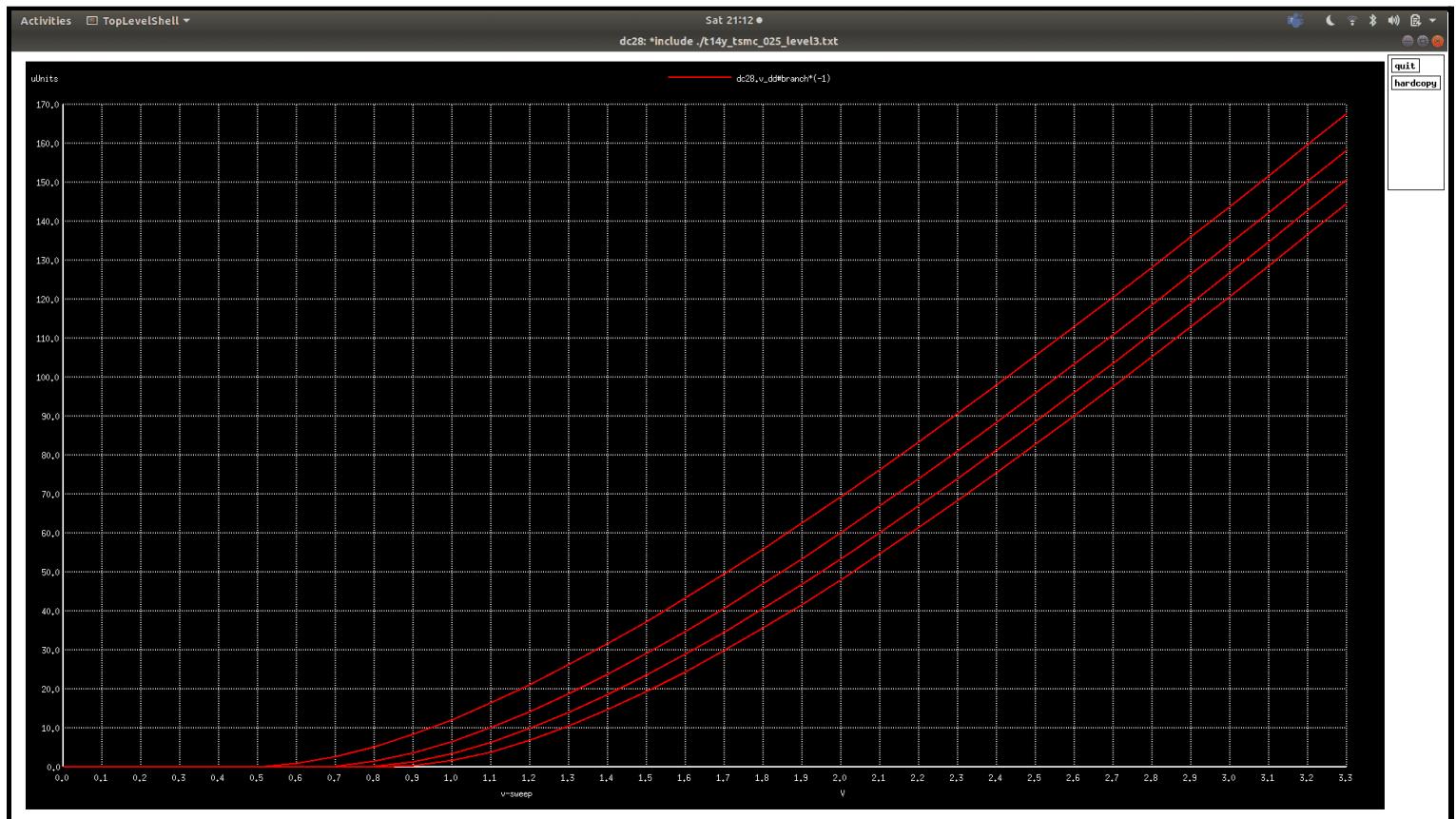
v_dd vdd 0 dc 3.3
v_in in 0 dc 3.3

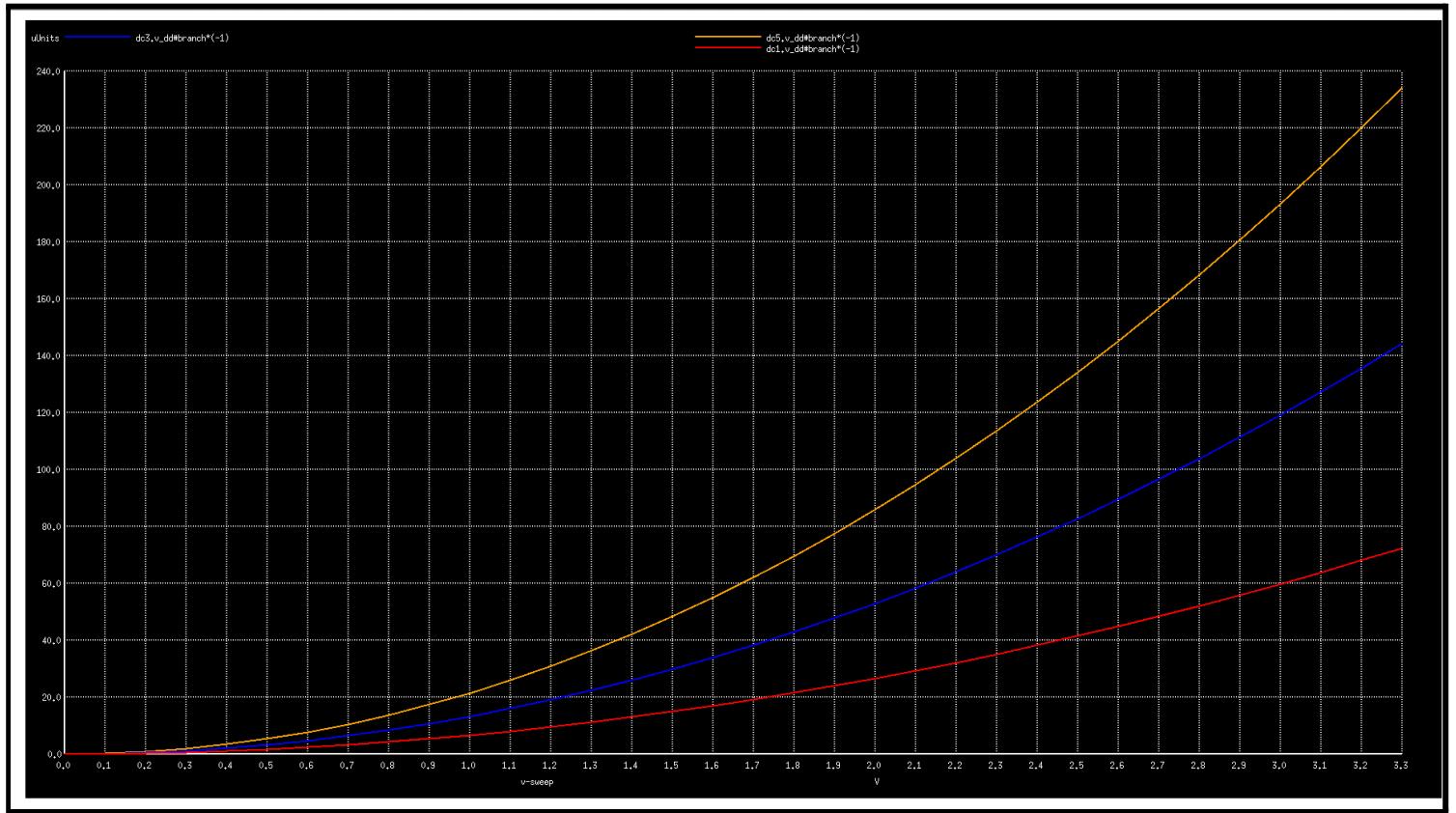
*Input to Output characteristics by varying the Lambda
.dc v_in 0 3.3 0.1 v_dd 0 3.3 1
.dc v_dd 0 3.3 0.1 v_in 0 3.3 1
.control
foreach lan 0.1 0.5 1
    altermod m3 lambda=$lan
    dc v_in 0 3.3 0.1
    dc v_dd 0 3.3 0.1
end
.endc

*Input characteristics LAMBDA
.control
plot dc1.v_dd#branch*(-1) dc3.v_dd#branch*(-1) dc5.v_dd#branch*(-1)
.endc

*Output characteristics
.control
plot dc2.v_dd#branch*(-1) dc4.v_dd#branch*(-1) dc6.v_dd#branch*(-1)
.endc
```







The above code and graphs are the simulation results of the Input and Output characteristics of the transistor.

First we change the **V<sub>SB</sub>** and plot the input and output characteristics, and the graph decreases as we increase V<sub>SB</sub> as the potential difference between drain and the source decreases causing less current to follow through the Mosfet and we can even see the increase in the V<sub>To</sub>.(first 2 graphs)

Second we change the **Lambda** of the transistor and plot the input and output characteristics, in the output characteristics the way that the current keeps on increasing even though it is supposed to be in the saturation region. (last 2 graphs)

### Conclusion:-

The experiment was performed, and all graphs were analysed. The obtained graphs movements agreed with theory, and hence simulations were verified. NGSPICE was the simulator used for this task.

## 2. Study of MOS Inverter with Resistive Load

### Objectives:-

Study the

- Transfer function

- Noise margin

- Effect on rise time, falltime

- Propagation delay,

And the power and energy consumed of a MOS inverter for various L, W of the transistor, load capacitance and rise/fall time of input.

### Introduction:-

Inverter is one that inverts the signal supplied at its input. If input is made high or logic level is 1, then the output has logic level 0 and vice-versa. A resistive load inverter is characterised by a resistive load between the pull down transistor and the voltage source. The output is taken at the junction of the load resistance and the pull down transistor. The pull-up circuit is constituted by the resistor and pull-down resistor by the NMOS. When the input is low, the NMOS is open circuited and the output capacitance is charged to VDD through RL.

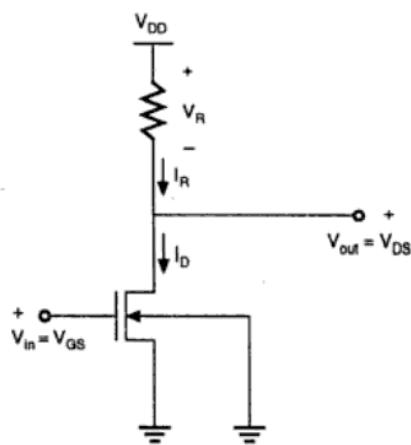


Fig: Inverter with resistive pull-up network

## Varying the Resistor:-

```
.include ./t14y_tsmc_025_level3.txt

m1 out in 0 0 cmosn w=6.4u l=1.8u ad=6.84p pd=10.8u as=6.84p ps=10.8u
r1 vdd out 1k
c1 out x 0.001p

V_x x 0 dc 0.00001
V_dd vdd 0 dc 5

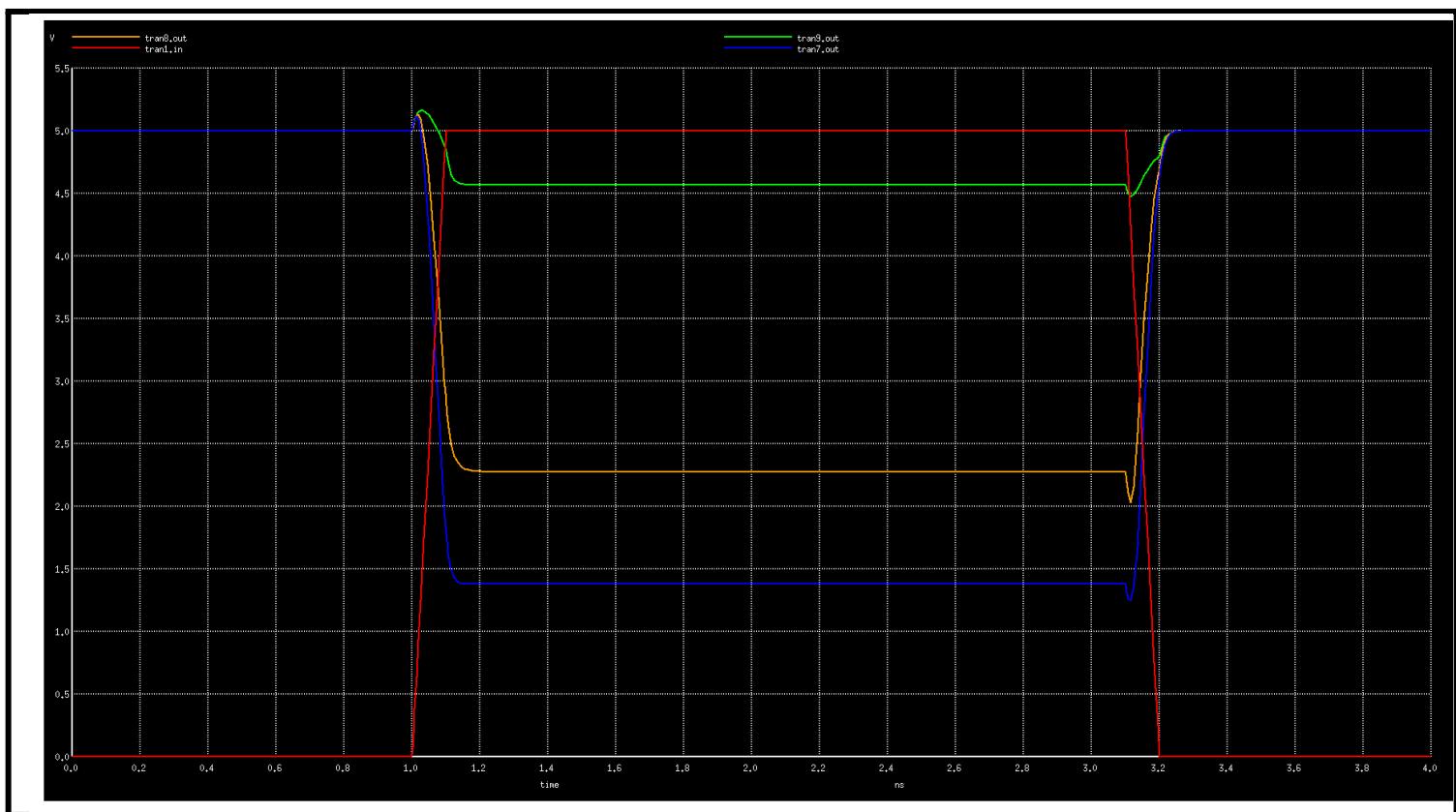
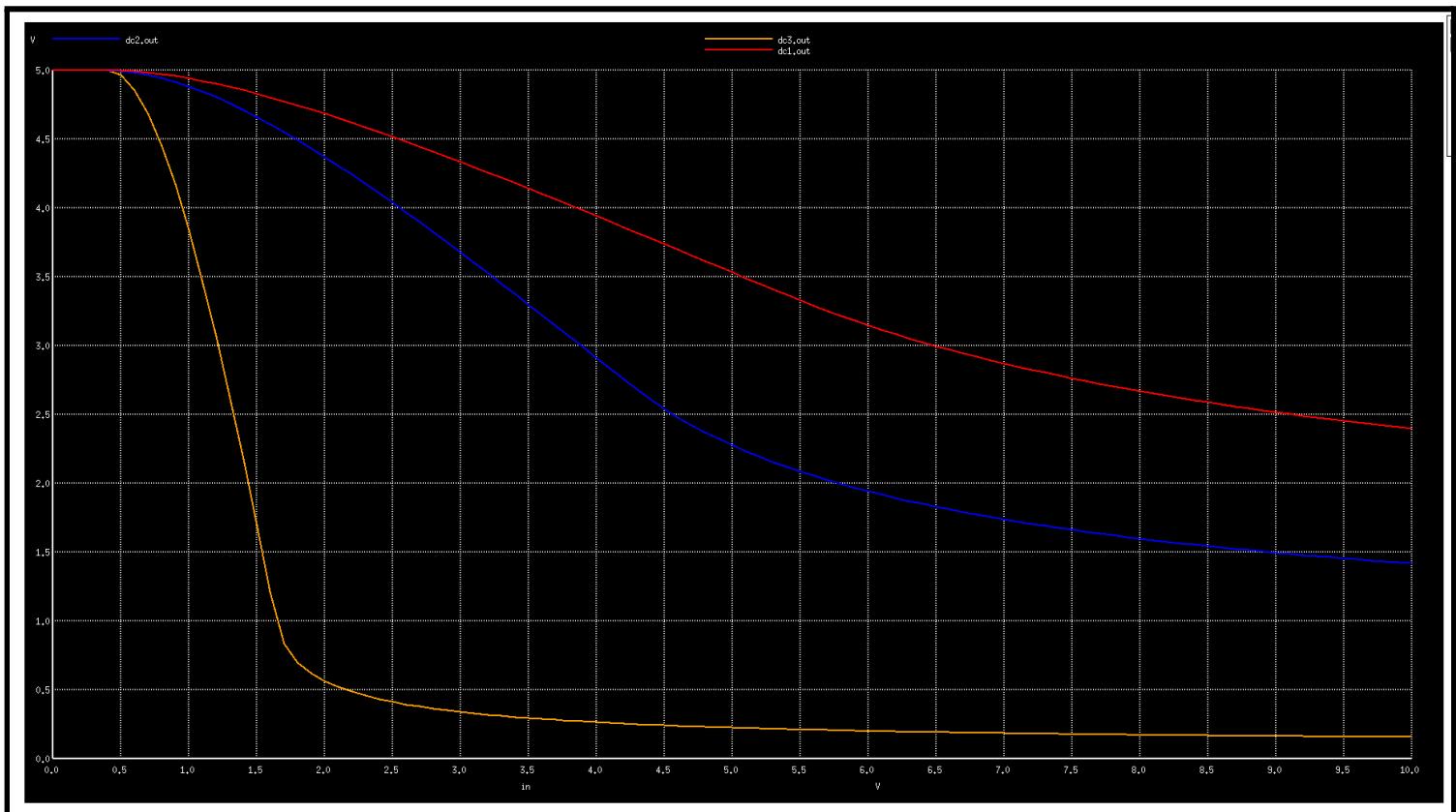
V_in in 0 dc 2.5 pulse(0 5 1n 0.1n 0.1n 2n 4n)

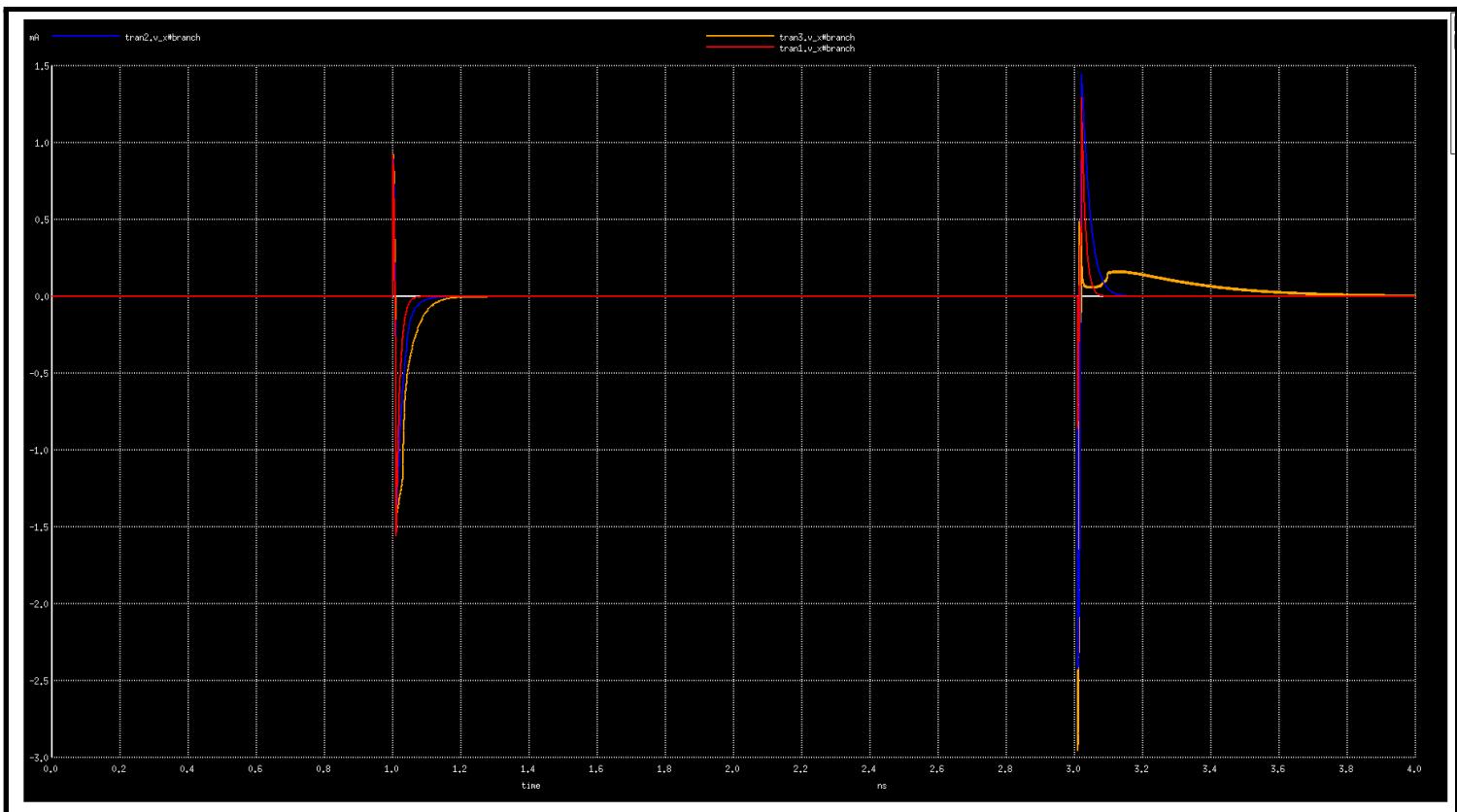
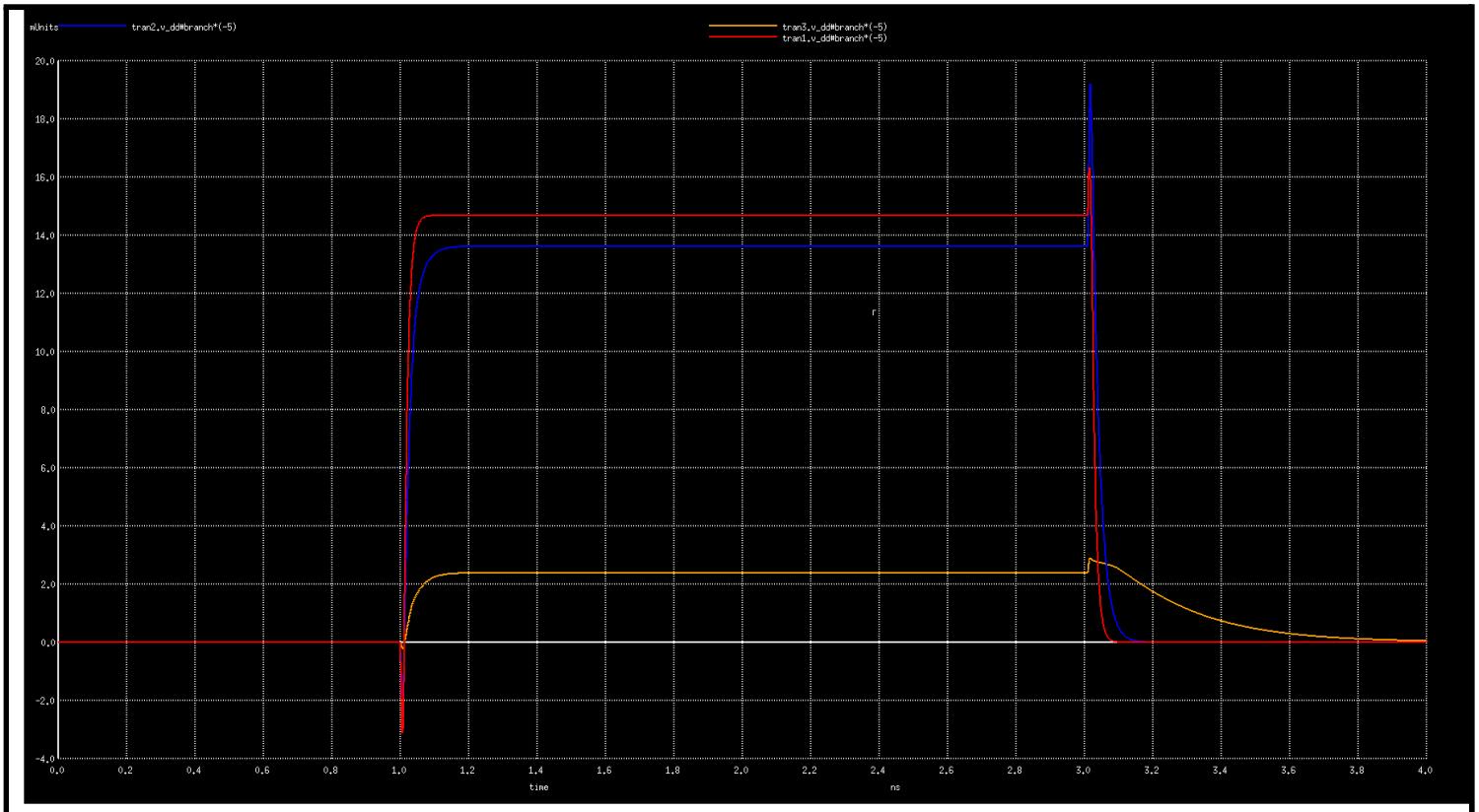
.tran 0.01ns 4n

***Varying Resistor***

.control
foreach res 500 1k 10k
alter r1 = $res
run
dc V_in 0 5 0.1
meas dc vol min out
meas dc voh max out
print voh
let slope = deriv(out)
meas dc vil find in when slope = -1 cross = 1
meas dc vih find in when slope = -1 cross = 2
let nmh = voh - vih
let nml = vil - vol
print nmh nml
end
alter r1 = 1K
.endc

.control
plot tran1.in tran1.out tran2.out tran3.out
plot dc1.out dc2.out dc3.out vs in
plot tran1.V_dd#branch*(-5) tran2.V_dd#branch*(-5) tran3.V_dd#branch*(-5)
plot tran1.V_x#branch tran2.V_x#branch tran3.V_x#branch
.endc
```





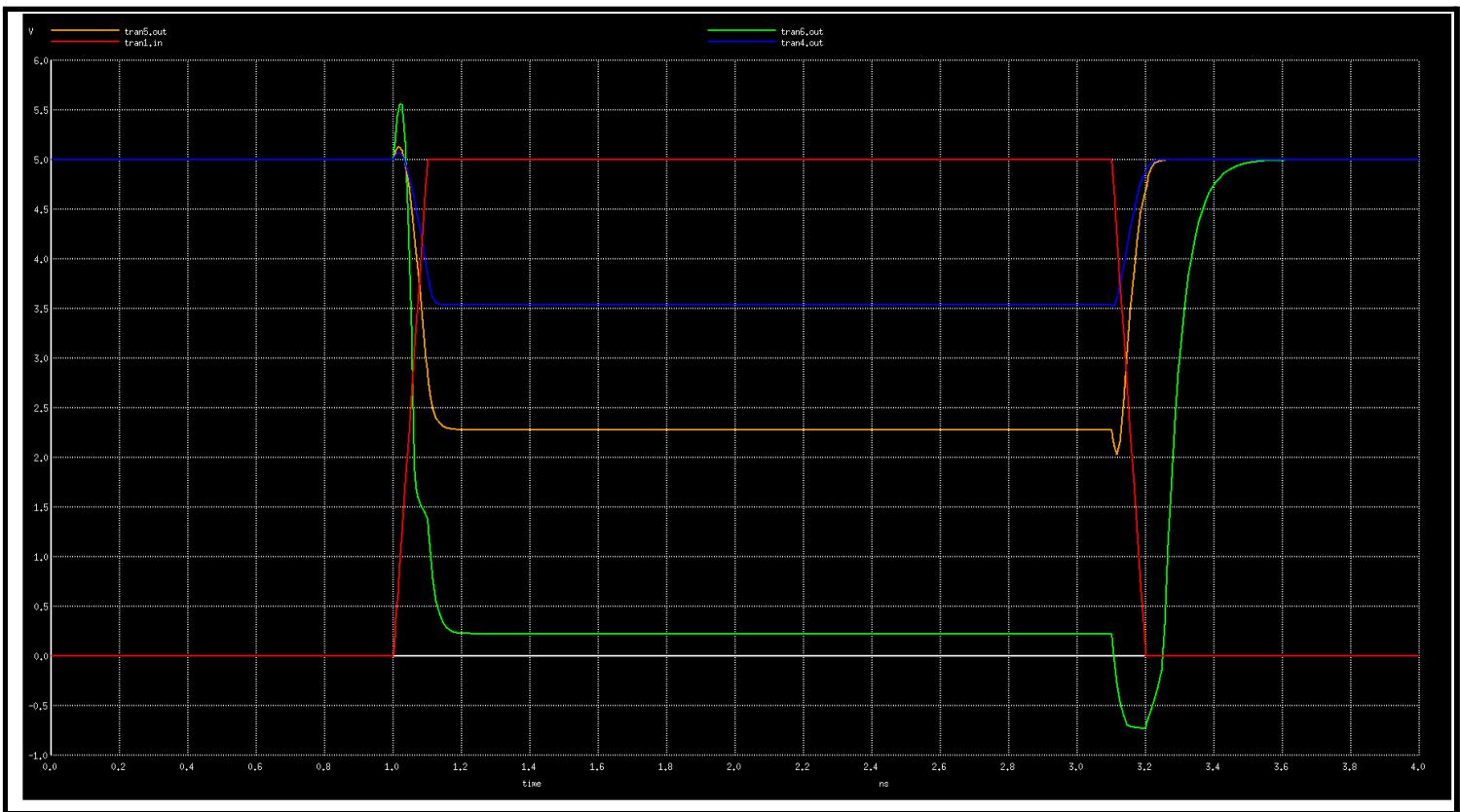
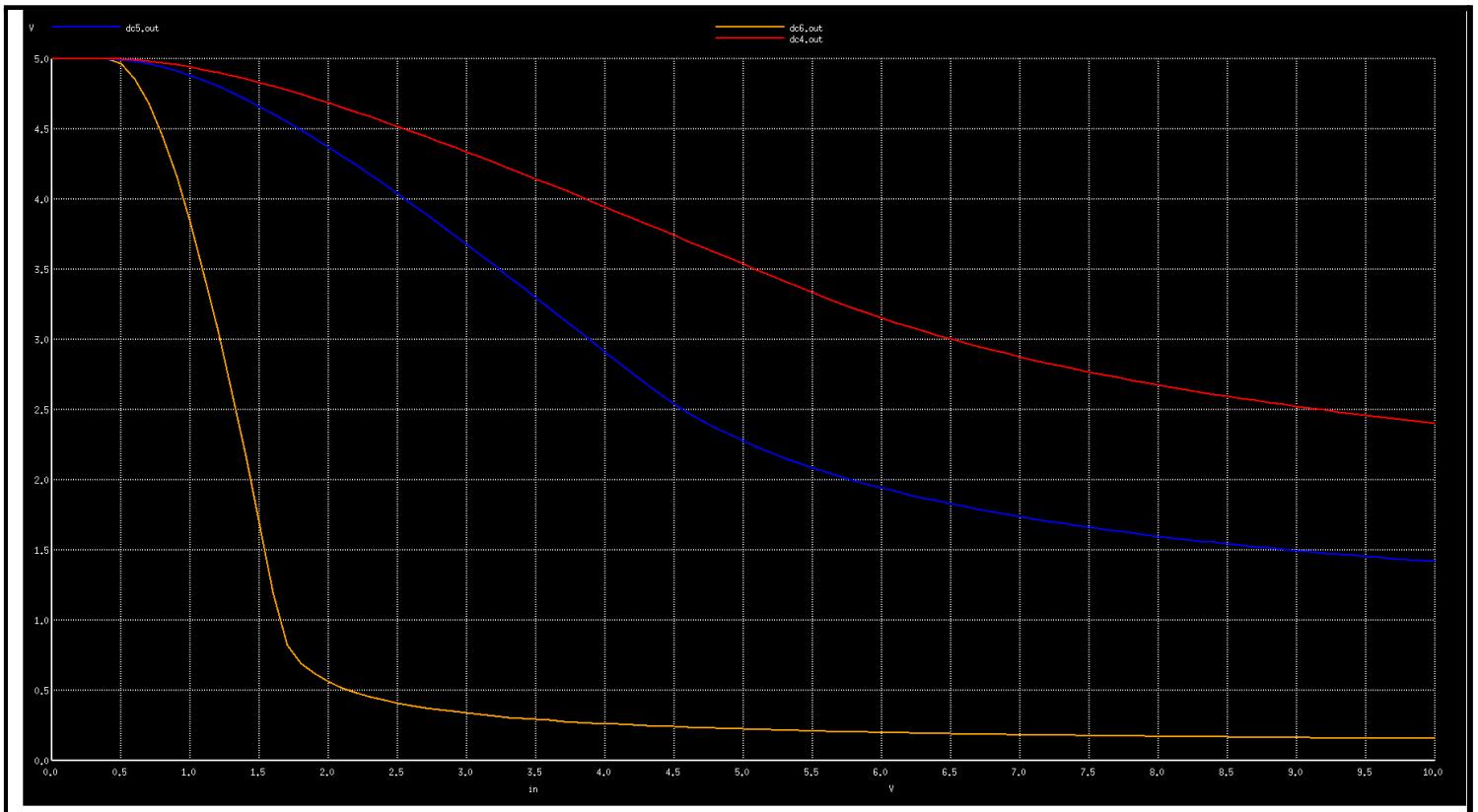
The above graphs show us the simulation plots of the DC input vs DC output, Transient response power consumed while increasing the dc value, and finally the current passing through the capacitor when varying the **Pull up Resistor**. We can see that as the resistance value increases the Dc in vs Dc out moves to the left and decreases the noise margin, then in the second graph we can see that as the resistance increases the output voltage is decreased due to the voltage divider circuit when the circuit is conducting, the third picture is the power that is consumed and we can see that it consumes power when it is in on state and the power consumed decreases as the current flowing through the circuit decreases. Then the last is the current through the capacitor for the various resistance values and we can see that the power increases and the energy consumed.

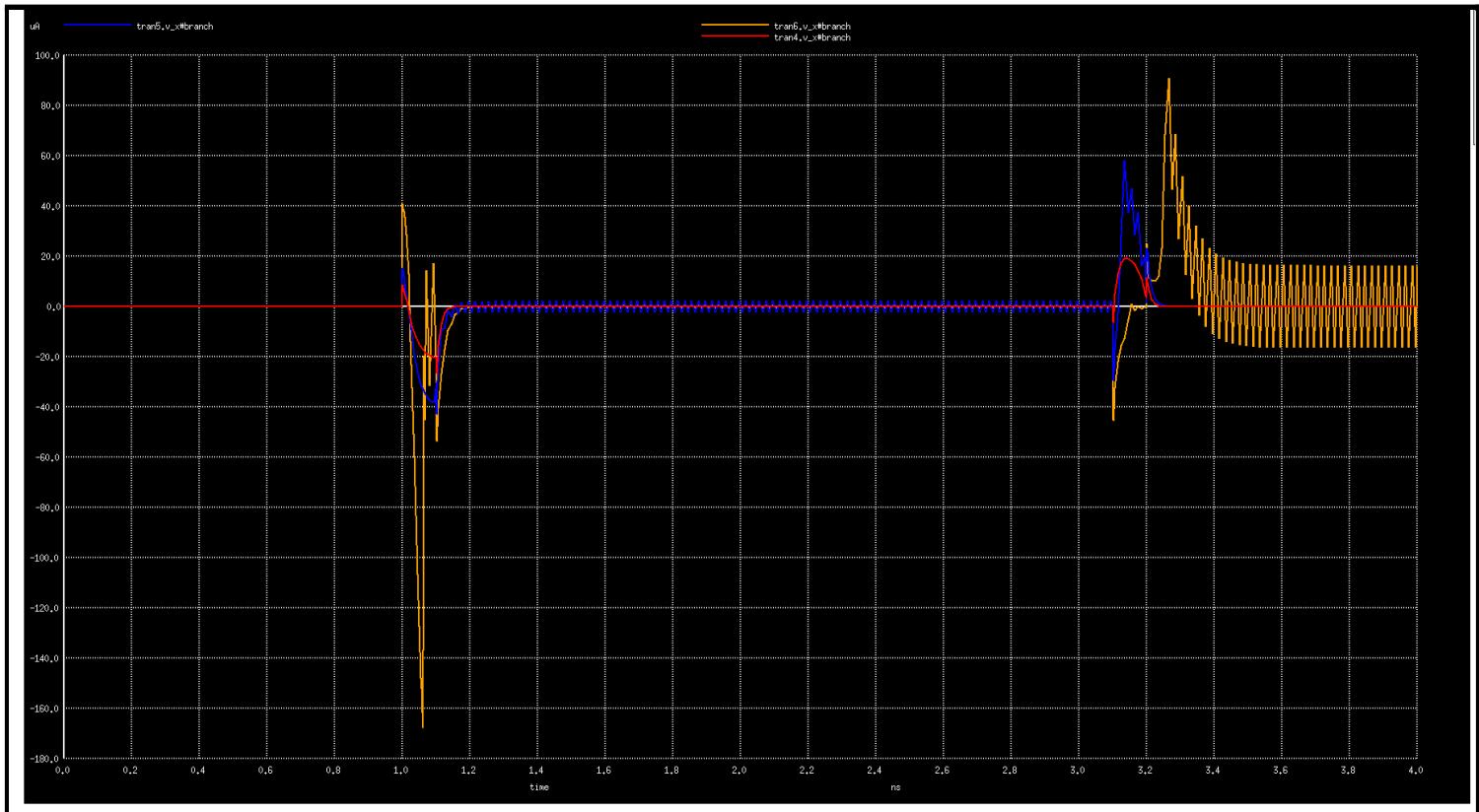
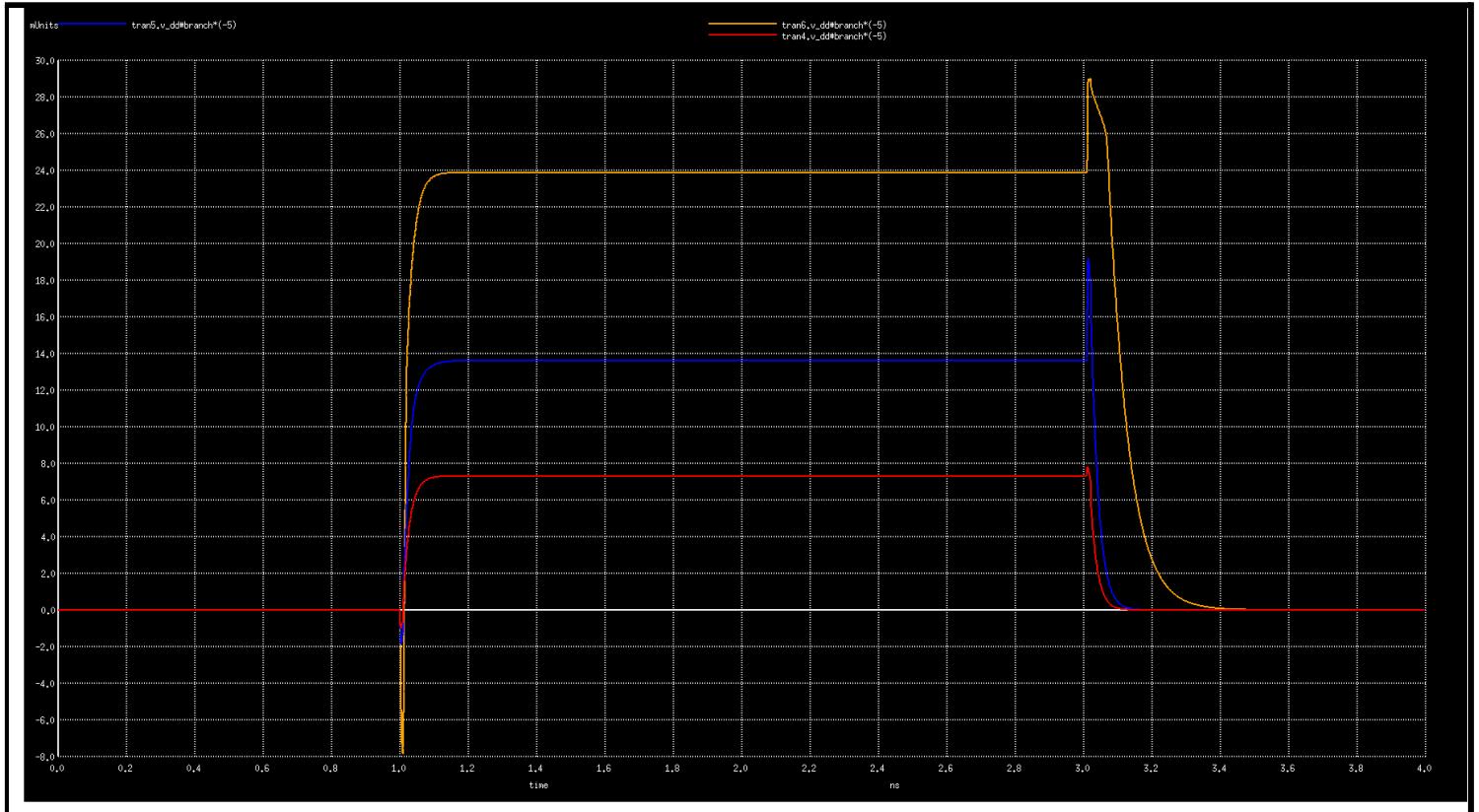
### Varying the Width of the Nmos:-

```
***Varing Width***

.control
foreach wid 3.2u 6.4u 64u
alter m1 w = $wid
run
dc V_in 0 5 0.1
meas dc vol min out
meas dc voh max out
print voh
let slope = deriv(out)
meas dc vil find in when slope = -1 cross = 1
meas dc vih find in when slope = -1 cross = 2
let nmh = voh - vih
let nml = vil - vol
print nmh nml
end
alter m1 w = 6.4u
.endc

.control
plot tran1.in tran4.out tran5.out tran6.out
plot dc4.out dc5.out dc6.out vs in
plot tran4.V_dd#branch*(-5) tran5.V_dd#branch*(-5) tran6.V_dd#branch*(-5)
plot tran4.V_x#branch tran5.V_x#branch tran6.V_x#branch
.endc
```





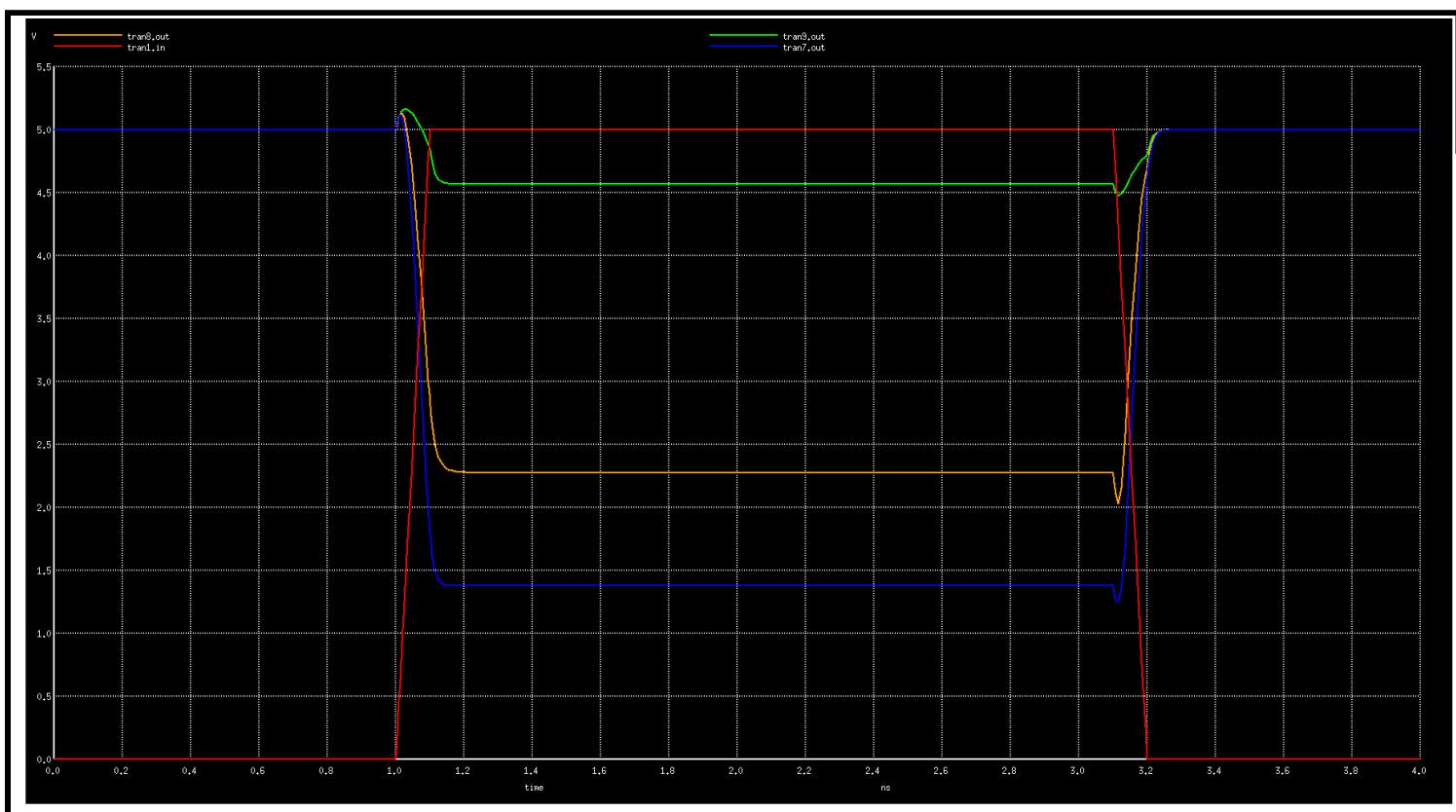
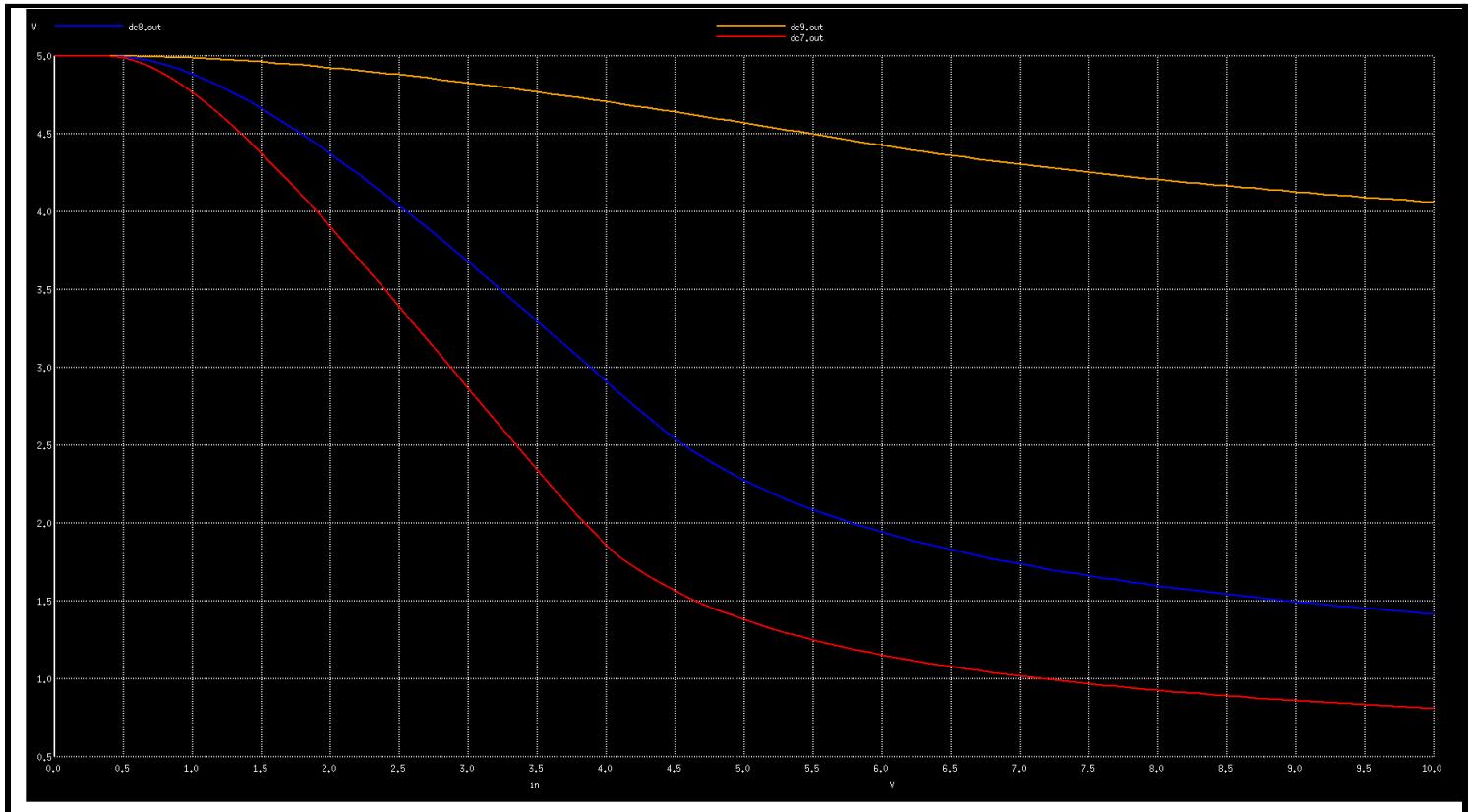
The above graphs show us the simulation plots of the DC input vs DC output, Transient response power consumed during transient analysis, and finally the current passing through the capacitor when varying the **Pull down Nmos**. We can see that as the width value increases the Dc in vs Dc out moves to the left and decreases the noise margin, then in the second graph we can see that as the width increases the output voltage is increases due to the voltage divider circuit when the circuit is conducting, the third picture is the power that is consumed and we can see that it consumes power when it is in on state and the power consumed increases as the current flowing through the circuit increases. Then the last is the current through the capacitor for the various resistance values and we can see that the power increases and the energy consumed.

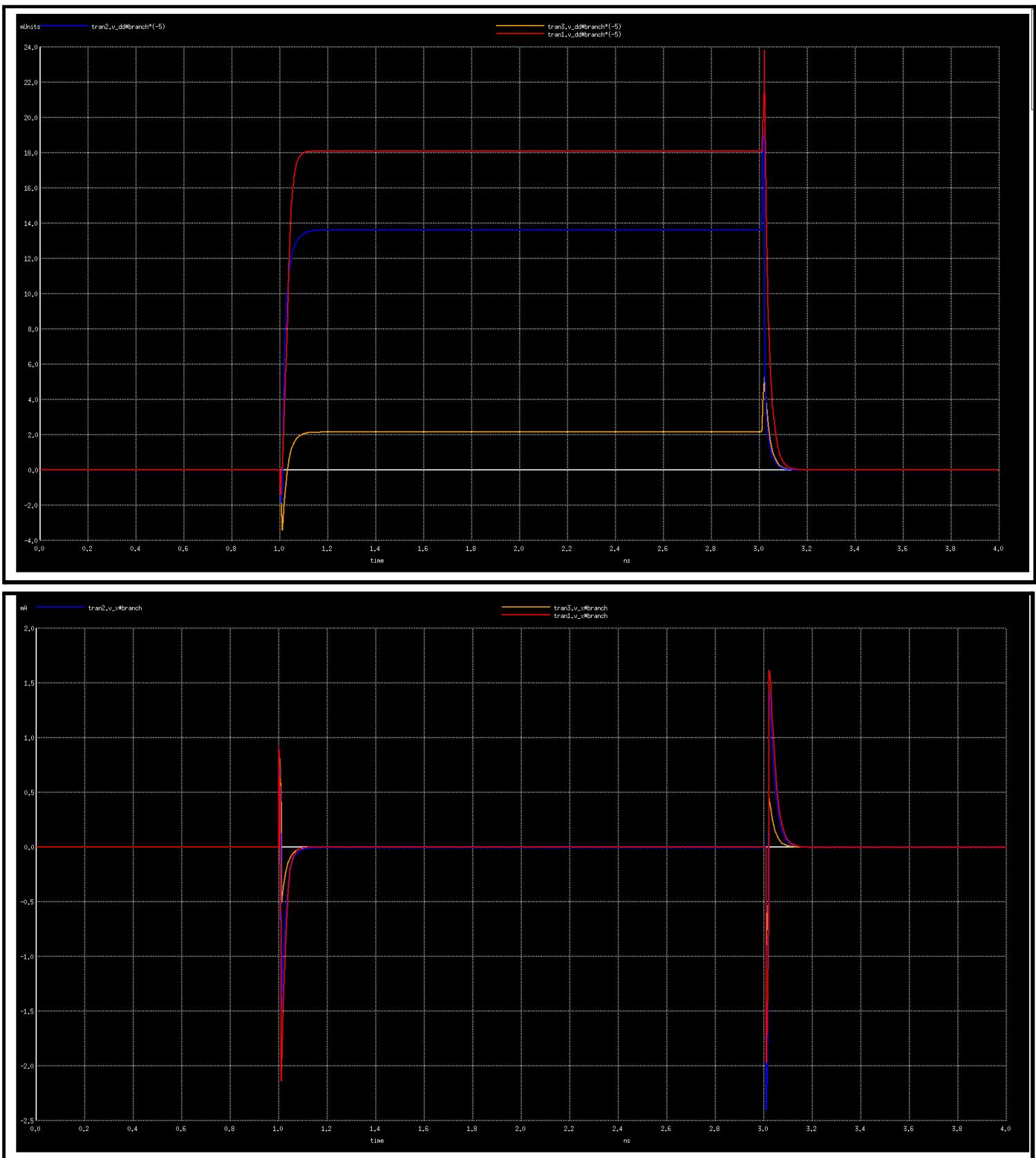
### Varying the Length of the Nmos:-

```
***Varing Length***

.control
foreach len 0.9u 1.8u 18u
alter m1 l = $len
run
dc V_in 0 5 0.1
meas dc vol min out
meas dc voh max out
print voh
let slope = deriv(out)
meas dc vil find in when slope = -1 cross = 1
meas dc vih find in when slope = -1 cross = 2
let nmh = voh - vih
let nml = vil - vol
print nmh nml
end
alter m1 l = 1.8u
.endc

.control
plot tran1.in tran7.out tran8.out tran9.out
plot dc7.out dc8.out dc9.out vs in
plot tran7.V_dd#branch*(-5) tran8.V_dd#branch*(-5) tran9.V_dd#branch*(-5)
plot tran7.V_x#branch tran8.V_x#branch tran9.V_x#branch
.endc
```





The above graphs show us the simulation plots of the DC input vs DC output, Transient response power consumed during transient analysis, and finally the current passing through the capacitor when varying the **Length Pull down Nmos**. We can see

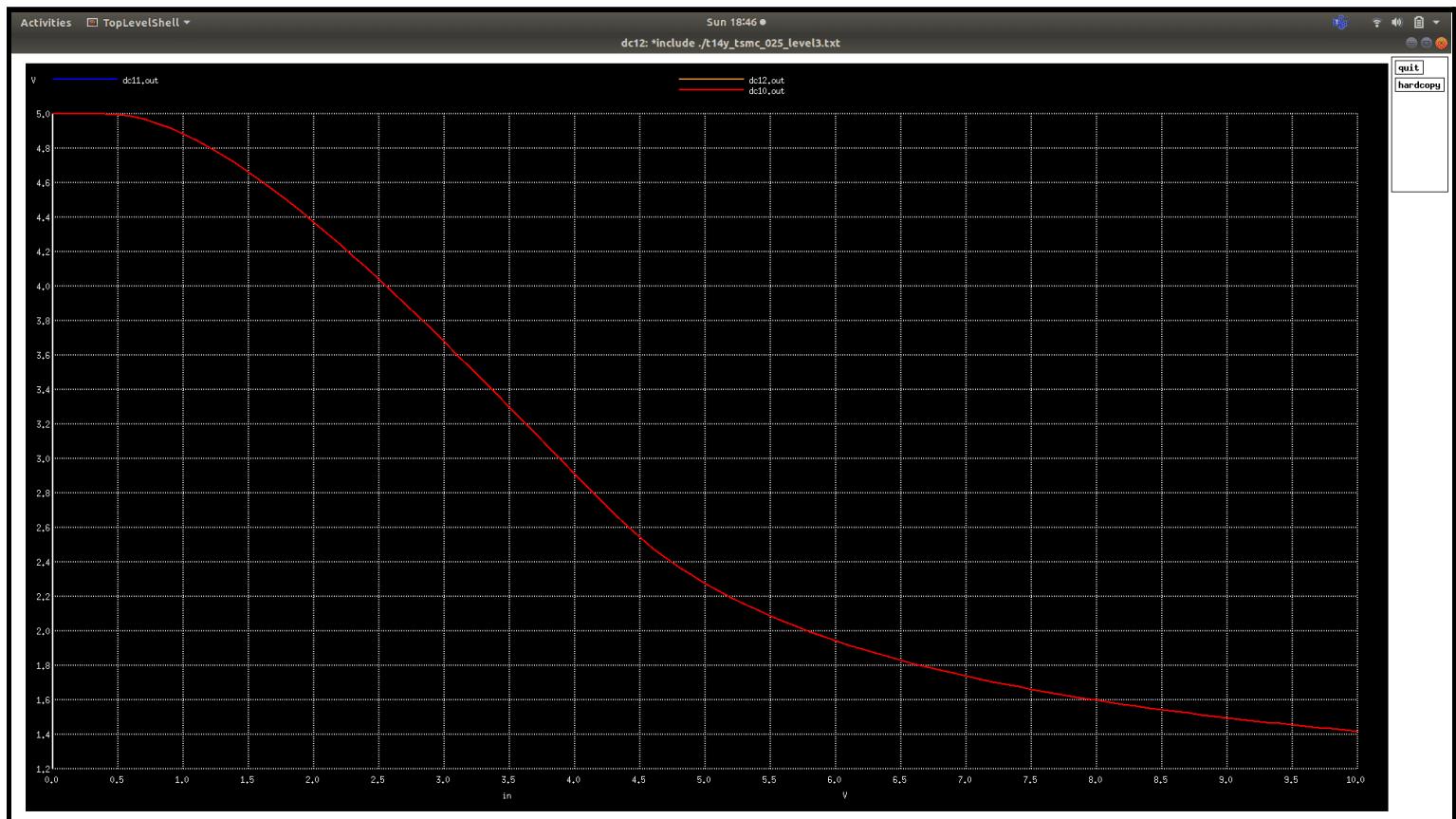
that as the length value increases the Dc in vs Dc out moves to the right and increases the noise margin, then in the second graph we can see that as the length decreases the output voltage is decreased as the resistance of mosfet increases and due to the voltage divider circuit, the drop is noticed. The third picture is the power that is consumed and we can see that it consumes power when it is in the steady state and the power consumed decreases as the current flowing through the circuit decreases. Then the last is the current through the capacitor decreases as the length increases for the various lengths.

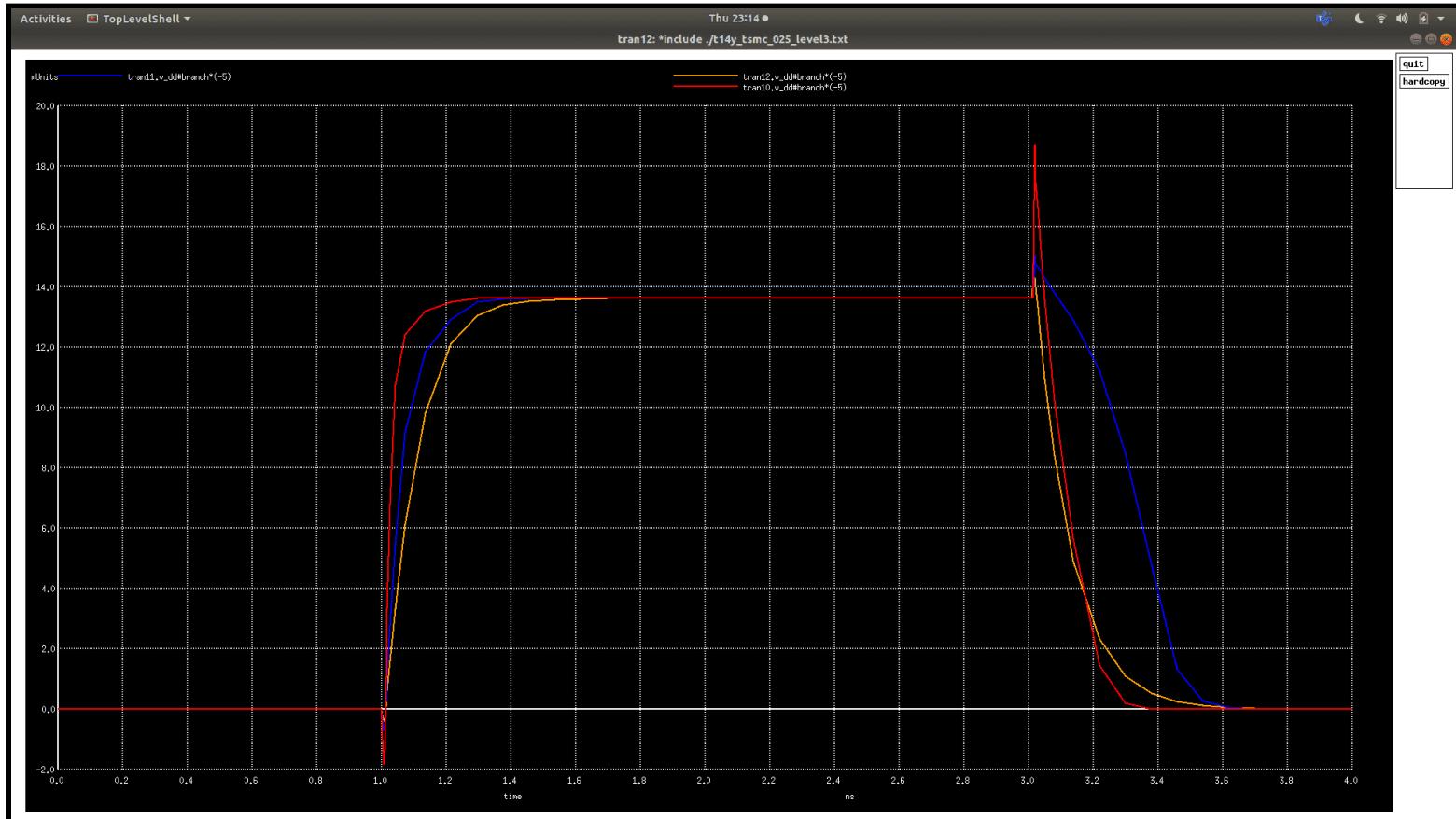
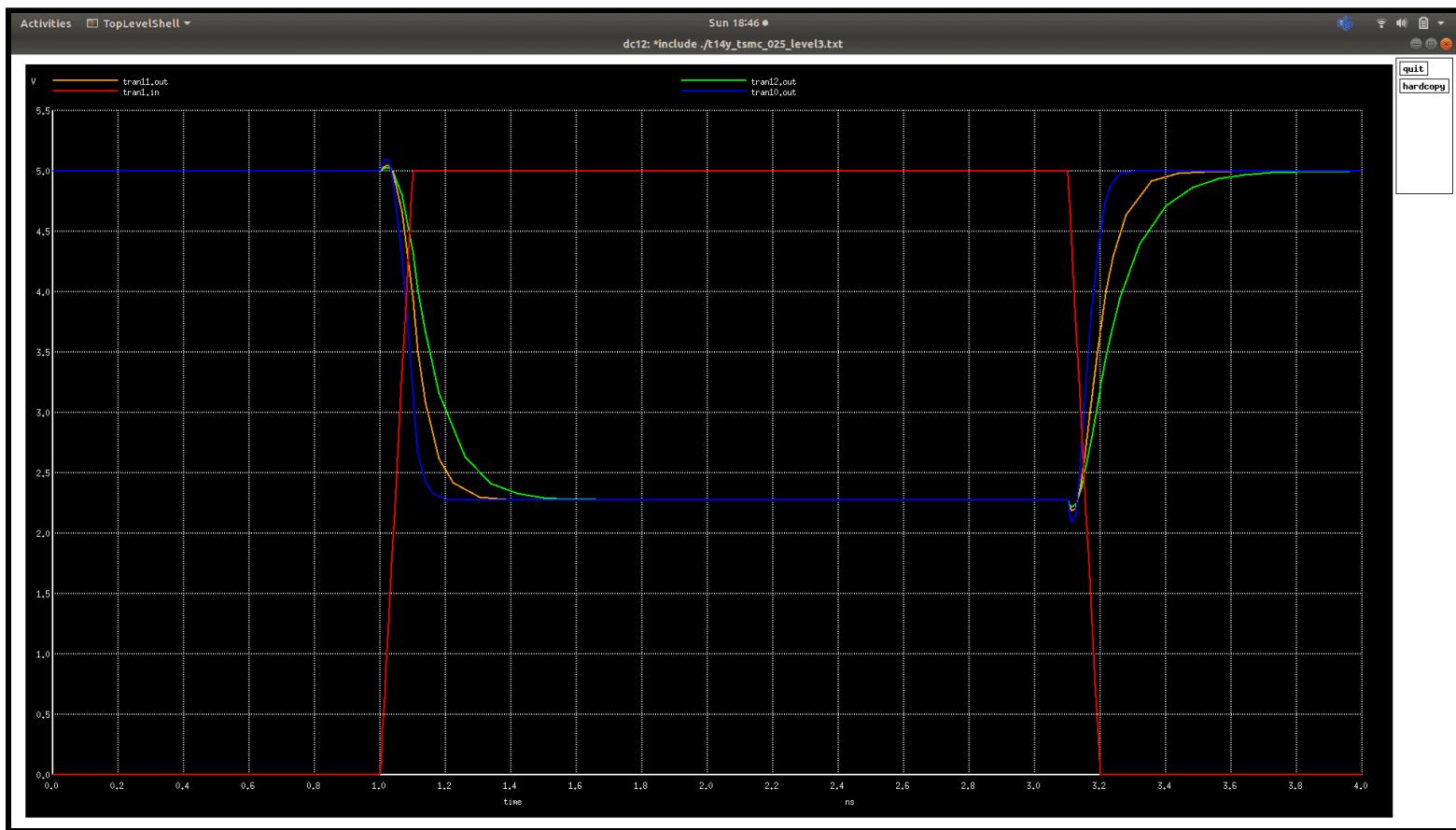
## Varying the Load Capacitance of the Inverter:-

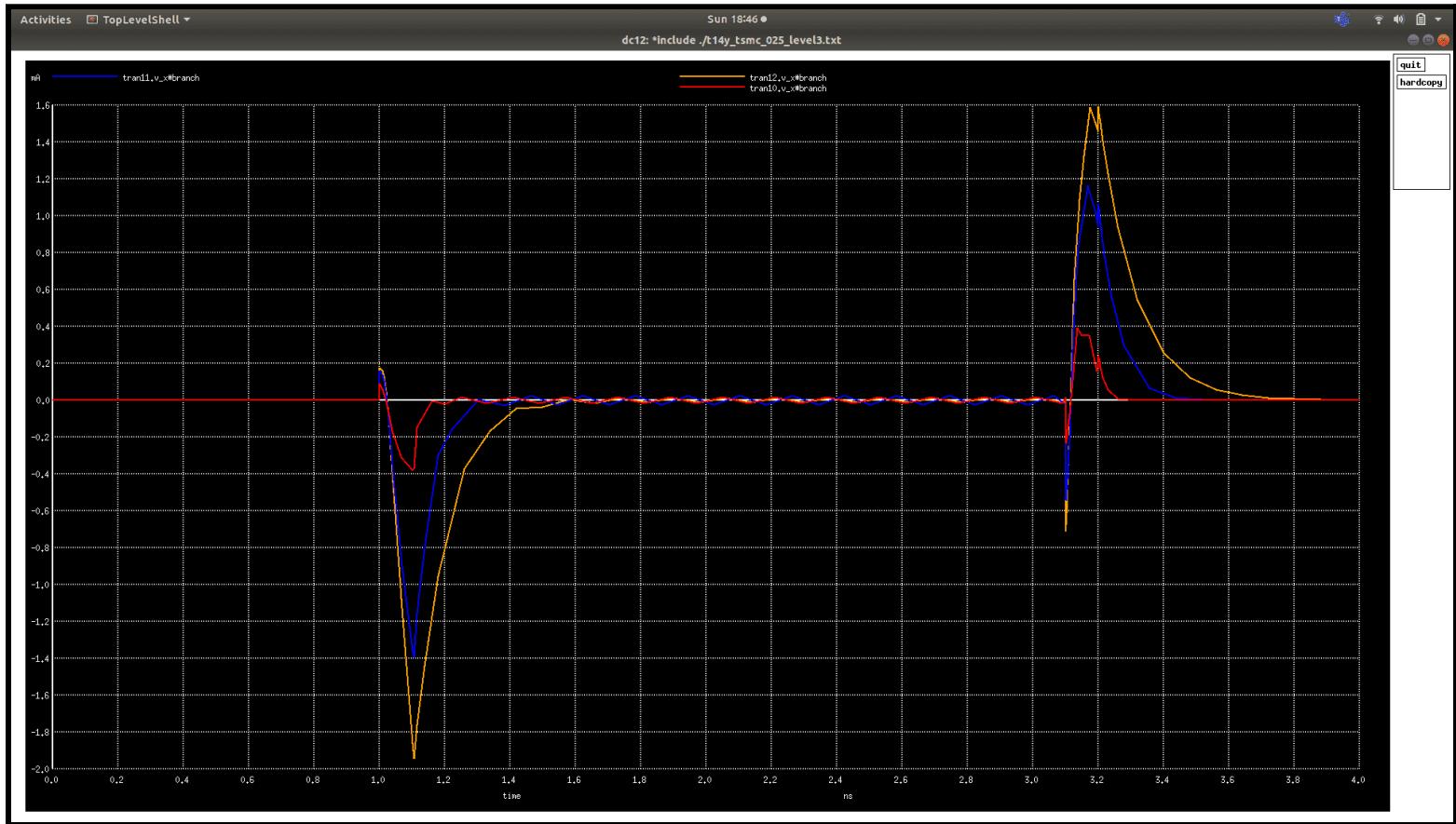
```
***Varying Capacitor***

.control
foreach cap 0.01p 0.05p 0.1p
  alter c1 = $cap
  tran 0.001 4n
  dc V_in 0 10 0.1
end
.endc

.control
plot tran1.in tran10.out tran11.out tran12.out
plot dc10.out dc11.out dc12.out vs in
plot dc10.V_dd#branch*(-5) dc11.V_dd#branch*(-5) dc12.V_dd#branch*(-5)
plot tran10.V_x#branch tran11.V_x#branch tran12.V_x#branch
.endc
.end
```







The above graphs show us the simulation plots of the DC input vs DC output, Transient response power consumed during transient analysis, and finally the current passing through the capacitor when varying the **Load Capacitance of the Nmos**. We can see that as the capacitance value increases the Dc in vs Dc out does not change, then in the second graph we can see that as the capacitance increases the rise time and fall time increases. The third picture is the power that is consumed and we can see that it consumes power when it is in the steady state and the power consumed decreases as the current flowing through the circuit decreases. Then the last is the current through the capacitor increases as the capacitance increases for the various capacitances.

### Conclusion:-

The experiment was performed, and all graphs were analysed. The obtained graphs movements agreed with theory, and hence simulations were verified. NGSPICE was the simulator used for this task.

### 3. Study of MOS Inverter with Active Load

#### Objectives:-

Study the

- Transfer function

- Noise margin

- Effect on rise time, falltime

- Propagation delay,

And the power and energy consumed of a MOS inverter for various L, W of the pull up pull down network, and energy consumed in non ideal step input.

#### Introduction:-

Inverter is one that inverts the signal supplied at its input. If input is made high or logic level is 1, then the output has logic level 0 and vice-versa. An active load inverter is characterised by a Pmos between the pull down transistor and the voltage source. The output is taken at the junction of the Pmos and the pull down transistor. The pull-up circuit is constituted by the Pmos and pull-down resistor by the NMOS. When the input is low, the NMOS is open circuited and the output capacitance is charged to VDD through Pmos.

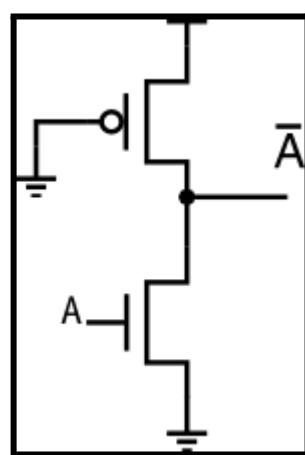


Fig: Inverter with Pmos Load

## Varying the Width of the Nmos:-

\*Inverter with pseudo NMOS load varying length  
 .include ./t14y\_tsmc\_025\_level3.txt

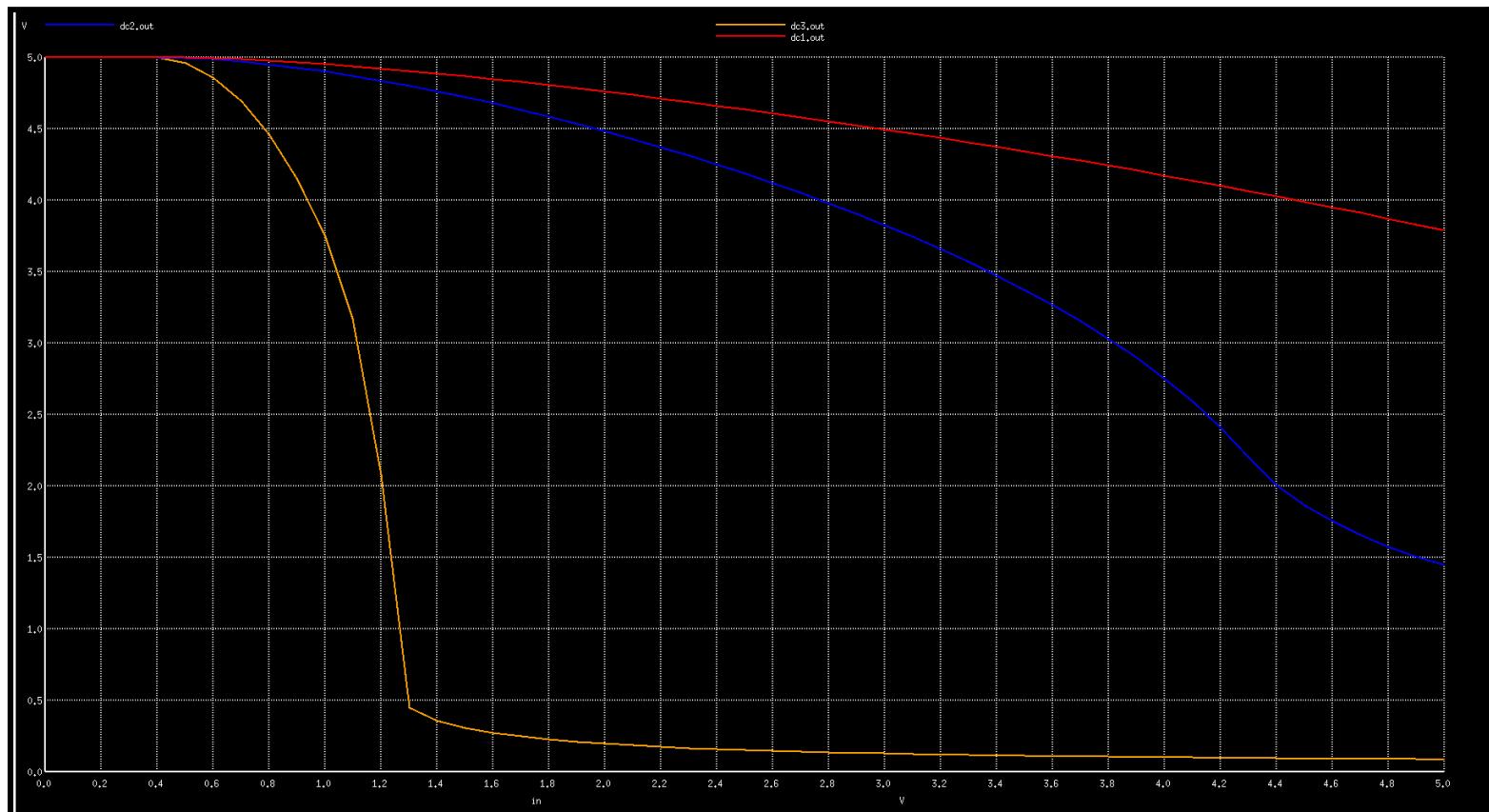
```
m0 out in 0 0 cmosn w=1u l=1u
m1 out 0 vdd vdd cmosp w=2.5u l=1u

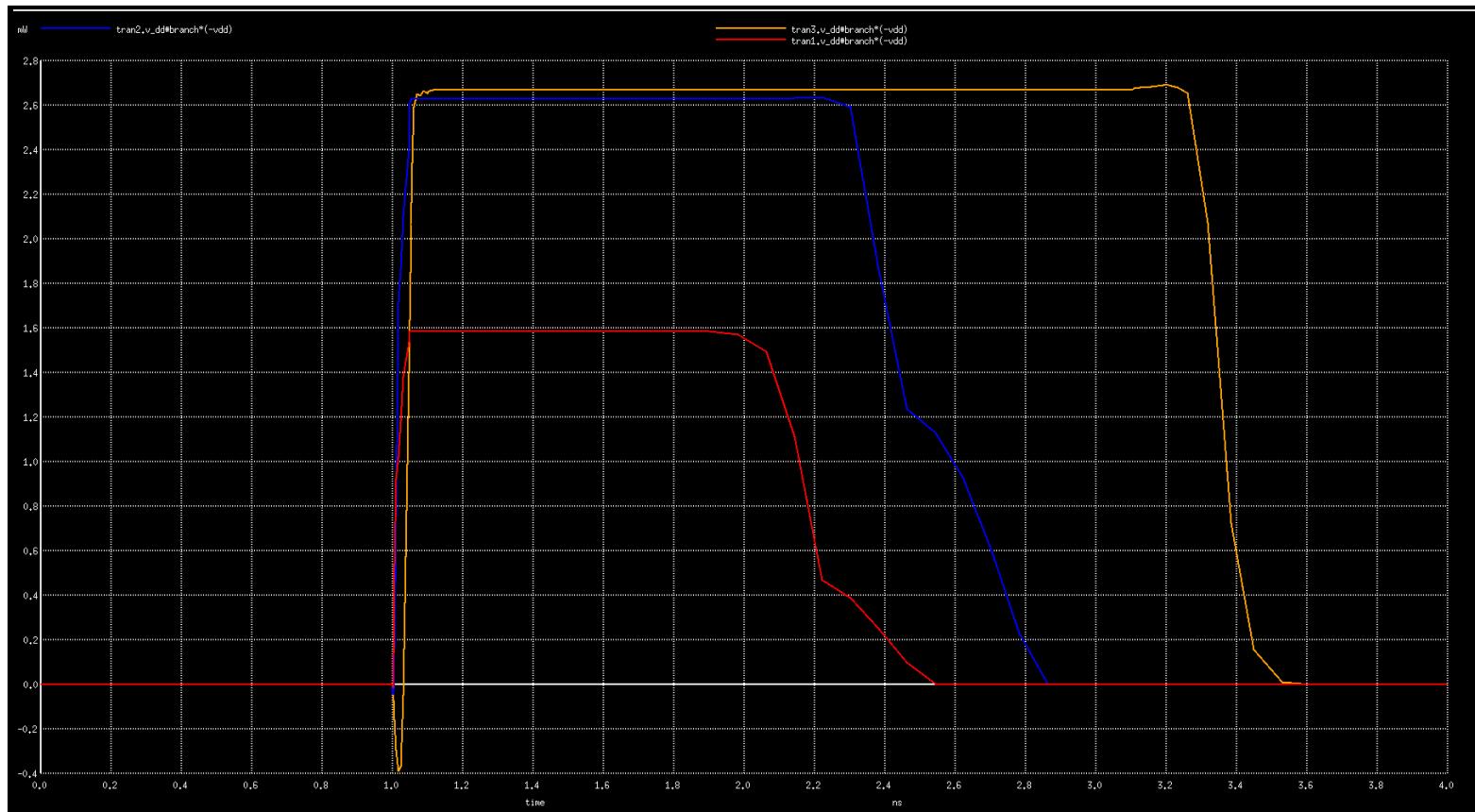
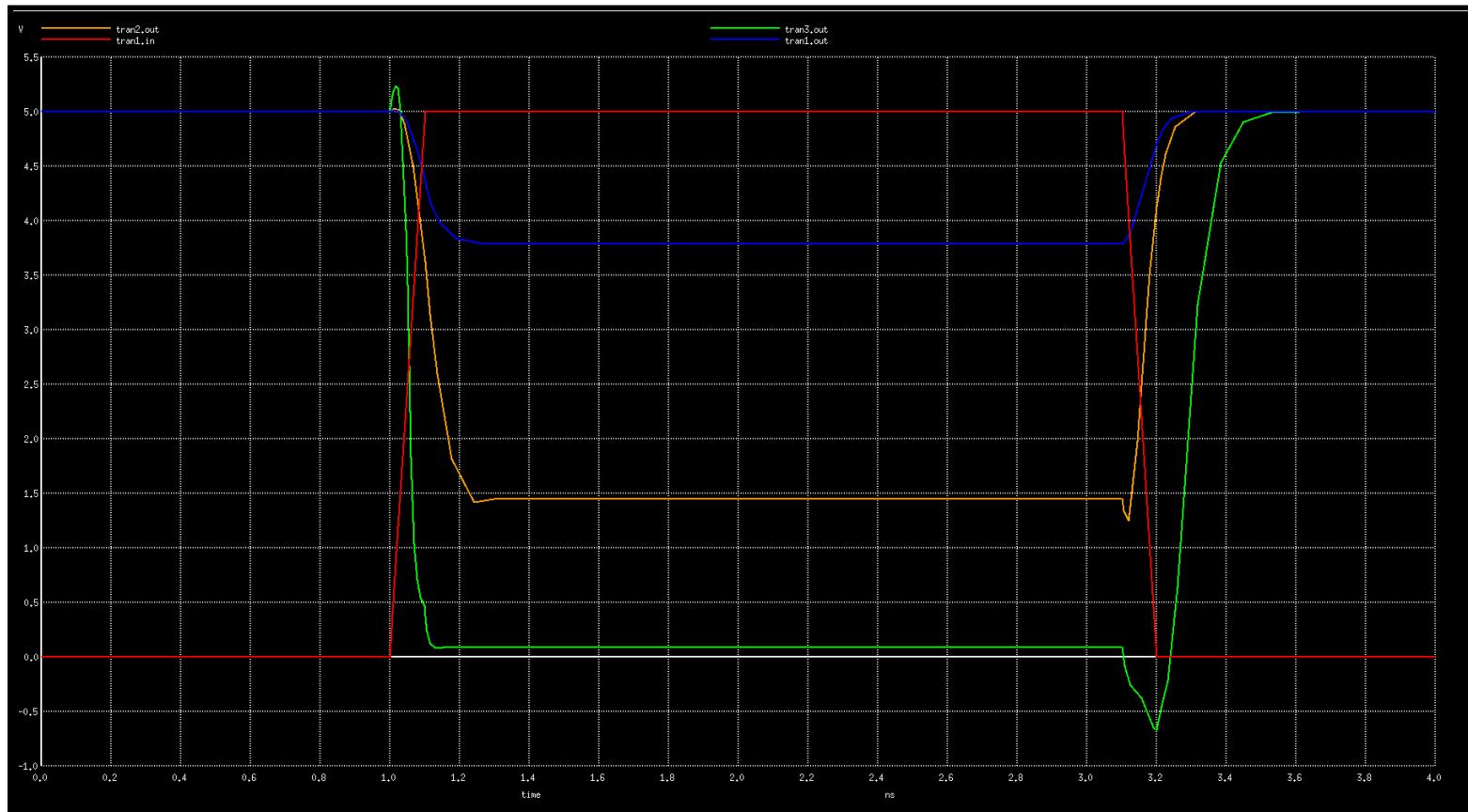
V_dd vdd 0 5
v_in in 0 dc 2.5 pulse(0 5 1n 0.1n 0.1n 2n 4n)
```

\*Transfer function and transient response on varying **WIDTH** of **DRIVER** mosfet

```
.control
foreach len 0.5u 1u 10u
alter m0 l=$len
tran 0.1n 4ns
dc v_in 0 5 0.1
end
alter m0 l=1u
.endc

.control
plot dc1.out dc2.out dc3.out vs in
plot tran1.in tran1.out tran2.out tran3.out
plot tran1.v_dd#branch*(-vdd) tran2.v_dd#branch*(-vdd) tran3.v_dd#branch*(-vdd)
.endc
```



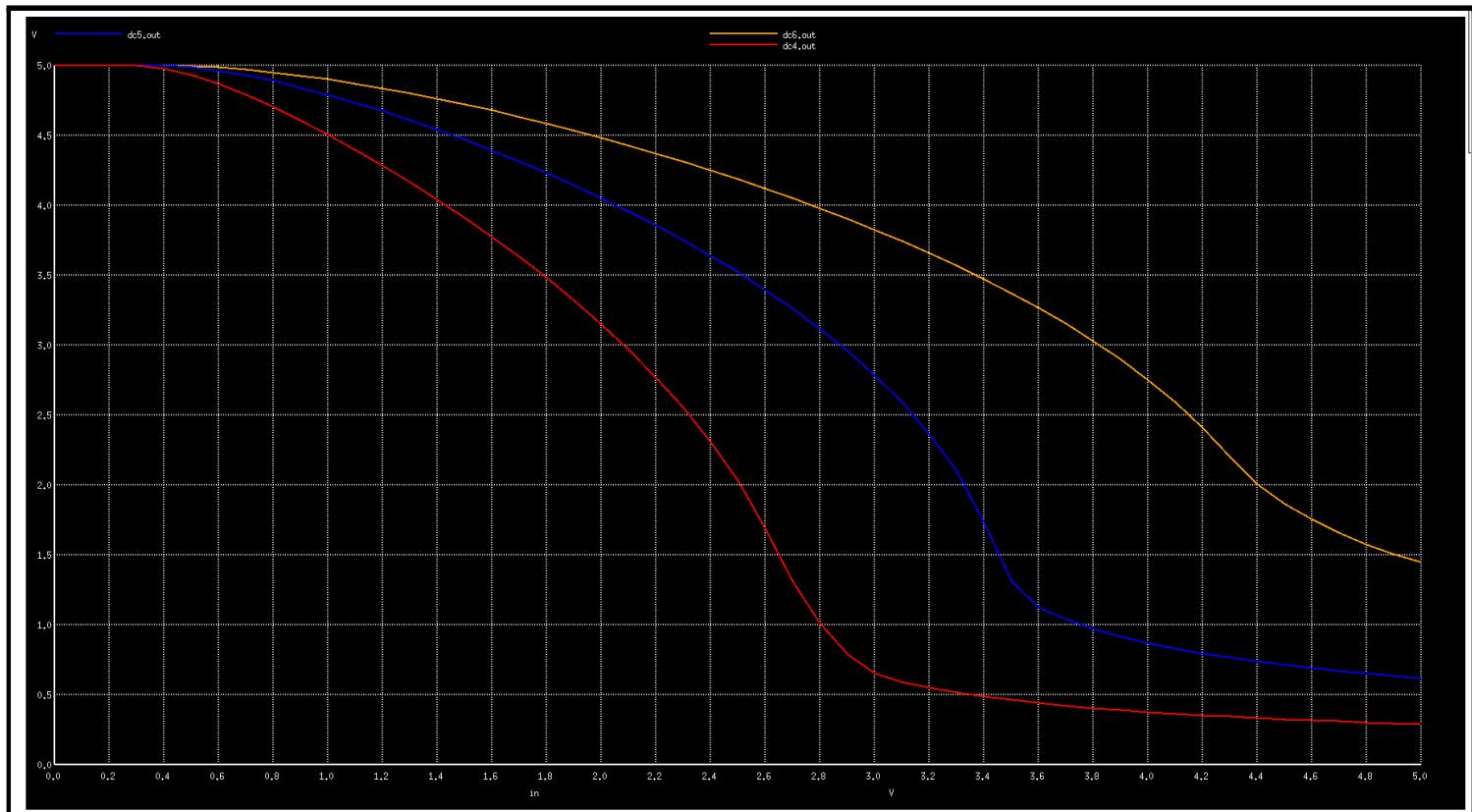


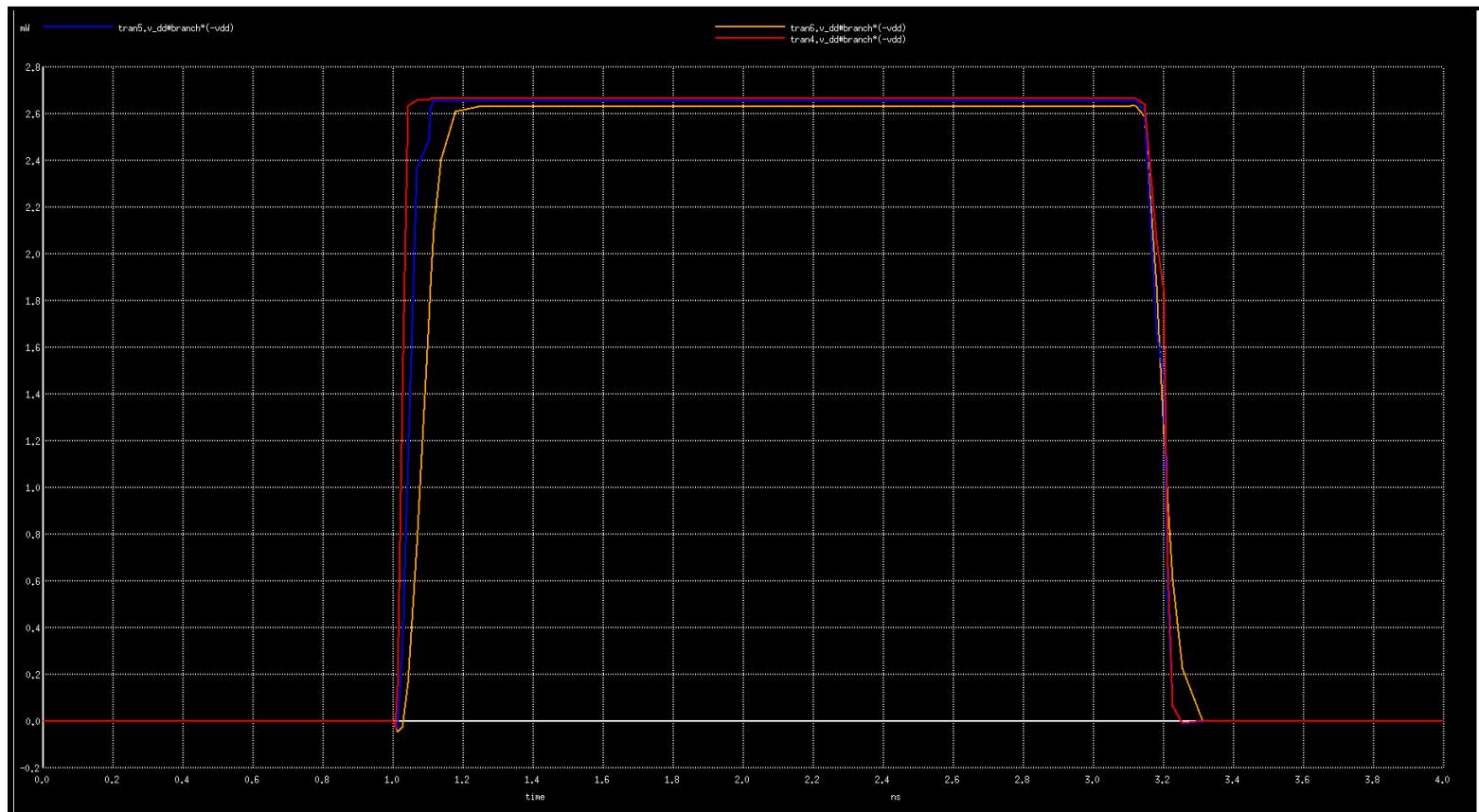
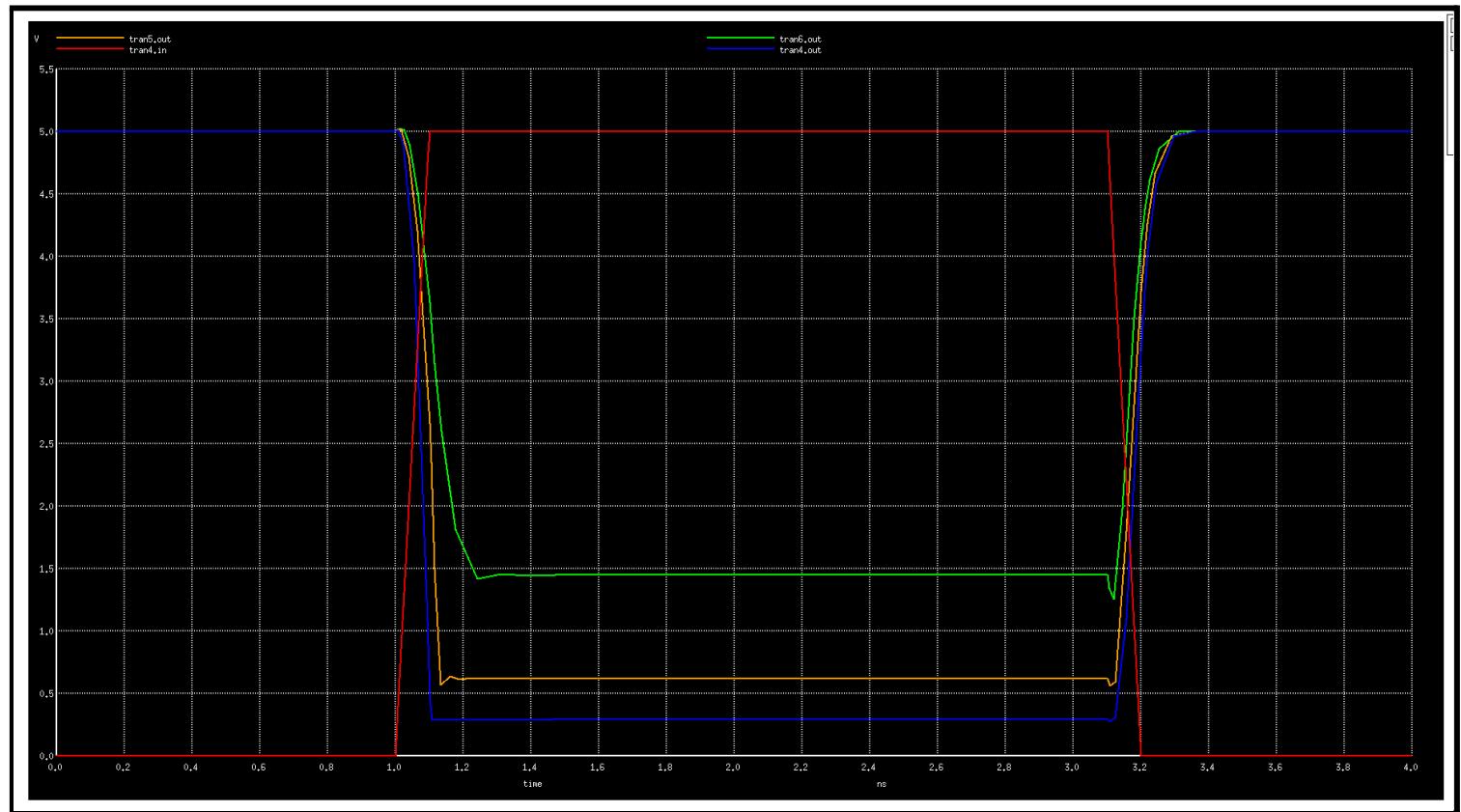
The above graphs show us the simulation plots of the DC input vs DC output, Transient response power consumed during transient analysis, when varying the width of **Pull down Nmos**. We can see that as the width value increases the Dc in vs Dc out moves to the left and decreases the noise margin, then in the second graph we can see that as the width increases the output voltage, it increases due to the voltage divider circuit when the circuit is conducting, the third picture is the power that is consumed and we can see that it consumes power when it is in on state and the power consumed increases as the current flowing through the circuit increases, this happened when the width increase.

### Varying the Length of the Nmos:-

```
*Transfer function and transient response on varying LENGTH of DRIVER mosfet
.control
foreach len 0.25u 0.5u 1u
alter m0 l=$len
tran 0.1n 4ns
dc v_in 0 5 0.1
end
alter m0 l=0.5
.endc

.control
plot dc4.out dc5.out dc6.out vs in
plot tran4.in tran4.out tran5.out tran6.out
plot tran4.v_dd#branch*(-vdd) tran5.v_dd#branch*(-vdd) tran6.v_dd#branch*(-vdd)
.endc
```



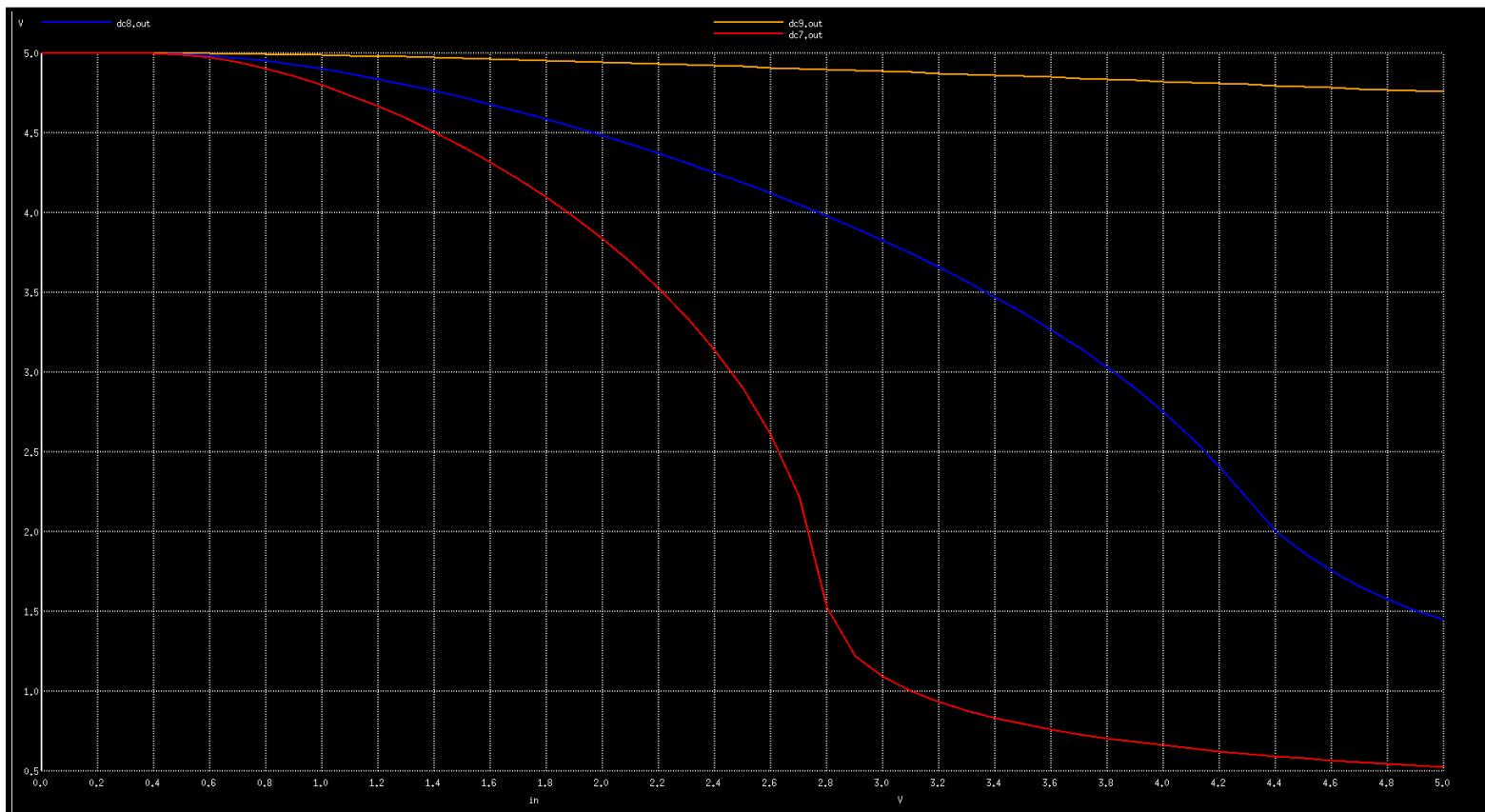


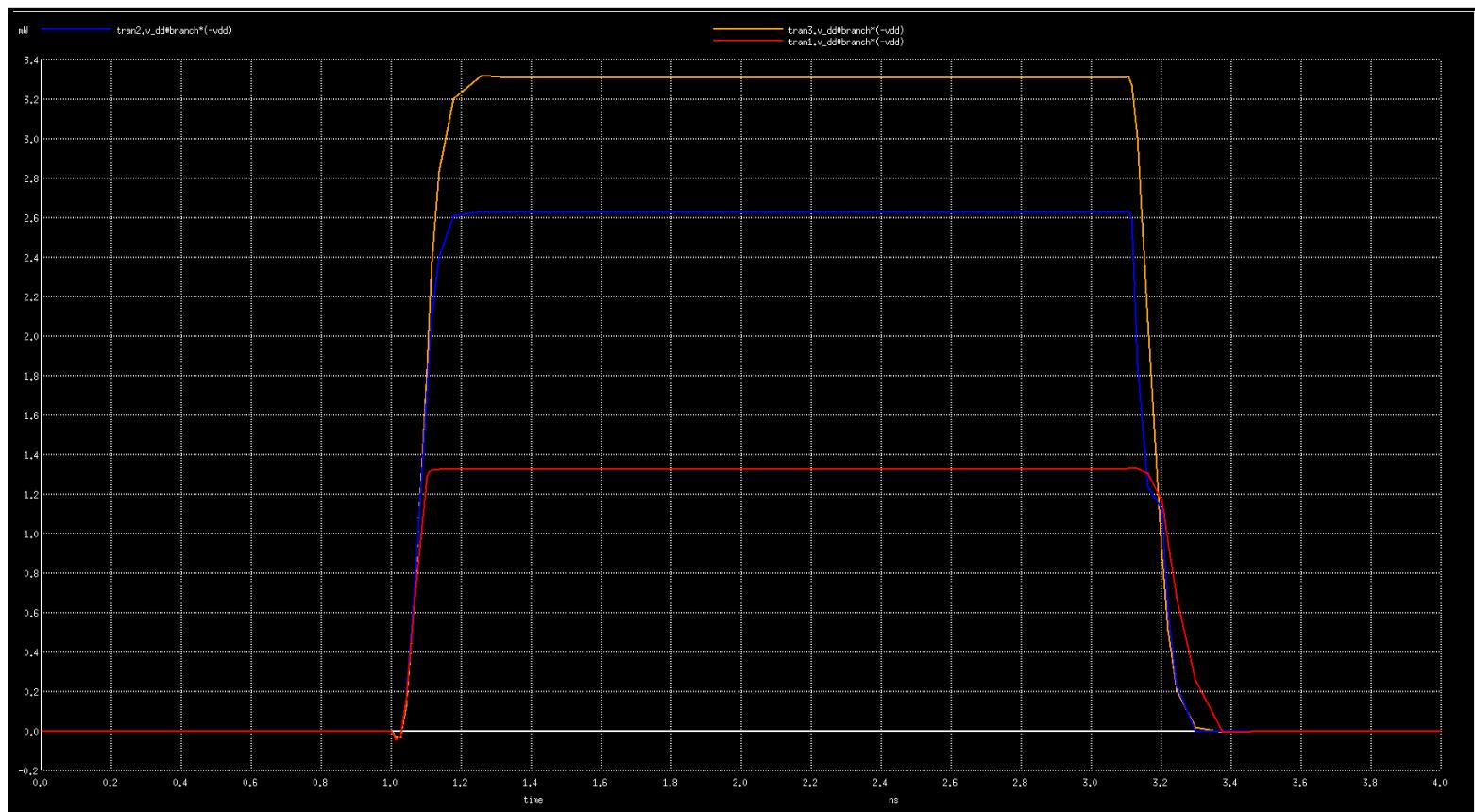
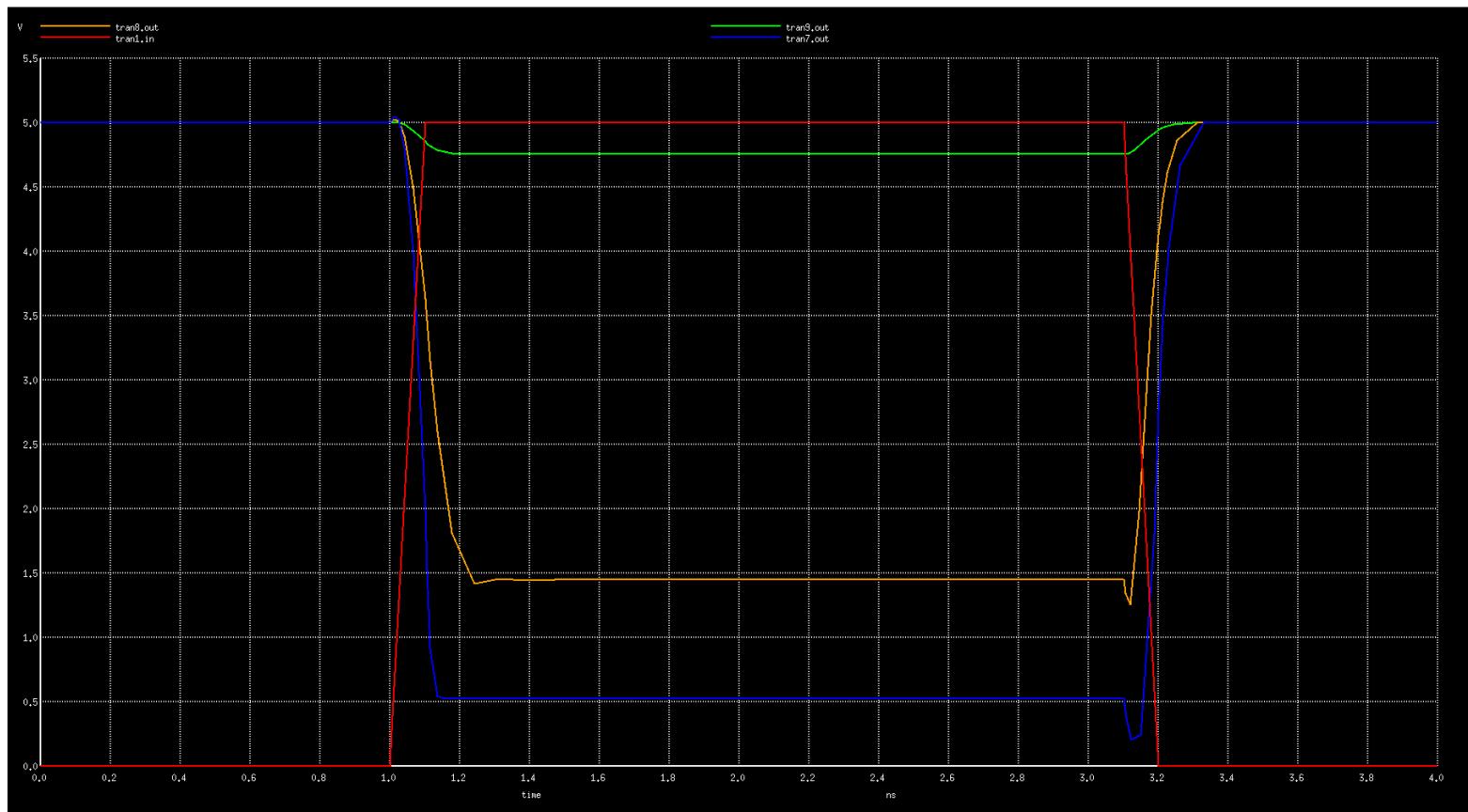
The above graphs show us the simulation plots of the DC input vs DC output, Transient response power consumed during transient analysis, when varying the **Length Pull down Nmos**. We can see that as the length value increases the Dc in vs Dc out moves to the right and increases the noise margin, then in the second graph we can see that as the length decreases the output voltage is decreased as the resistance of mosfet increases and due to the voltage divider circuit, the drop is noticed. The third picture is the power that is consumed and we can see that it consumes power when it is in the steady state and the power consumed decreases as the current flowing through the circuit decreases.

### Varying the Width of the Load Pmos:-

```
*Transfer function and transient response on varying WIDTH of LOAD mosfet
.control
foreach wid 1.25u 2.5u 25u
    alter m1 w=$wid
    tran 0.1n 4ns
    dc v_in 0 5 0.1
end
alter m1 w=2.5u
.endc

.control
    plot dc7.out dc8.out dc9.out vs in
    plot tran1.in tran7.out tran8.out tran9.out
    plot tran7.v_dd#branch*(-vdd) tran8.v_dd#branch*(-vdd) tran9.v_dd#branch*(-vdd)
.endc
```





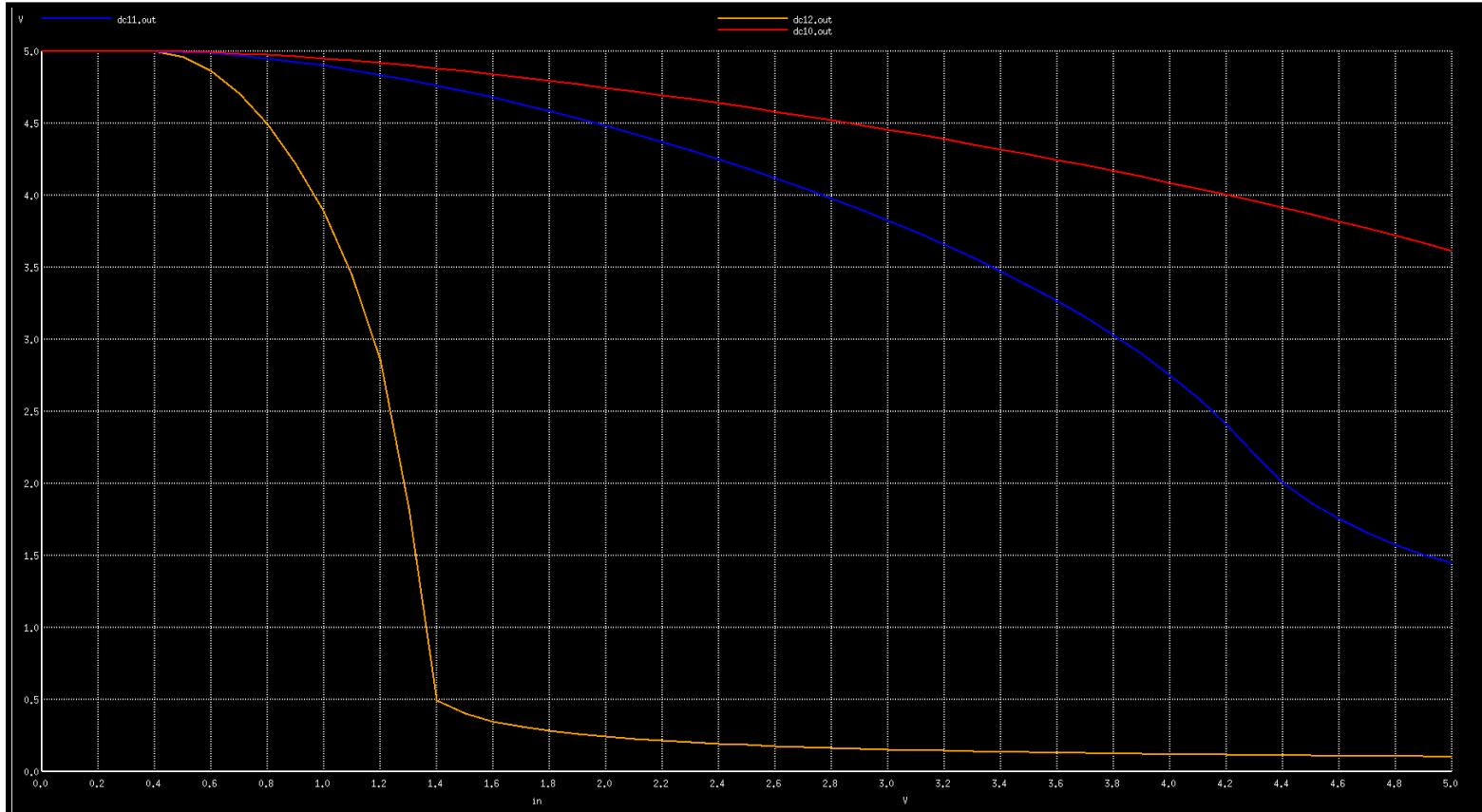
The above graphs show us the simulation plots of the DC input vs DC output, Transient response power consumed during transient analysis, when varying the **Width Pull up Pmos**. We can see that as the width value increases the Dc in vs Dc out moves to the right and increases the noise margin, then in the second graph we can see that as the width increase decreases the output voltage, this happened because the resistance value is decreased. The third picture is the power that is consumed and we can see that it consumes power when it is in the steady state and the power consumed increases as the current flowing through the circuit increases.

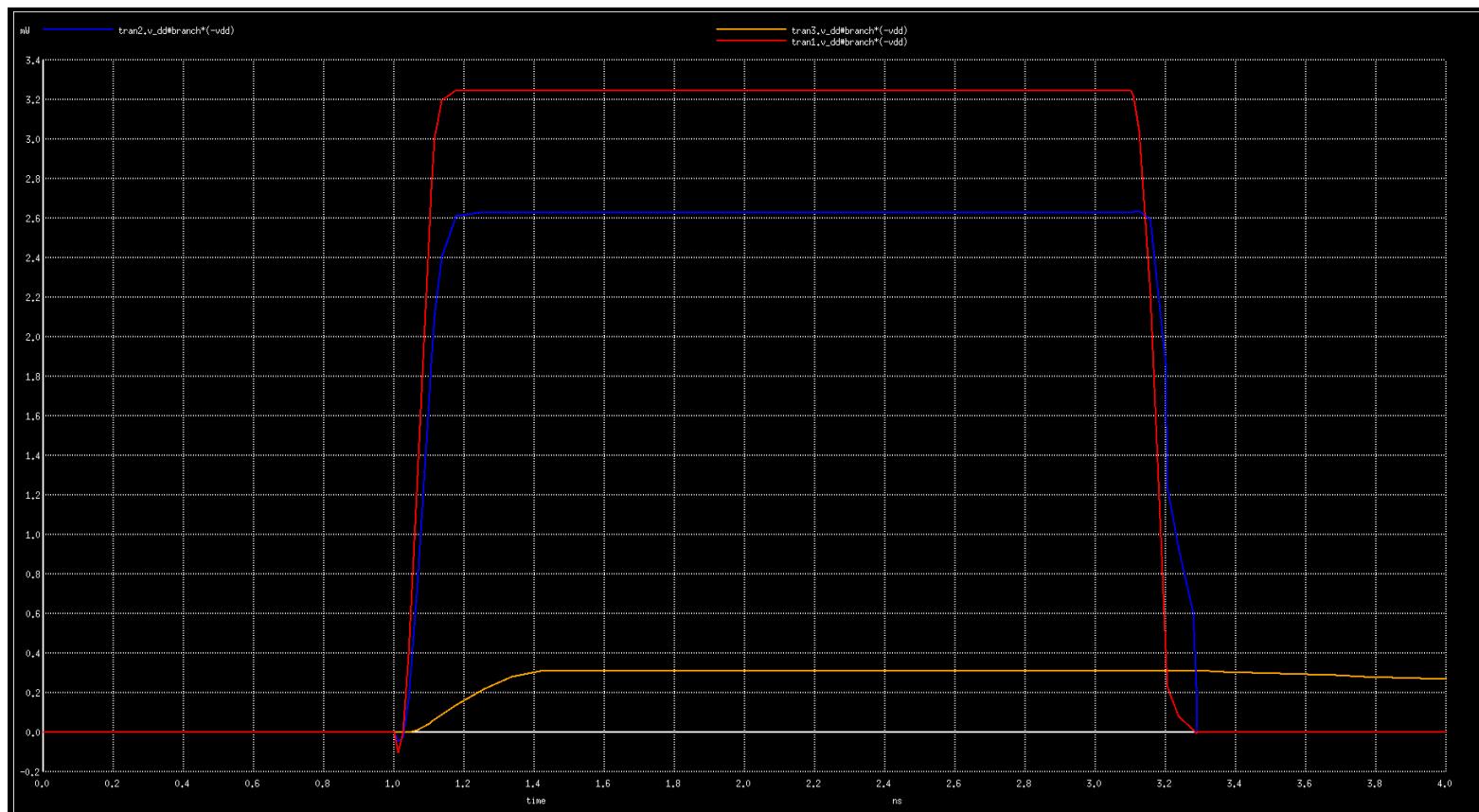
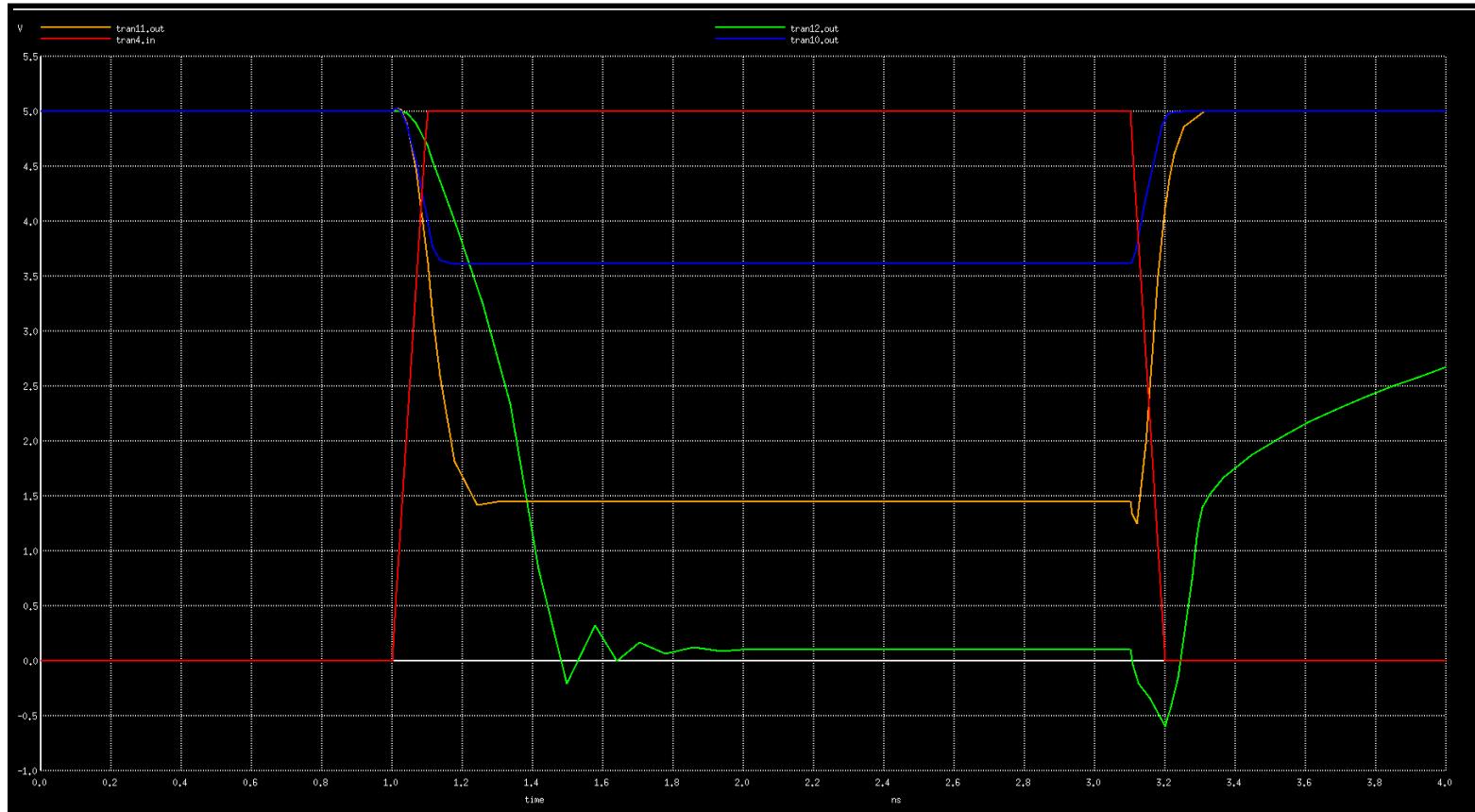
### Varying the Length of the Load Pmos:-

\*Transfer function and transient response on varying LENGTH of LOAD mosfet

```
.control
foreach len 0.5u 1u 10u
alter m1 l=$len
tran 0.1n 4ns
dc v_in 0 5 0.1
end
.endc

.control
plot dc10.out dc11.out dc12.out vs in
plot tran4.in tran10.out tran11.out tran12.out
plot tran10.v_dd#branch*(-vdd) tran11.v_dd#branch*(-vdd) tran12.v_dd#branch*(-vdd)
.endc
```





The above graphs show us the simulation plots of the DC input vs DC output, Transient response power consumed during transient analysis, when varying the length of **Pull up Pmos**. We can see that as the length value increases the Dc in vs Dc out moves to the left and decreases the noise margin, then in the second graph we can see that as the length increases the output voltage, this happens because the resistance value is increased. The third picture is the power that is consumed and we can see that it consumes power when it is in the steady state and the power consumed decreases as the current flowing through the circuit decreases.

Varying rise time fall time:-

```
*3_b*
*Varying input rise time and fall time
.include ./t14y_tsmc_025_level3.txt

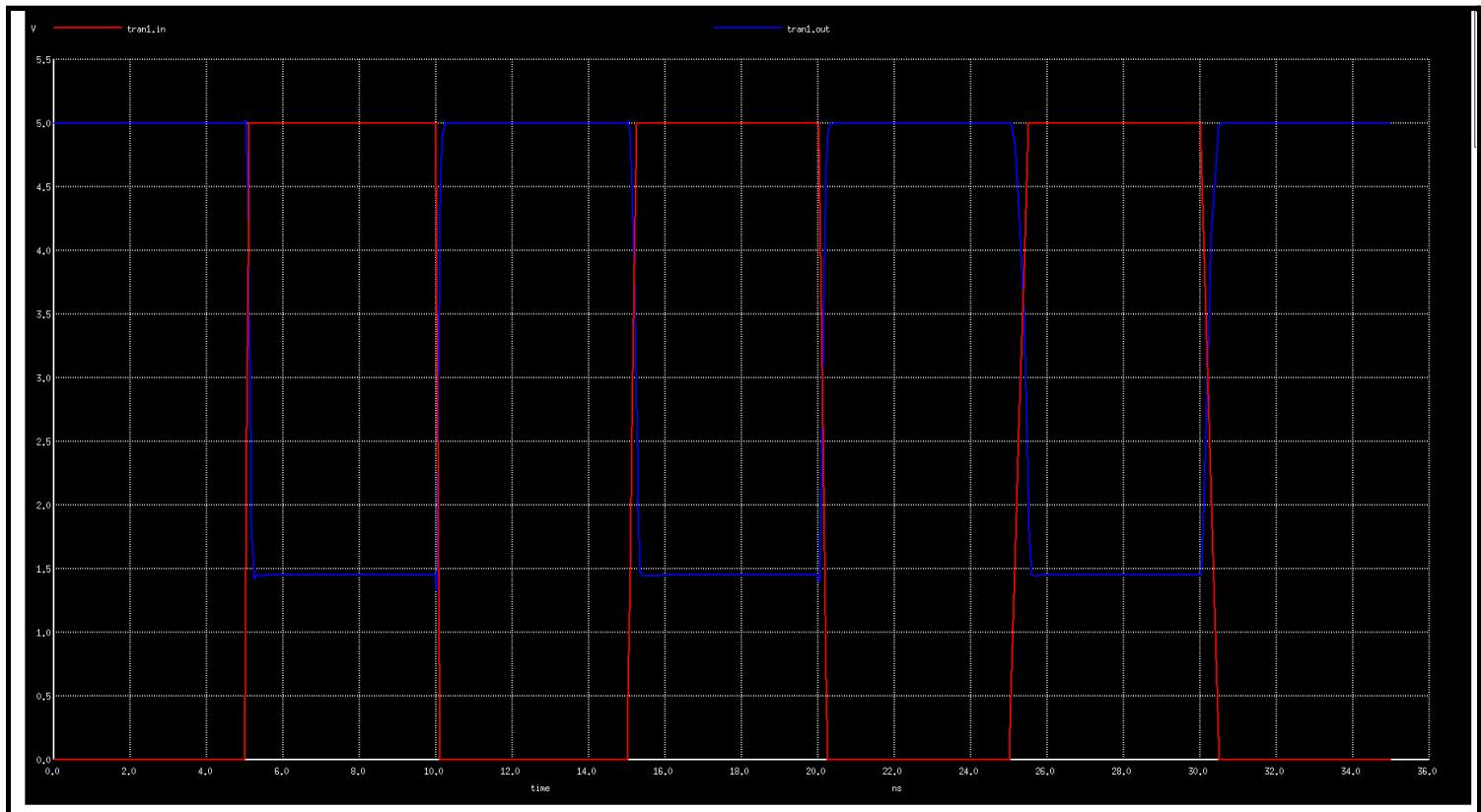
m0 out in 0 0 cmosn w=1u l=1u
m1 out 0 vdd vdd cmosp w=2.5u l=1u

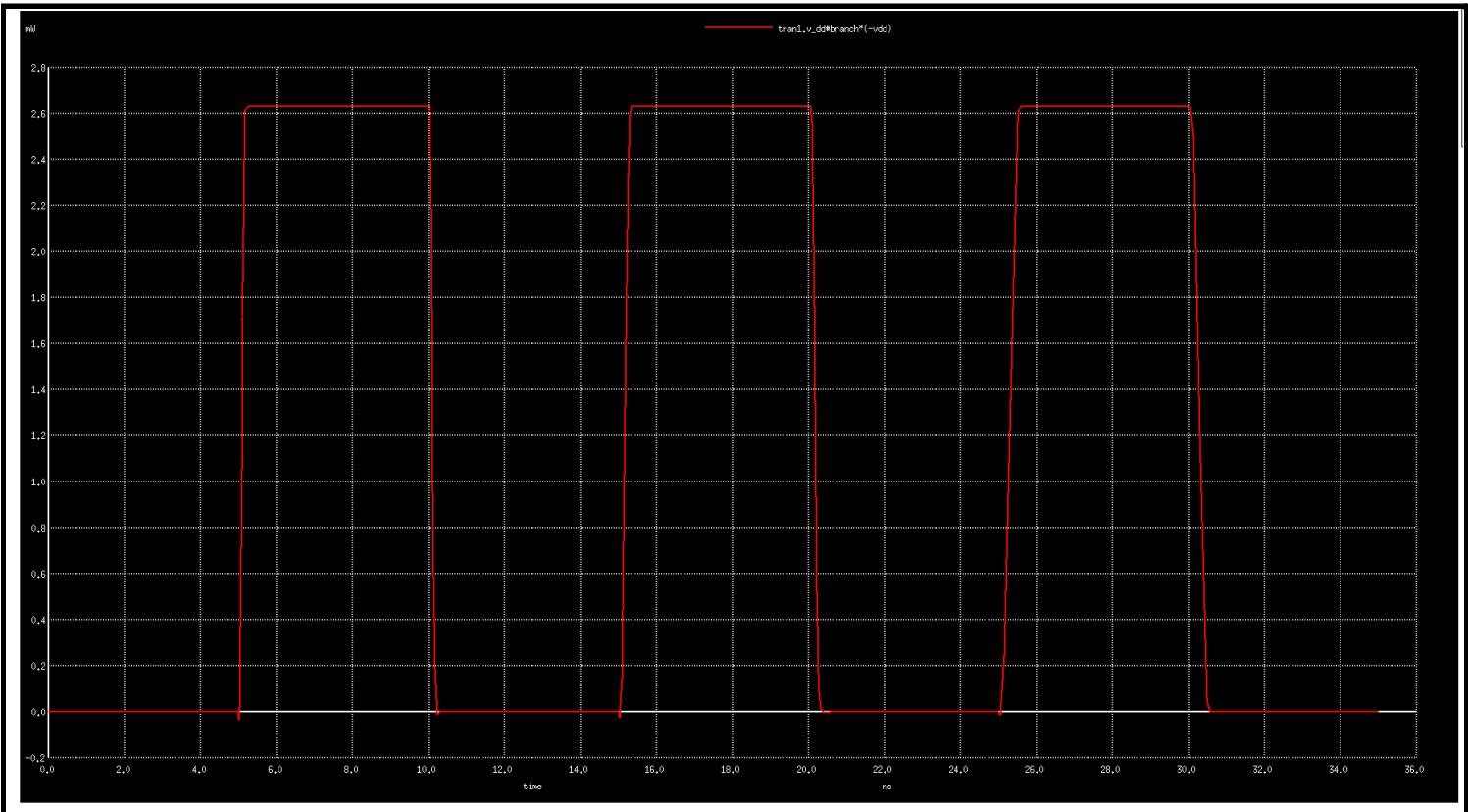
v_dd vdd 0 5
*v_in vin 0 5

v_in in 0 dc 5 pwl(0 0, 5n 0, 5.1n 5, 10n 5, 10.1n 0, 15n 0, 15.25n 5, 20n 5, 20.25n 0, 25n 0, 25.5n 5, 30n 5, 30.5n 0, 35 0)

.control
  tran 0.001 35n
.endc

.control
  plot tran1.in tran1.out
  plot tran1.v_dd#branch*(-vdd)
.endc
```





From the First graph we can see that as we increase the rise time and fall time the amount of power consumed increases and the time it take to reach a state increases and those increasing the energy consumed in the process

### Varying the capacitive load:-

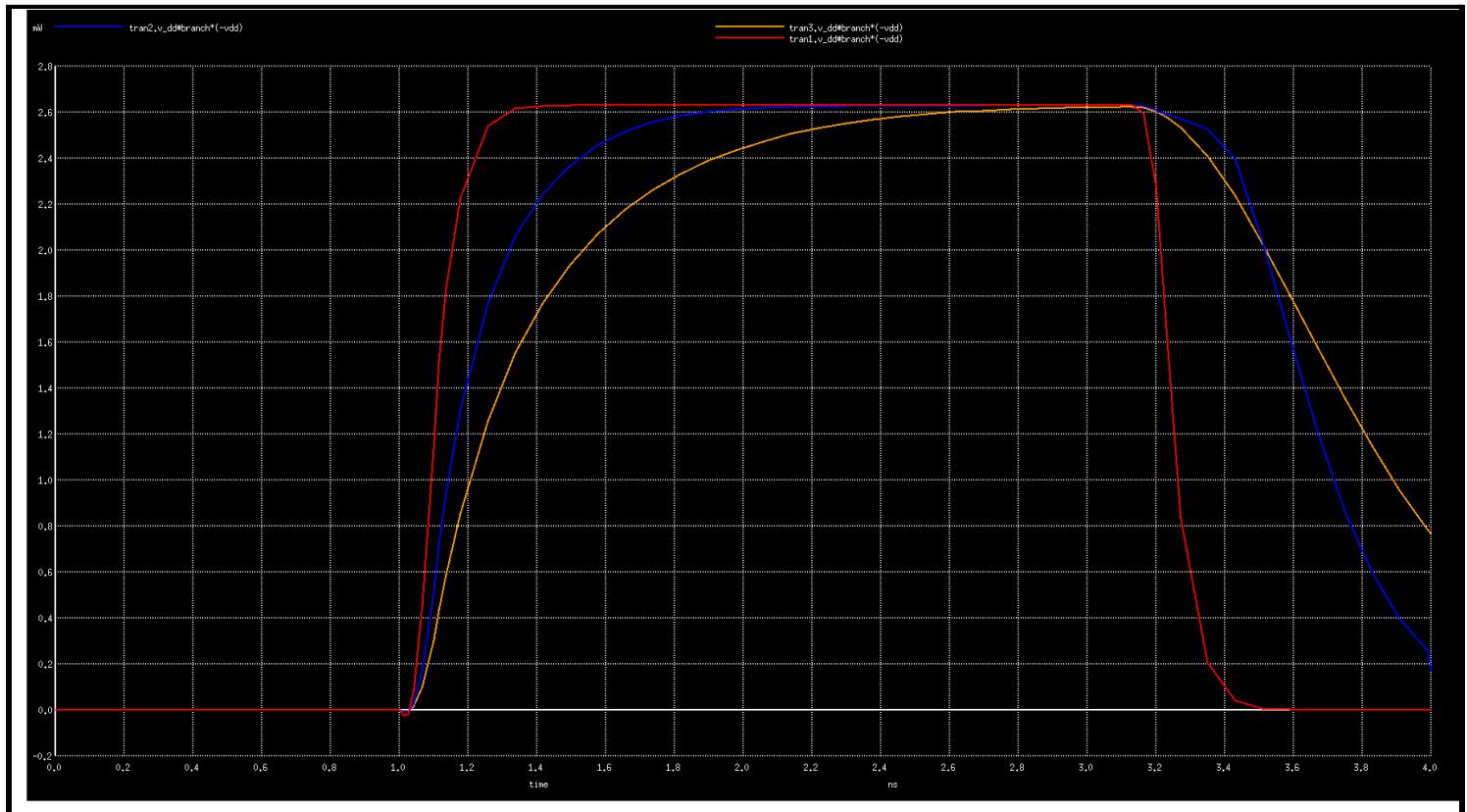
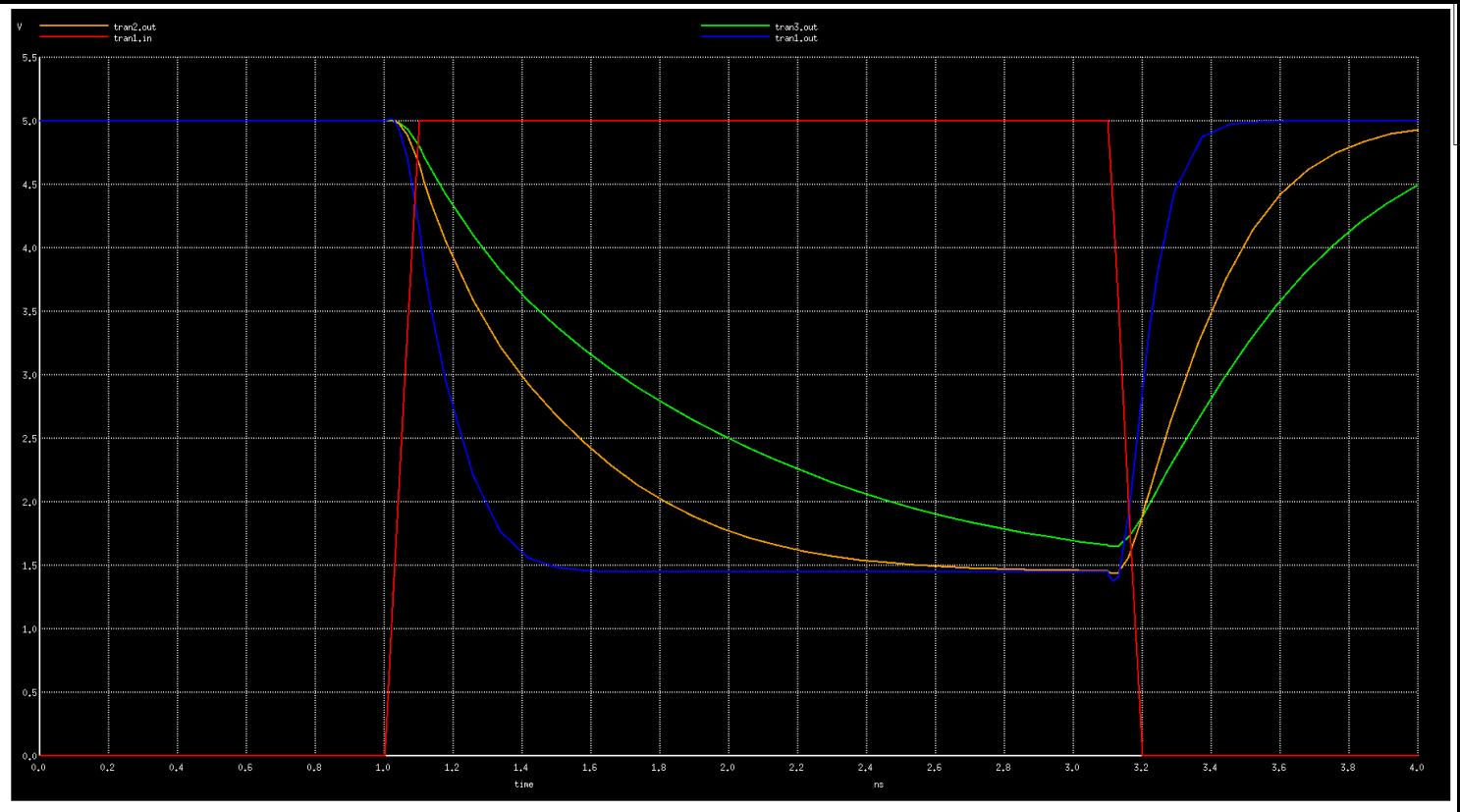
```
*3_c*
*Varying input rise time and fall time
.include ./t14y_tsmc_025_level3.txt

m0 out in 0 0 cmosn w=1u l=1u
m1 out 0 vdd vdd cmosp w=2.5u l=1u
c0 out 0 0.01p

v_dd vdd 0 5
v_in in 0 dc 2.5 pulse(0 5 1n 0.1n 0.1n 2n 4n)

.control
foreach cap 0.01p 0.05p 0.1p
alter c0 = $cap
tran 0.001 4n
end
.endc

.control
plot tran1.in tran1.out tran2.out tran3.out
plot tran1.v_dd#branch*(-vdd) tran2.v_dd#branch*(-vdd) tran3.v_dd#branch*(-vdd)
.endc
```



We can see from the graphs that as we increase the capacitance value the rise time and the fall time of the circuit increases and the power consumed, but the highest power consumed stays the same, also increases and as we take a longer time to reach that highest value the energy consumed is more

**Conclusion:-**

The experiment was performed, and all graphs were analysed. The obtained graphs movements agreed with theory, and hence simulations were verified. NGSPICE was the simulator used for this task.

## 4. Study of CMOS Inverter

### Objectives:-

- Study the
- Transfer function
- Noise margin
- Effect on rise time, falltime
- Propagation delay,

And the power and energy consumed of a CMOS inverter for various L, W of the pull up pull down network, and energy consumed in non ideal step input.

### Introduction:-

Inverter is one that inverts the signal supplied at its input. If input is made high or logic level is 1, then the output has logic level 0 and vice-versa. A CMOS inverter is characterised by a PMOs between the pull down transistor and the voltage source the input is fed to the Pull up network also. The output is taken at the junction of the Pmos and the pull down transistor. The pull-up circuit is constituted by the PMOS and pull-down resistor by the NMOS. When the input is low, the NMOS is open circuited and the output capacitance is charged to VDD through Pmos.

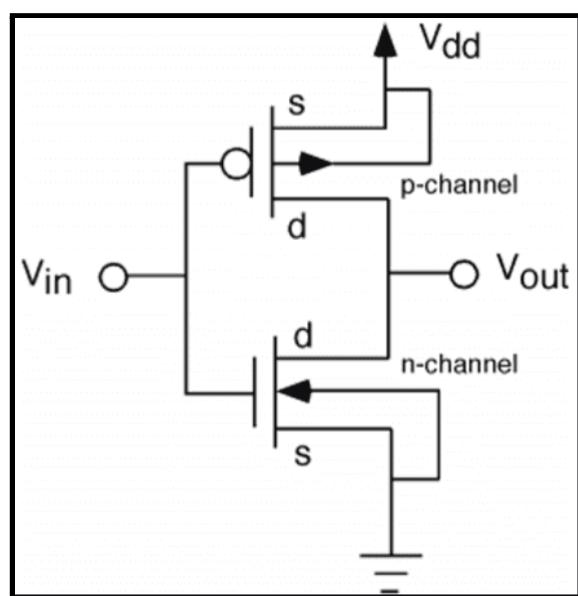


Fig: CMOS inverter

## Varying Width of NMOS:

```

.include ./t14y_tsmc_025_level3.txt

m1 out in 0 0 cmosn l=1u w=1u
m2 out in vdd vdd cmosp l=1u w=2u

c0 out 0 0.01p

v_dd vdd 0 dc 3.3
v_in in 0 dc 3.3 pulse(0 3.3 0 0.05n 0.05n 0.5n 1n)

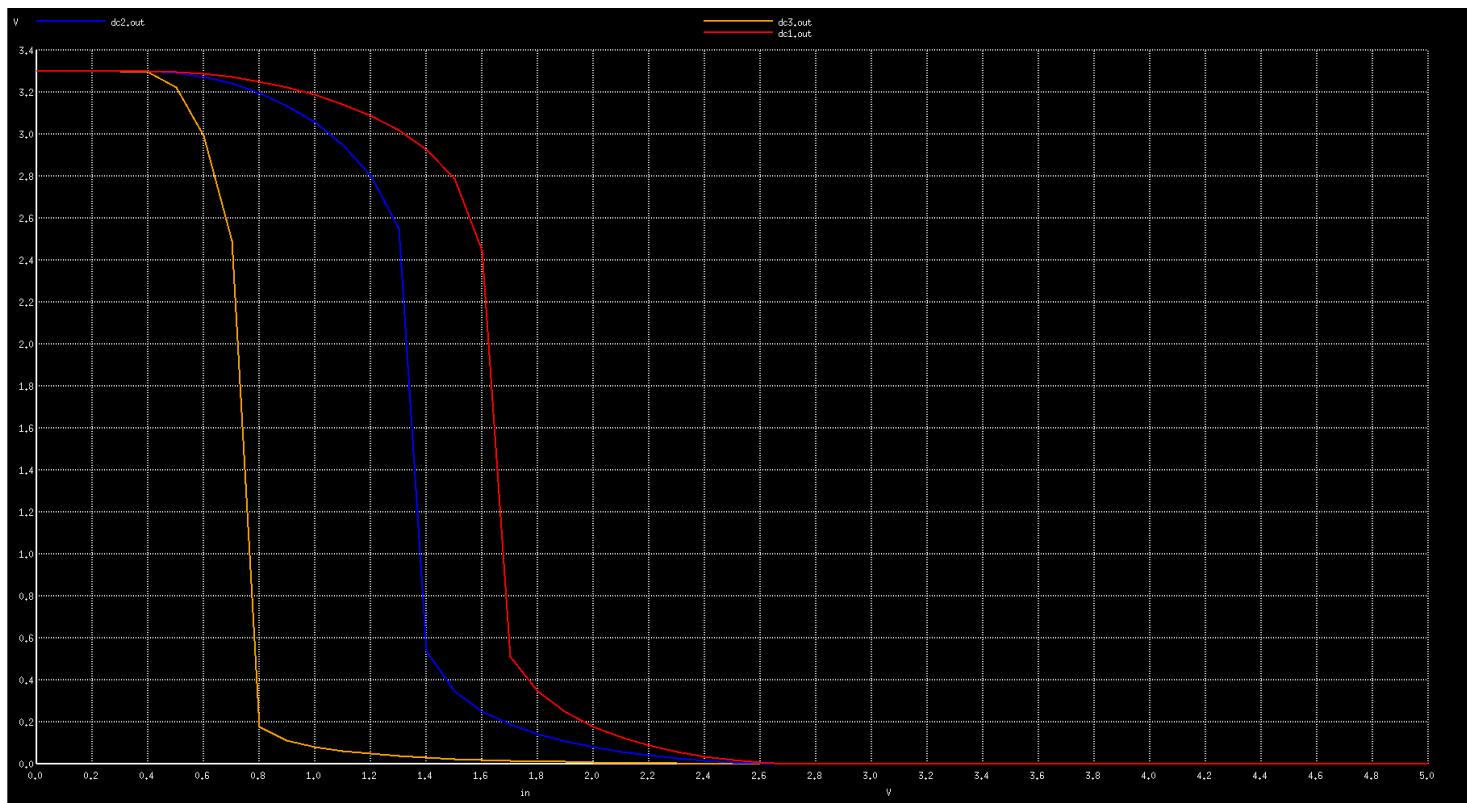
.tran 0.01n 2n
.dc v_in 0 3.3 0.1

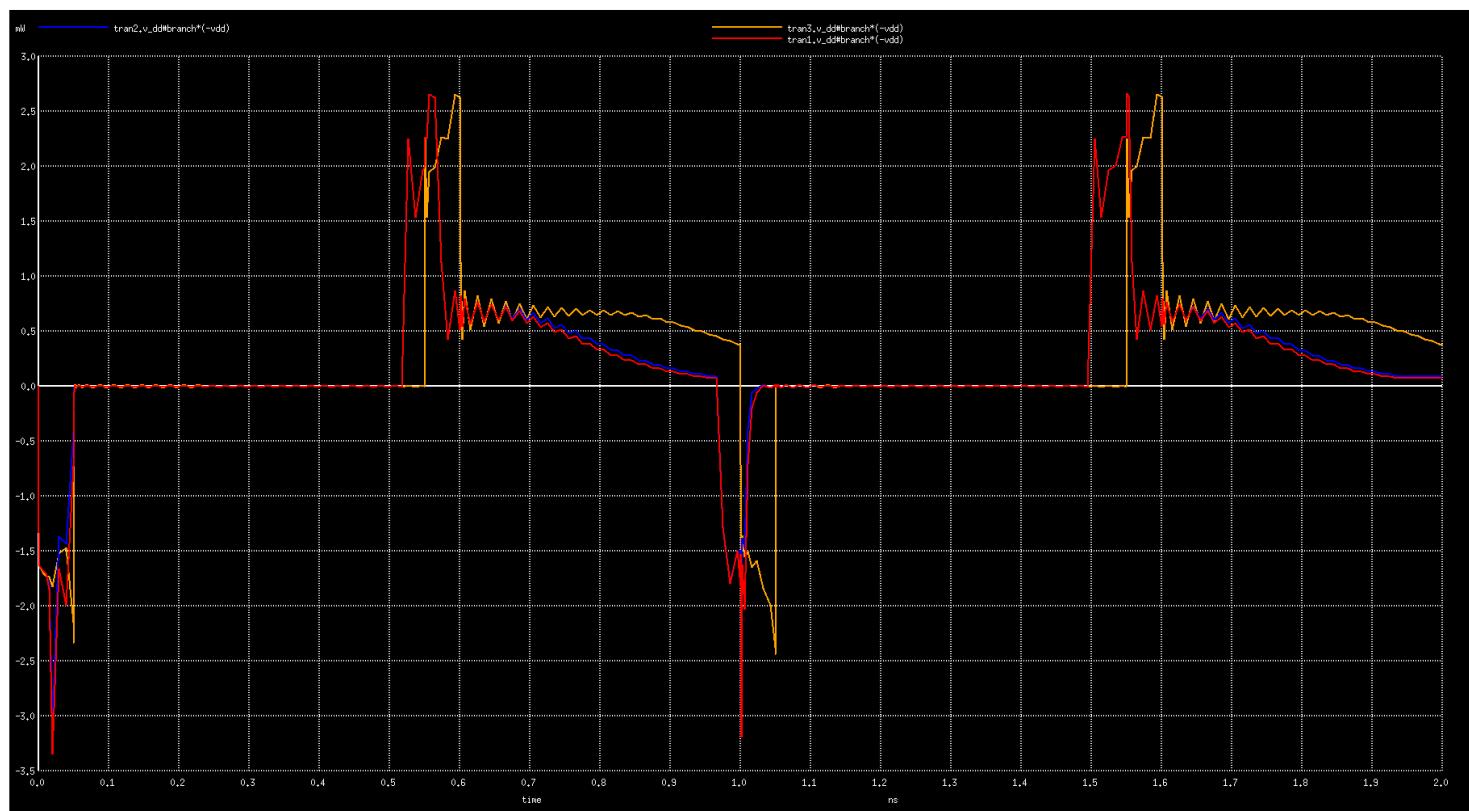
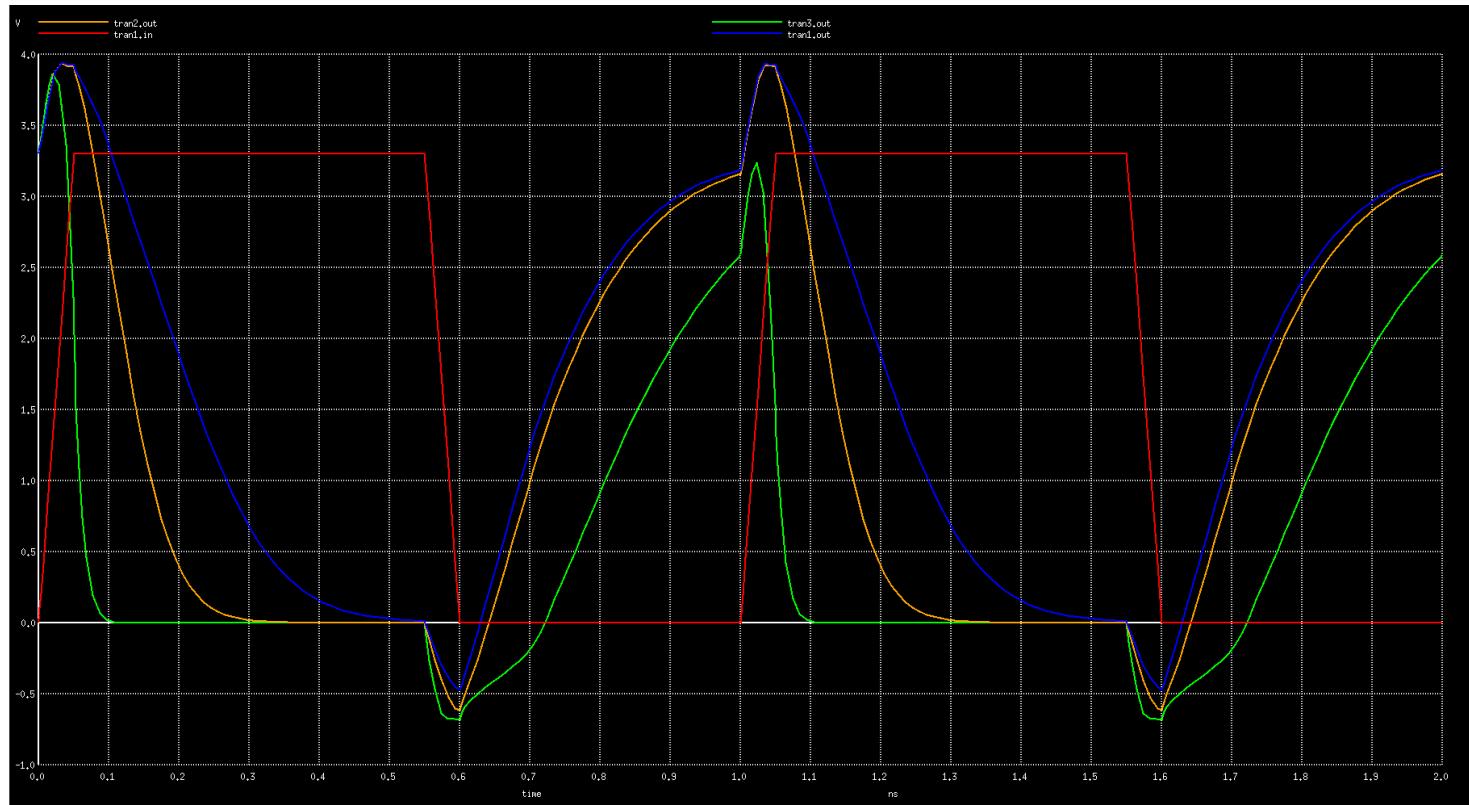
*Changing Width of bottom mosfet*

.control
foreach wid 0.5u 1u 10u
alter m1 w = $wid
dc v_in 0 5 0.1
tran 0.01n 2n
end
alter m1 w = 1u
.endc

.control
plot dc2.out dc3.out vs in
plot tran1.in tran1.out tran2.out tran3.out
plot tran1.v_dd#branch*(-vdd) tran2.v_dd#branch*(-vdd) tran3.v_dd#branch*(-vdd)
.endc

```



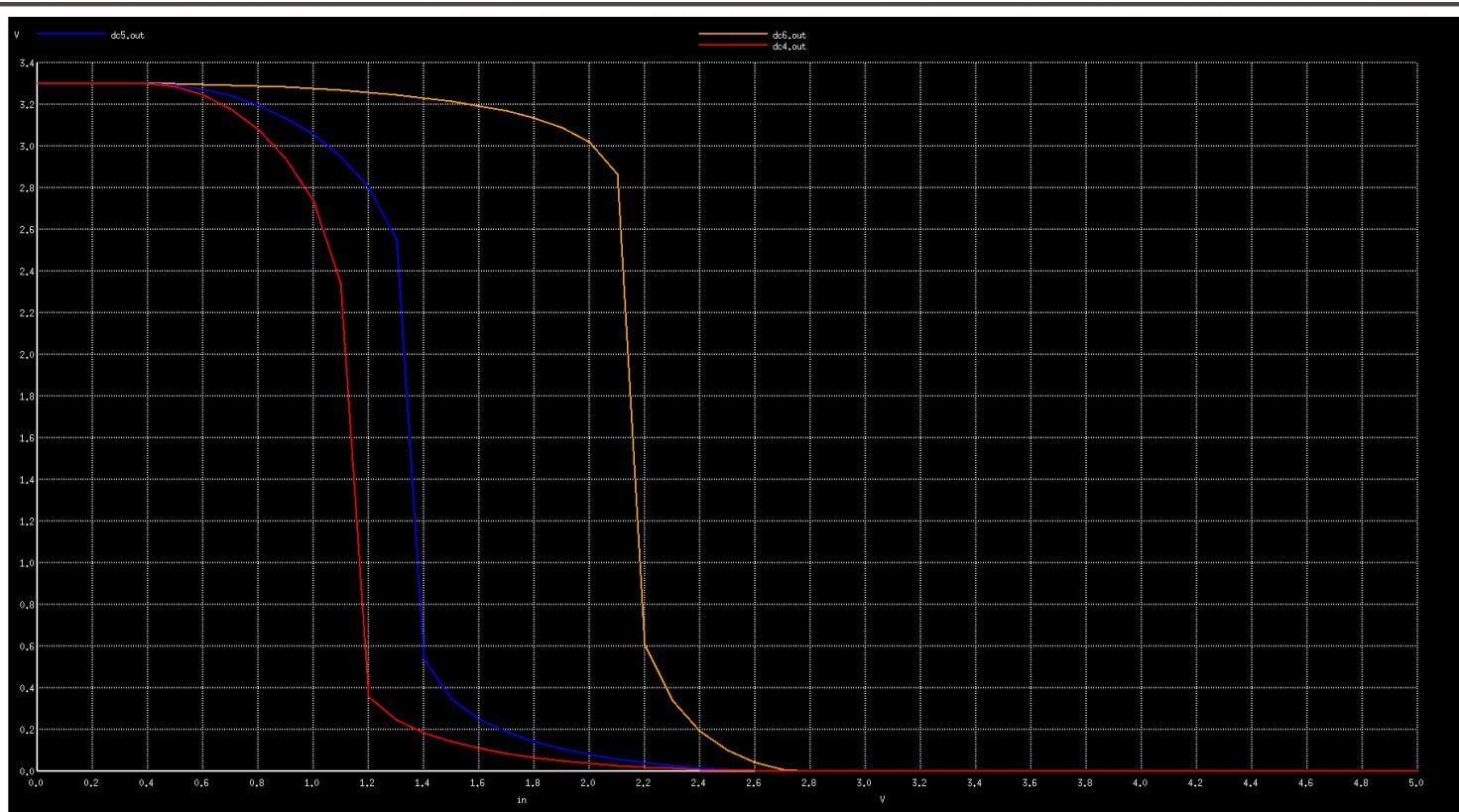


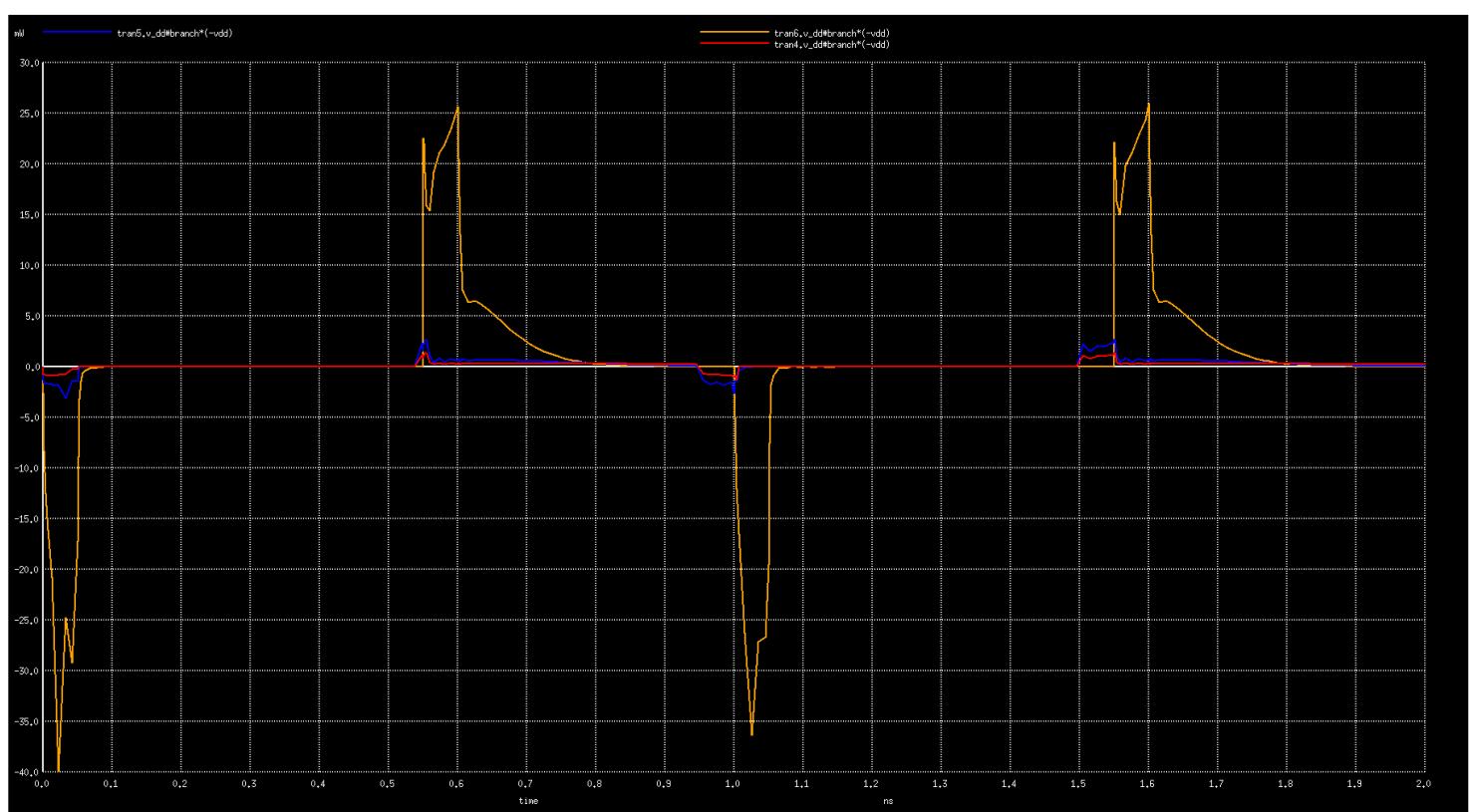
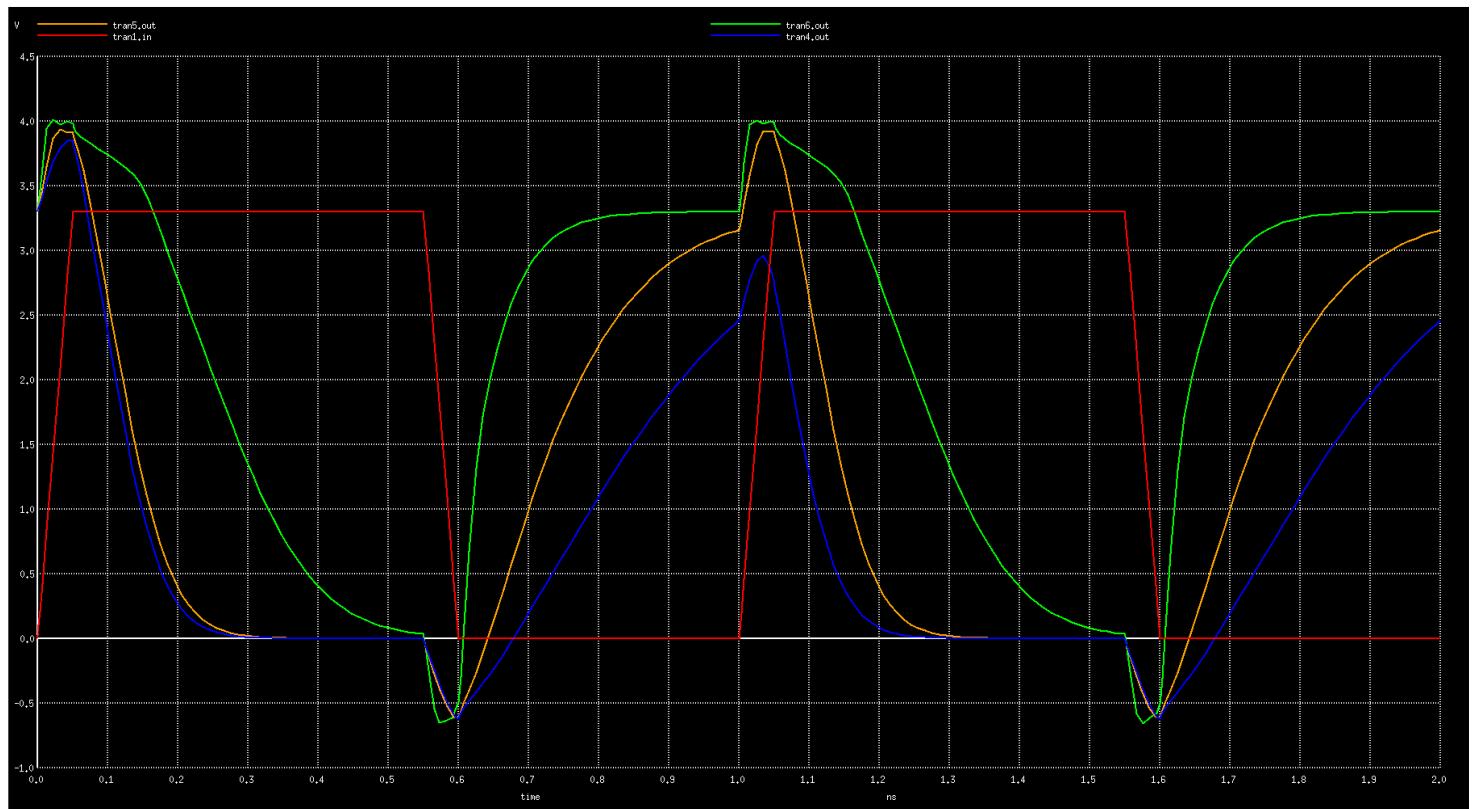
These are the results obtained when we vary the **width of the bottom Mosfet** the first graph is the dc output vs the dc input after doing dc analysis, the Noise Margin decreases as we increase the width, the rise time increases and one case does not even reach maximum, and fall time decreases, and the power consumed increases as the resistance decreases and the current increases the energy consumed also increase, and power is consumed in steady state due to sub threshold current.

## Varying Width of PMOS:

```
*Changing Width of top mosfet*
.control
foreach wid1 1u 2u 20u
alter m2 w = $wid1
dc v_in 0 5 0.1
tran 0.01n 2n
end
alter m2 w = 2u
.endc

.control
plot dc5.out dc6.out dc4.out vs in
plot tran1.in tran4.out tran5.out tran6.out
plot tran4.v_dd#branch*(-vdd) tran5.v_dd#branch*(-vdd) tran6.v_dd#branch*(-vdd)
.endc
```



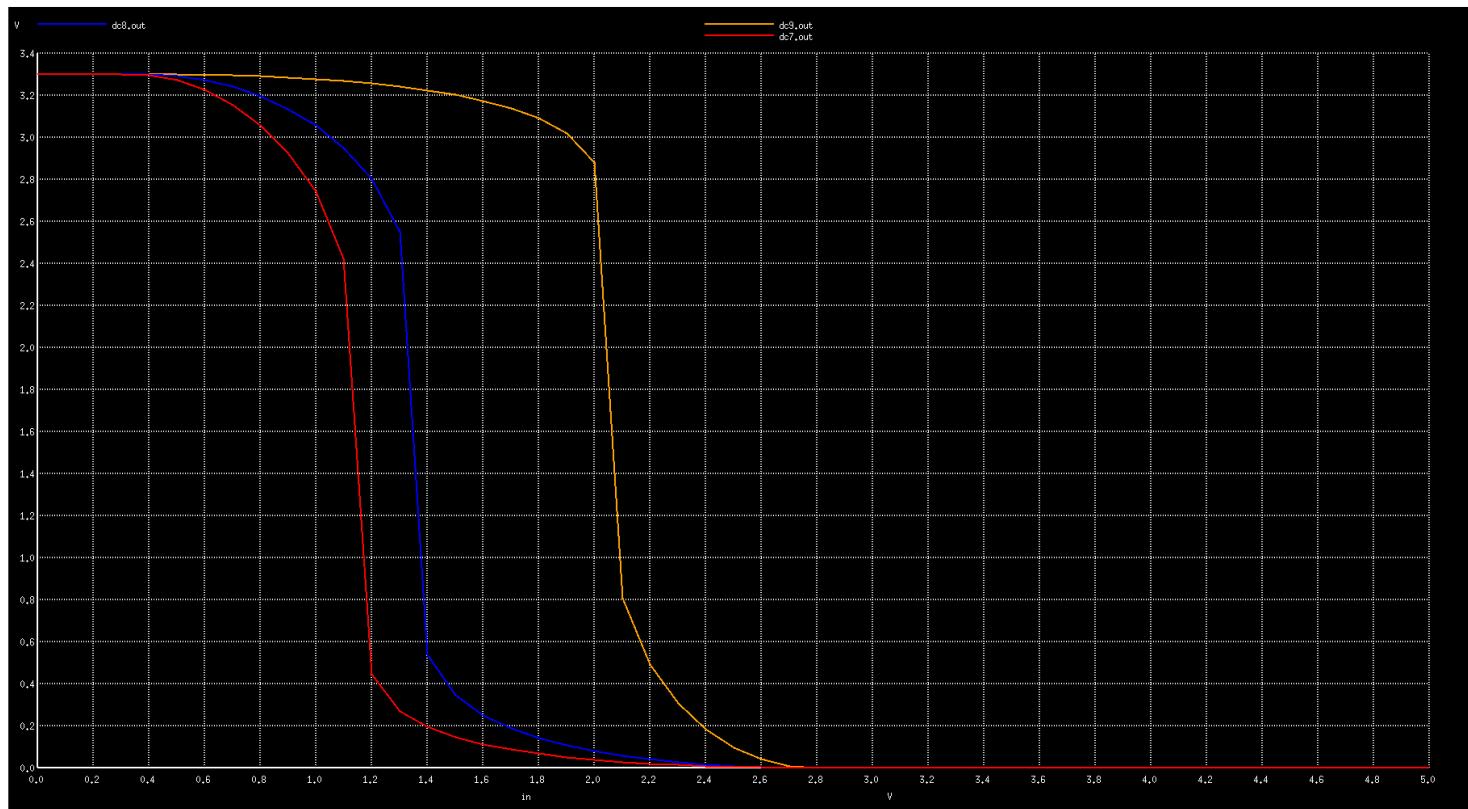


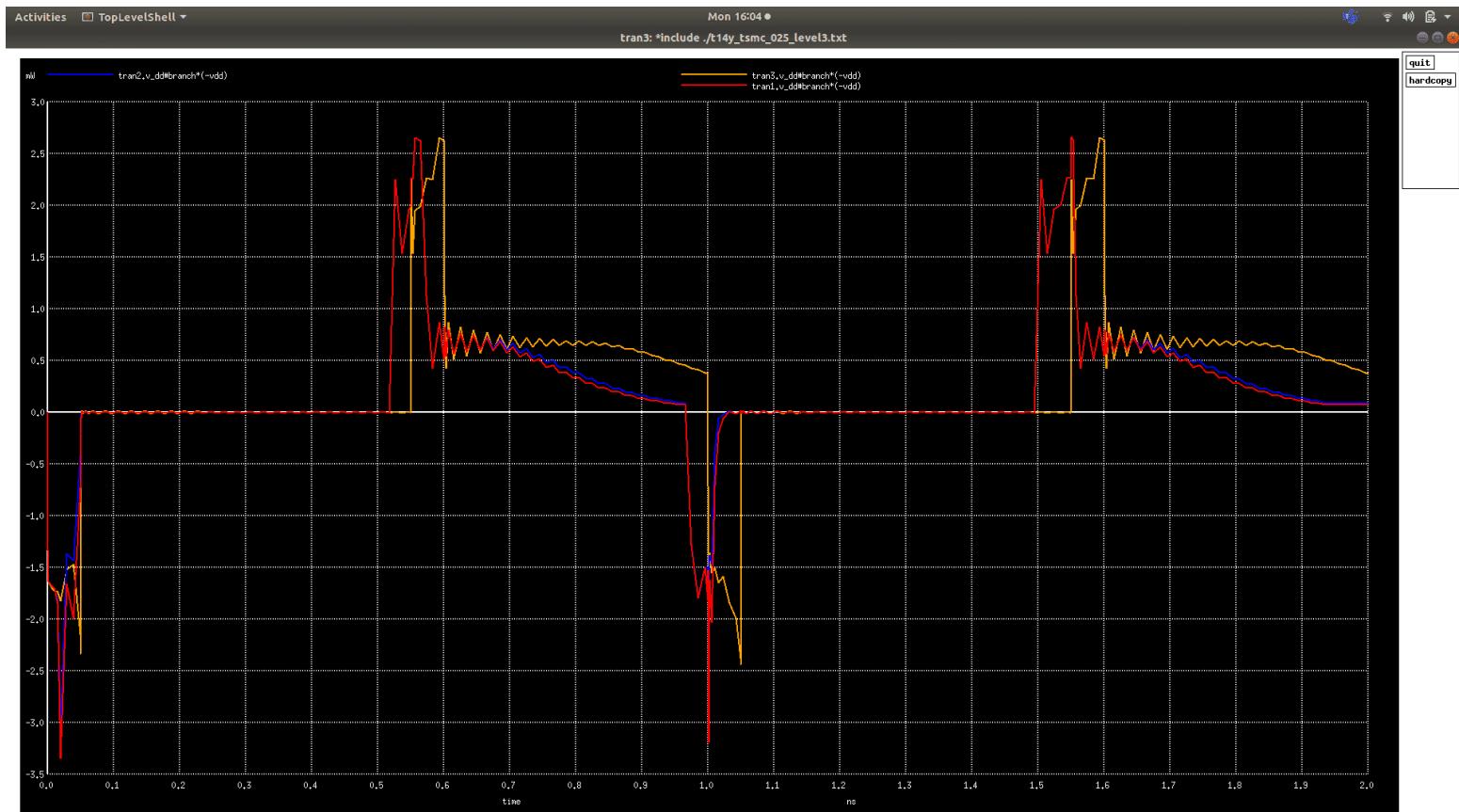
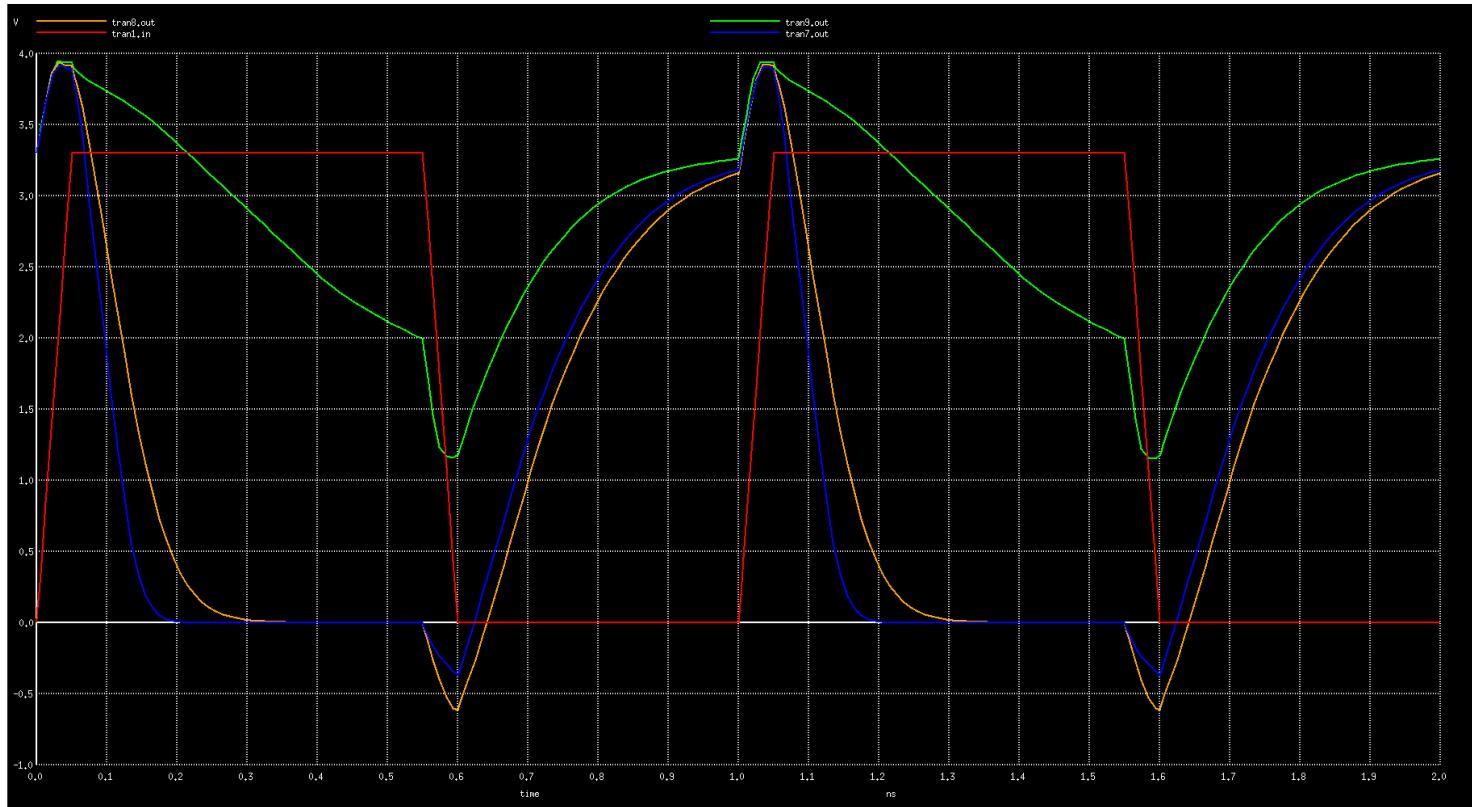
These are the results obtained when we vary the **width of the Top Mosfet** the first graph is the dc output vs the dc input after doing dc analysis, as we increase the width-the noise margin increases, Looking at second graph the rise time deceases, but fall time increases, Looking at the third graph the power consumed increases as the resistance decreases and the current increases the energy consumed also increase, and power is consumed in steady state due to sub threshold current.

### Varying the Length of NMOS:

```
*Changing len of bottom mosfet*
.control
foreach len 0.5u 1u 10u
alter m1 l = $len
dc v_in 0 5 0.1
tran 0.01n 2n
end
alter m1 l = 1u
.endc

.control
plot dc7.out dc8.out dc9.out vs in
plot tran1.in tran7.out tran8.out tran9.out
plot tran7.v_dd#branch*(-vdd) tran8.v_dd#branch*(-vdd) tran9.v_dd#branch*(-vdd)
.endc
```





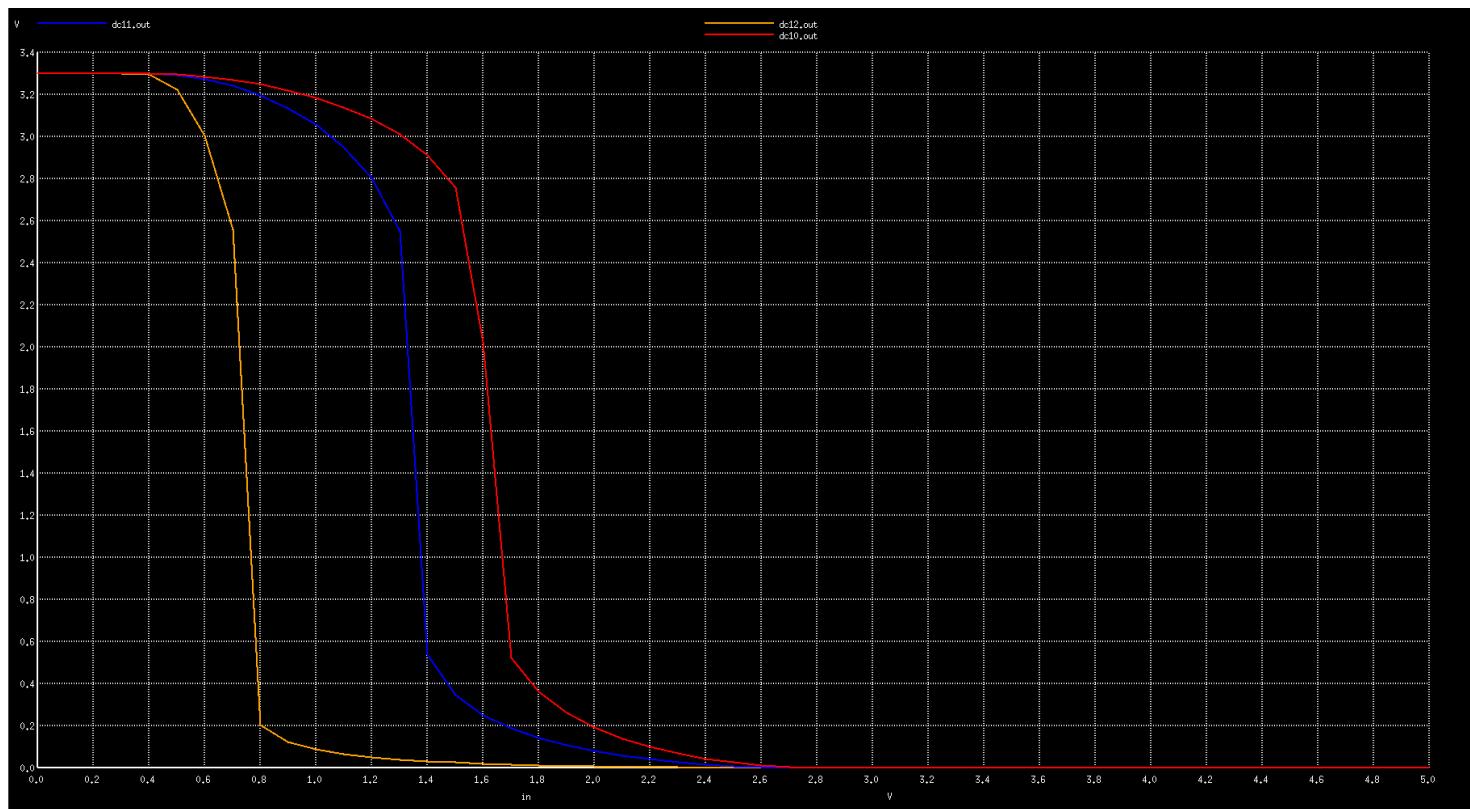
These are the results obtained when we vary the **length of the bottom Mosfet** the first graph is the dc output vs the dc input after doing dc analysis, as we increase the length-the noise margin increases, Looking at second graph the rise time increases, but fall time increases by a huge amount, Looking at the third graph the power consumed decrease, but the amount of energy consumed is more as the resistance increase and the current decrease, and power is consumed in steady state due to sub threshold current.

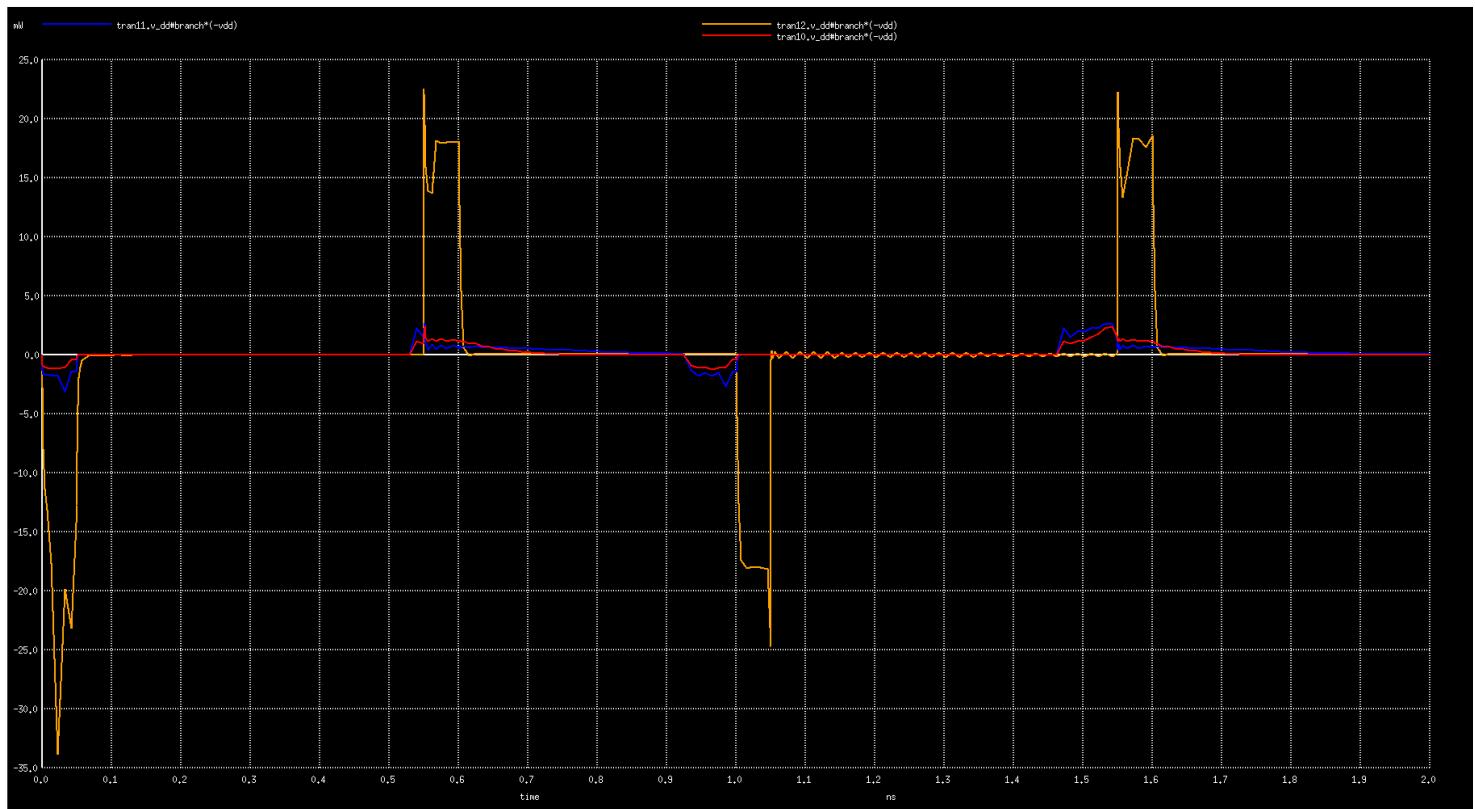
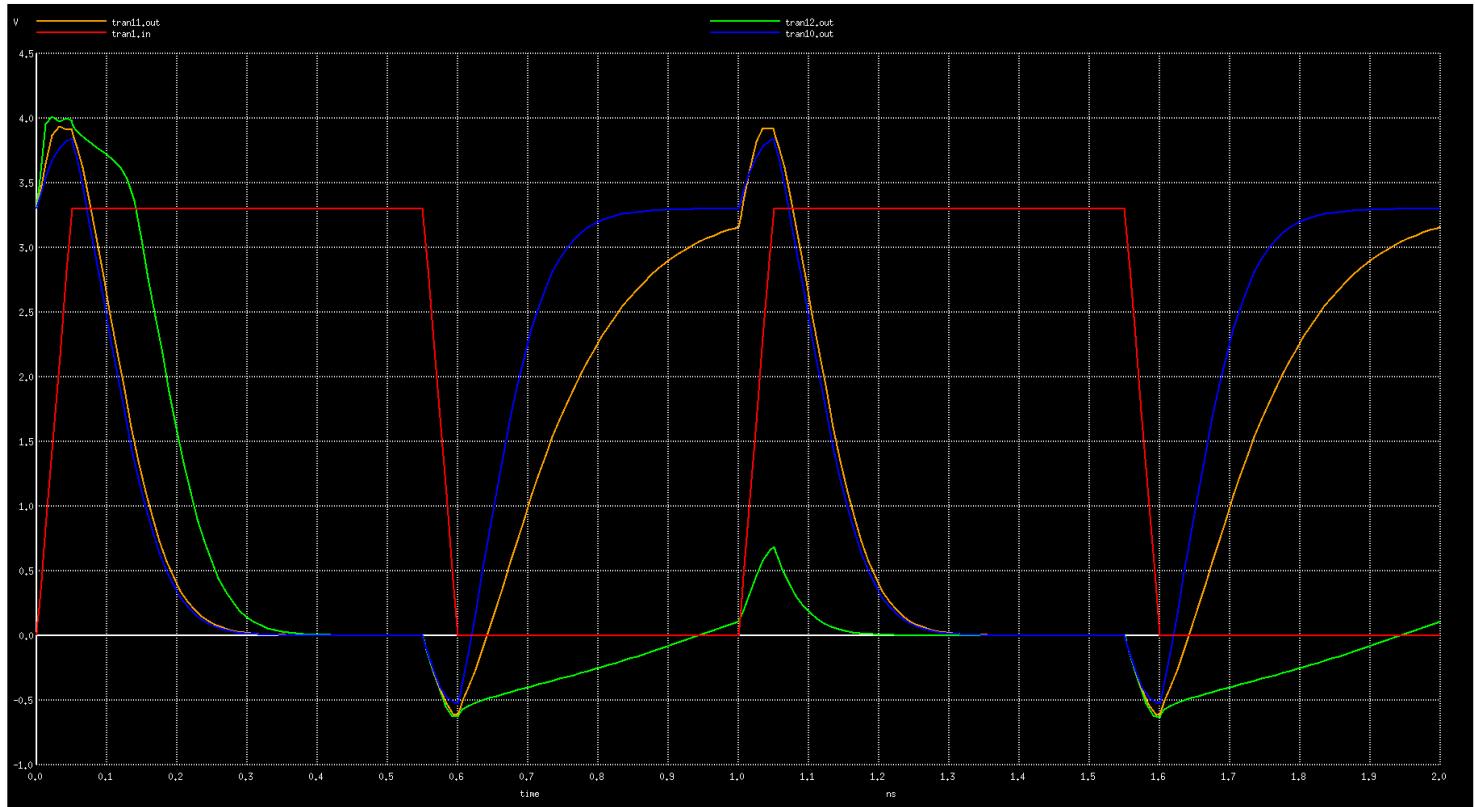
## Varying Length of PMOS:

\*Changing len of top mosfet\*

```
.control
foreach len1 0.5u 1u 10u
alter m2 l = $len1
dc v_in 0 5 0.1
tran 0.01n 2n
end
alter m2 l = 1u
.endc

.control
plot dc10.out dc11.out dc12.out vs in
plot tran1.in tran10.out tran11.out tran12.out
plot tran10.v_dd#branch*(-vdd) tran11.v_dd#branch*(-vdd) tran12.v_dd#branch*(-vdd)
.endc
```



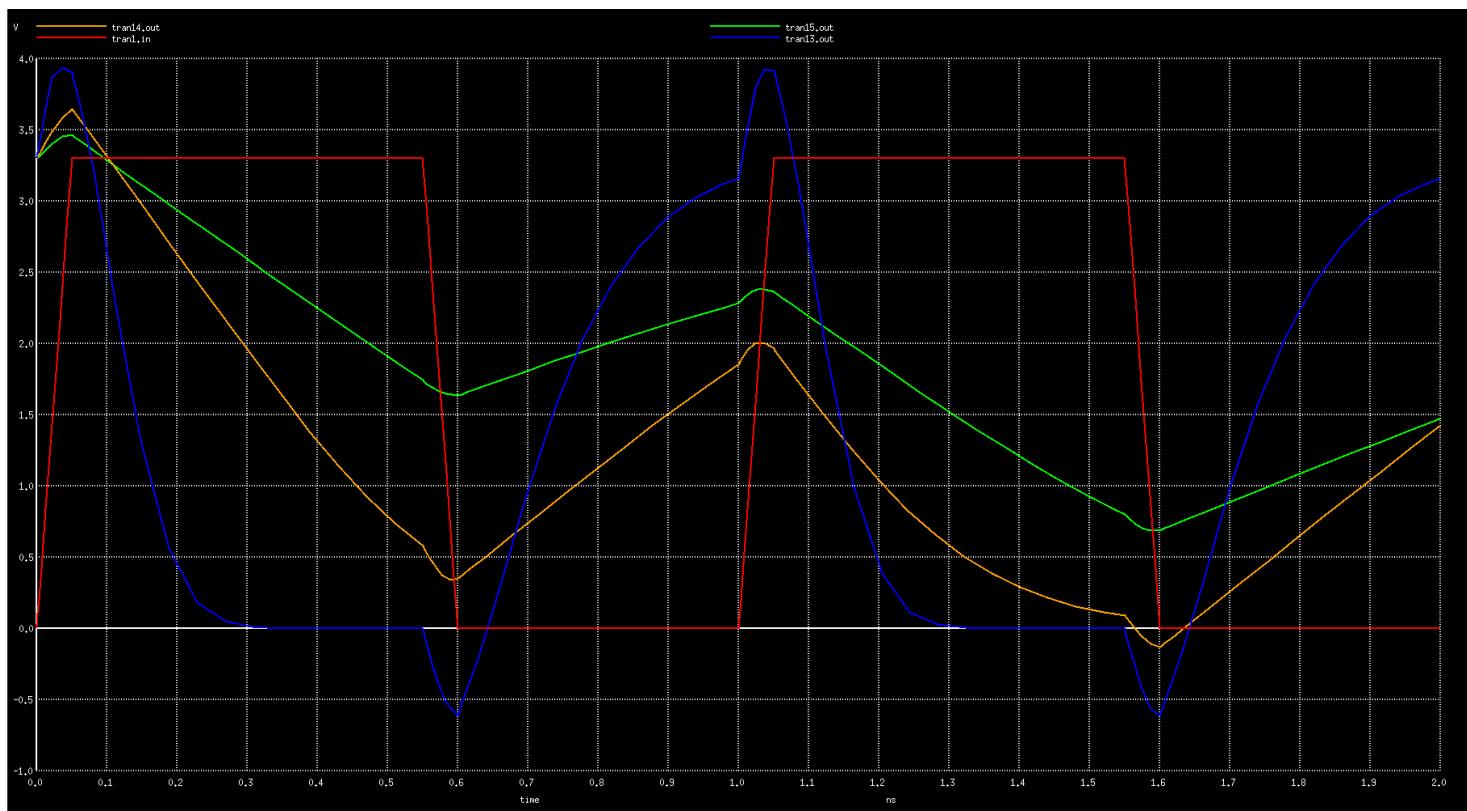


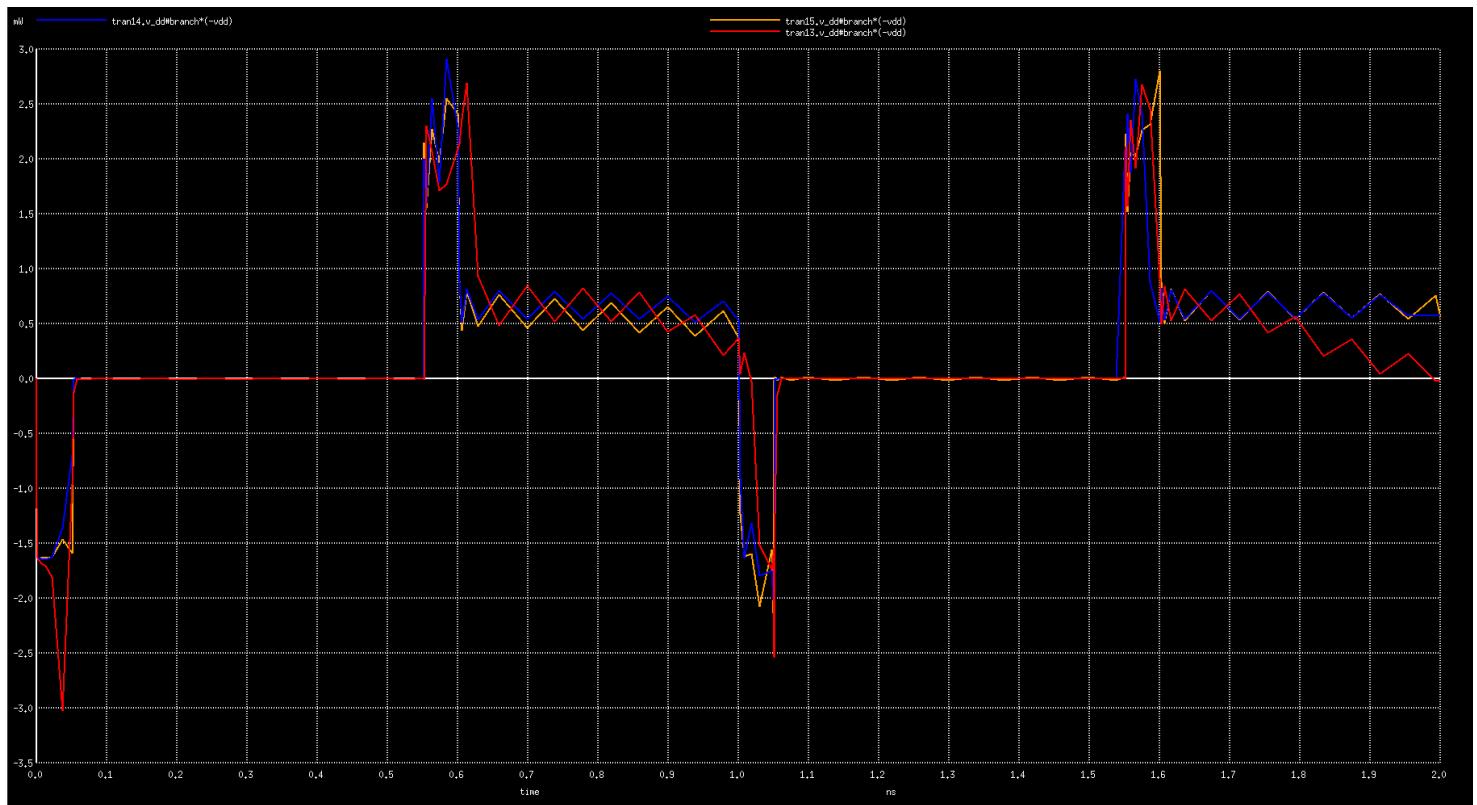
These are the results obtained when we vary the **length of the Top Mosfet** the first graph is the dc output vs the dc input after doing dc analysis for Noise Margin as we increase the length-the noise margin decreases and those not in the range do not act as an gate, Looking at second graph the rise time deceases, but fall time increases, Looking at the third graph the power consumed increases as the resistance decreases and the current increases the energy consumed also increase, and power is consumed in steady state due to sub threshold current.

### Varying Load capacitor:-

\*Changing load capacitance\*

```
.control
foreach cap 0.01p 0.05p 0.1p
alter c0 = $cap
dc v_in 0 5 0.1
tran 0.001 2n
end
.endc
.control
plot dc13.out dc14.out dc15.out vs in
plot tran1.in tran13.out tran14.out tran15.out
plot tran13.v_dd#branch*(-vdd) tran14.v_dd#branch*(-vdd) tran15.v_dd#branch*(-vdd)
.endc
.end
```





These are the results obtained when we vary the **load capacitance**, as the capacitance increase, Looking at first graph the rise time increase, also fall time increases, Looking at the second graph the power consumed increases and the energy consumed also increase, and power is consumed in steady state due to sub threshold current.

### Varying the rise time fall time:-

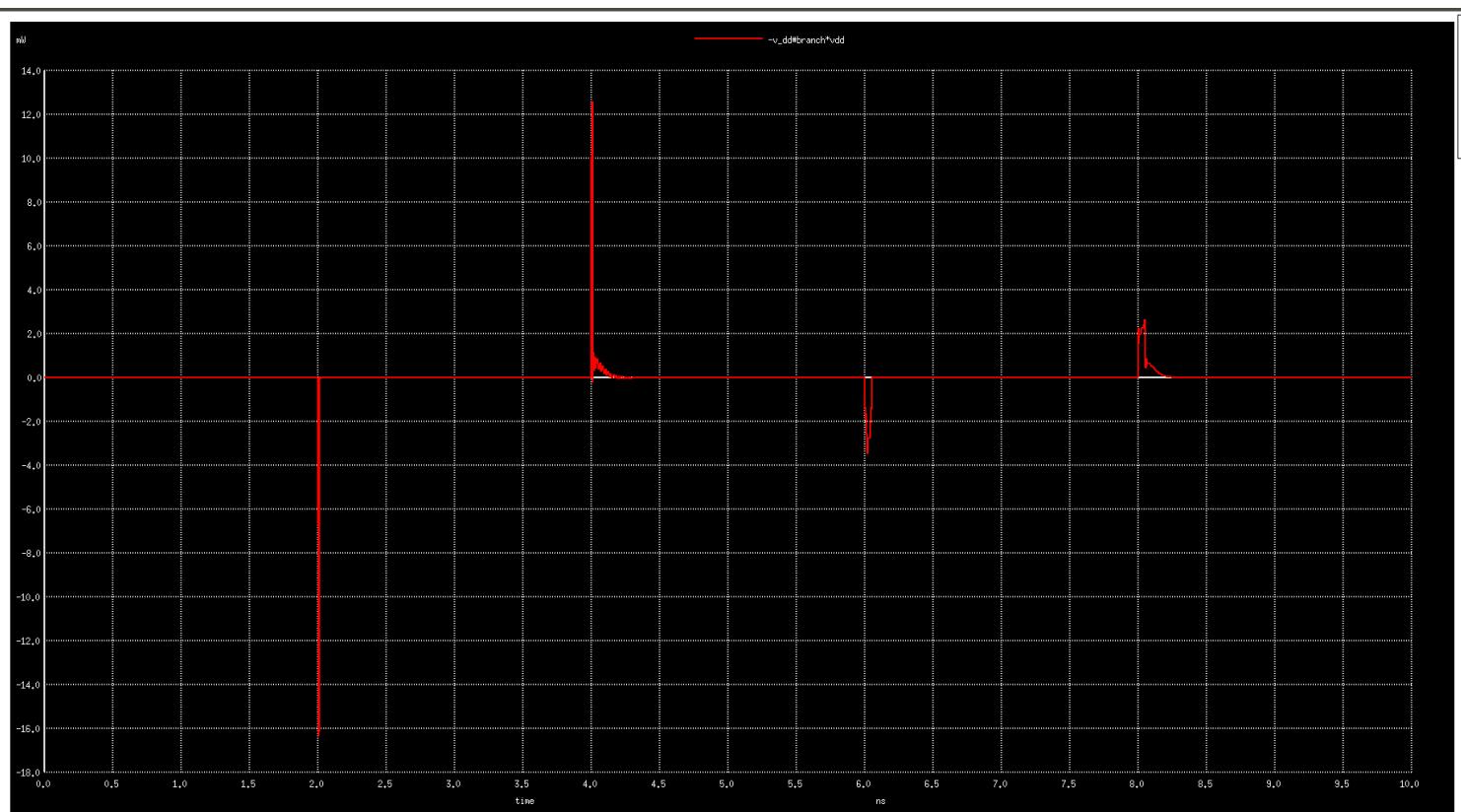
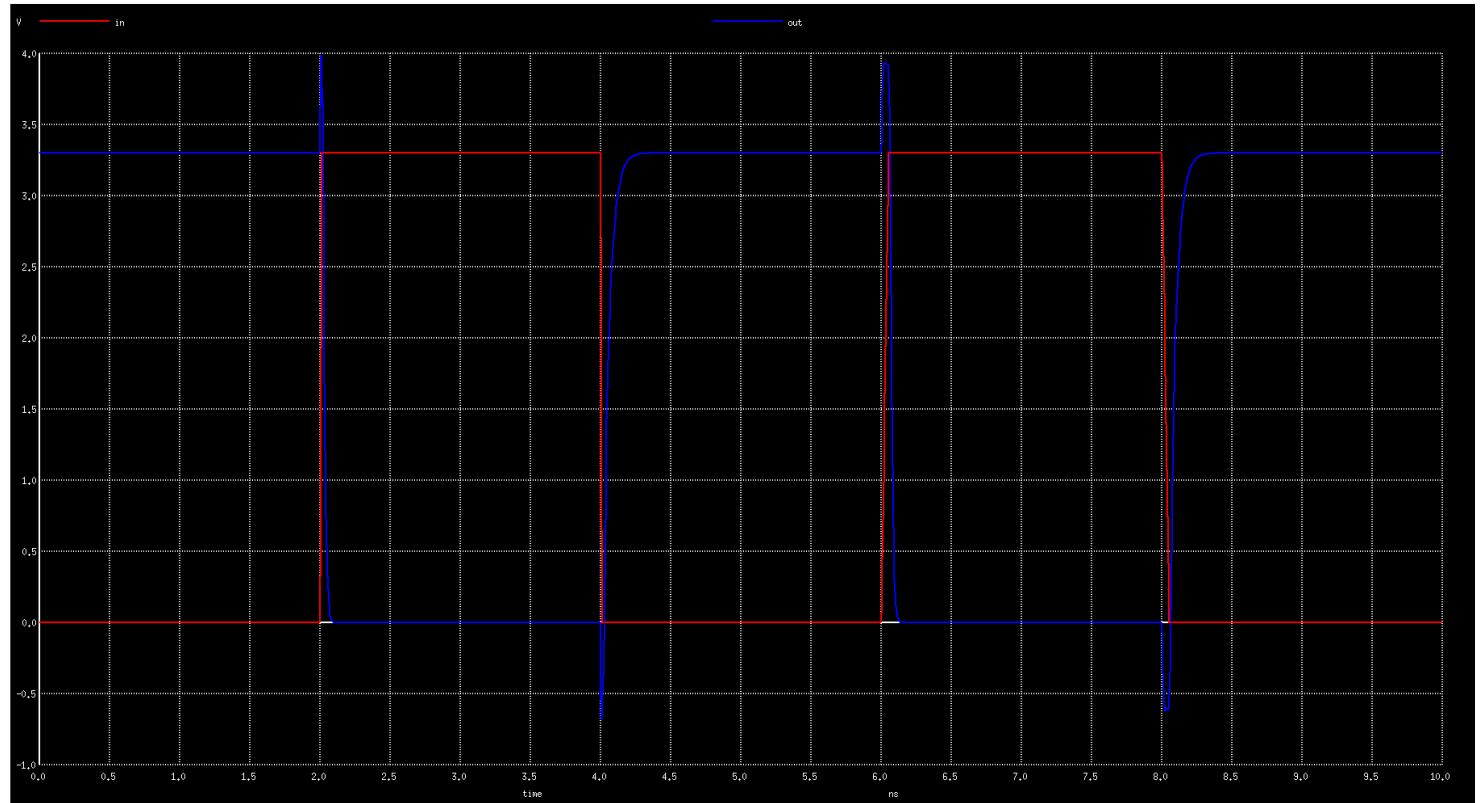
\*variable input rise time and fall time\*

```
.include ./t14y_tsmc_025_level3.txt

m1 out in 0 0 cmosn l=1u w=1u
m2 out in vdd vdd cmosp l=1u w=2u

v_dd vdd 0 3.3
v_in in 0 3.3 pwl(0 0 2n 0 2.01n 3.3 4n 3.3 4.01n 0 6n 0 6.05n 3.3 8n 3.3 8.05n 0 10n 0 10.1n 3.3 12n 3.3 12.1n 0)

.control
tran 0.01n 10n
run
setplot tran1
plot in out
plot -v_dd#branch*vdd
.endc
.end
```



These are the results obtained when we vary the **rise time and fall time**, as the rise time fall time increases we can see that the power consumed at a particular point increases but the overall energy consumed increases. This can be seen with the second graph.

**1) For increasing width of NMOS:**

W	0.5u	1u	10u
VIL	2.338v	1.722v	5.301v
VIH	3.111v	2.555v	1.198v
VOL	4.713v	5.150v	2.588v
VOH	4.379v	4.438v	4.922v
NML	1.867v	1.207v	2.712v
NMH	1.267v	1.883v	3.723v

**2) For increasing width of PMOS:**

W	1u	2u	20u
VIL	6.833v	1.003v	2.833v
VIH	1.498v	1.892v	3.269v
VOL	3.539v	4.543v	8.585v
VOH	4.850v	4.694v	4.430v
NML	3.294v	5.492v	1.975v
NMH	3.351v	2.802v	1.161v

### Conclusion:-

The experiment was performed, and all graphs were analysed. The obtained graphs movements agreed with theory, and hence simulations were verified. NGSPICE was the simulator used for this task.

# 5. Study Of Logic Gates

## Objectives:-

Study the

- Transfer function

- Noise margin

- Effect on rise time, falltime

- Propagation delay,

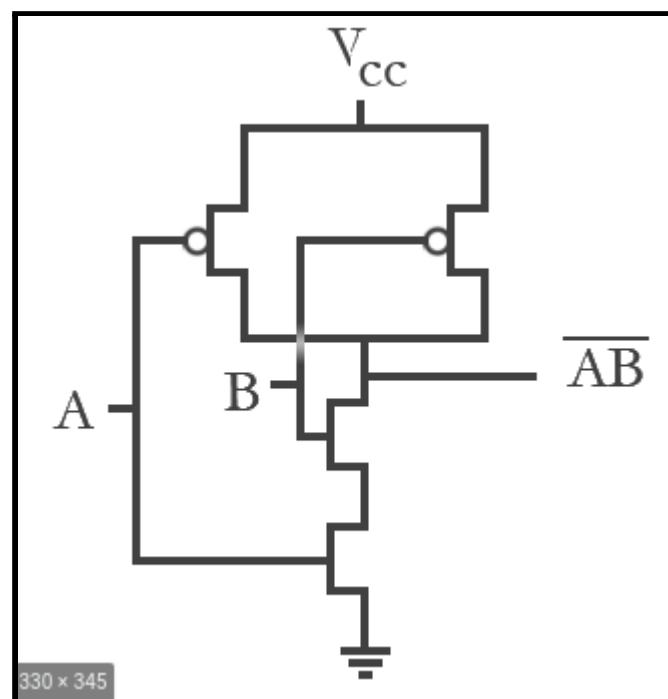
With the variations of the W and L of the Pullup and Pulldown network, for various gates like Nand, Nor, And, Or, and Xor.

## Introduction:-

Logic gates are the basic building blocks of any digital system. It is an electronic circuit having one or more than one input and only one output. The relationship between the input and the output is based on a certain logic. Based on this, logic gates are named as AND gate, OR gate, NOT gate etc.

## Nand:-

### Circuit:-



**Fig:-Nand Gate**

## Varying the Width of the NMOS:-

```
*Nand*
.include ./t14y_tsmc_025_level3.txt

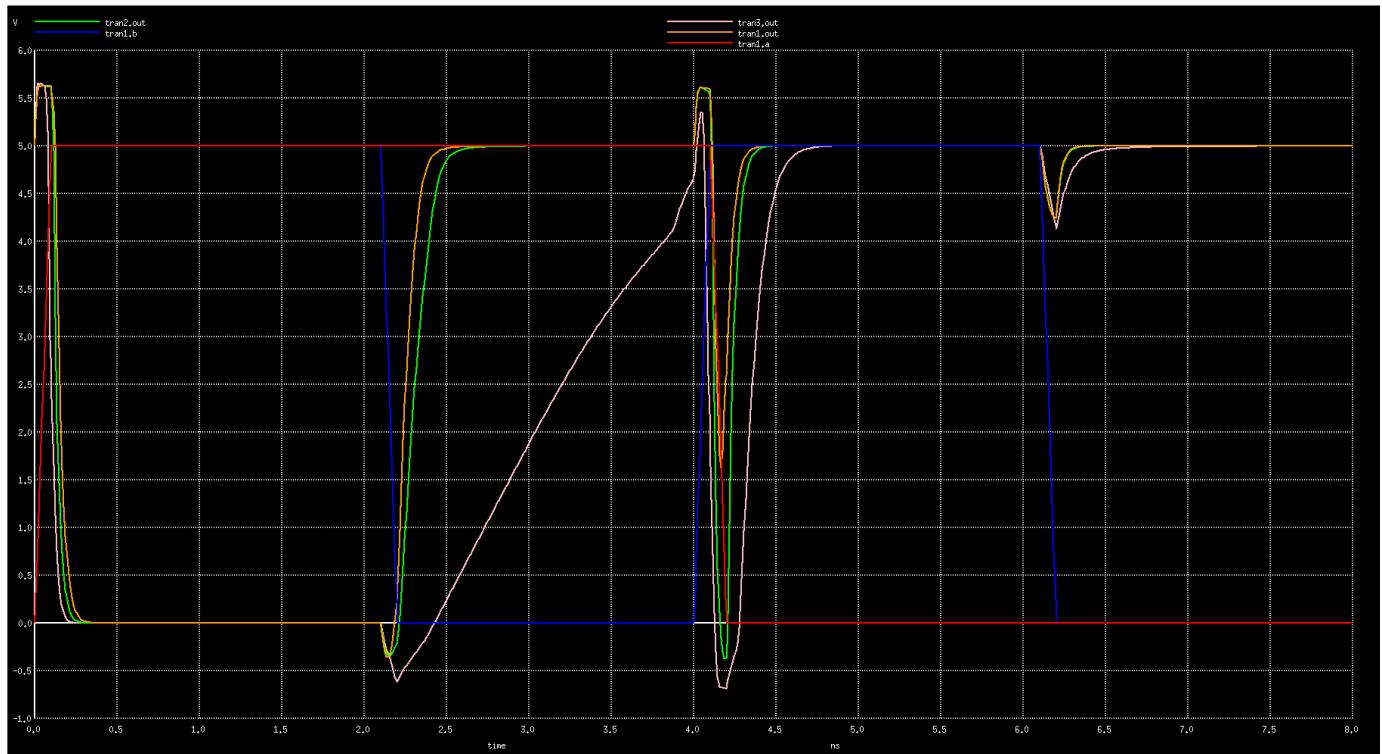
*Pull down network
m0 out a x 0 cmosn w=2u l=1u
m1 x b 0 0 cmosn w=2u l=1u

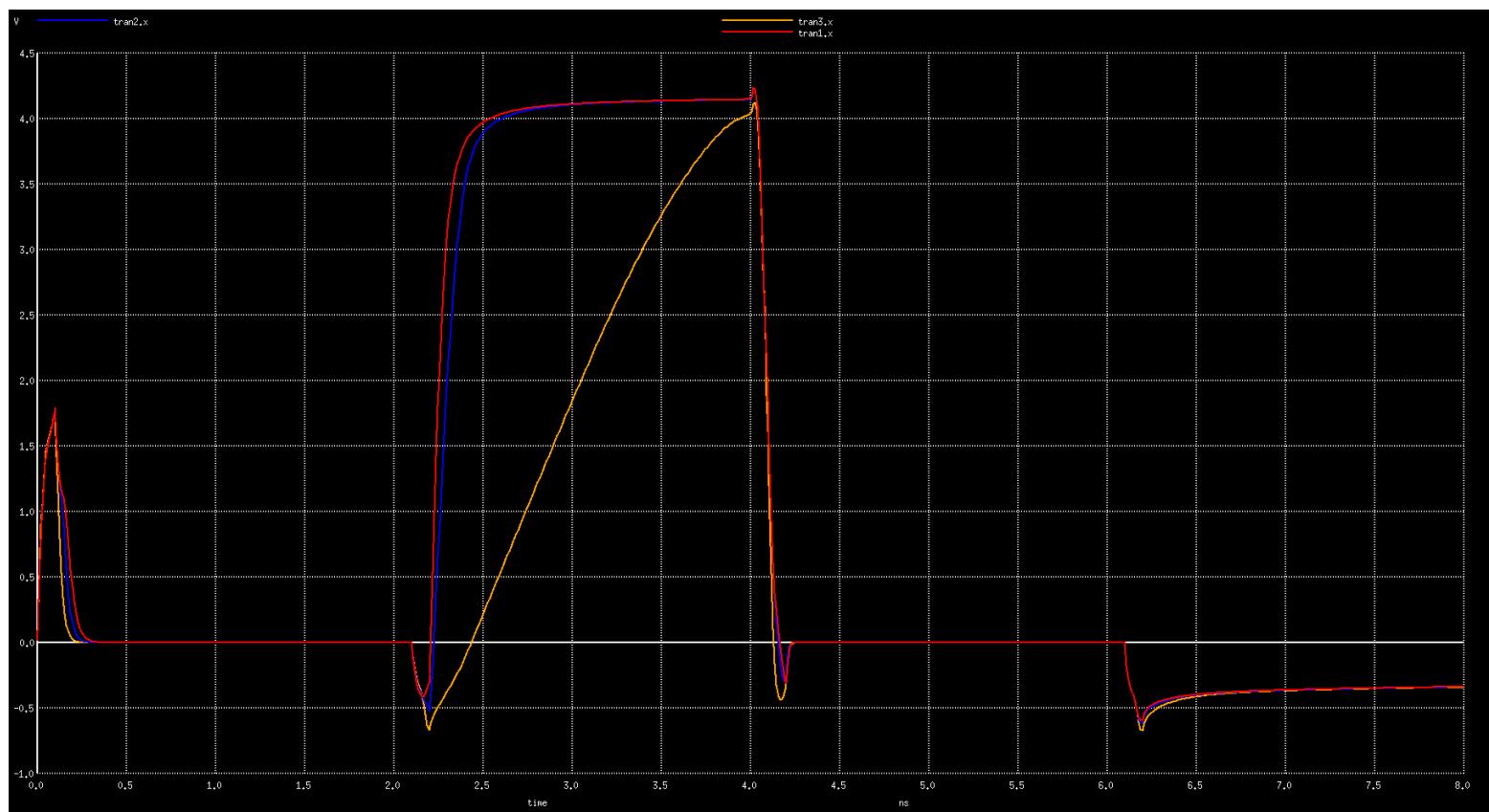
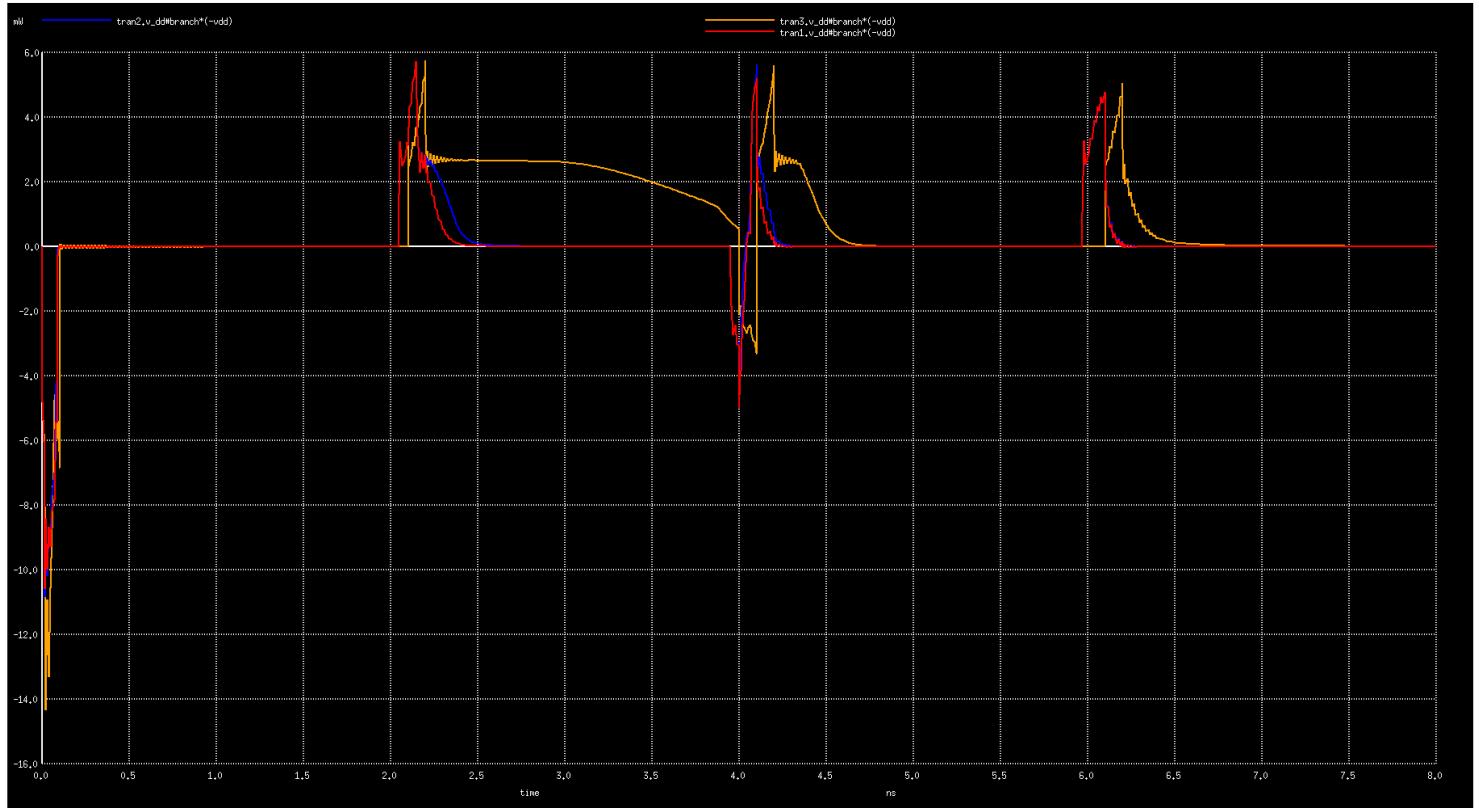
*Pull up network
m2 vdd a out vdd cmosp w=2.5u l=1u
m3 vdd b out vdd cmosp w=2.5u l=1u

v_dd vdd 0 5
v_a a 0 5 pulse(0 5 0 0.1n 0.1n 4n 8n)
v_b b 0 5 pulse(0 5 0 0.1n 0.1n 2n 4n)

*Transfer function and transient response on varying WIDTH of both the NMOS
.control
foreach wid 1u 2u 20u
alter m0 w=$wid
alter m1 w=$wid
tran 0.01n 8ns
end
alter m0 w=2u
alter m1 w=2u
.endc

.control
plot tran1.a tran1.b tran1.out tran2.out tran3.out
plot tran1.v_dd#branch*(-vdd) tran2.v_dd#branch*(-vdd) tran3.v_dd#branch*(-vdd)
plot tran1.x tran2.x tran3.x
.endc
```



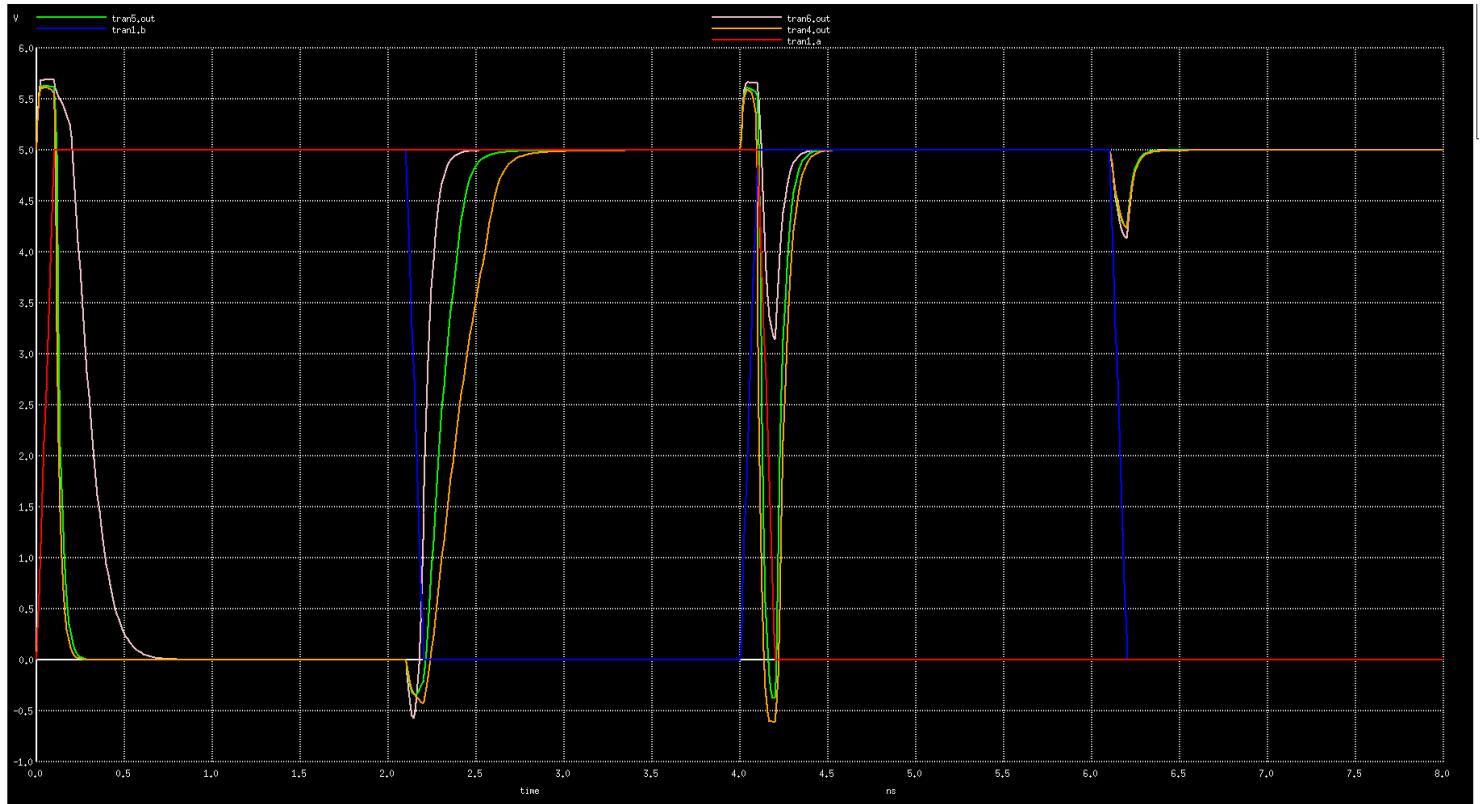


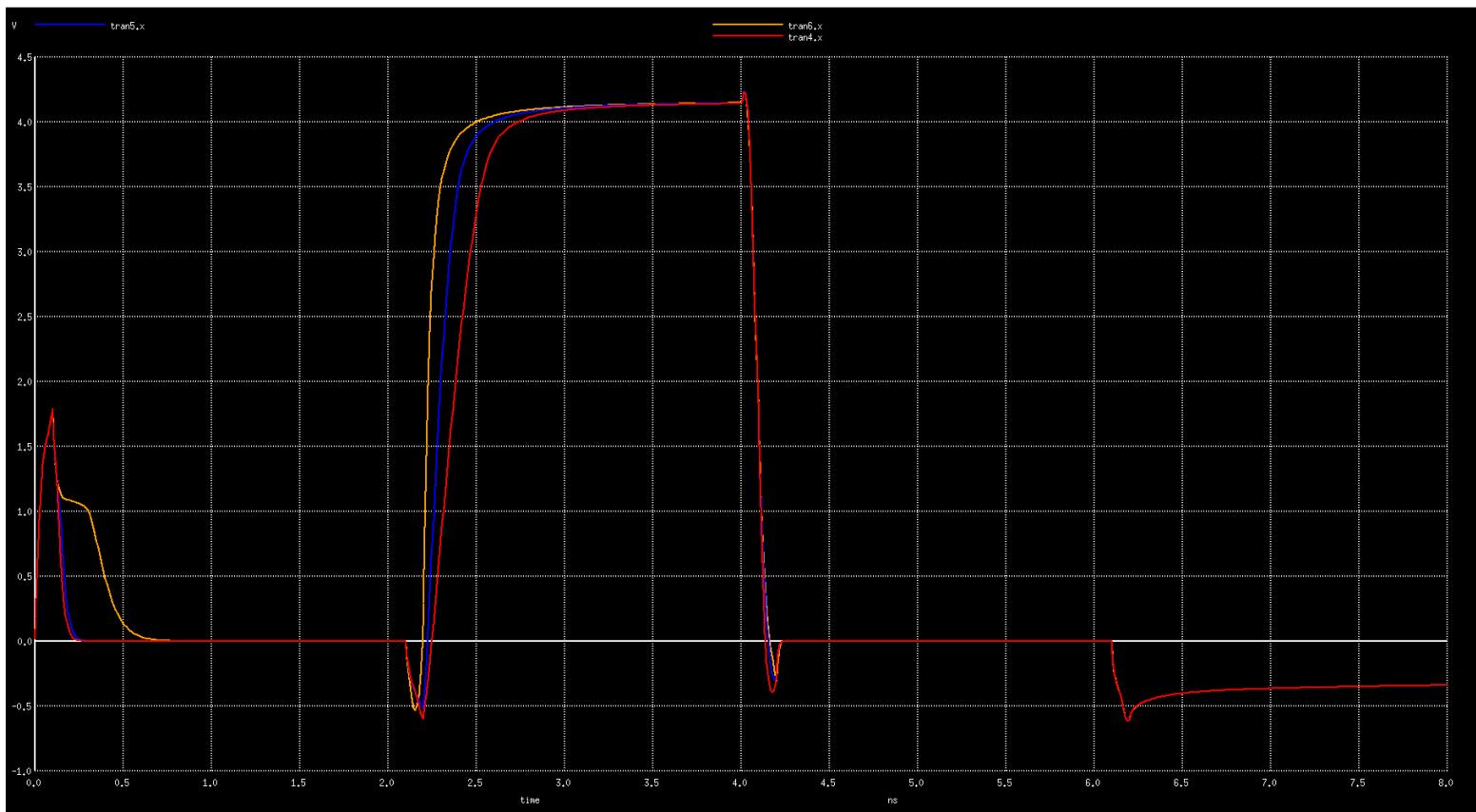
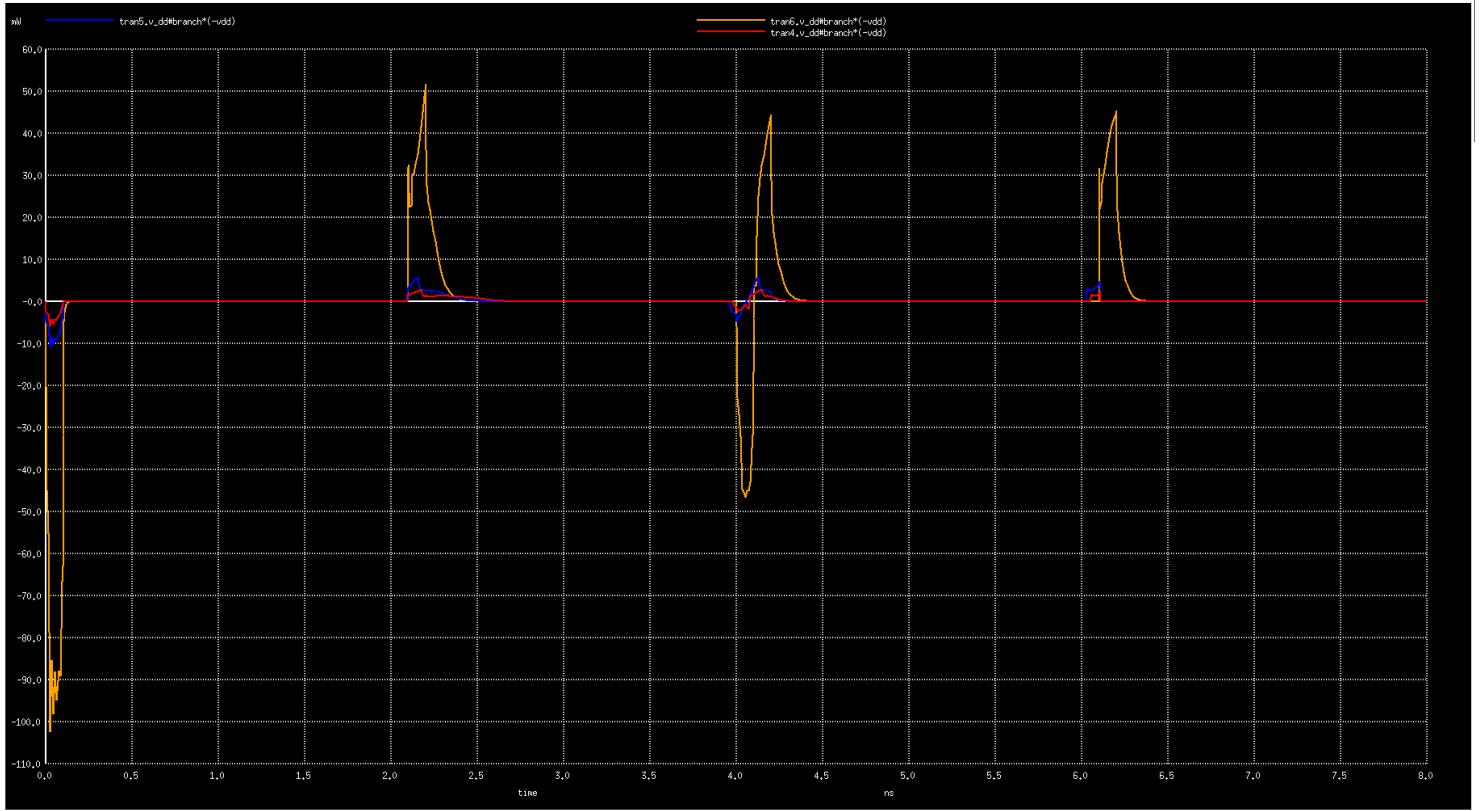
These are the results obtained when we vary the **width of the bottom Mosfet** the first graph is the dc output vs the dc input after doing dc analysis the Noise Margin as we increase the width-the noise margin decreases, the rise time increase and fall time decreases, and the power consumed increases as the resistance decreases as the current increases the energy consumed also increase, and power is consumed in steady state due to sub threshold current. The last graph shows us the voltages at the intermediate node X for the various widths

### Varying the Width of both the PMOS:-

```
*Transfer function and transient response on varying WIDTH of both the PMOS
.control
foreach wid 1.25u 2.5u 25u
alter m2 w=$wid
alter m3 w=$wid
tran 0.01n 8ns
end
alter m2 w=2.5u
alter m3 w=2.5u
.endc

.control
plot tran1.a tran1.b tran4.out tran5.out tran6.out
plot tran4.v_dd#branch*(-vdd) tran5.v_dd#branch*(-vdd) tran6.v_dd#branch*(-vdd)
plot tran4.x tran5.x tran6.x
.endc
```



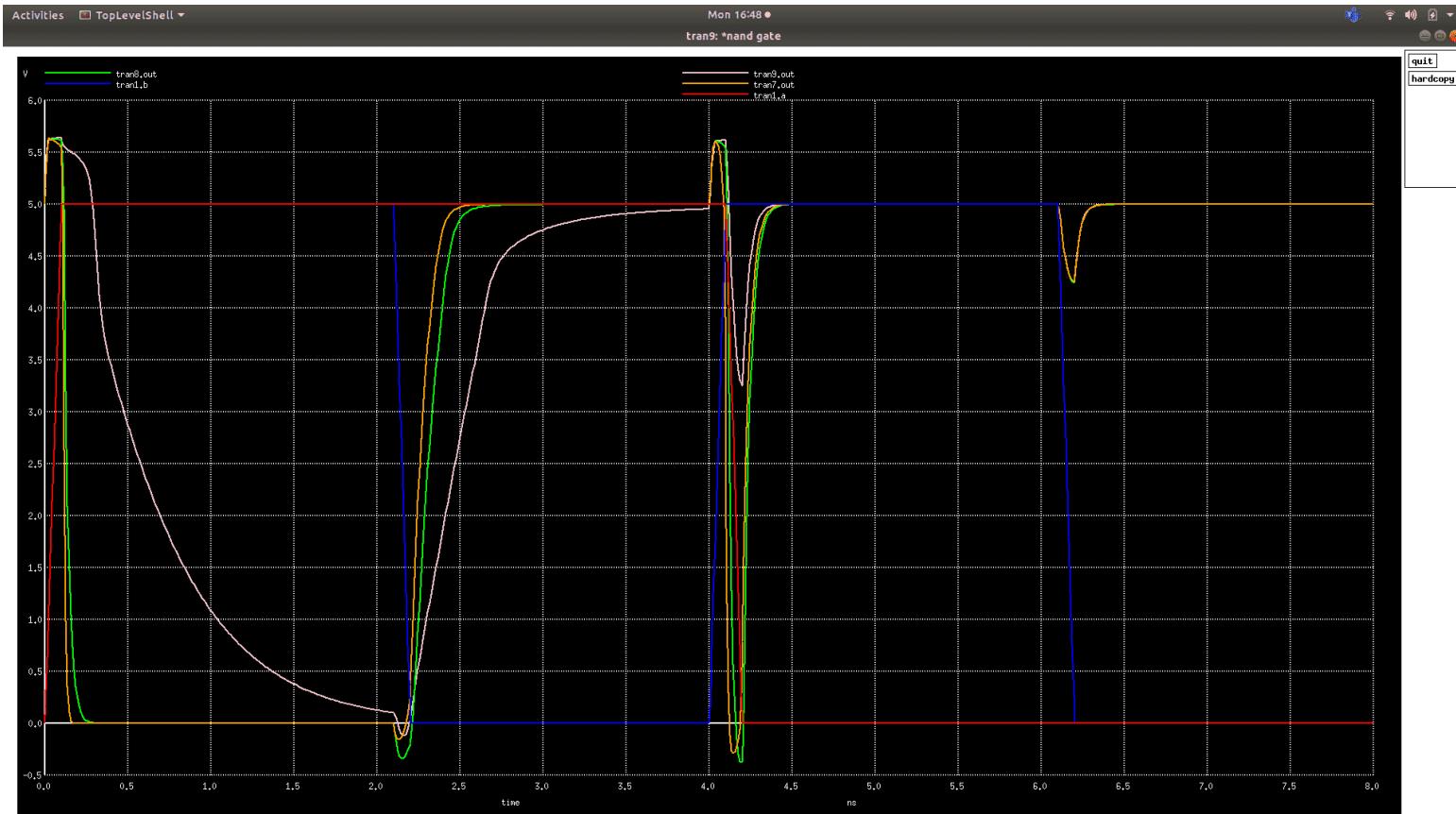


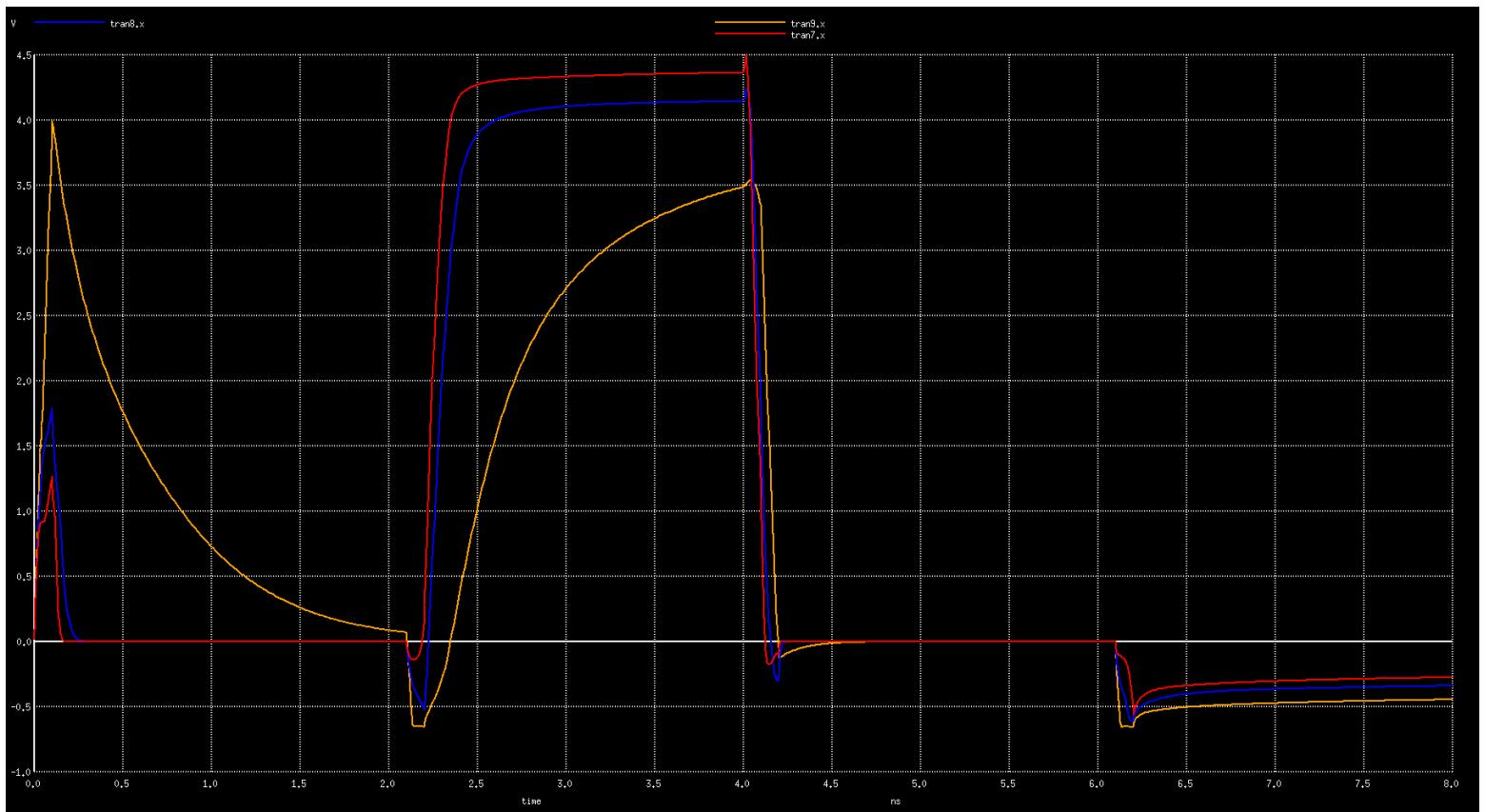
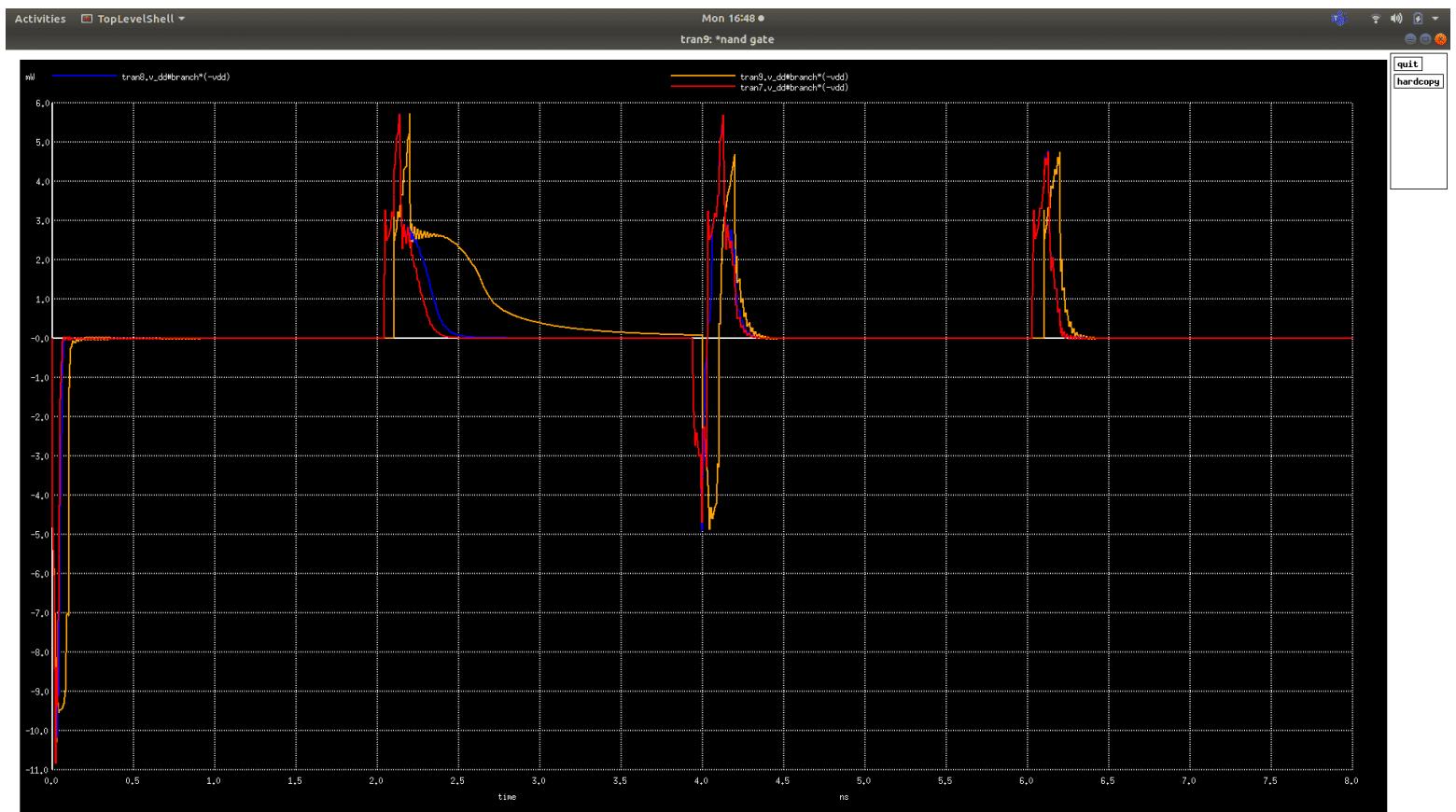
These are the results obtained when we vary the **width of the Top Mosfet** the first graph is the dc output vs the dc input after doing dc analysis the Noise Margin as we increase the width-the noise margin decreases, Looking at first graph the rise time deceases, but fall time increases, Looking at the second graph the power consumed increases as the resistance of the mosfet decreases and the current increases, the energy consumed also increase, and power is consumed in steady state due to sub threshold current. Third graph is the voltage at the node X for various widths.

### Varying Length of Both NMOS:

```
*Transfer function and transient response on varying LENGTH of both the NMOS
.control
foreach len 0.5u 1u 5u
end
alter m0 l=1u
alter m1 l=1u
tran 0.01n 8ns
.endc

.control
plot tran1.a tran1.b tran7.out tran8.out tran9.out
plot tran7.v_dd#branch*(-vdd) tran8.v_dd#branch*(-vdd) tran9.v_dd#branch*(-vdd)
plot tran7.x tran8.x tran9.x
.endc
```





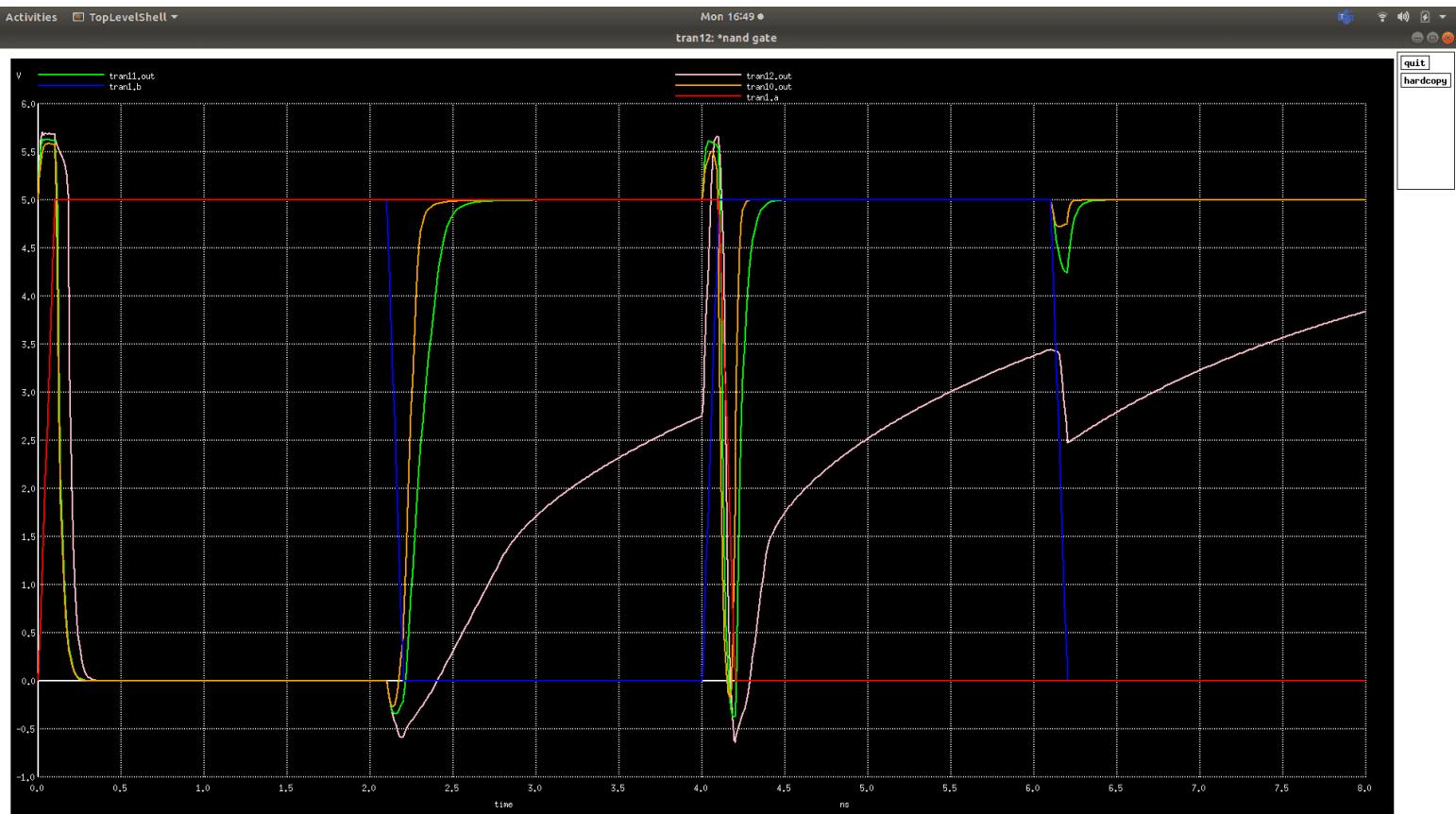
These are the results obtained when we vary the **length of the bottom Mosfet** the first graph is the dc output vs the dc input after doing dc analysis the Noise Margin as we increase the length-the noise margin increases, Looking at the first graph the rise time increase, also the fall time increases, Looking at the second graph the power consumed decreases, but the amount of energy consumed is more, and power is consumed in steady state due to sub threshold current. The third graph is the voltage at the intermediate node.

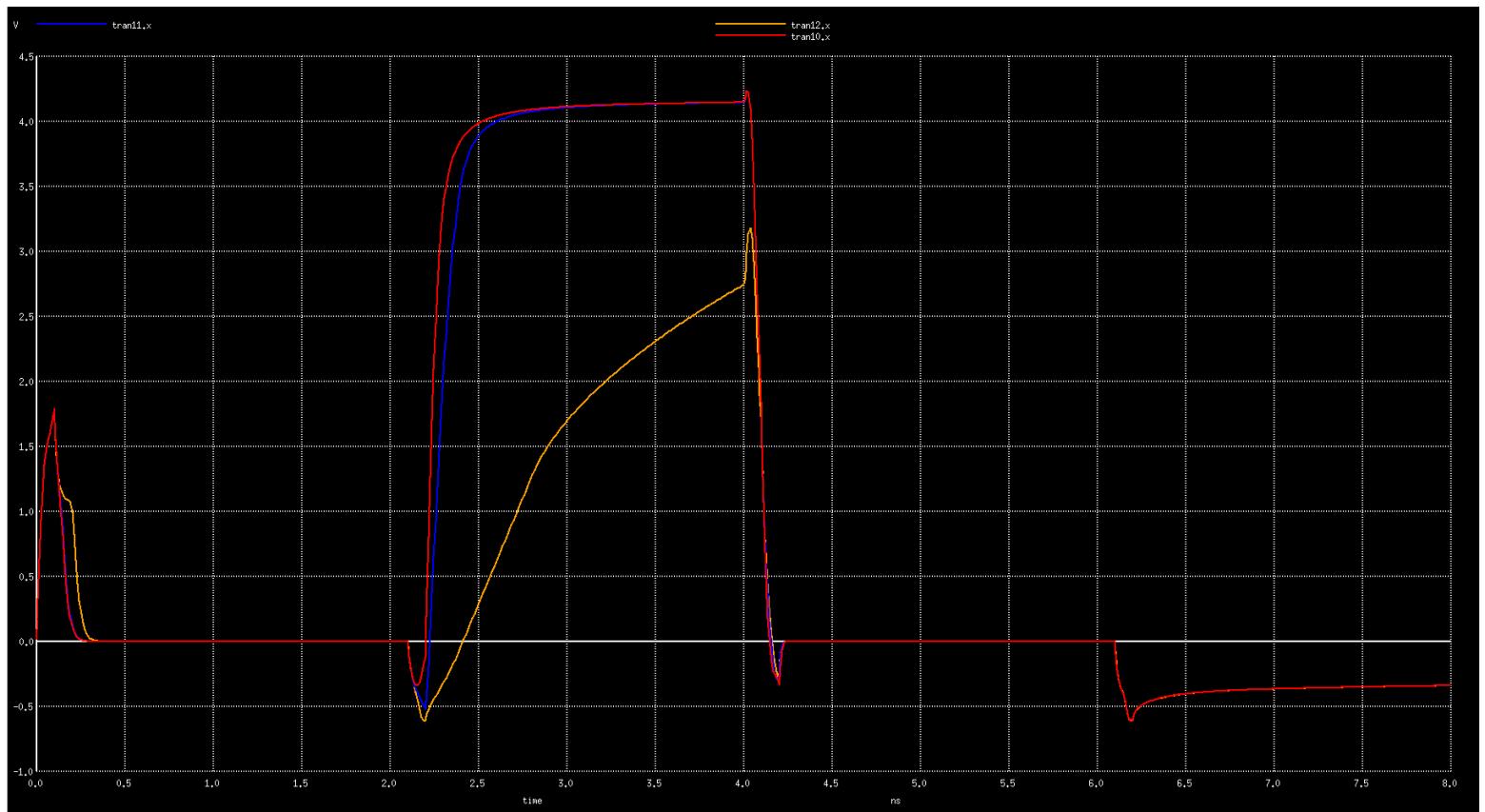
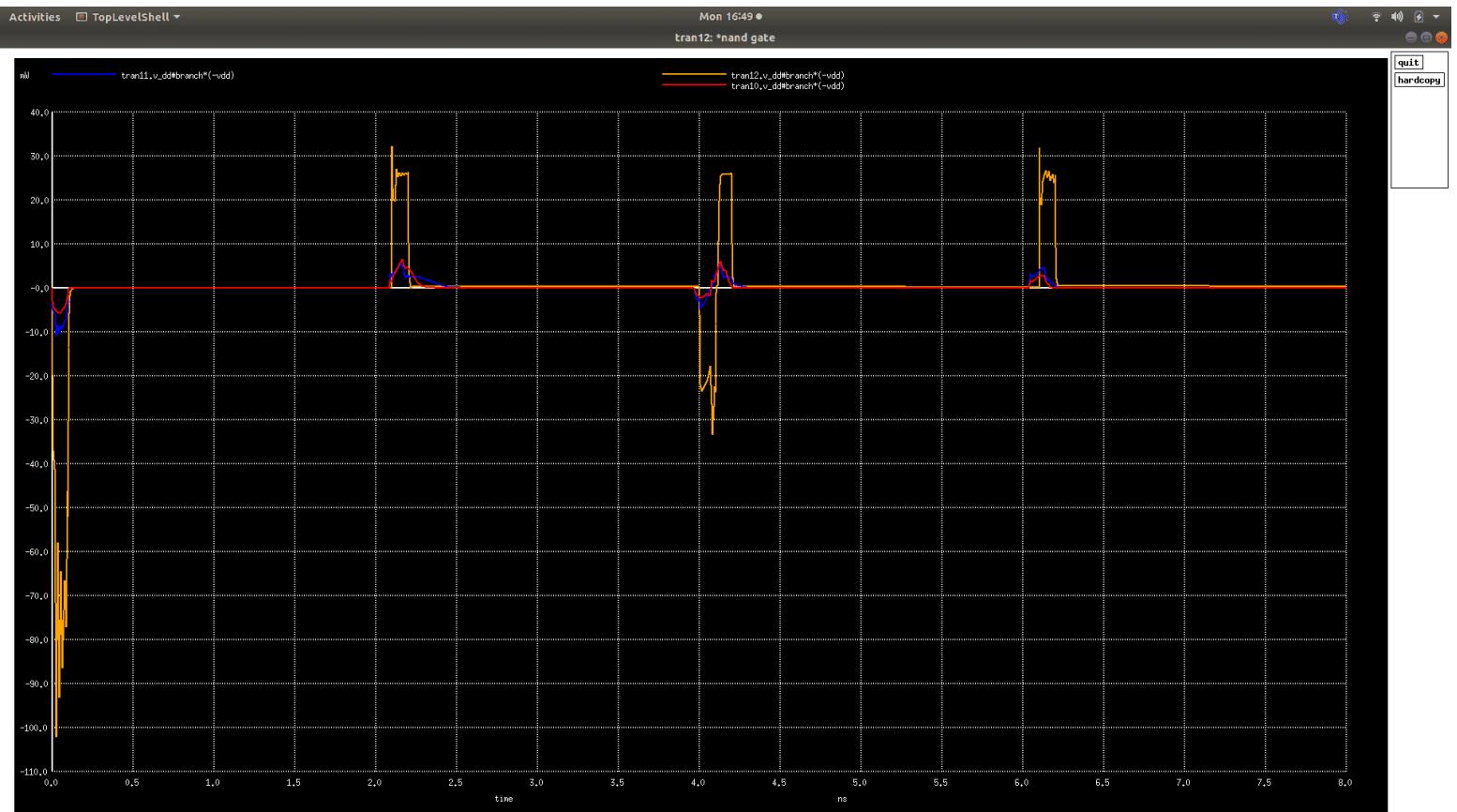
### Varying Length of Both PMOS:-

\*Transfer function and transient response on varying LENGTH of both the PMOS

```
.control
foreach len 0.5u 1u 10u
alter m2 l=$len
alter m3 l=$len
tran 0.01n 8ns
end
.endc

.control
plot tran1.a tran1.b tran10.out tran11.out tran12.out
plot tran10.v_dd#branch*(-vdd) tran11.v_dd#branch*(-vdd) tran12.v_dd#branch*(-vdd)
tran10.x tran11.x tran12.x
.endc
```



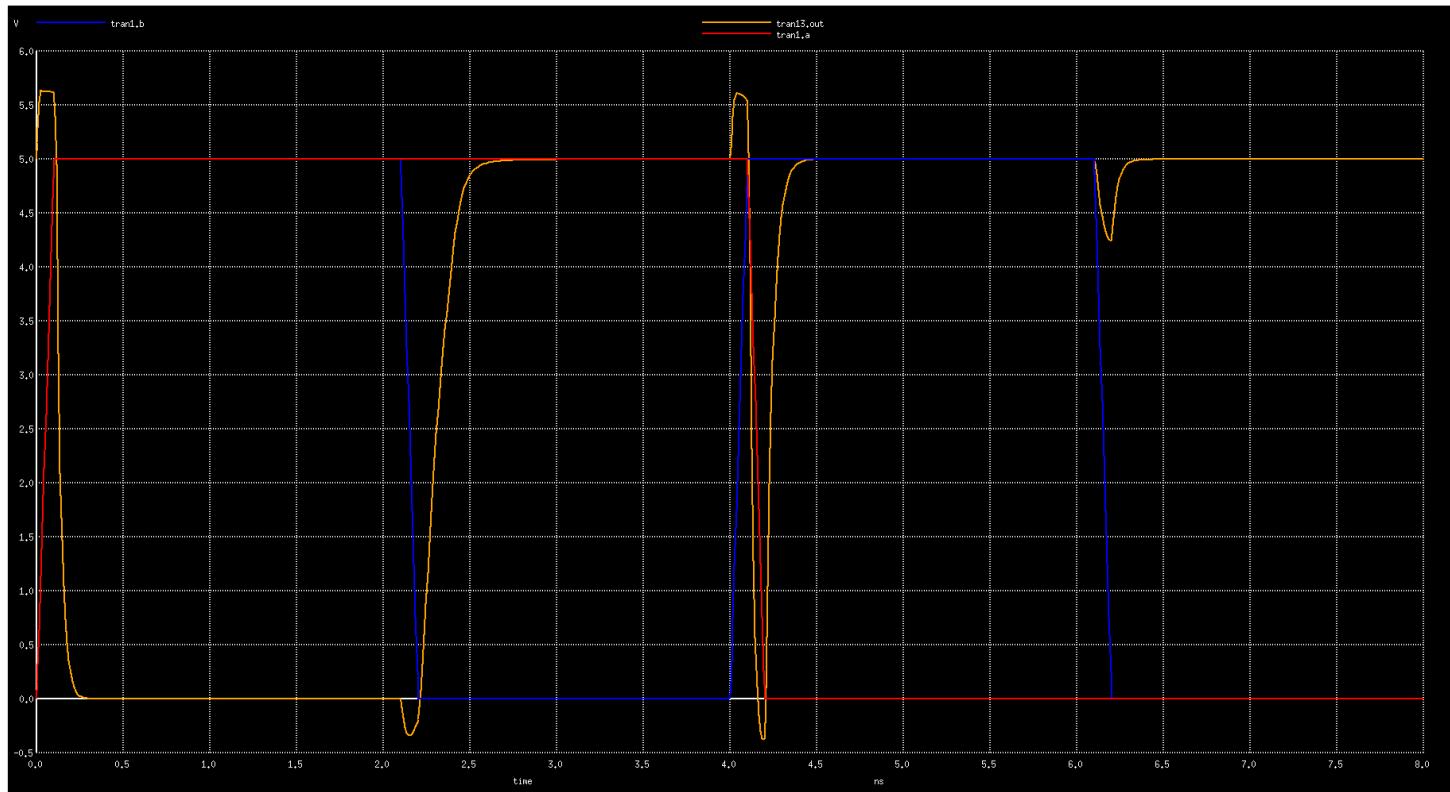


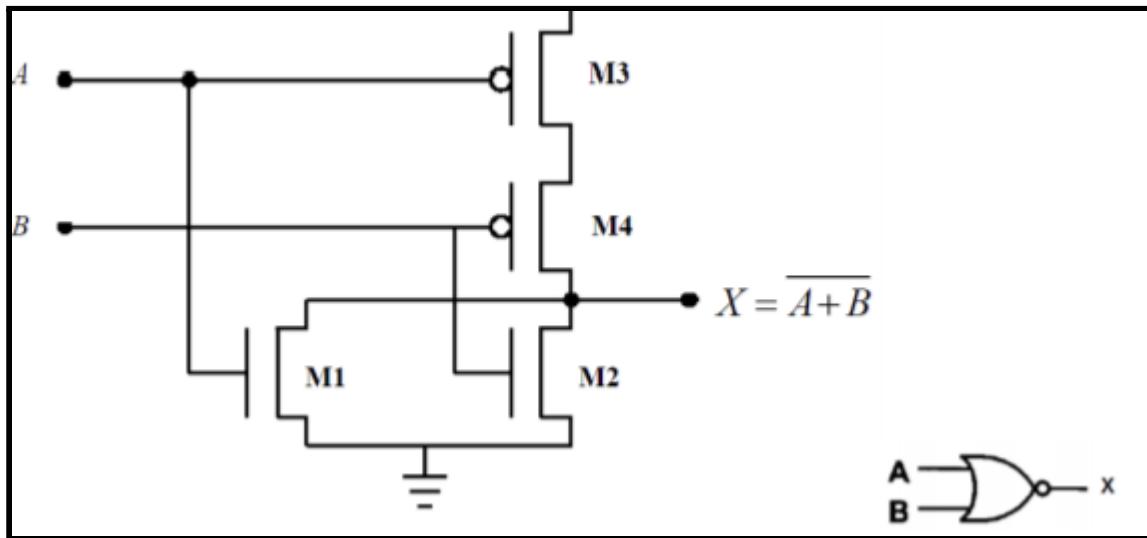
These are the results obtained when we vary the **length of the Top Mosfets**, Looking at the first graph the rise time increase, but also fall time increases, Looking at the second graph the power consumed increases as the resistance increase the energy consumed also increase, and power is consumed in steady state due to sub threshold current. The last graph shows us the voltage at the intermediate node.

### Regular Response:-

```
.control
  tran 0.01n 8n
  run
.endc

.control
  plot tran1.a tran1.b tran13.out
.endc
.end
```



**Nor:****Circuit:-****Fig: Nor Gate****Varying the Width of Both NMOS:-**

```
.include ./t14y_tsmc_025_level3.txt

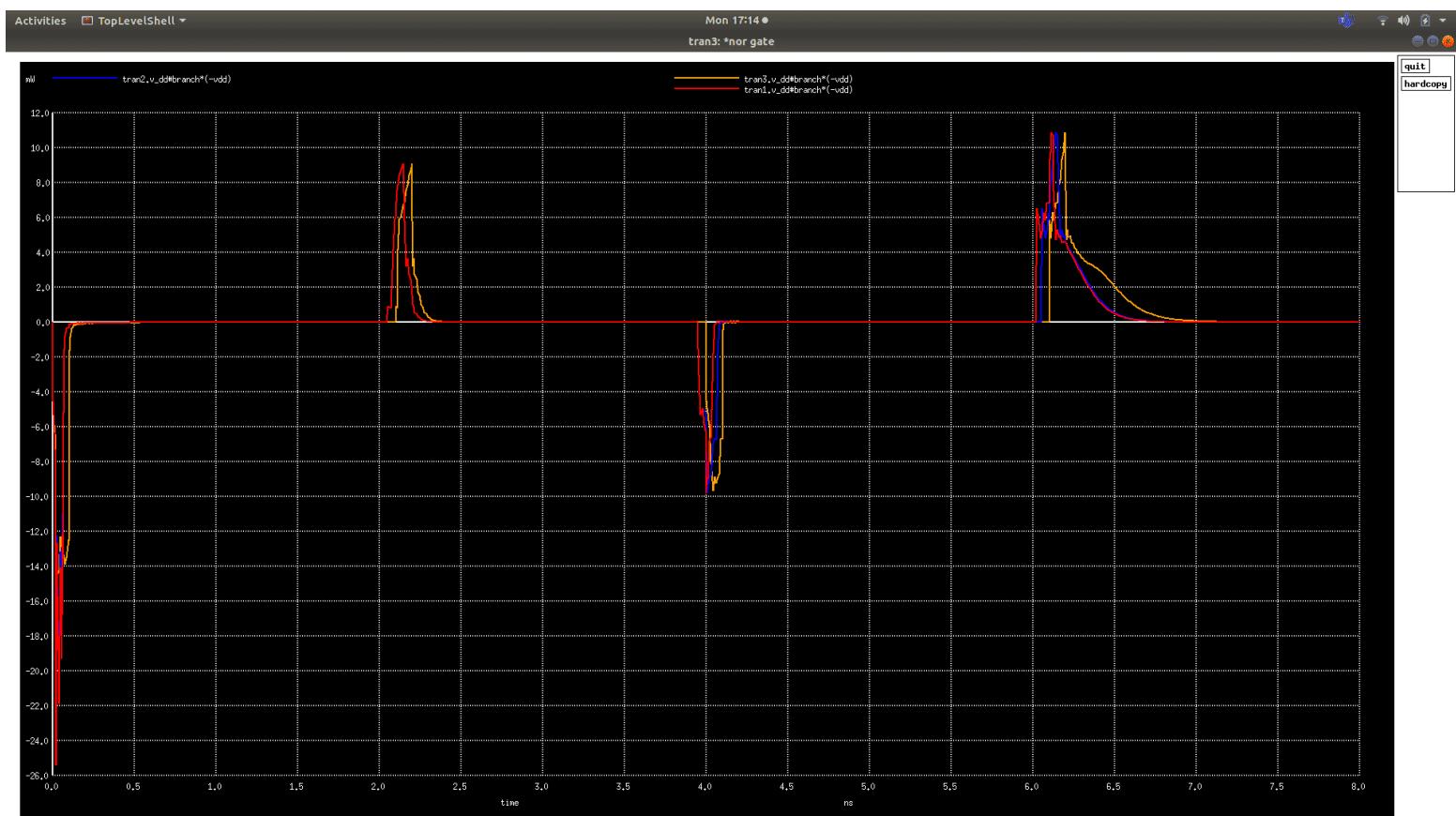
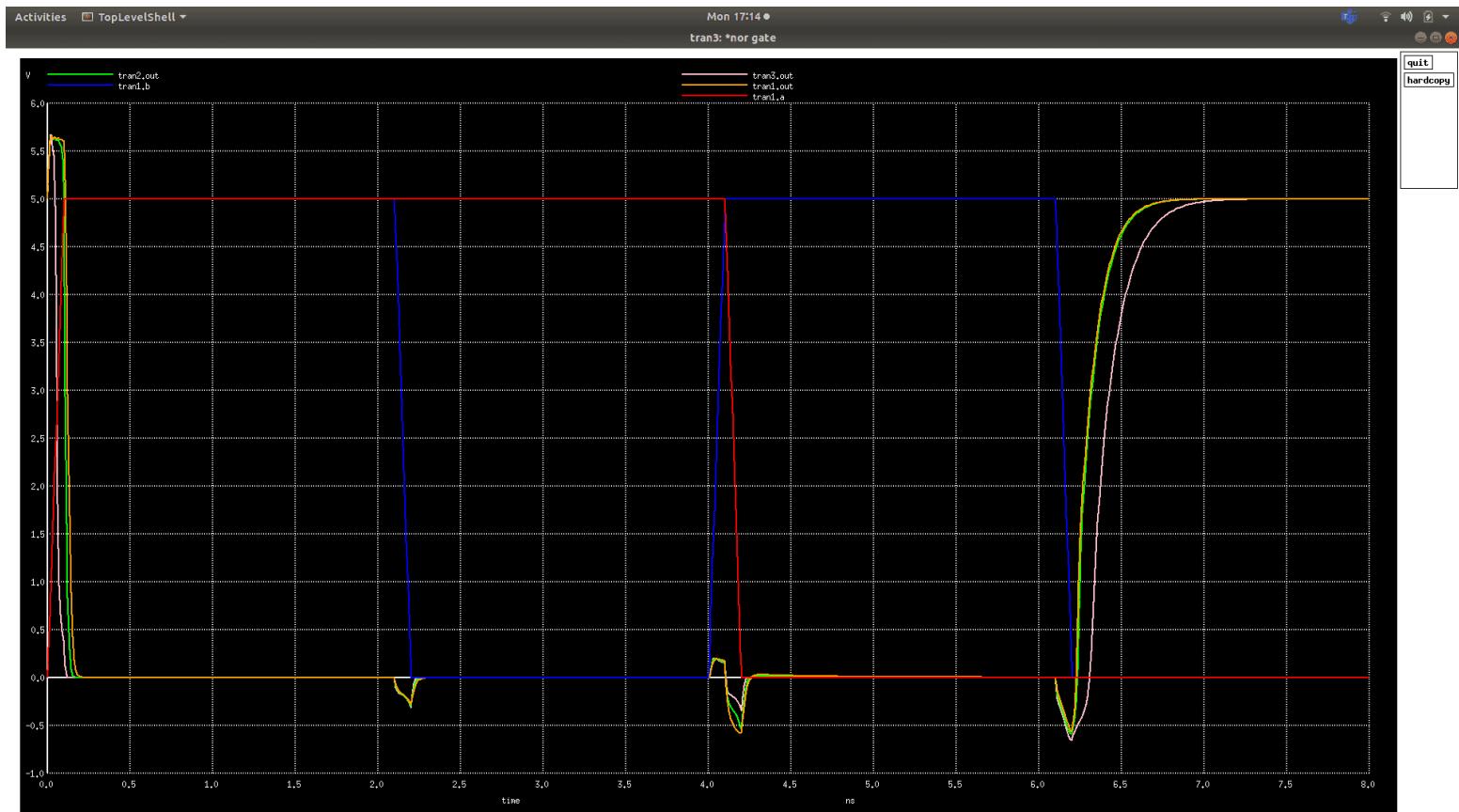
*Pull down network
m0 out a 0 0 cmosn l=1u w=1u
m1 out b 0 0 cmosn l=1u w=1u

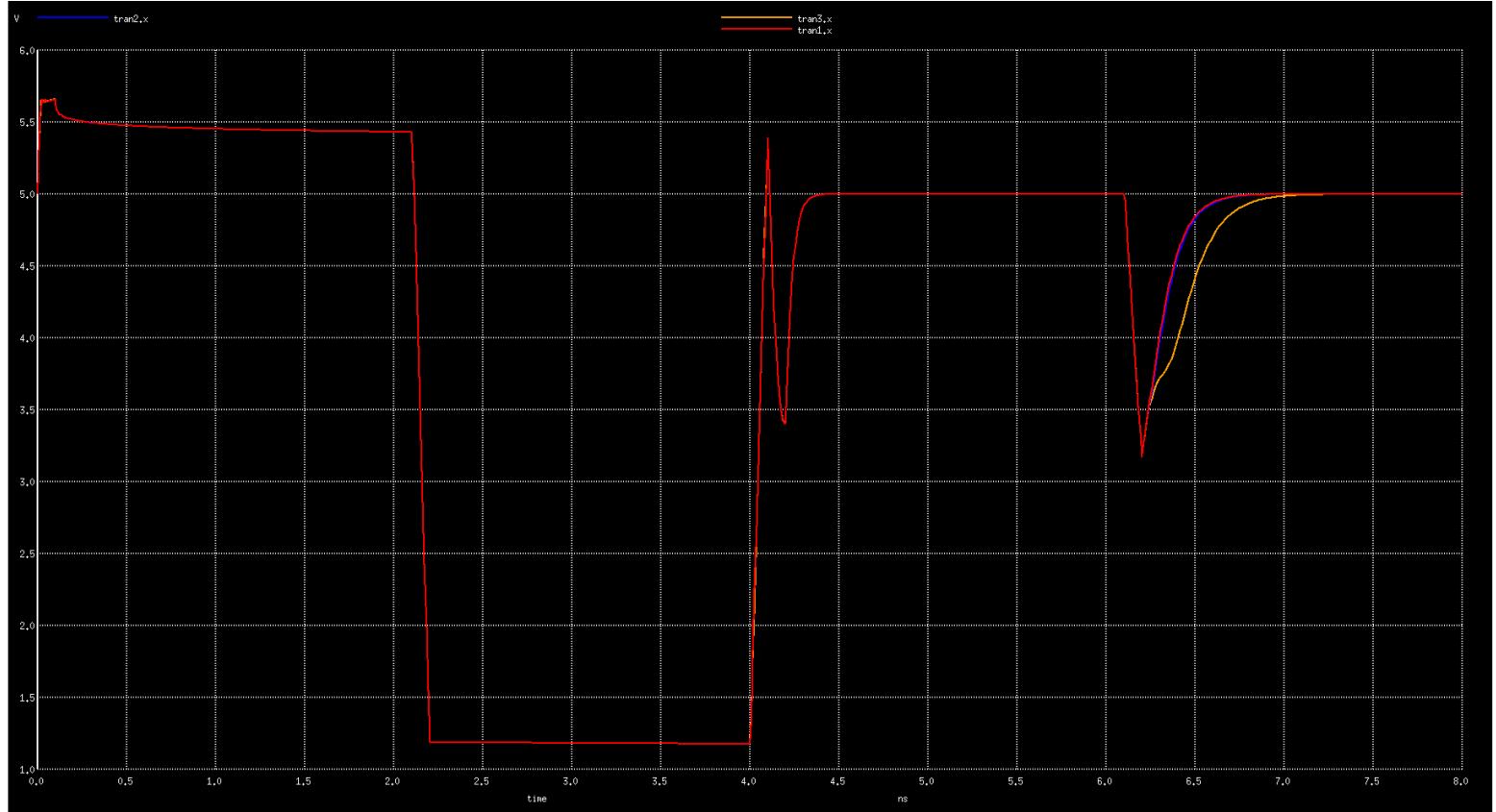
*Pull up network
m2 vdd a x vdd cmosp l=1u w=5u
m3 x b out vdd cmosp l=1u w=5u

v_dd vdd 0 5
v_a a 0 5 pulse(0 5 0 0.1n 0.1n 4n 8n)
v_b b 0 5 pulse(0 5 0 0.1n 0.1n 2n 4n)

*Transfer function and transient response on varying WIDTH of both the NMOS
.control
foreach wid 0.5u 1u 10u
alter m0 w=$wid
alter m1 w=$wid
tran 0.01n 8ns
end
alter m0 w=1u
alter m1 w=1u
.endc

.control
plot tran1.a tran1.b tran1.out tran2.out tran3.out
plot tran1.v_dd#branch*(-vdd) tran2.v_dd#branch*(-vdd) tran3.v_dd#branch*(-vdd)
tran1.x tran2.x tran3.x
.endc
```



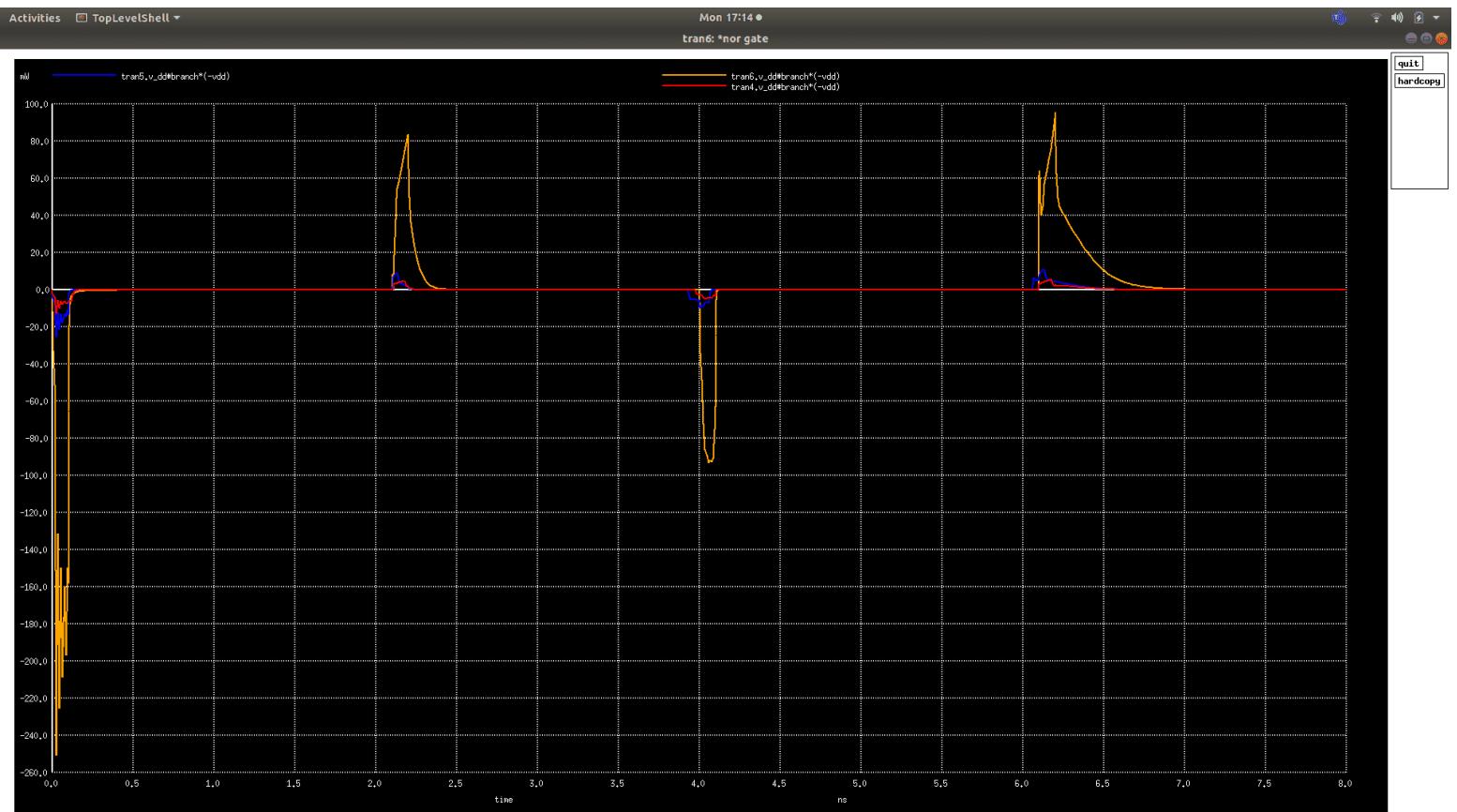
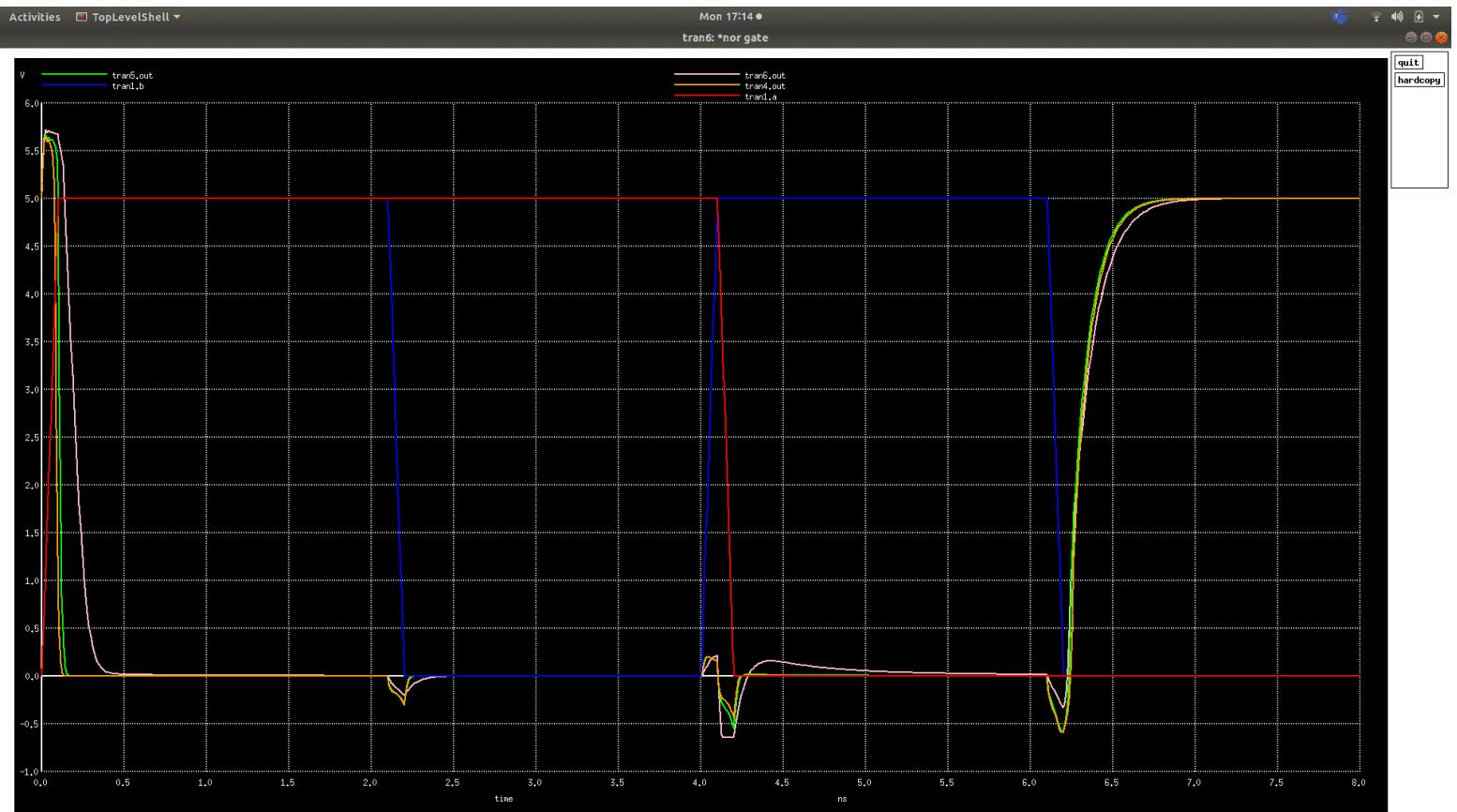


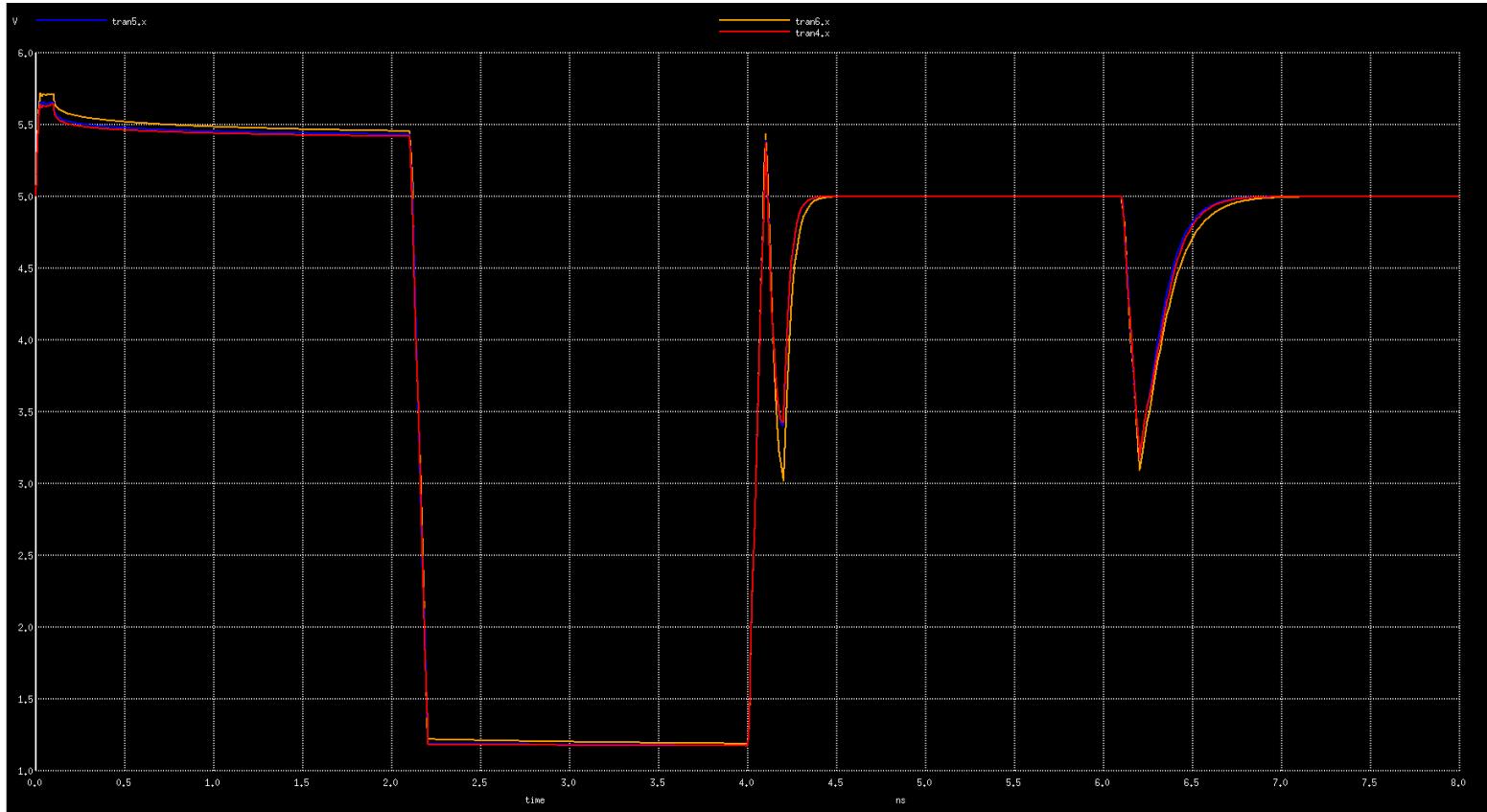
These are the results obtained when we vary the **width of the bottom Mosfets** doing dc analysis the Noise Margin as we increase the width-the noise margin decreases and those not in the range do not act as an gate,, the rise time stays the same but when width is to big it will increase but fall time decreases, and the power consumed increases as the resistance decreases and the current increases the energy consumed also increase, and power is consumed in steady state due to sub threshold current. The last graph is the voltage at the intermediate node

### Varying the Width of Both PMOS:-

```
*Transfer function and transient response on varying WIDTH of both the PMOS
.control
foreach wid 2.5u 5u 50u
alter m2 w=$wid
alter m3 w=$wid
tran 0.01n 8ns
end
alter m2 w=5u
alter m3 w=5u
.endc

.control
    plot tran1.a tran1.b tran4.out tran5.out tran6.out
    plot tran4.v_dd#branch*(-vdd) tran5.v_dd#branch*(-vdd) tran6.v_dd#branch*(-vdd)
    tran4.x tran5.x tran6.x
.endc
```



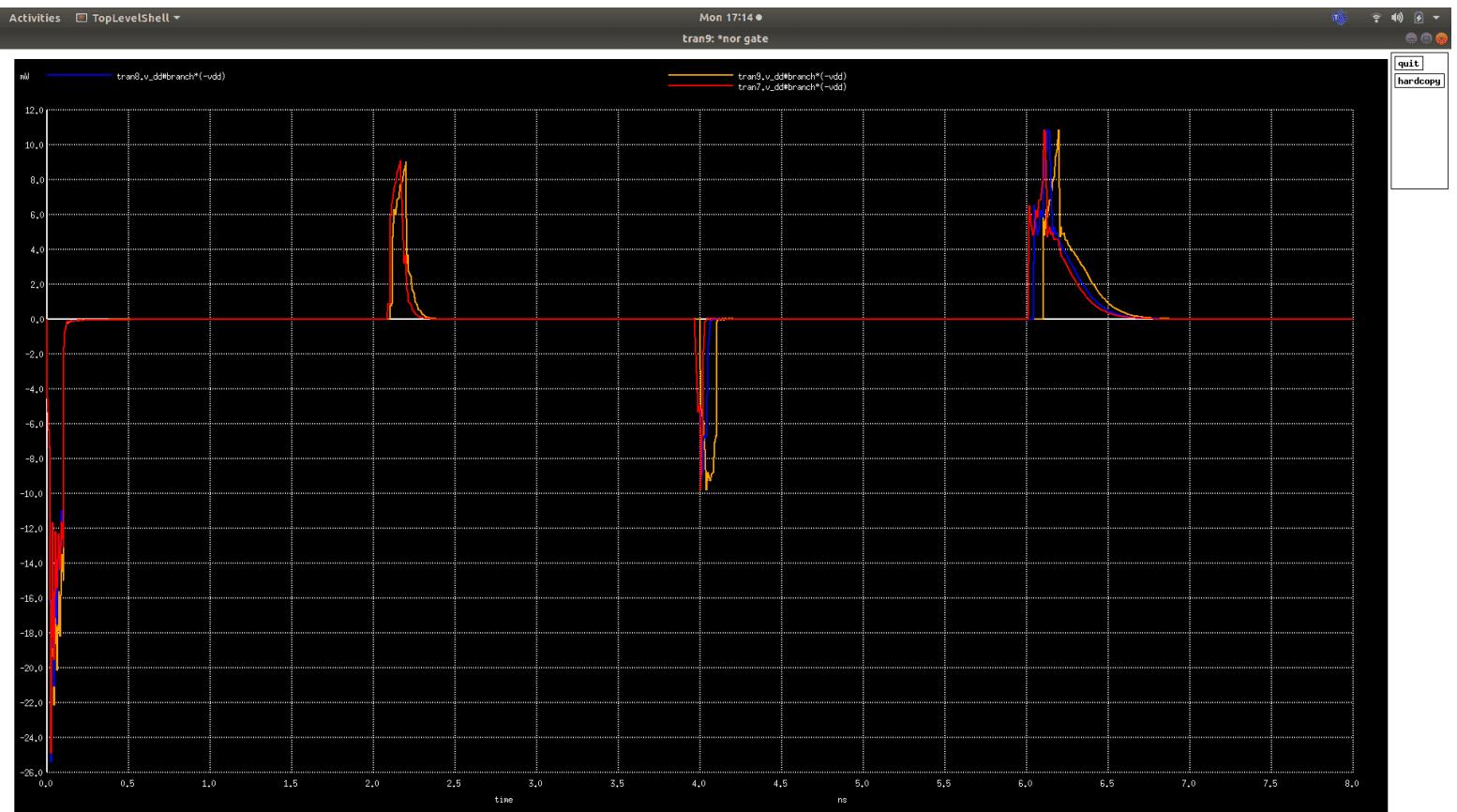
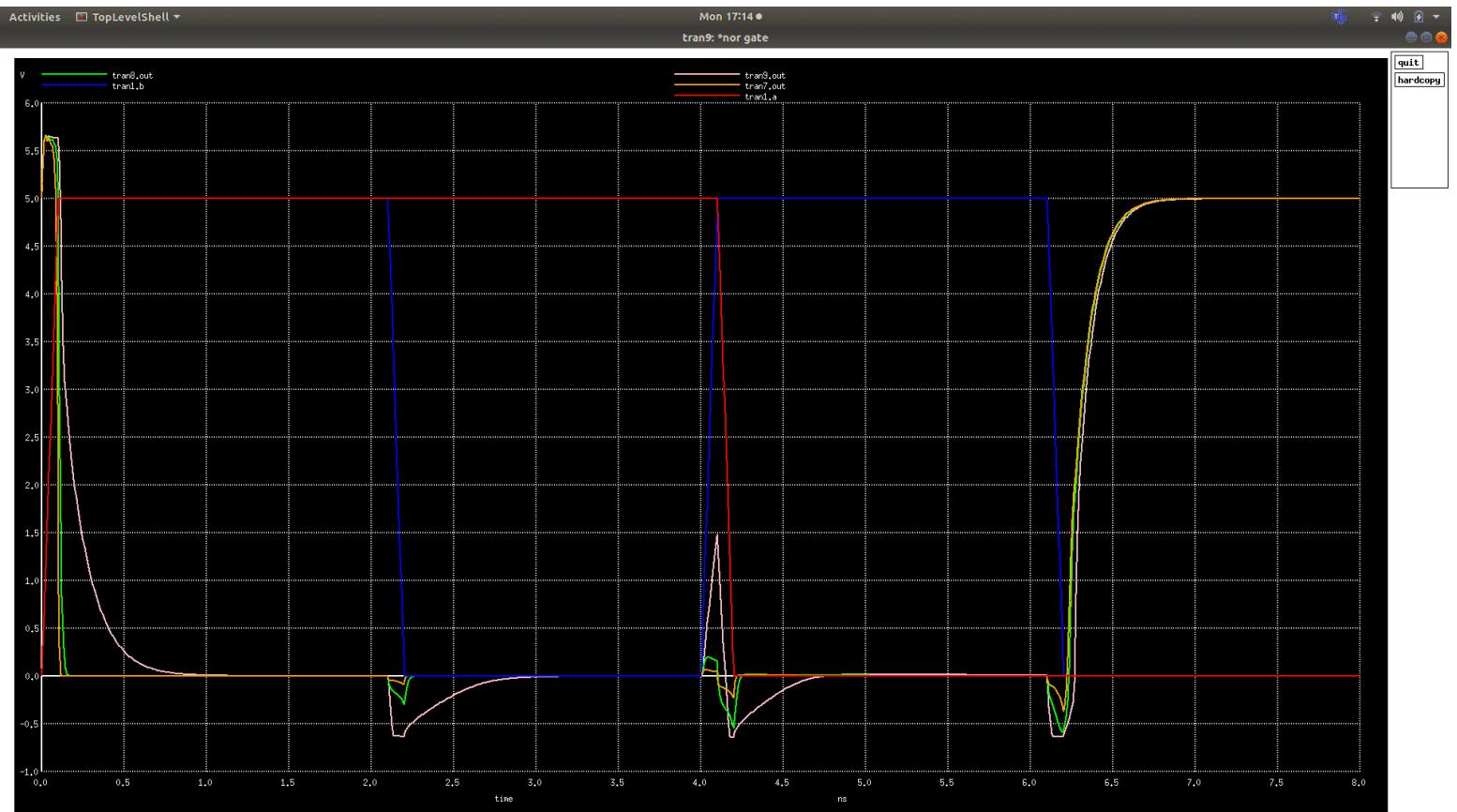


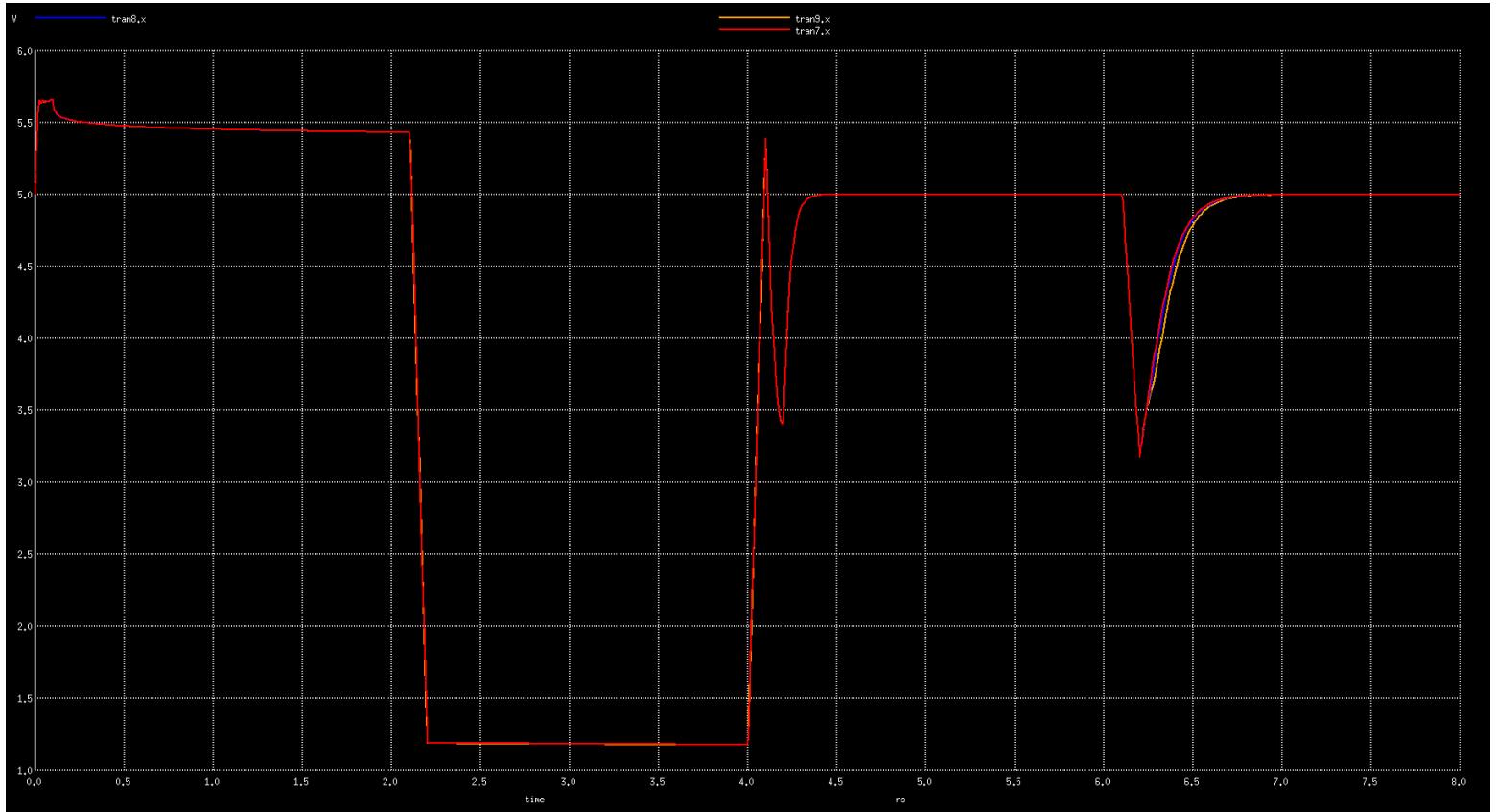
These are the results obtained when we vary the **width of the Top Mosfets** after doing dc analysis the Noise Margin as we increase the width-the noise margin decreases and those not in the range do not act as an gate, Looking at first graph the rise time deceases, but fall time increases, Looking at the second graph the power consumed increases as the resistance decreases and the current increases the energy consumed also increase, and power is consumed in steady state due to sub threshold current. The third graph is the intermediate node voltages while varying width of Pmos.

### Varying the Length of Both NMOS:-

```
*Transfer function and transient response on varying LENGTH of both the NMOS
.control
foreach len 0.5u 1u 5u
alter m0 l=$len
alter m1 l=$len
tran 0.01n 8ns
end
alter m0 l=1u
alter m1 l=1u
.endc

.control
plot tran1.a tran1.b tran7.out tran8.out tran9.out
plot tran7.v_dd#branch*(-vdd) tran8.v_dd#branch*(-vdd) tran9.v_dd#branch*(-vdd)
tran7.x tran8.x tran9.x
.endc
```





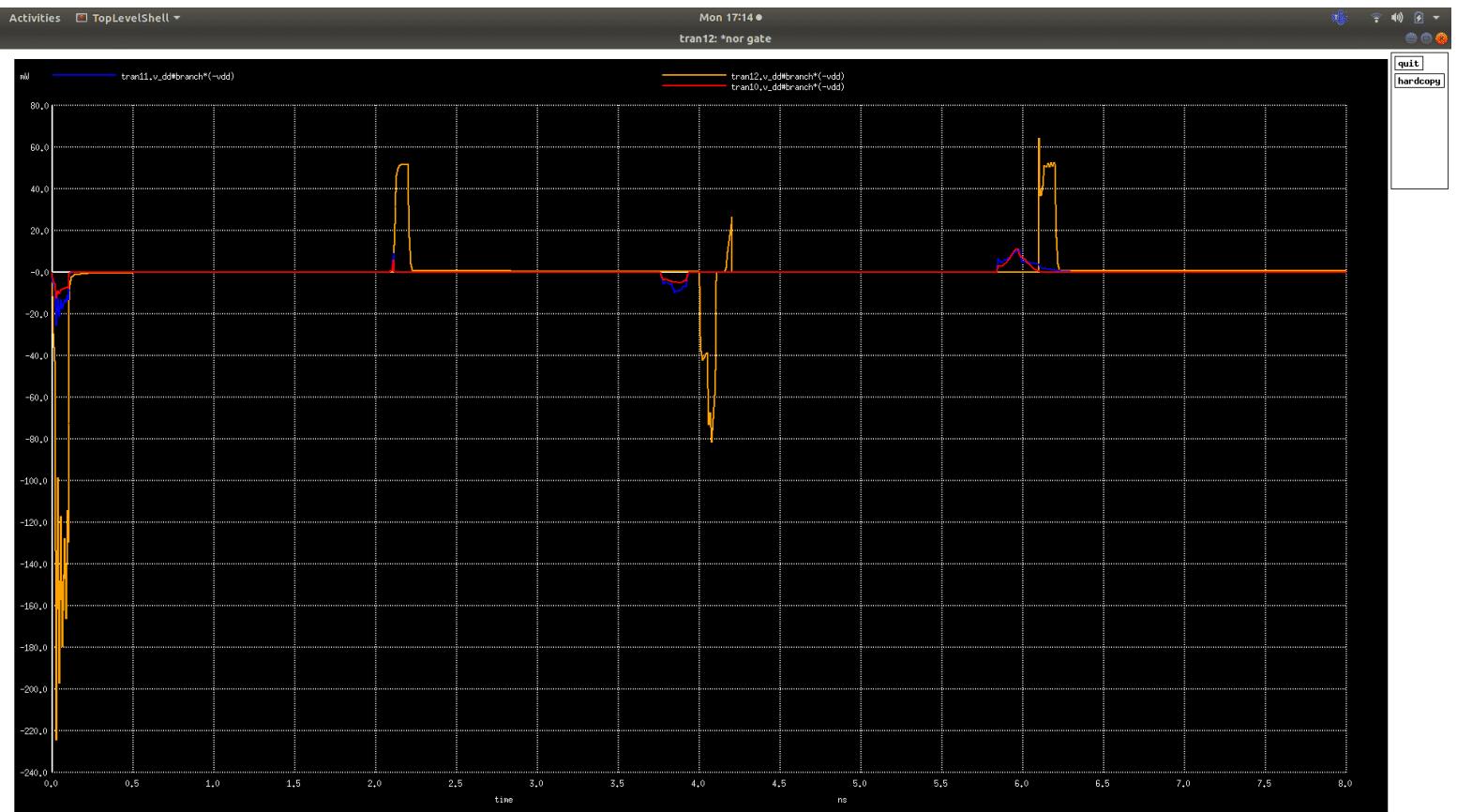
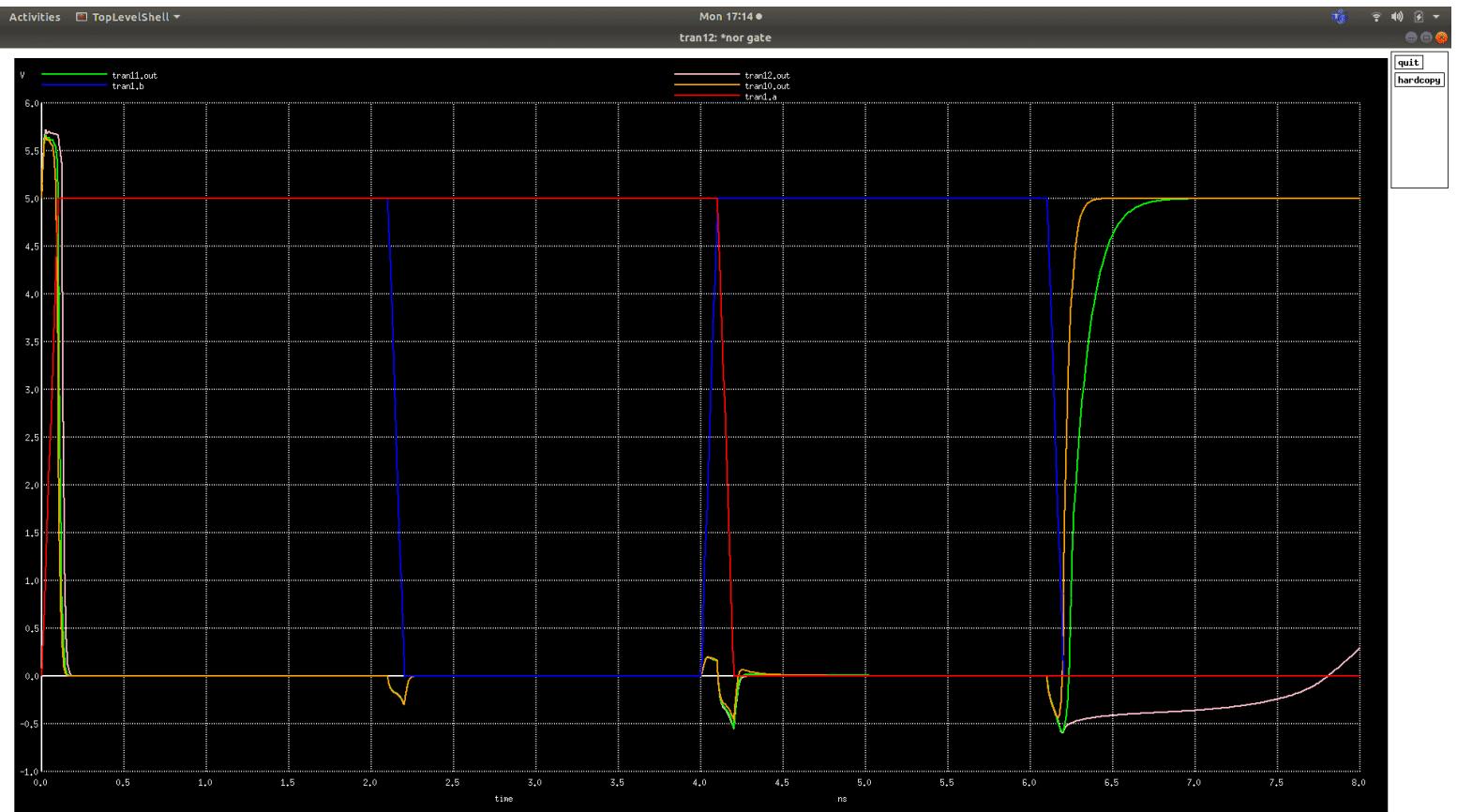
These are the results obtained when we vary the **length of the bottom Mosfets** after doing dc analysis, as we increase the length-the noise margin increases and those not in the range do not act as an gate,, Looking at first graph the rise time increase, also fall time increases, Looking at the second graph the power consumed increases, and the amount of energy consumed is more, and power is consumed in steady state due to sub threshold current. The third graph is the intermediate voltage of X when varying the length

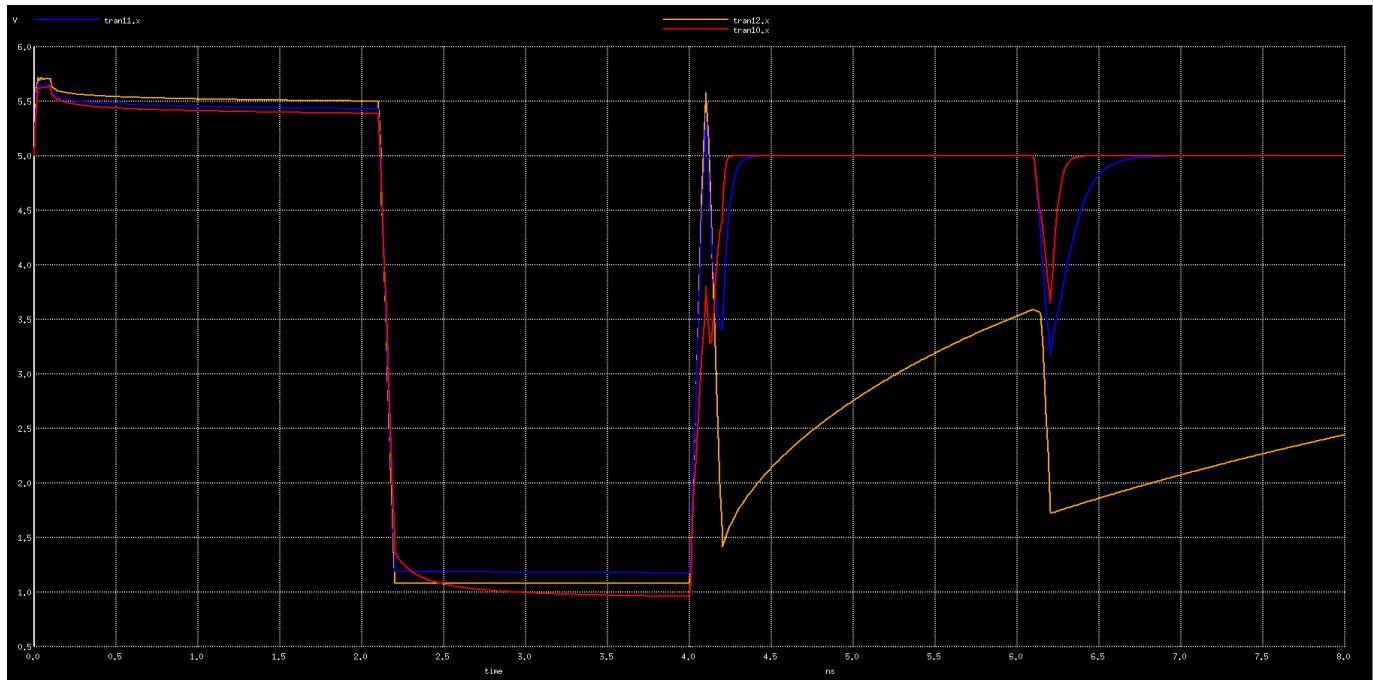
### Varying Length of Both the PMOS:

\*Transfer function and transient response on varying LENGTH of both the PMOS

```
.control
foreach len 0.5u 1u 10u
alter m2 l=$len
alter m3 l=$len
tran 0.01n 8ns
end
alter m2 l=1u
alter m3 l=1u
.endc

.control
  plot tran1.a tran1.b tran10.out tran11.out tran12.out
  plot tran10.v_dd#branch*(-vdd) tran11.v_dd#branch*(-vdd) tran12.v_dd#branch*(-vdd)
.endc
```



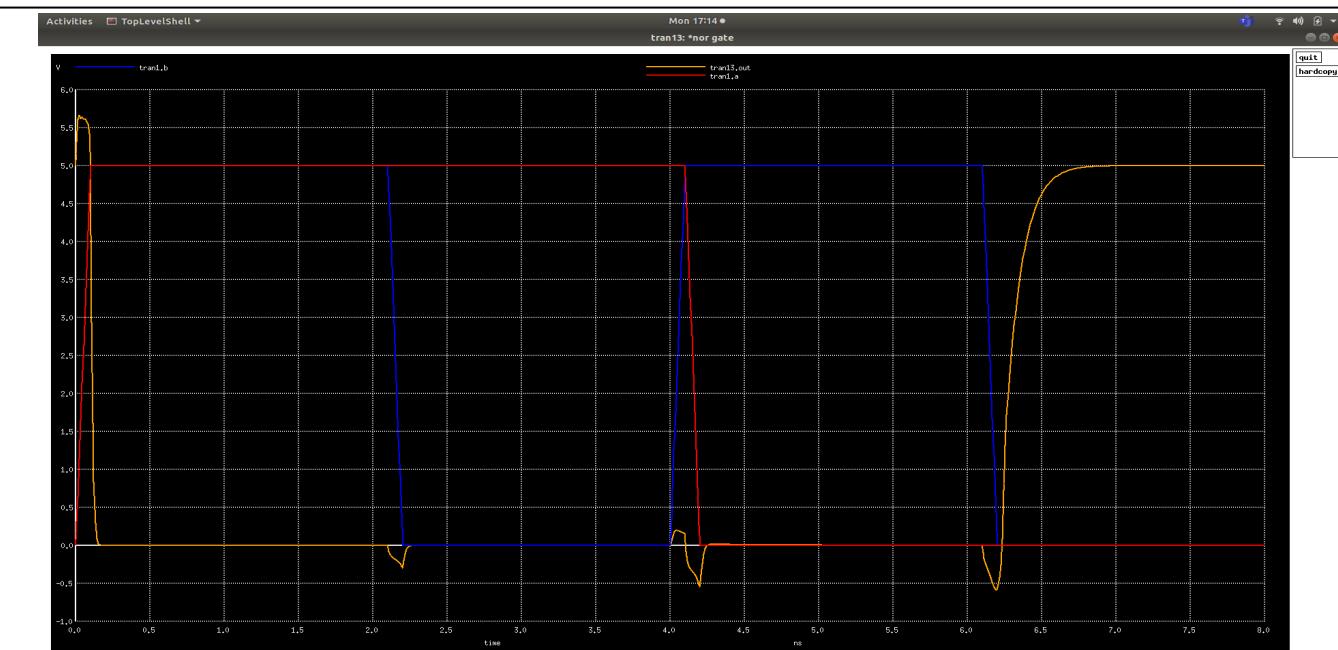


These are the results obtained when we vary the **length of the Top Mosfets** as we increase the length-the noise margin decreases and those not in the range do not act as an gate, Looking at first graph the rise time increase, but fall time increases, Looking at the second graph the power consumed increases as the resistance increase the energy consumed also increase, and power is consumed in steady state due to sub threshold current. The third graph is the intermediate node voltages for the varying lengths.

### Regular Response:-

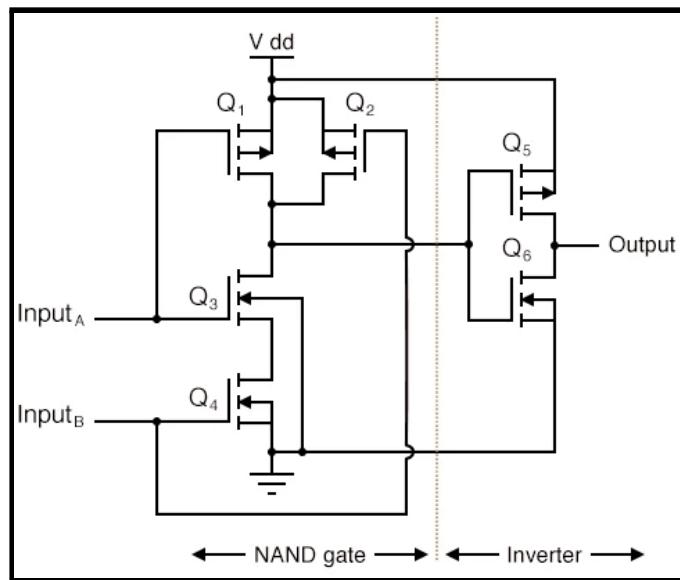
```
.control
  tran 0.01n 8n
.endc

.control
  plot tran1.a tran1.b tran13.out
.endc
.end
```



**And:**

**Circuit:-**



**Fig:-And Gate**

**Varying the Width Of Both NMOS:-**

```

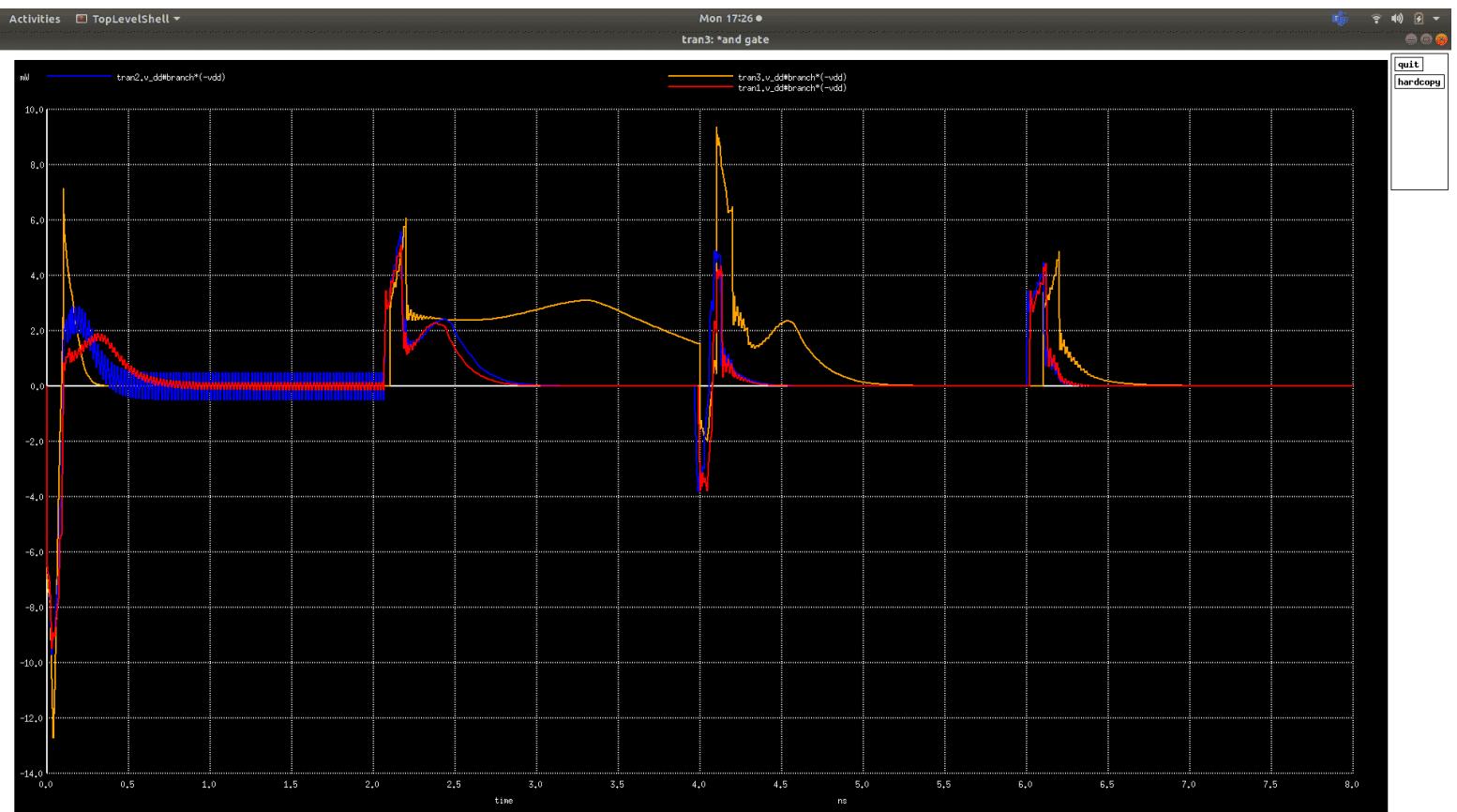
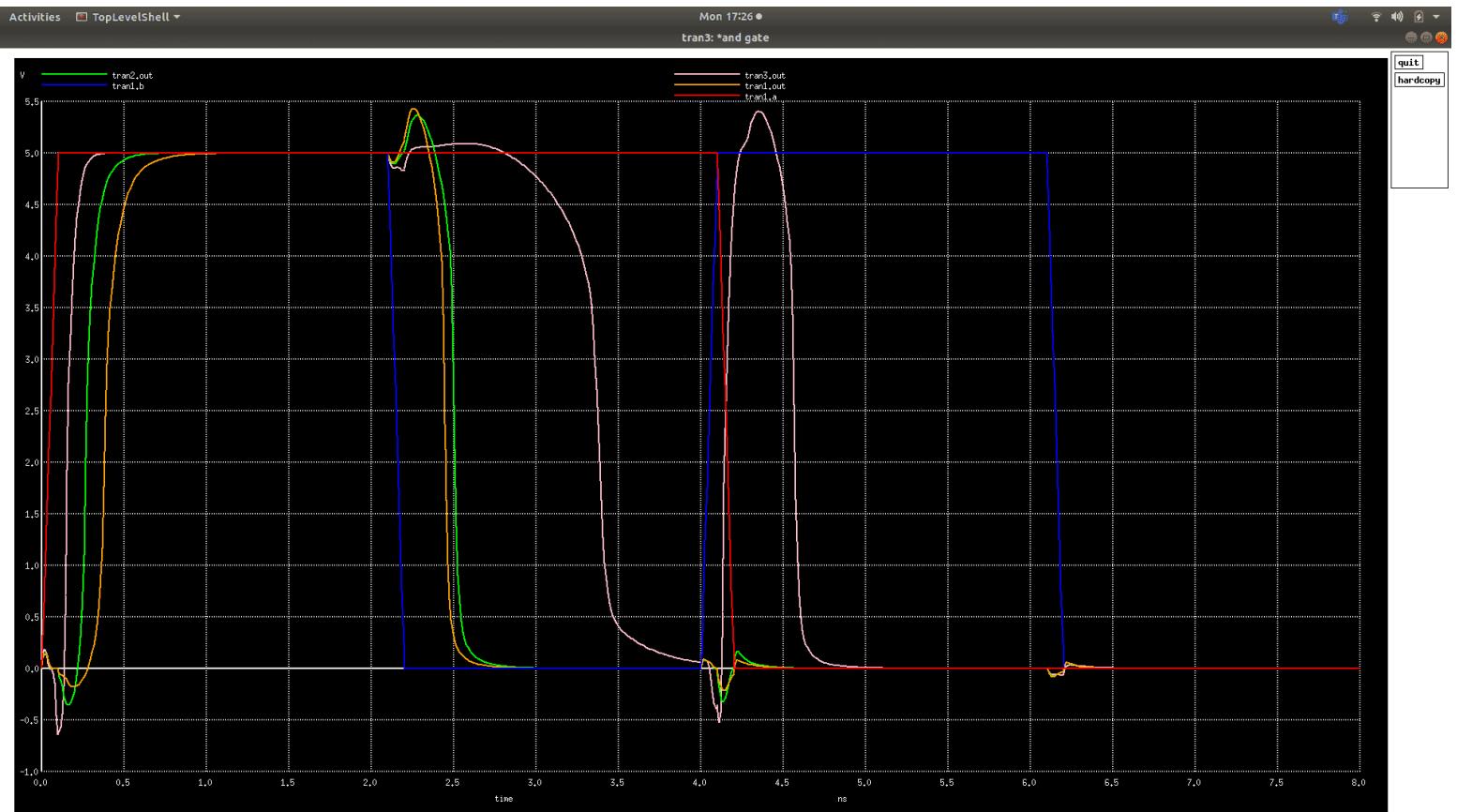
.include ./t14y_tsmc_025_level3.txt
*Pull down network
m0 y a x 0 cmosn w=2u l=1u
m1 x b 0 0 cmosn w=2u l=1u

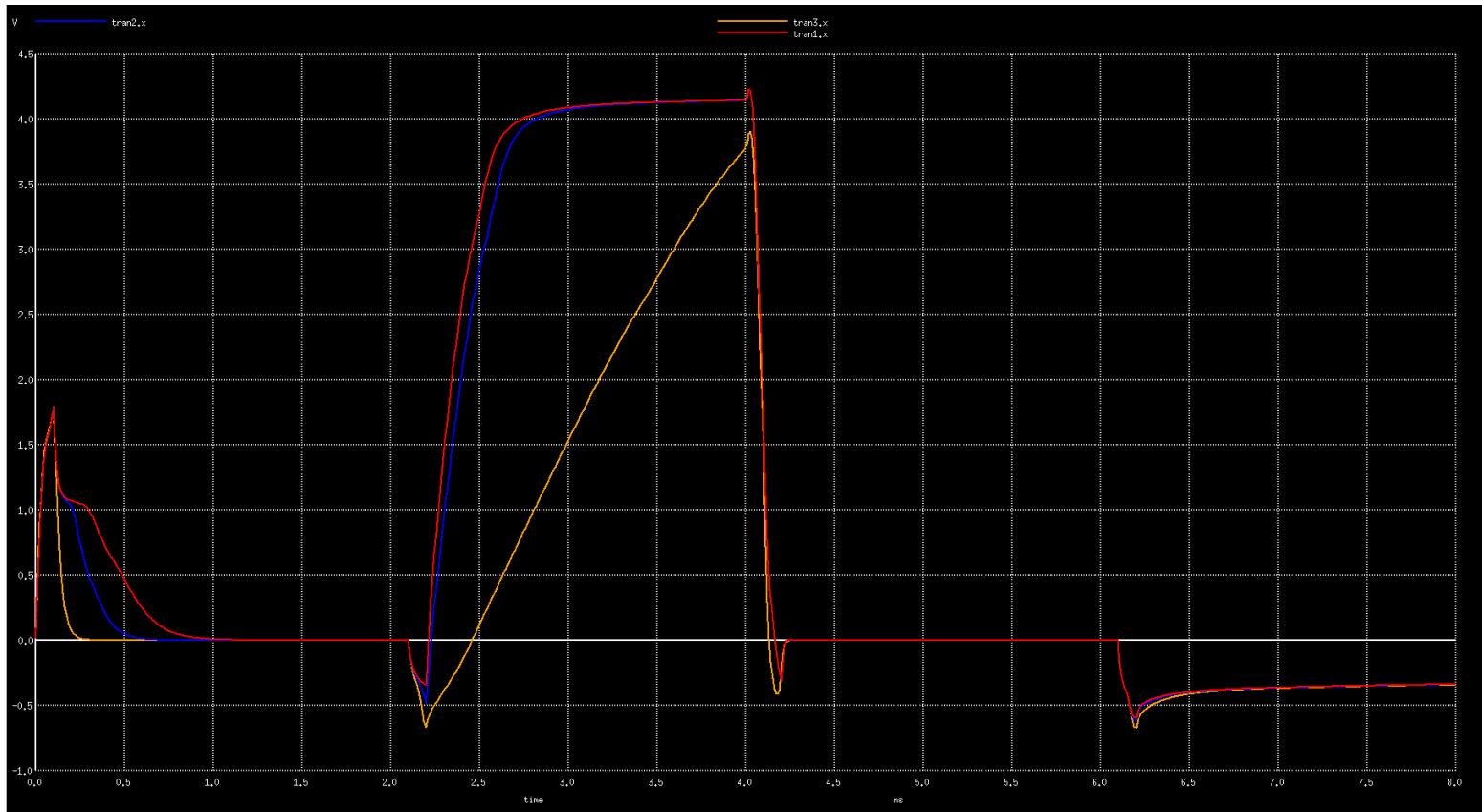
*Pull up network
m2 vdd a y vdd cmosp w=2.5u l=1u
m3 vdd b y vdd cmosp w=2.5u l=1u

*inverter
m4 out y 0 0 cmosn w=1u l=1u
m5 vdd y out vdd cmosp w=2.5u l=1u
v_dd vdd 0 5
v_a a 0 5 pulse(0 5 0 0.1n 0.1n 4n 8n)
v_b b 0 5 pulse(0 5 0 0.1n 0.1n 2n 4n)
*Transfer function and transient response on varying WIDTH of both the NMOS
.control
foreach wid 1u 2u 20u
alter m0 w=$wid
alter m1 w=$wid
tran 0.01n 8ns
end
alter m0 w=2u
alter m1 w=2u
.endc

.control
plot tran1.a tran1.b tran1.out tran2.out tran3.out
plot tran1.v_dd#branch*(-vdd) tran2.v_dd#branch*(-vdd) tran3.v_dd#branch*(-vdd)
tran1.x tran2.x tran3.x
.endc

```



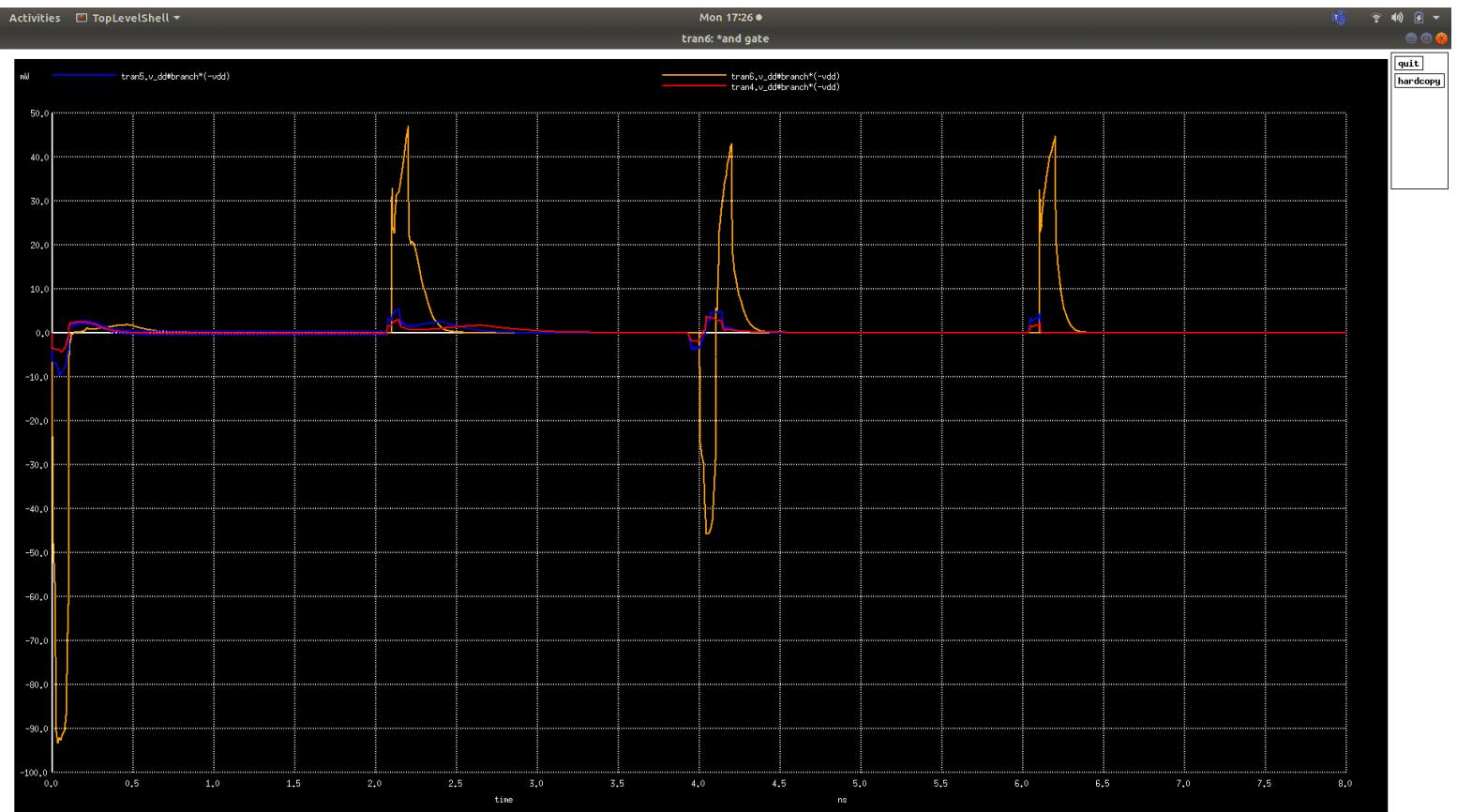
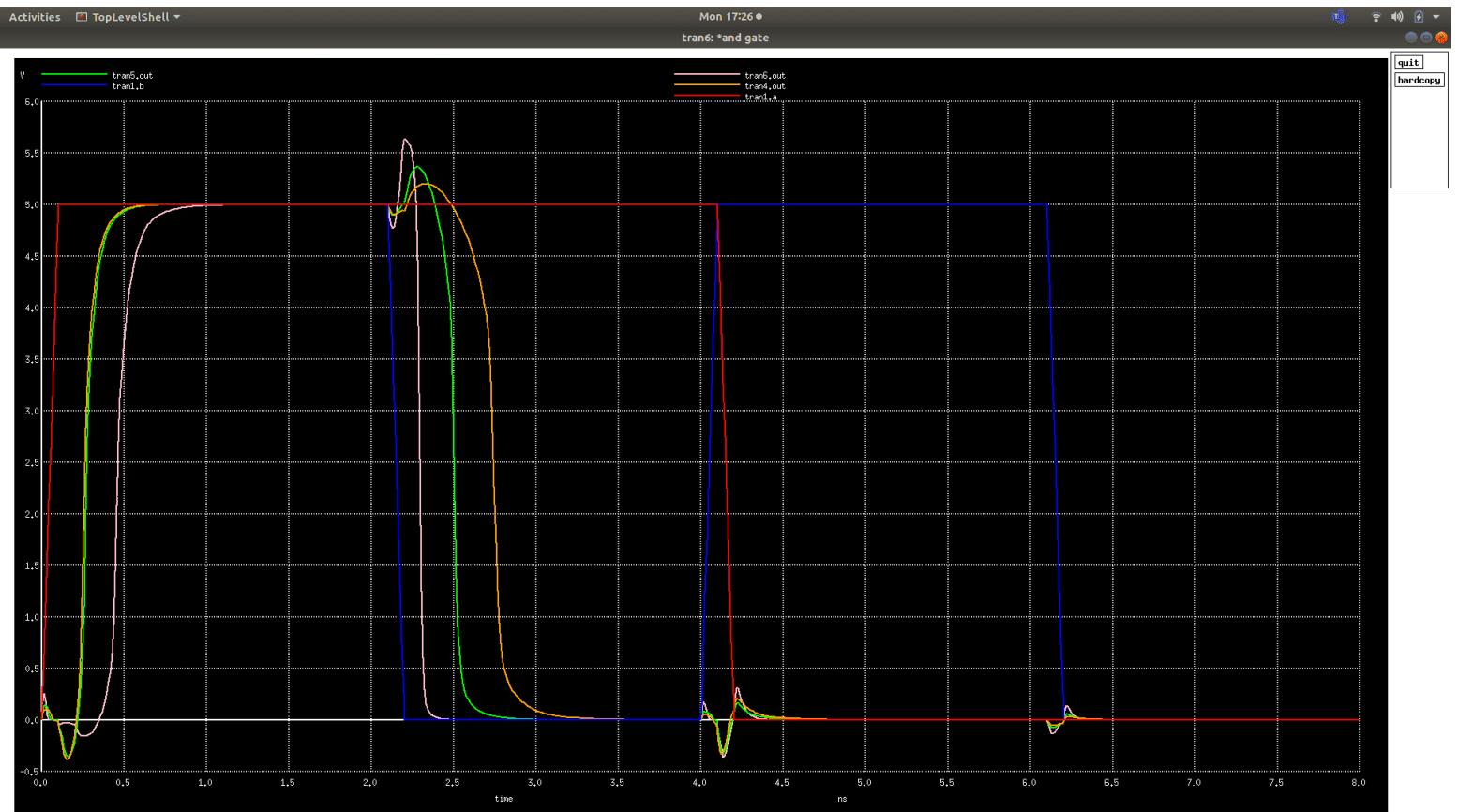


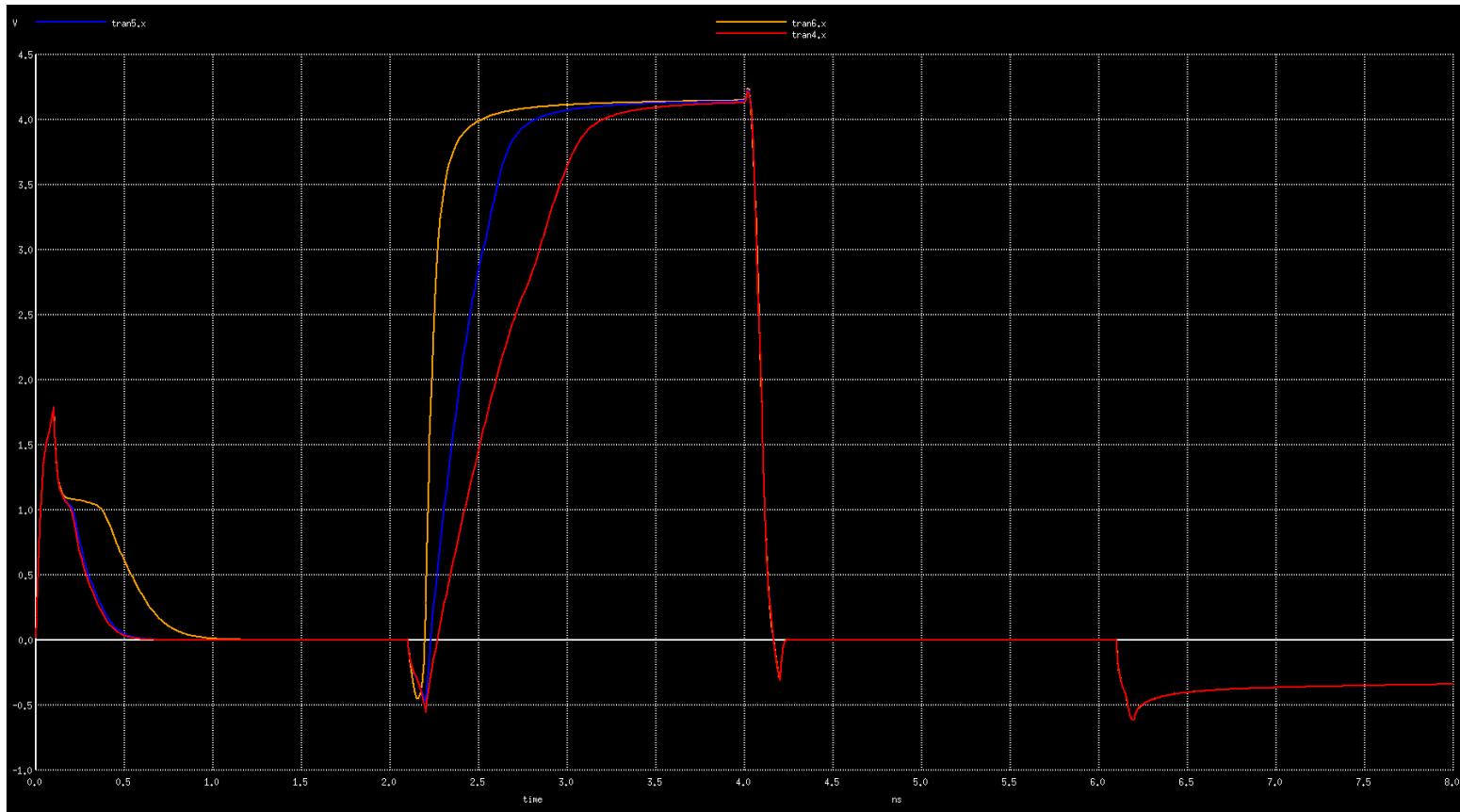
These are the results obtained when we vary the **width of the bottom Mosfets**, as we increase the width-the noise margin decreases and those not in the range do not act as an gate, the rise time decrease the fall time increases, and the power consumed increases as the resistance decreases and the current increases the energy consumed also increase, and power is consumed in steady state due to sub threshold current. The third graph is the one plot of the node x voltage for various widths.

### Varying the Width of Both the PMOS:-

```
*Transfer function and transient response on varying WIDTH of both the PMOS
.control
foreach wid 1.25u 2.5u 25u
alter m2 w=$wid
alter m3 w=$wid
tran 0.01n 8ns
end
alter m2 w=2.5u
alter m3 w=2.5u
.endc

.control
plot tran1.a tran1.b tran4.out tran5.out tran6.out
plot tran4.v_dd#branch*(-vdd) tran5.v_dd#branch*(-vdd) tran6.v_dd#branch*(-vdd)
tran4.x tran5.x tran6.x
.endc
```



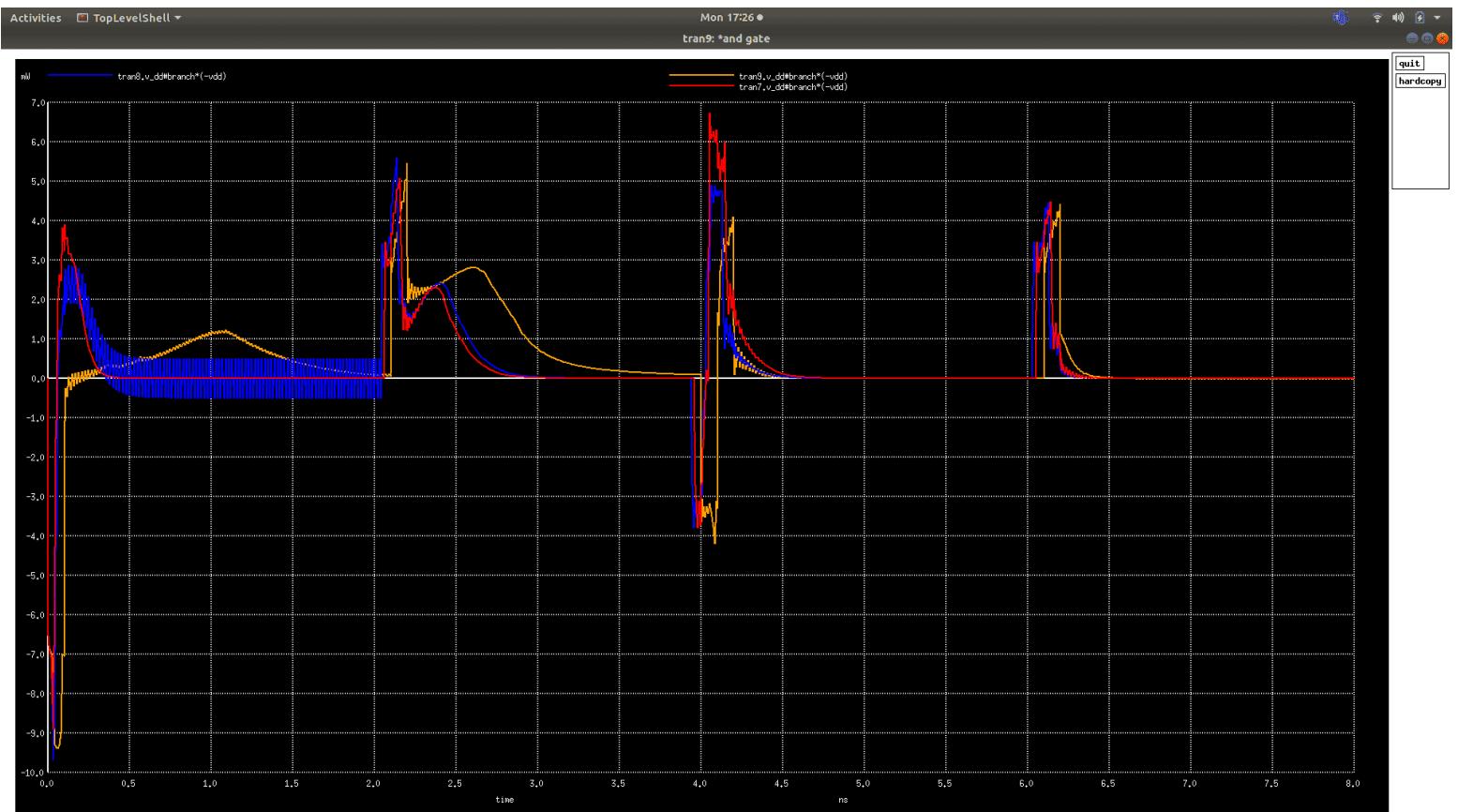
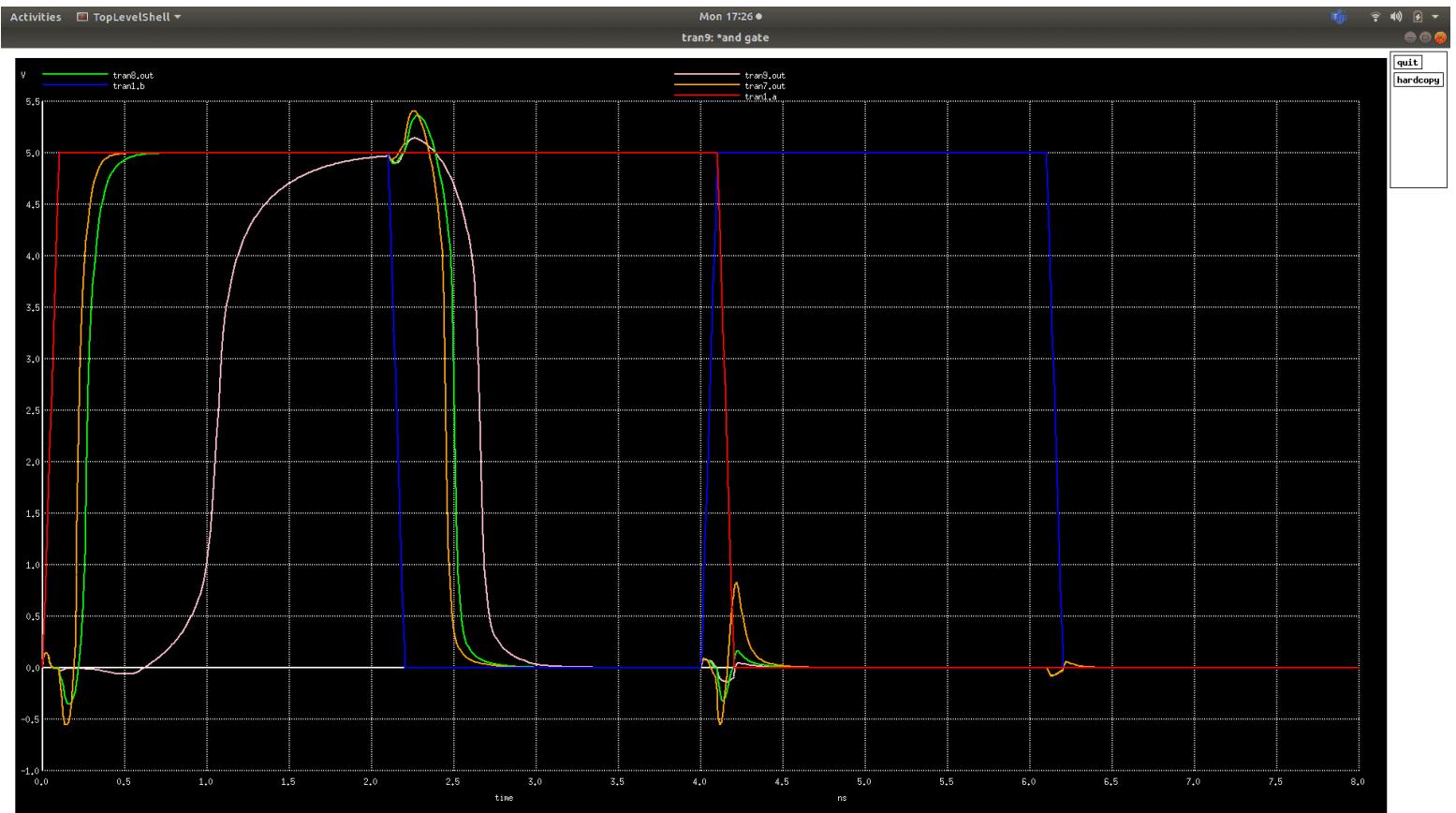


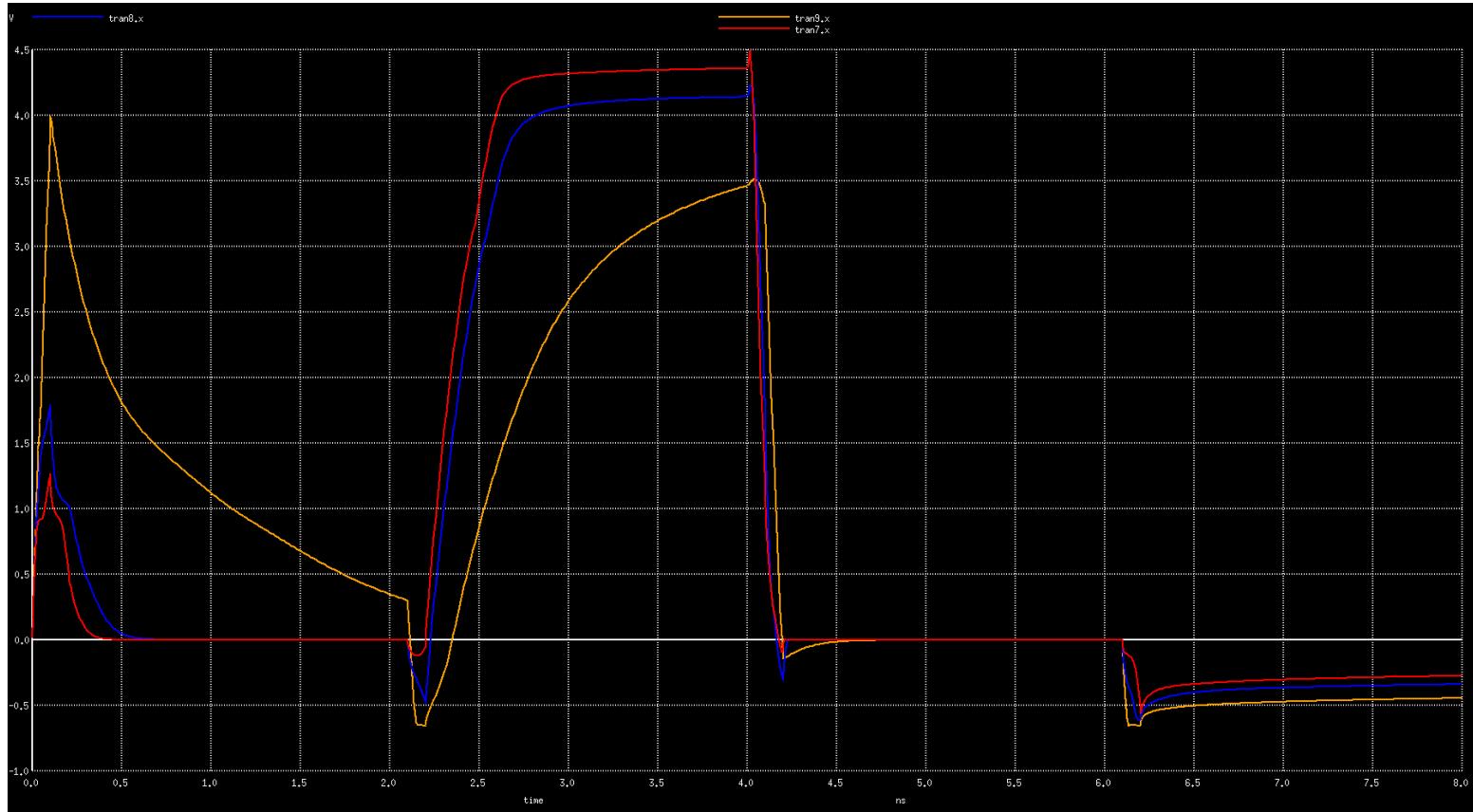
These are the results obtained when we vary the **width of the Top Mosfets** as we increase the width-the noise margin decreases and those not in the range do not act as an gate,, Looking at second graph the rise time increases, but fall time decreases, Looking at the third graph the power consumed increases as the resistance decreases and the current increases the energy consumed also increase, and power is consumed in steady state due to sub threshold current. The third graph is the node X voltage for various width of PMOS

### Varying the Length of Both the NMOS:-

```
*Transfer function and transient response on varying LENGTH of both the NMOS
.control
foreach len 0.5u 1u 5u
alter m0 l=$len
alter m1 l=$len
tran 0.01n 8ns
end
alter m0 l=1u
alter m1 l=1u
.endc

.control
plot tran1.a tran1.b tran7.out tran8.out tran9.out
plot tran7.v_dd#branch*(-vdd) tran8.v_dd#branch*(-vdd) tran9.v_dd#branch*(-vdd)
tran7.x tran8.x tran9.x
.endc
```



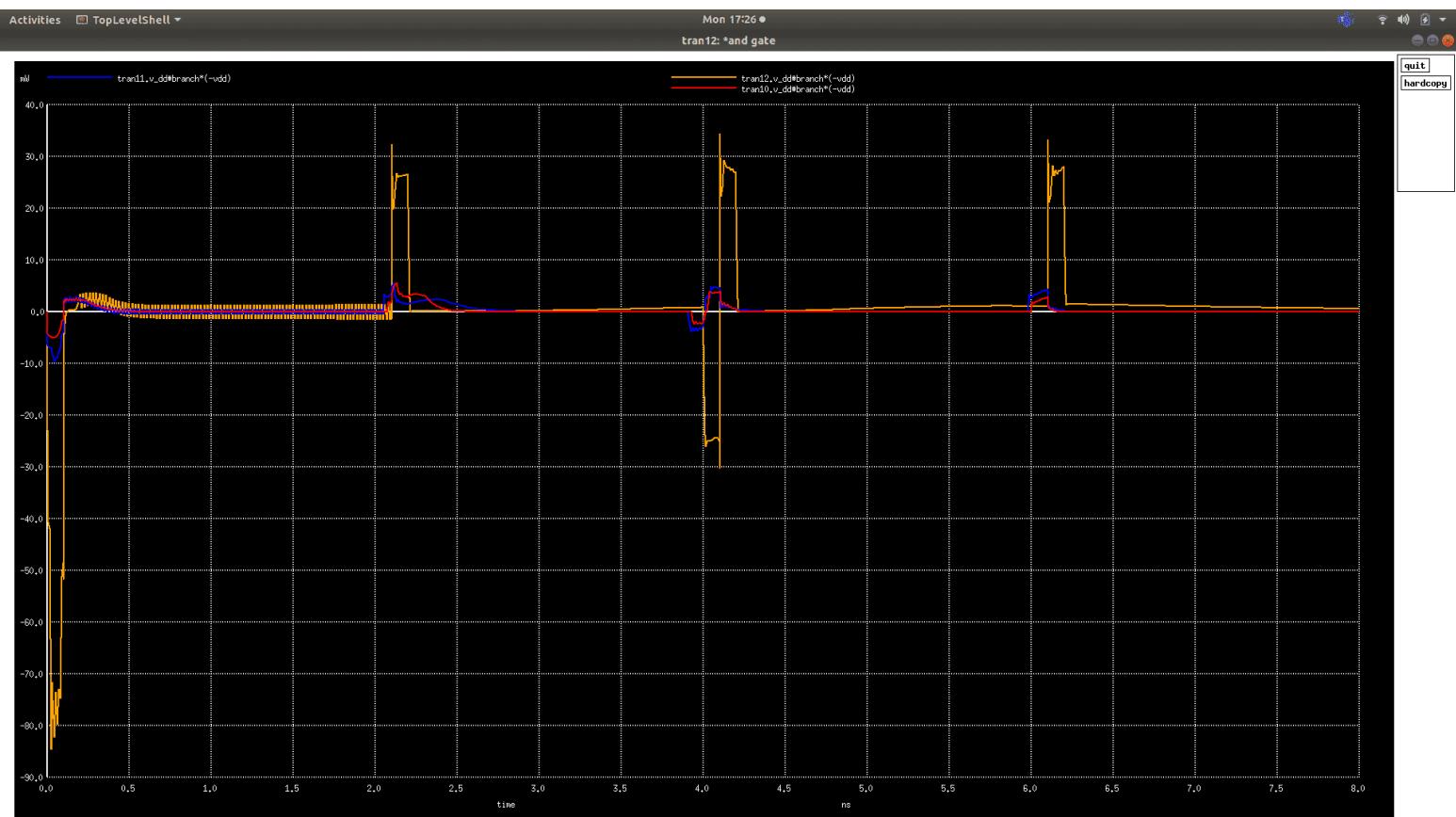
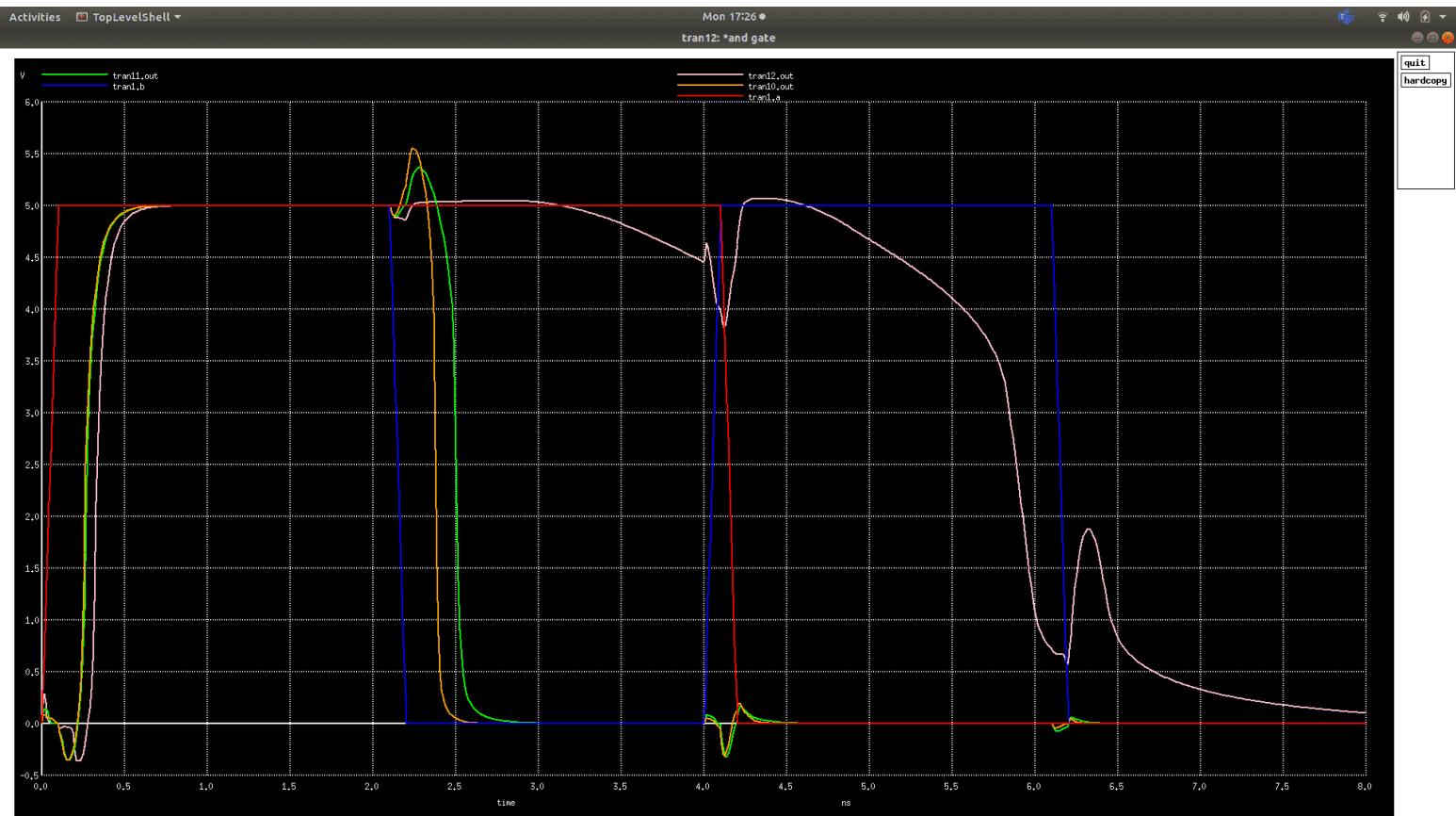


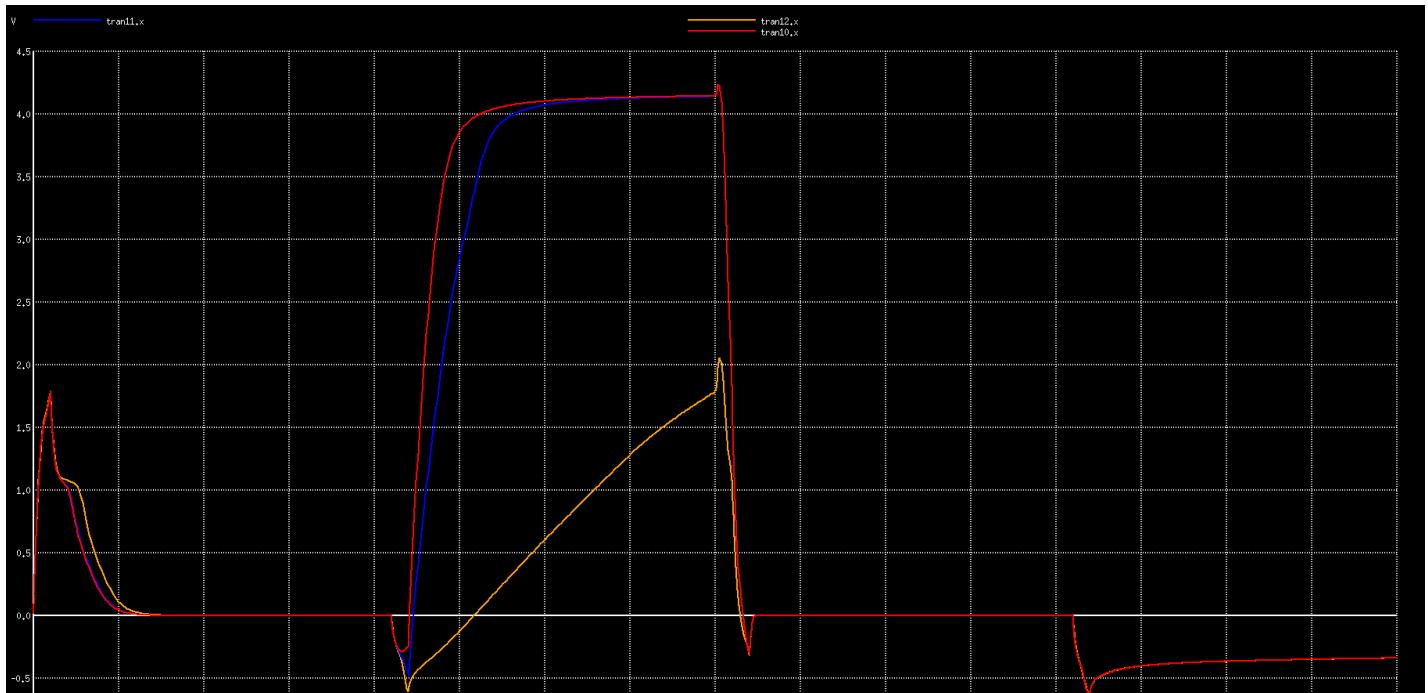
These are the results obtained when we vary the **length of the bottom Mosfets** as we increase the length-the noise margin increases and those not in the range do not act as an gate, Looking at second graph the rise time increase, also fall time increases, Looking at the third graph the power consumed increases, and the amount of energy consumed is more, and power is consumed in steady state due to sub threshold current. The third graph is the node X voltage for various Lengths through the transient response.

### Varying the Length of Both the PMOS:-

```
*Transfer function and transient response on varying LENGTH of both the PMOS
.control
foreach len 0.5u 1u 10u
alter m2 l=$len
alter m3 l=$len
tran 0.01n 8ns
end
alter m2 l=1u
alter m3 l=1u
.endc

.control
plot tran1.a tran1.b tran10.out tran11.out tran12.out
plot tran10.v_dd#branch*(-vdd) tran11.v_dd#branch*(-vdd) tran12.v_dd#branch*(-vdd)
tran10.x tran11.x tran12.x
.endc
```



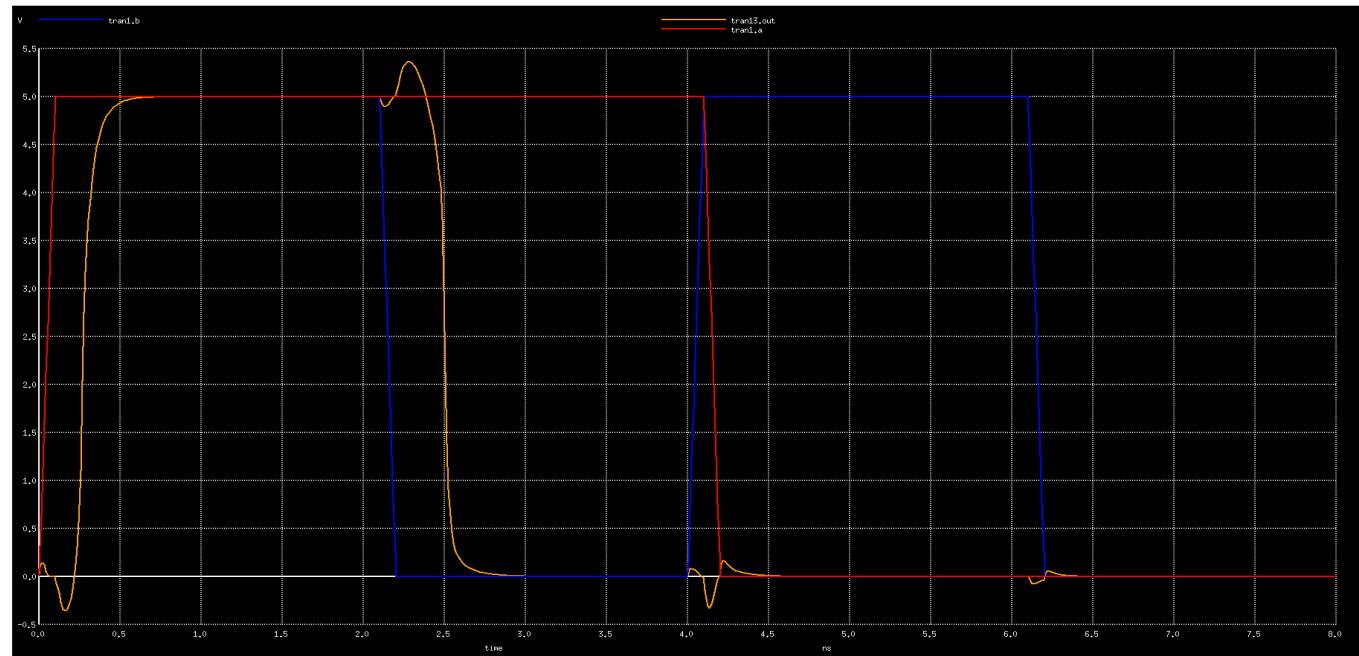


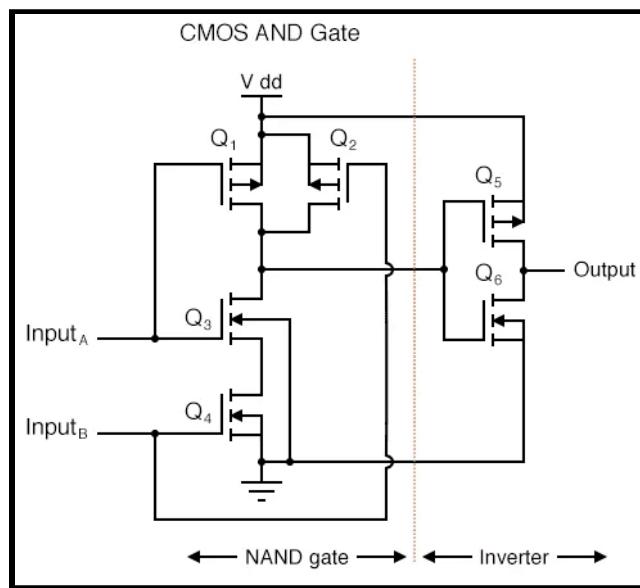
These are the results obtained when we vary the **length of the Top Mosfets** as we increase the length-the noise margin decreases and those not in the range do not act as an gate, Looking at second graph the rise time increase, also fall time increases, Looking at the third graph the power consumed increases as the resistance increase the energy consumed also increase, and power is consumed in steady state due to sub threshold current. The third graph is the node x voltages at various lengths and response time.

### Regular Response:-

```
.control
  tran 0.01n 8n
.endc

.control
  plot tran1.a tran1.b tran13.out
.endc
.end
```



**Or:****Circuit:-****Fig: Or Gate****Varying the Width of Both NMOS:-**

```
.include ./t14y_tsmc_025_level3.txt
```

\*Pull down network

```
m0 y a 0 0 cmosn l=1u w=1u
m1 y b 0 0 cmosn l=1u w=1u
```

\*Pull up network

```
m2 vdd a x vdd cmosp l=1u w=5u
m3 x b y vdd cmosp l=1u w=5u
```

\*Inverter

```
m4 out y 0 0 cmosn w=1u l=1u
m5 vdd y out vdd cmosp w=2.5u l=1u
```

v\_dd vdd 0 5

```
v_a a 0 5 pulse(0 5 0 0.1n 0.1n 4n 8n)
v_b b 0 5 pulse(0 5 0 0.1n 0.1n 2n 4n)
```

\*Transfer function and transient response on varying WIDTH of both the NMOS

.control

foreach wid 0.5u 1u 10u

alter m0 w=\$wid

alter m1 w=\$wid

tran 0.01n 8ns

end

alter m0 w=1u

alter m1 w=1u

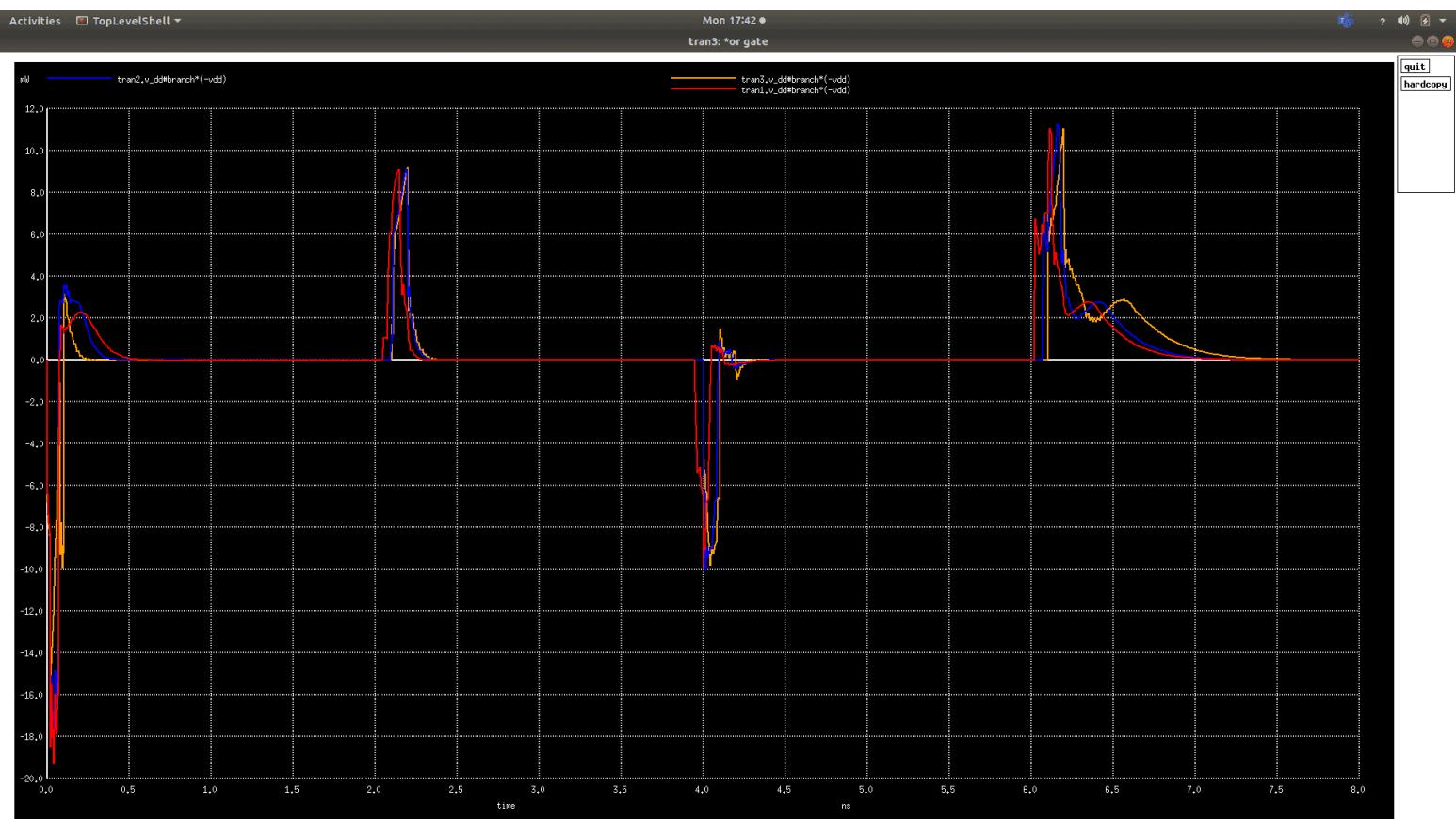
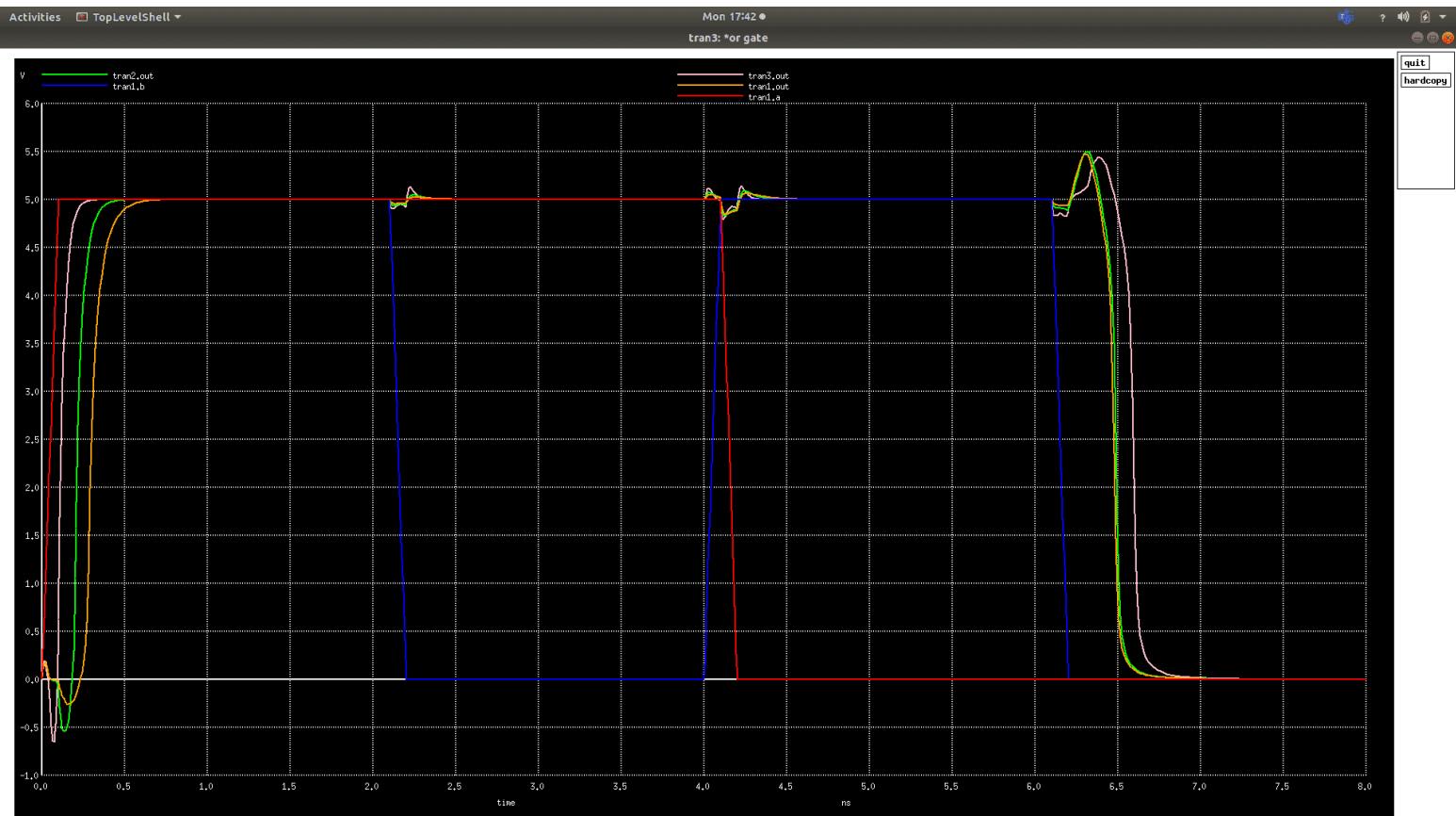
.endc

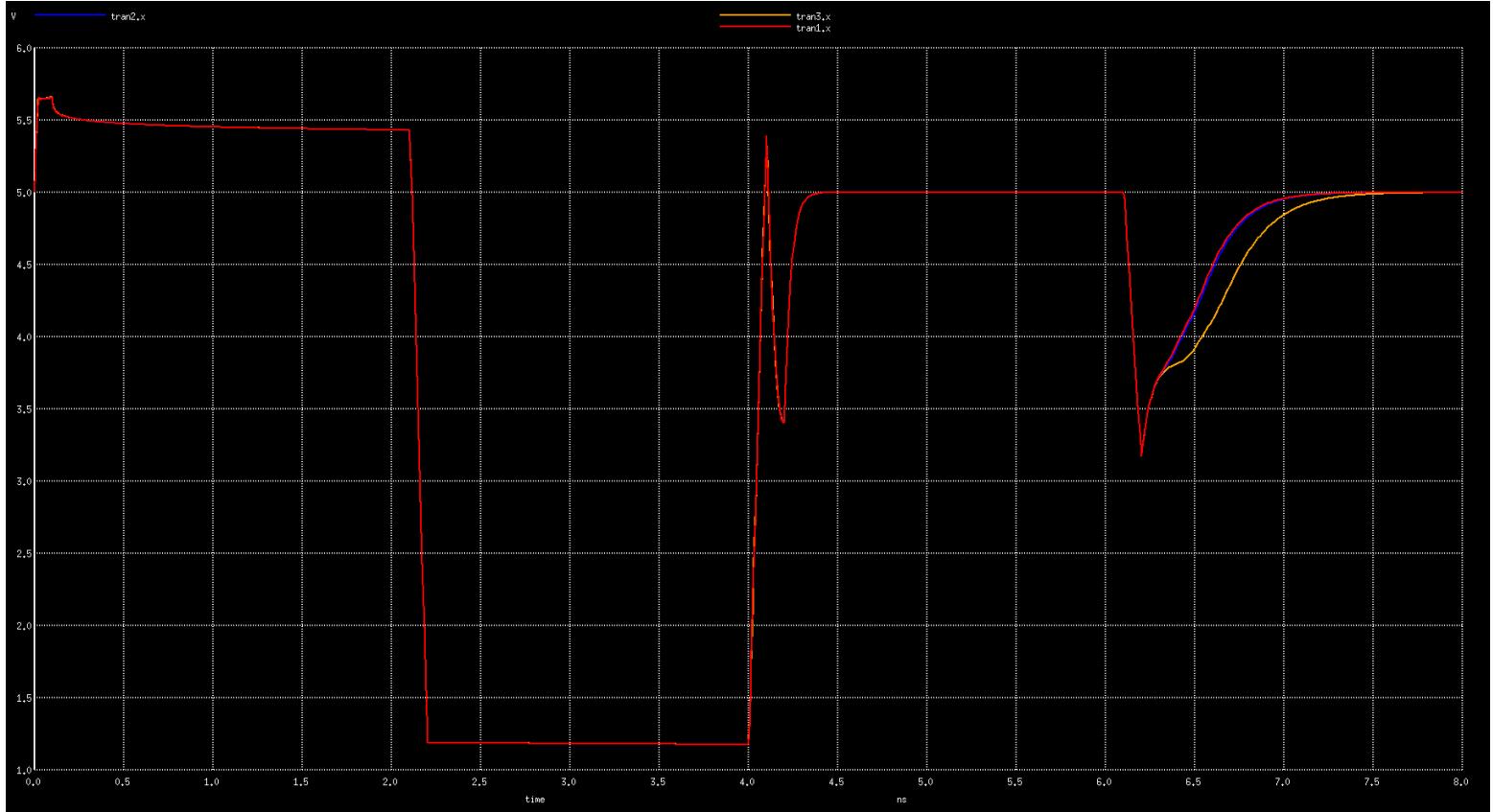
.control

```
plot tran1.a tran1.b tran1.out tran2.out tran3.out
```

```
plot tran1.v_dd#branch*(-vdd) tran2.v_dd#branch*(-vdd) tran3.v_dd#branch*(-vdd)
tran1.x tran2.x tran3.x
```

.endc



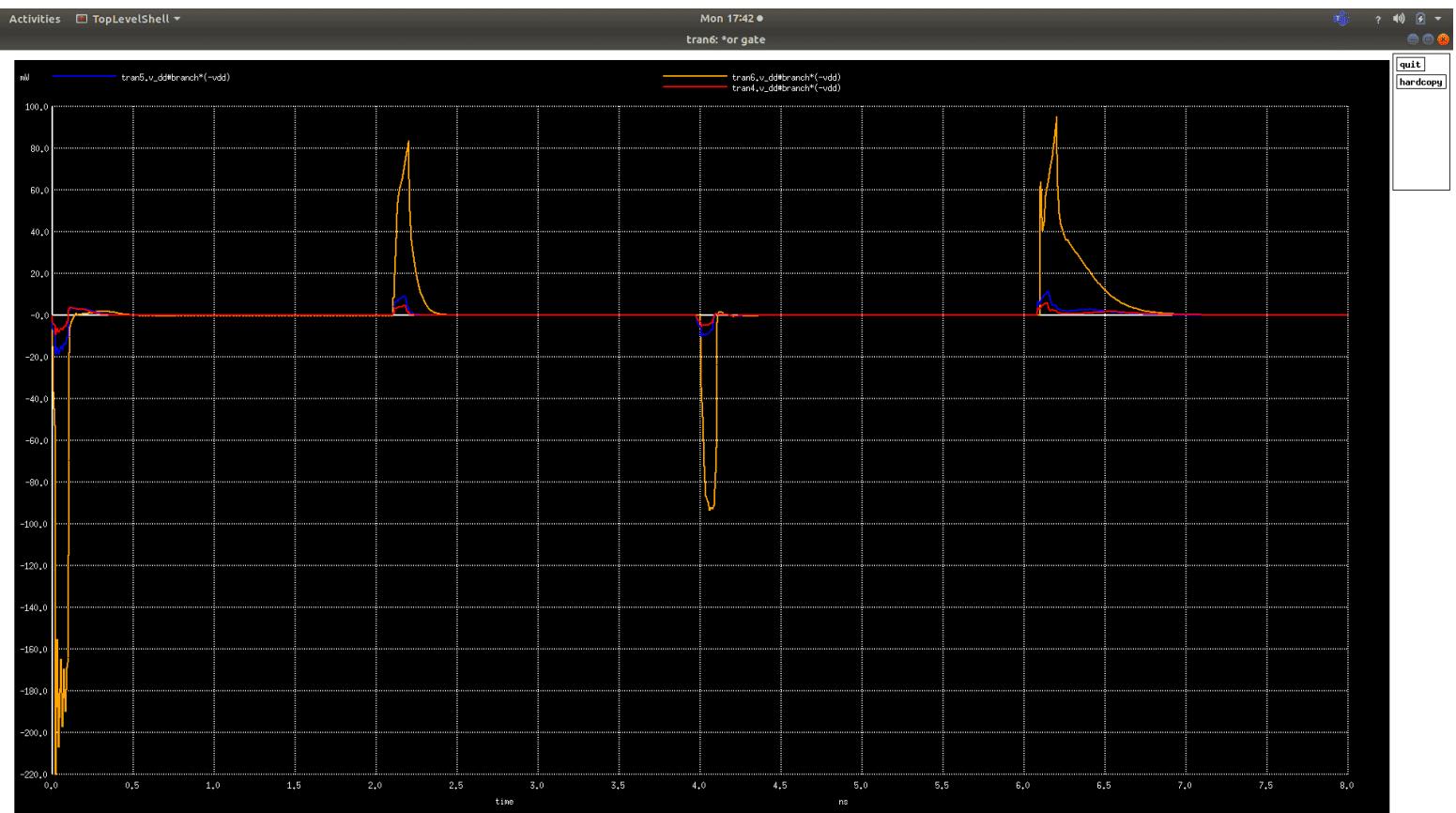
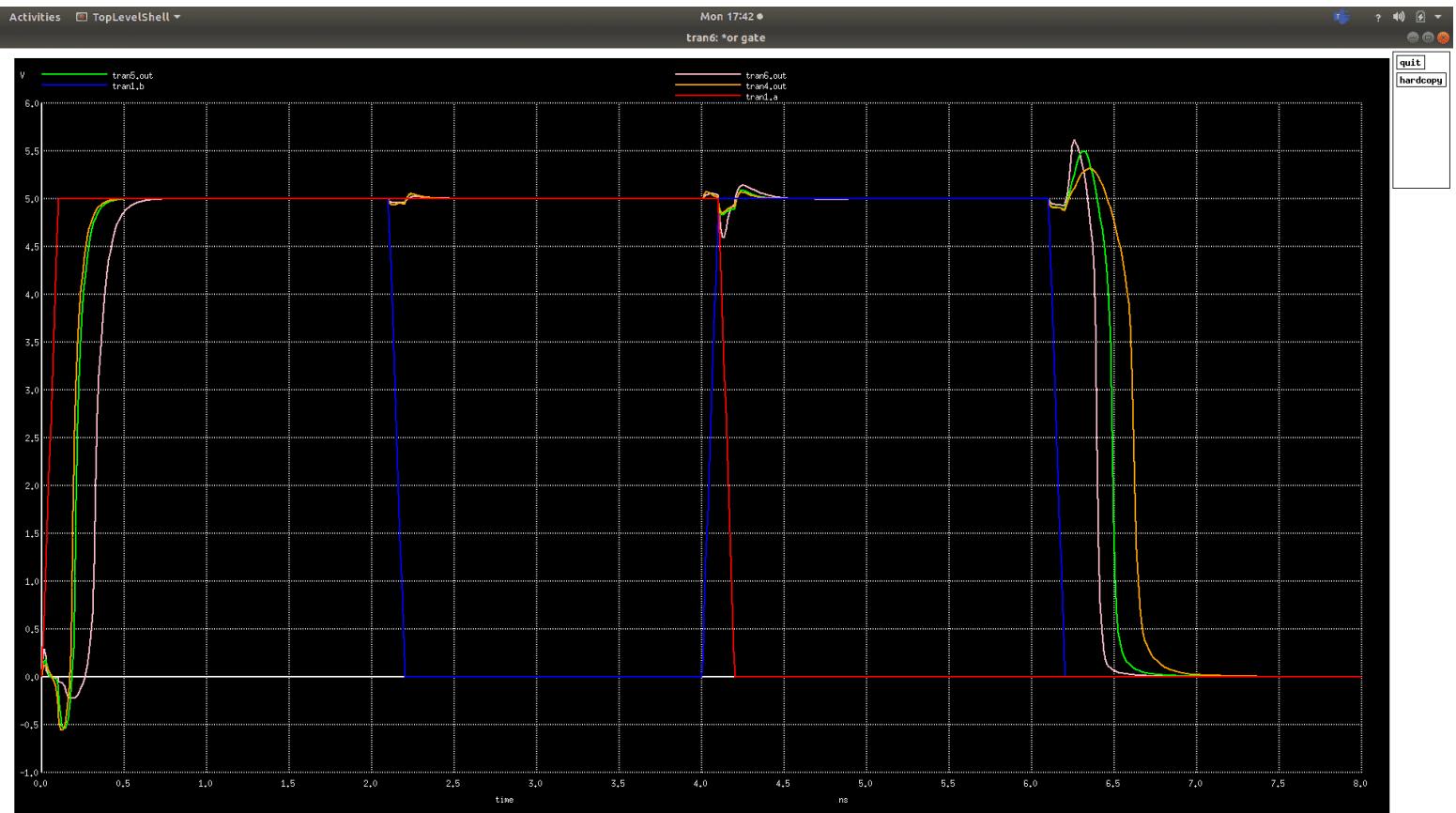


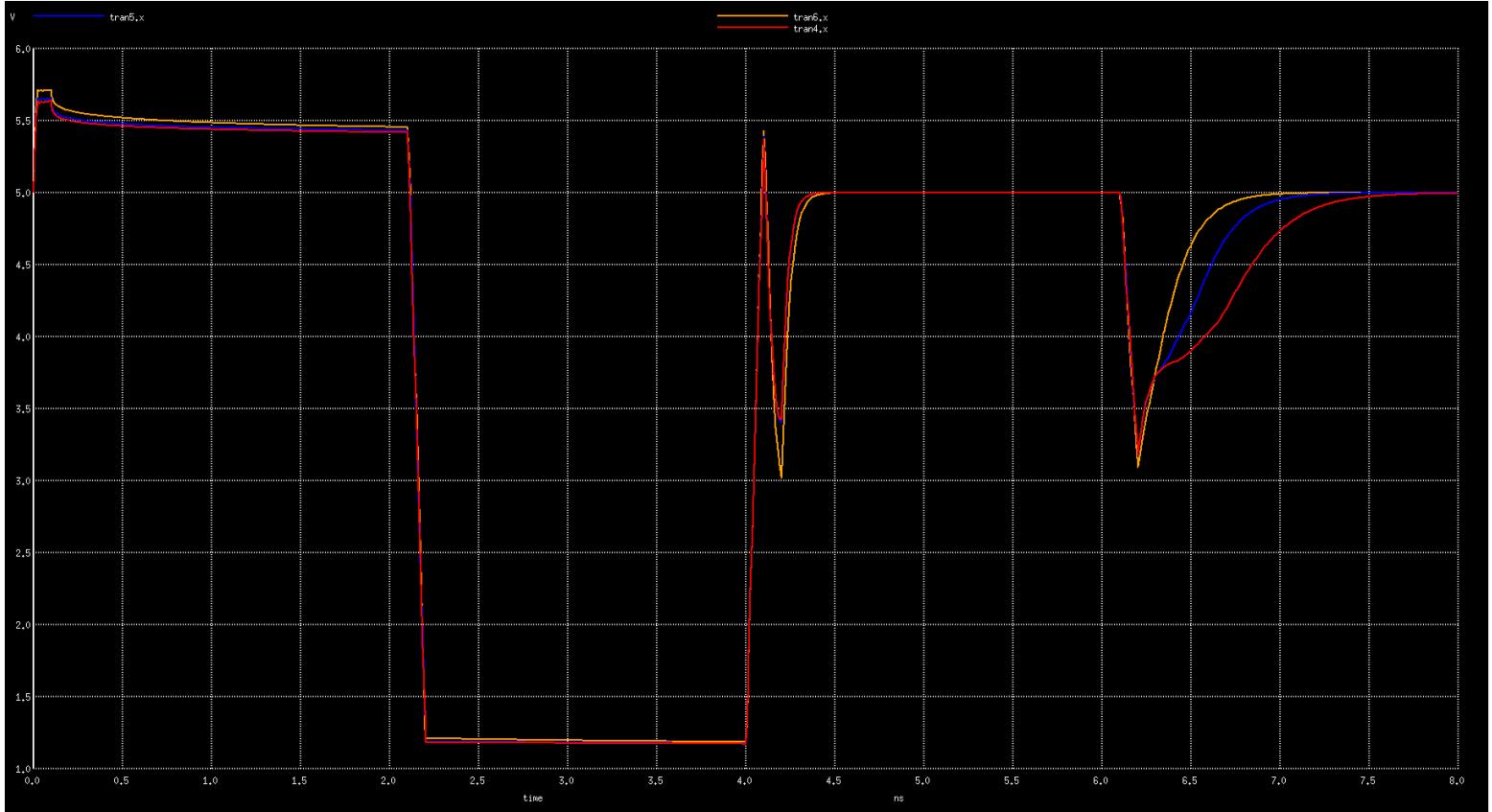
These are the results obtained when we vary the **width of the bottom Mosfets** as we increase the width-the noise margin decreases and those not in the range do not act as an gate,, the rise time decreases but fall time increases, and the power consumed increases as the resistance decreases and the current increases the energy consumed also increase, and power is consumed in steady state due to sub threshold current. The Third graph is the node X voltage during the analysis.The Third graph is the node X voltage during the analysis

### Varying the Width of Both the PMOS:-

```
*Transfer function and transient response on varying WIDTH of both the PMOS
.control
foreach wid 2.5u 5u 50u
alter m2 w=$wid
alter m3 w=$wid
tran 0.01n 8ns
end
alter m2 w=5u
alter m3 w=5u
.endc

.control
plot tran1.a tran1.b tran4.out tran5.out tran6.out
plot tran4.v_dd#branch*(-vdd) tran5.v_dd#branch*(-vdd) tran6.v_dd#branch*(-vdd)
tran4.x tran5.x tran6.x
.endc
```



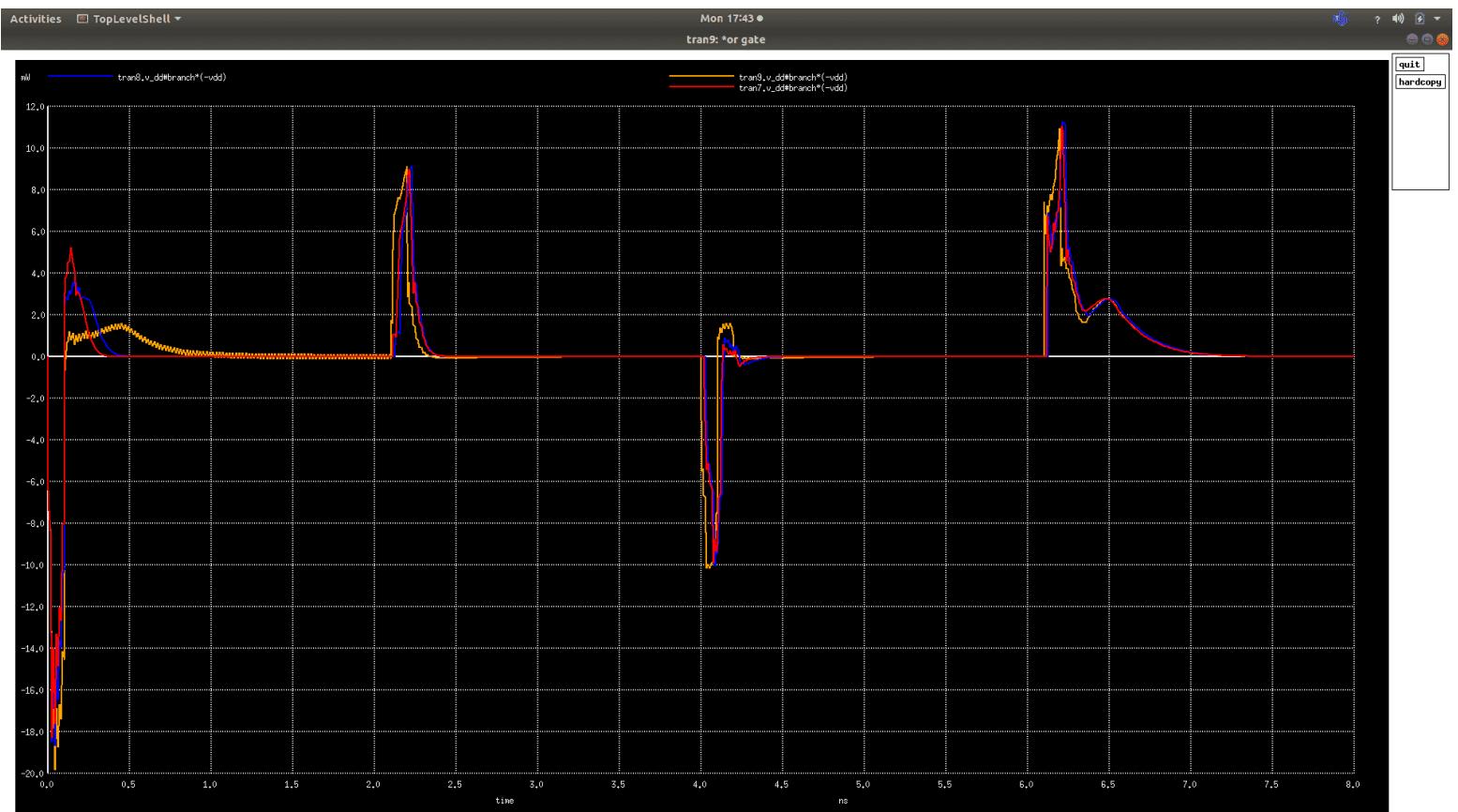
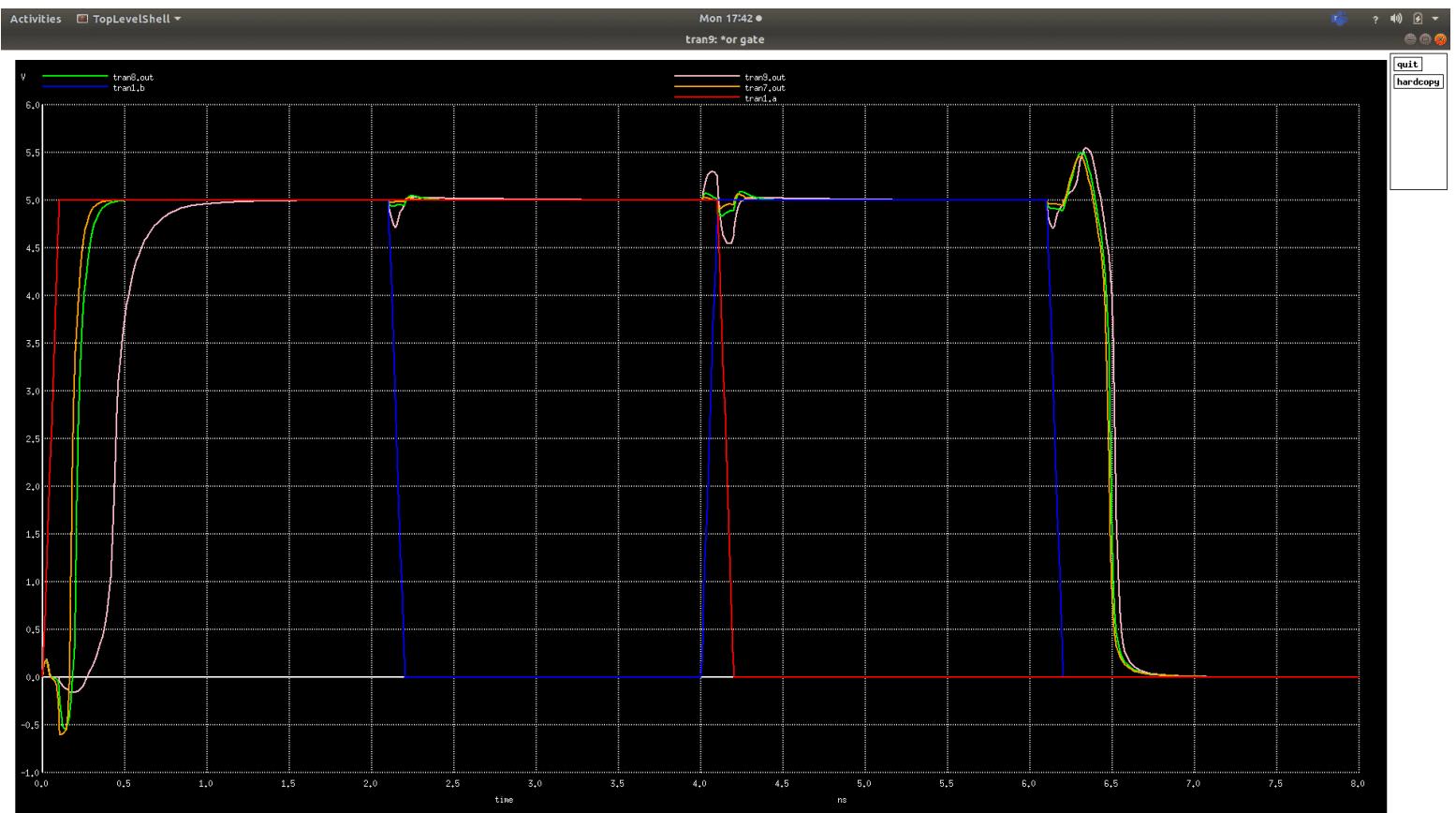


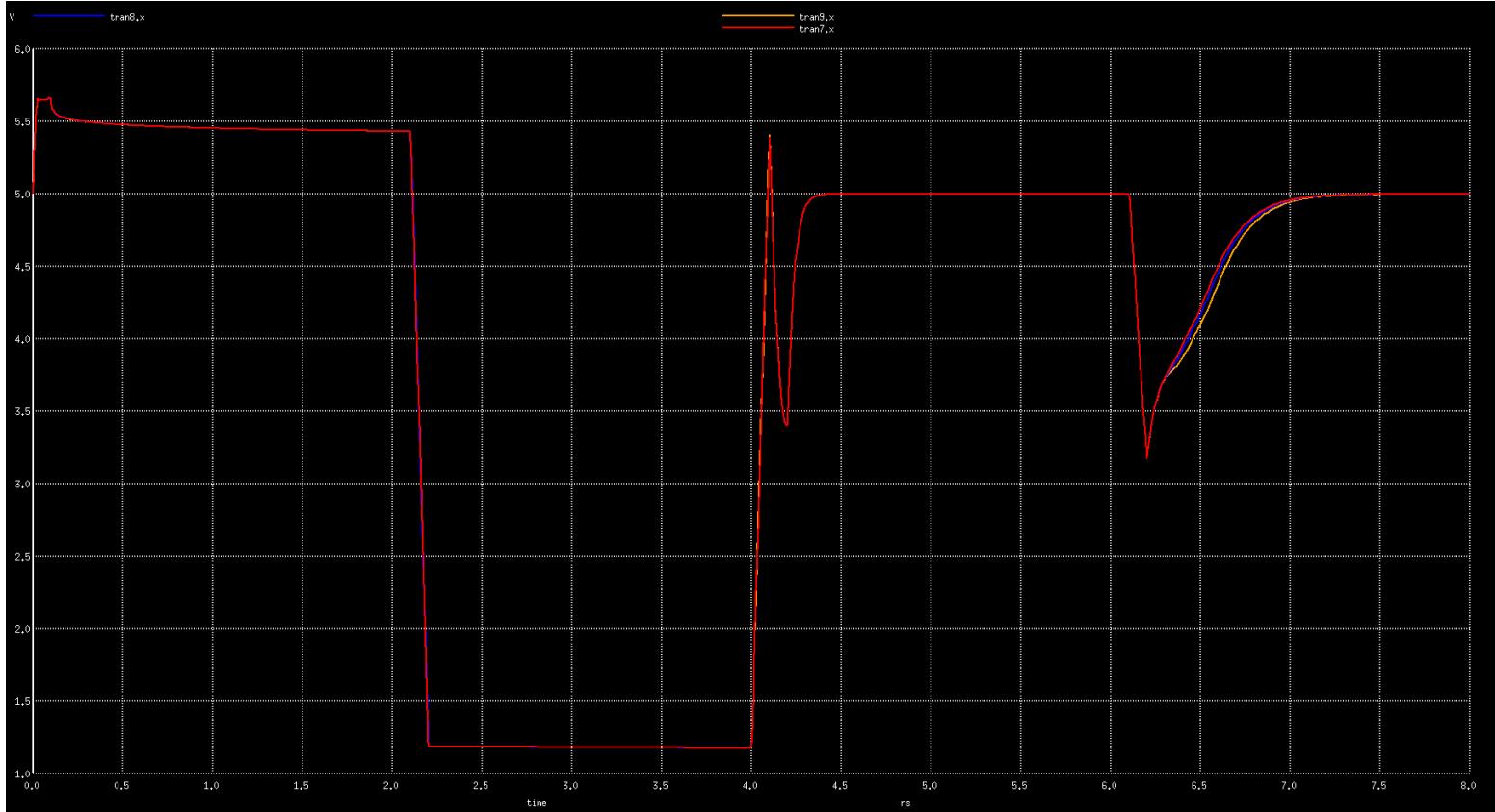
These are the results obtained when we vary the **width of the Top Mosfets** as we increase the width-the noise margin decreases and those not in the range do not act as an gate,, Looking at second graph the rise time increases, but fall time increases, Looking at the third graph the power consumed increases as the resistance decreases and the current increases the energy consumed also increase, and power is consumed in steady state due to sub threshold current. The Third graph is the node X voltage during the analysis

### Varying Length of Both NMOS:-

```
*Transfer function and transient response on varying LENGTH of both the NMOS
.control
foreach len 0.5u 1u 5u
alter m0 l=$len
alter m1 l=$len
tran 0.01n 8ns
end
alter m0 l=1u
alter m1 l=1u
.endc

.control
plot tran1.a tran1.b tran7.out tran8.out tran9.out
plot tran7.v_dd#branch*(-vdd) tran8.v_dd#branch*(-vdd) tran9.v_dd#branch*(-vdd)
tran7.x tran8.x tran9.x
.endc
```





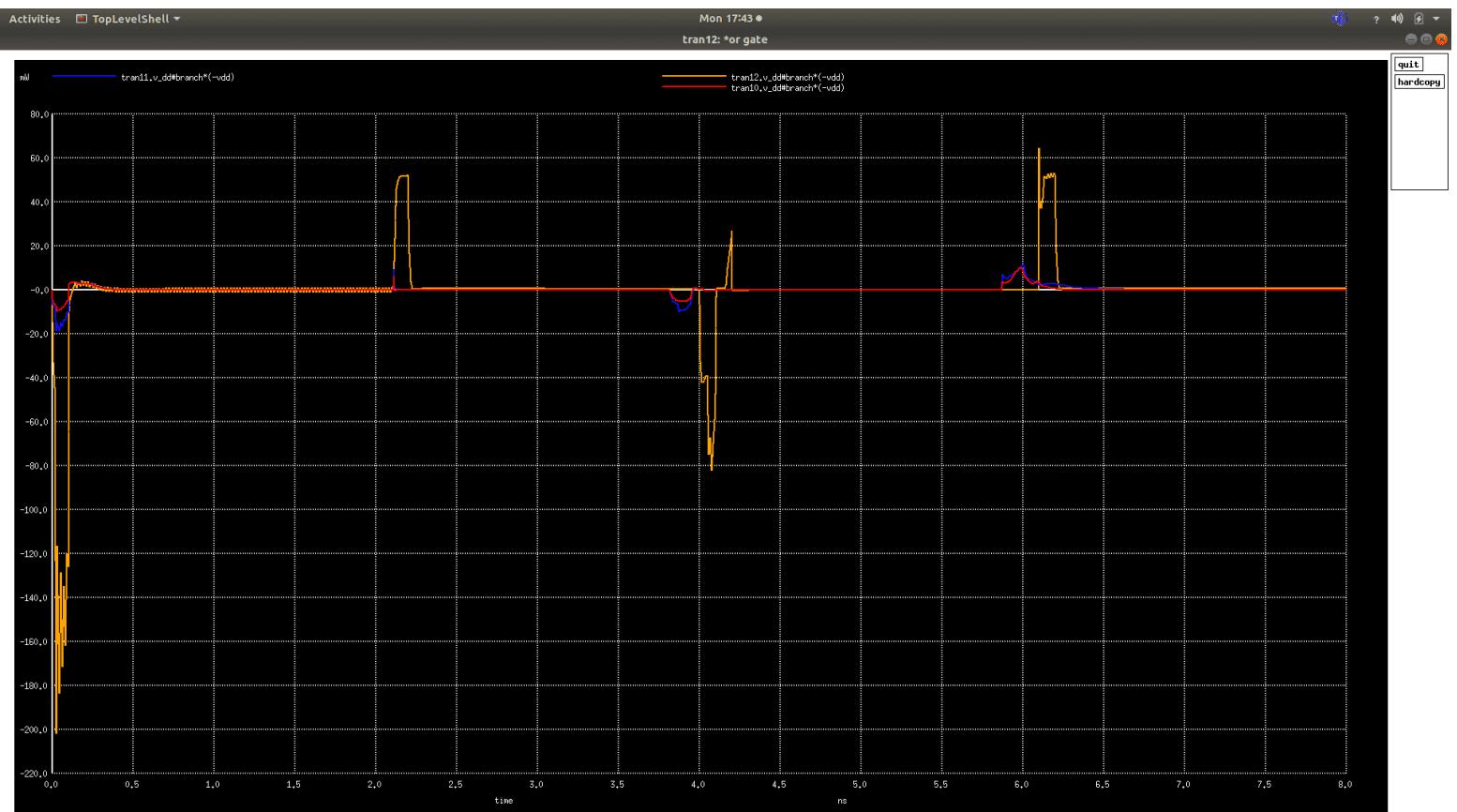
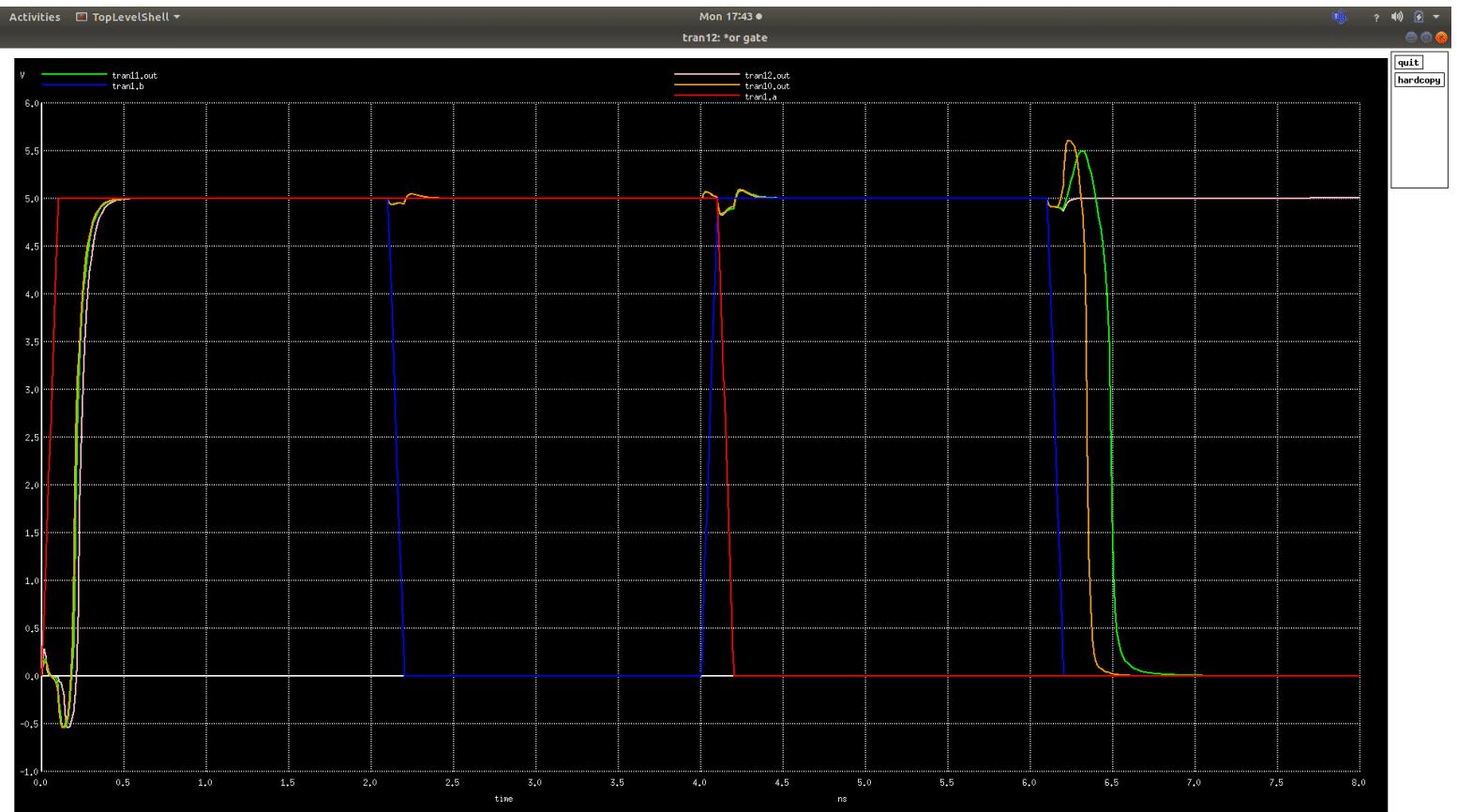
These are the results obtained when we vary the **length of the bottom Mosfets** as we increase the length-the noise margin increases and those not in the range do not act as an gate,, Looking at second graph the rise time increase, also fall time increases very slightly but if there is a huge increase in length then it will stop working as a gate, Looking at the third graph the power consumed increases, and the amount of energy consumed is more, and power is consumed in steady state due to sub threshold current. The Third graph is the node X voltage during the analysis.

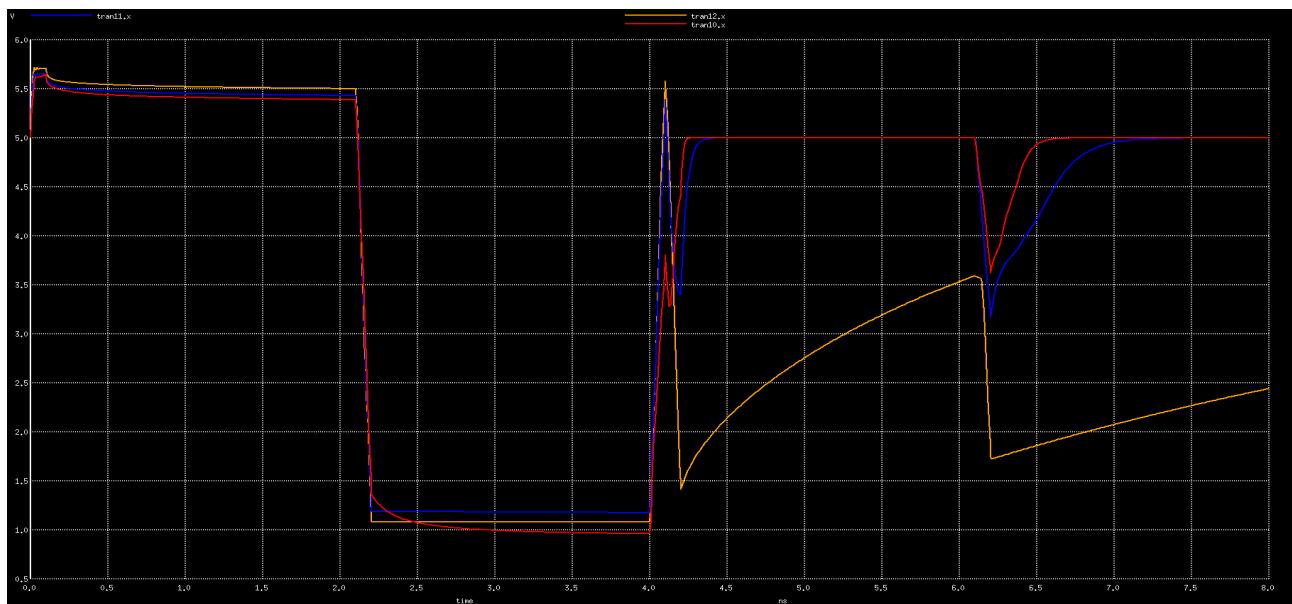
### Varying the Length of Both PMOS:-

Transfer function and transient response on varying LENGTH of both the PMOS

```
.control
foreach len 0.5u 1u 10u
alter m2 l=$len
alter m3 l=$len
tran 0.01n 8ns
end
alter m2 l=1u
alter m3 l=1u
.endc

.control
plot tran1.a tran1.b tran10.out tran11.out tran12.out
plot tran10.v_dd#branch*(-vdd) tran11.v_dd#branch*(-vdd) tran12.v_dd#branch*(-vdd)
tran10.x tran11.x tran12.x
.endc
```





These are the results obtained when we vary the **length of the Top Mosfets** as we increase the length-the noise margin decreases and those not in the range do not act as an gate, Looking at second graph the rise time increases, but fall time increases and stops working as a high length value, Looking at the third graph the power consumed increases as the resistance increase the energy consumed also increase, and power is consumed in steady state due to sub threshold current. The Third graph is the node X voltage during the analysis

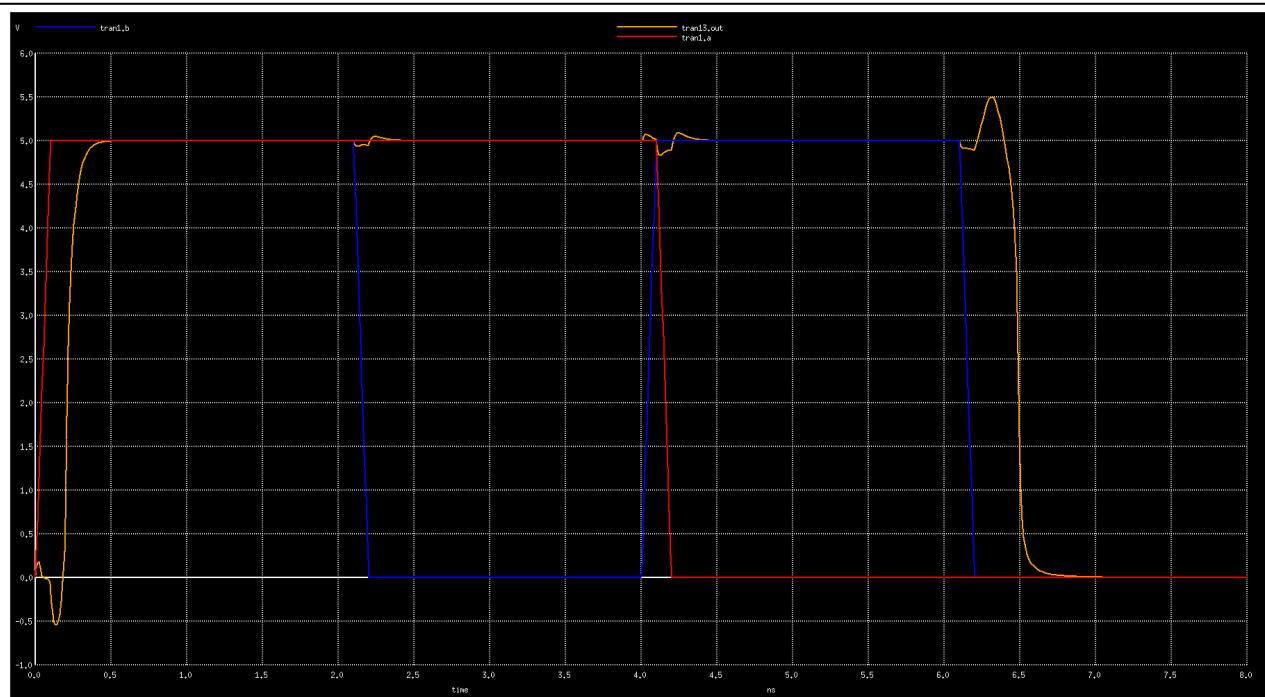
### Regular Response:-

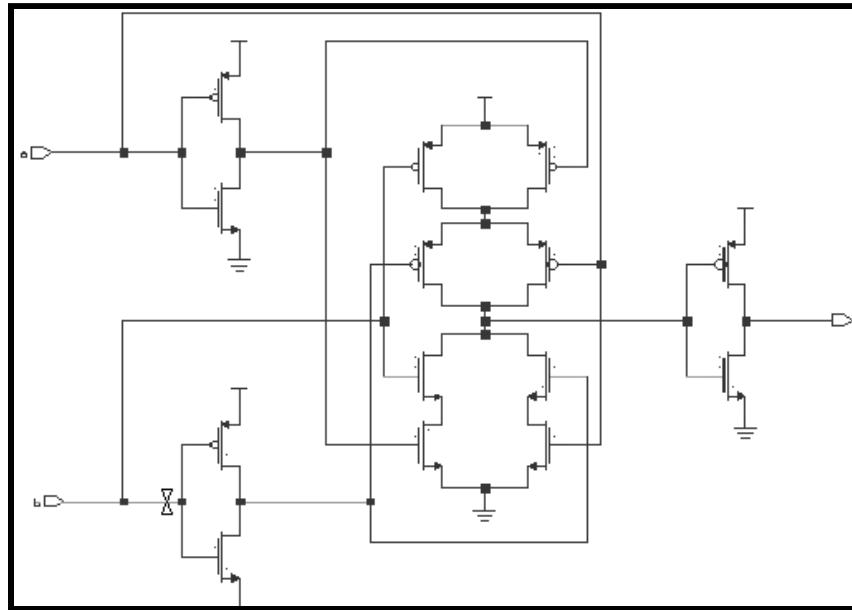
```

control
  tran 0.01n 8n
.endc

.control
  plot tran1.a tran1.b tran13.out
.endc
.end

```



**Xor:****Circuit:-****Fig: Xor Gate**

This one was split into 2 programs not like the previous ones, the varying the length and width were done in different programs

**Varying the Width of Both NMOS:-**

```
.include ./t14y_tsmc_025_level3.txt

*Input A inverter
m0 aneg a 0 0 cmosn w=1u l=1u
m1 aneg a vdd vdd cmosp w=2.5u l=1u

*Input B inverter
m2 bneg b 0 0 cmosn w=1u l=1u
m3 bneg b vdd vdd cmosp w=2.5u l=1u

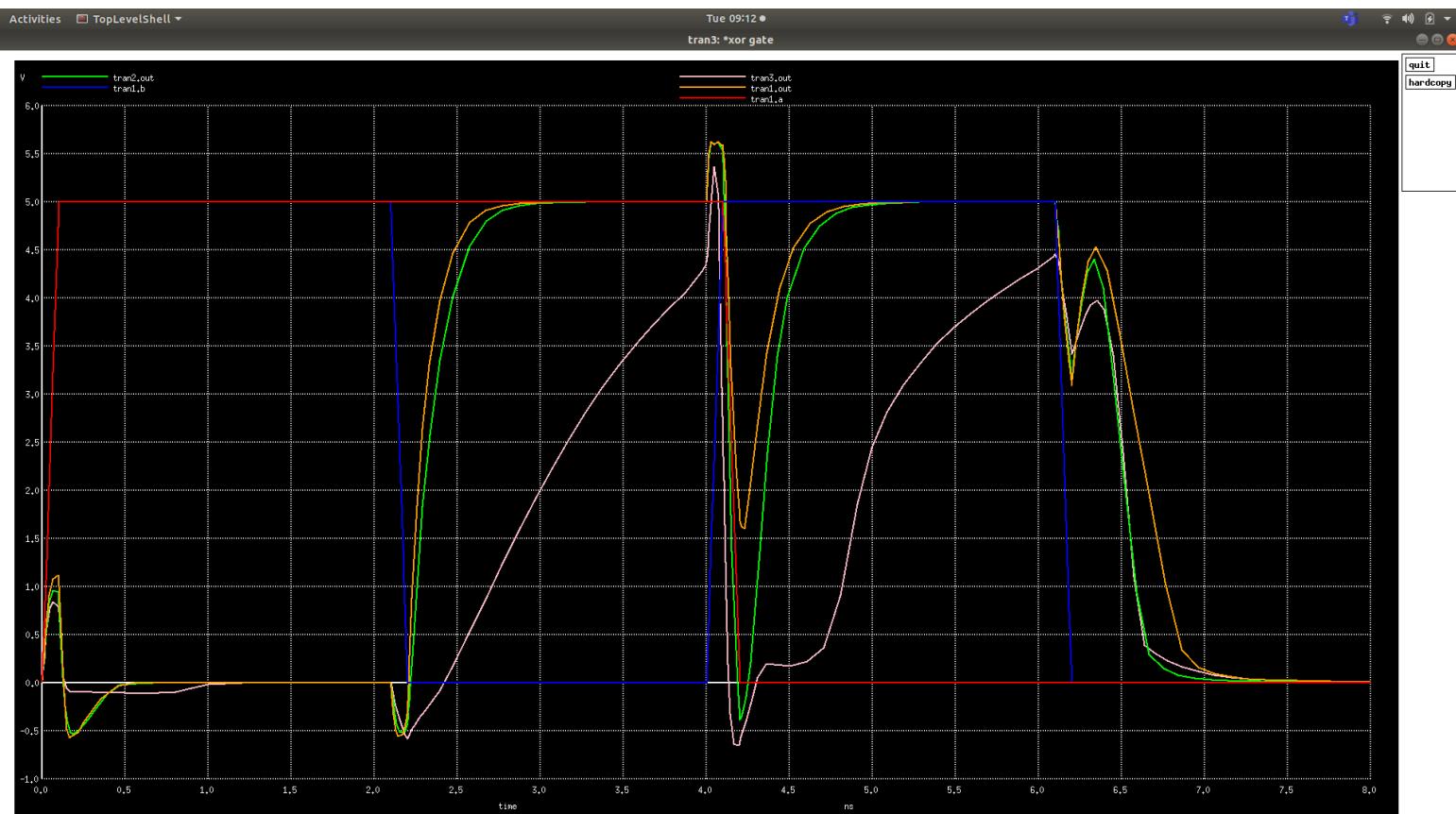
*Pull down network
m4 out a x1 0 cmosn w=1u l=1u
m5 out aneg x2 0 cmosn w=1u l=1u
m6 x1 b 0 0 cmosn w=1u l=1u
m7 x2 bneg 0 0 cmosn w=1u l=1u

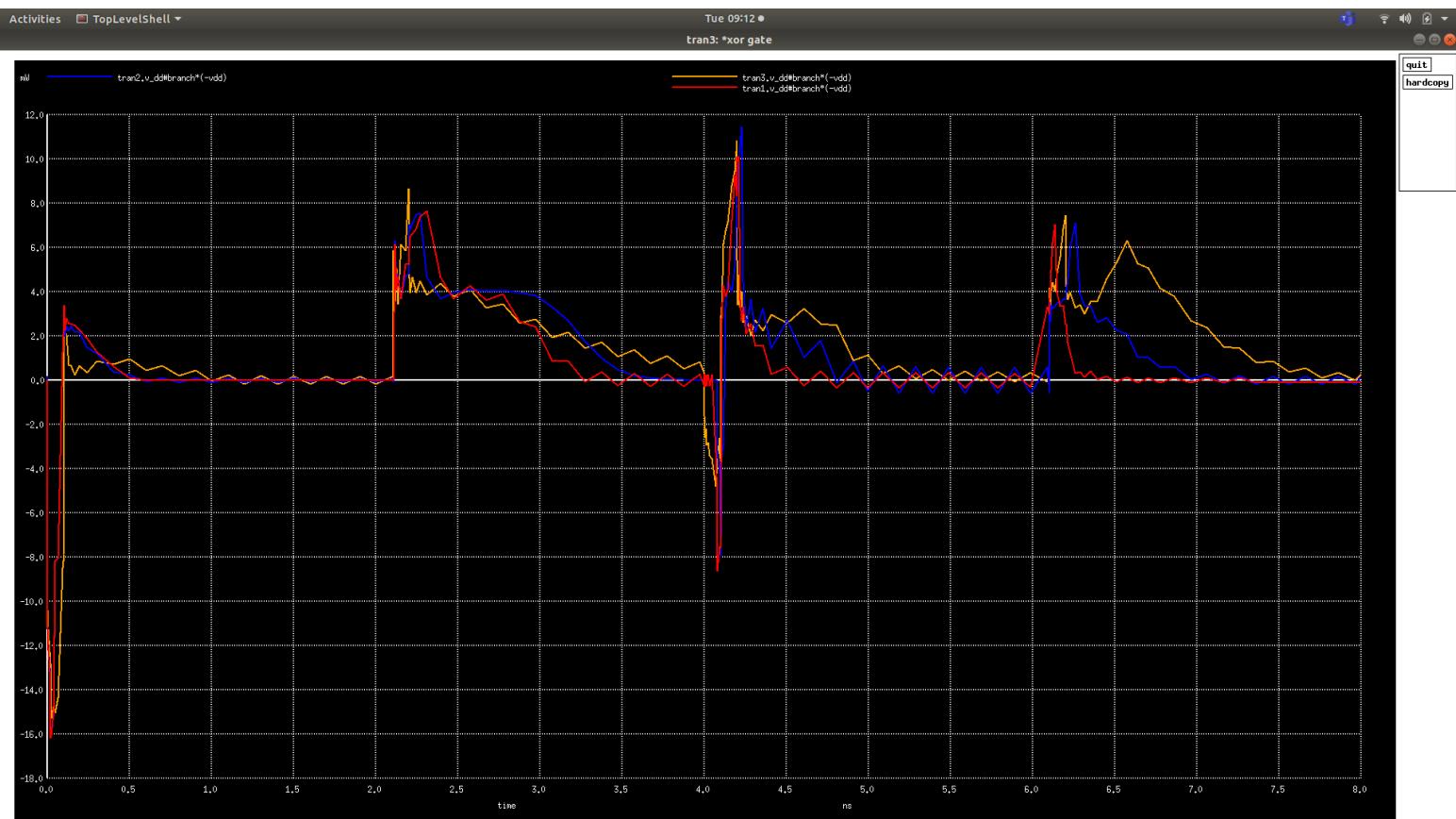
*Pull up network
m8 out b x3 vdd cmosp w=2.5u l=1u
m9 out bneg x4 vdd cmosp w=2.5u l=1u
m10 x3 aneg vdd vdd cmosp w=2.5u l=1u
m11 x4 a vdd vdd cmosp w=2.5u l=1u

v_dd vdd 0 5
v_a a 0 pulse(0 5 0 0.1n 0.1n 4n 8n)
v_b b 0 pulse(0 5 0 0.1n 0.1n 2n 4n)
```

```
*Transfer function and transient response on varying WIDTH of all the NMOS in PDN
.control
foreach wid 0.5u 1u 10u
alter m4 w=$wid
alter m5 w=$wid
alter m6 w=$wid
alter m7 w=$wid
tran 0.1n 8ns
end
alter m4 w=1u
alter m5 w=1u
alter m6 w=1u
alter m7 w=1u
.endc

.control
plot tran1.a tran1.b tran1.out tran2.out tran3.out
plot tran1.v_dd#branch*(-vdd) tran2.v_dd#branch*(-vdd) tran3.v_dd#branch*(-vdd)
.endc
```



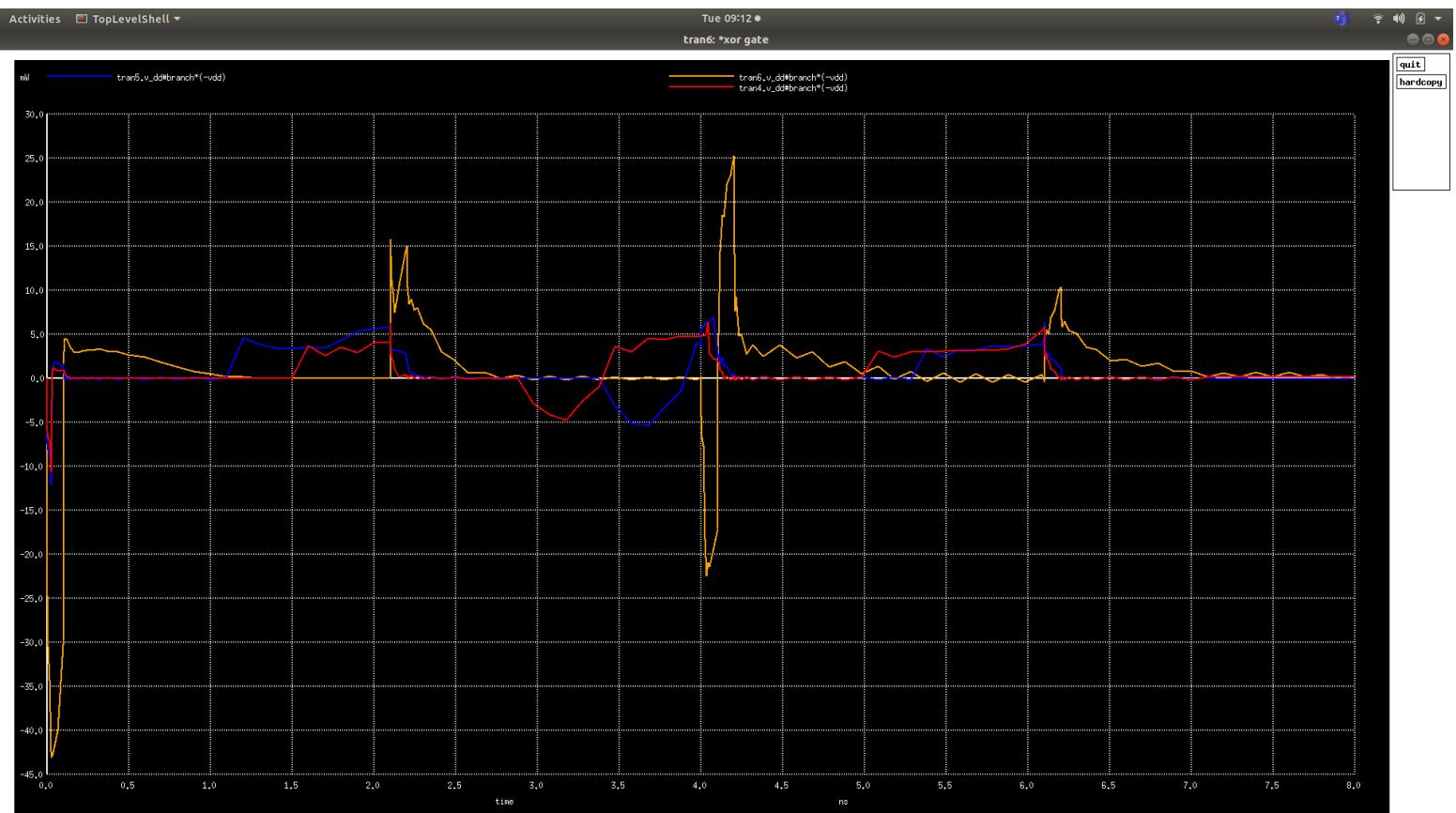
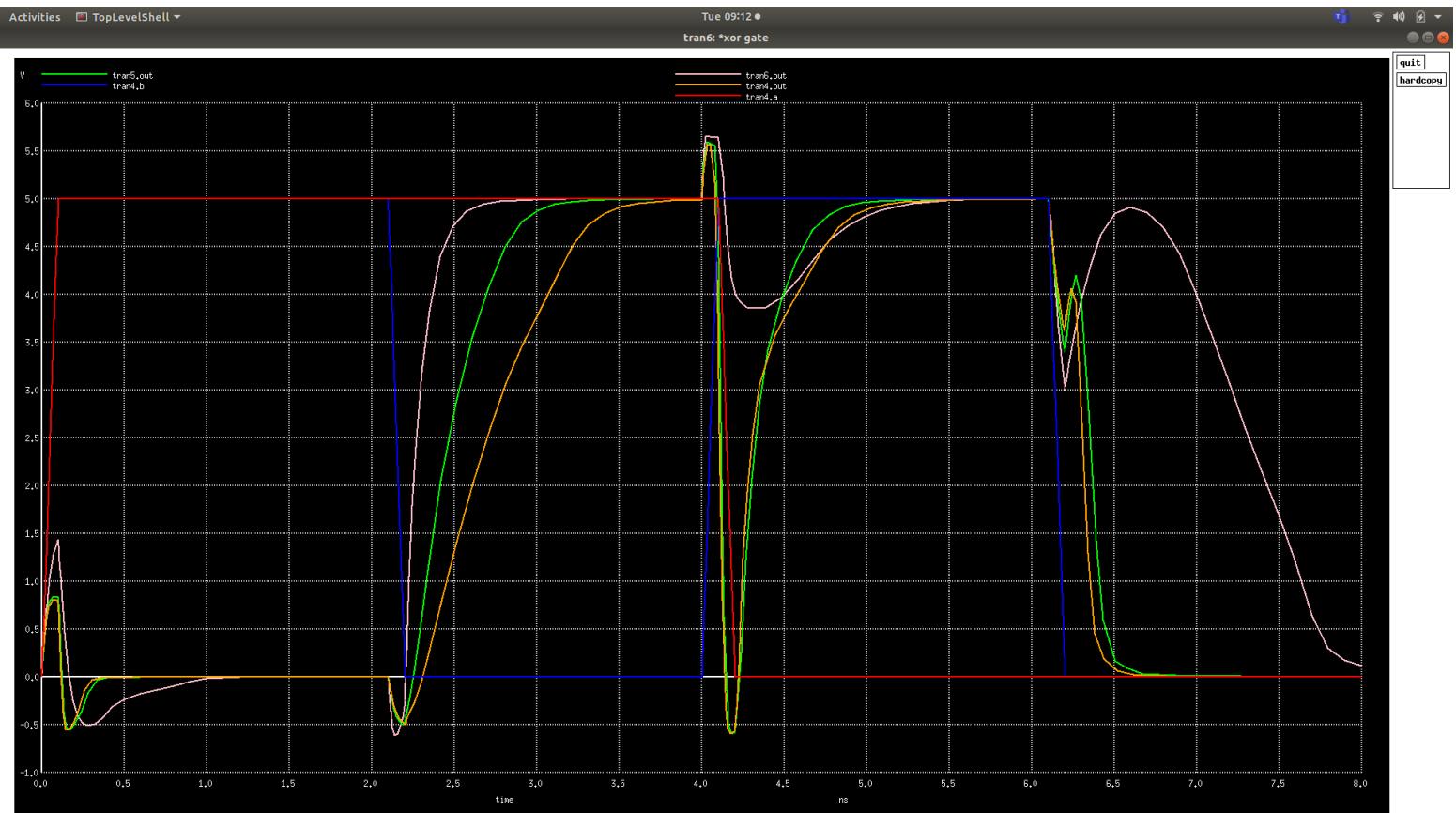


These are the results obtained when we vary the **width of the bottom Mosfets** the first graph is the dc output vs the dc input after doing dc analysis the Noise Margin as we increase the width-the noise margin decreases and those not in the range do not act as an gate,, the rise time increases but fall time decreases, and the power consumed increases as the resistance decreases and the current increases the energy consumed also increase, and power is consumed in steady state due to sub threshold current.

### Varying the Width of Both the PMOS:-

```
*Transfer function and transient response on varying WIDTH of all the PMOS in PUN
.control
foreach wid 0.5u 1u 10u
alter m8 w=$wid
alter m9 w=$wid
alter m10 w=$wid
alter m11 w=$wid
tran 0.1n 8ns
end
.endc

.control
plot tran4.a tran4.b tran4.out tran5.out tran6.out
plot tran4.v_dd#branch*(-vdd) tran5.v_dd#branch*(-vdd) tran6.v_dd#branch*(-vdd)
.endc
```

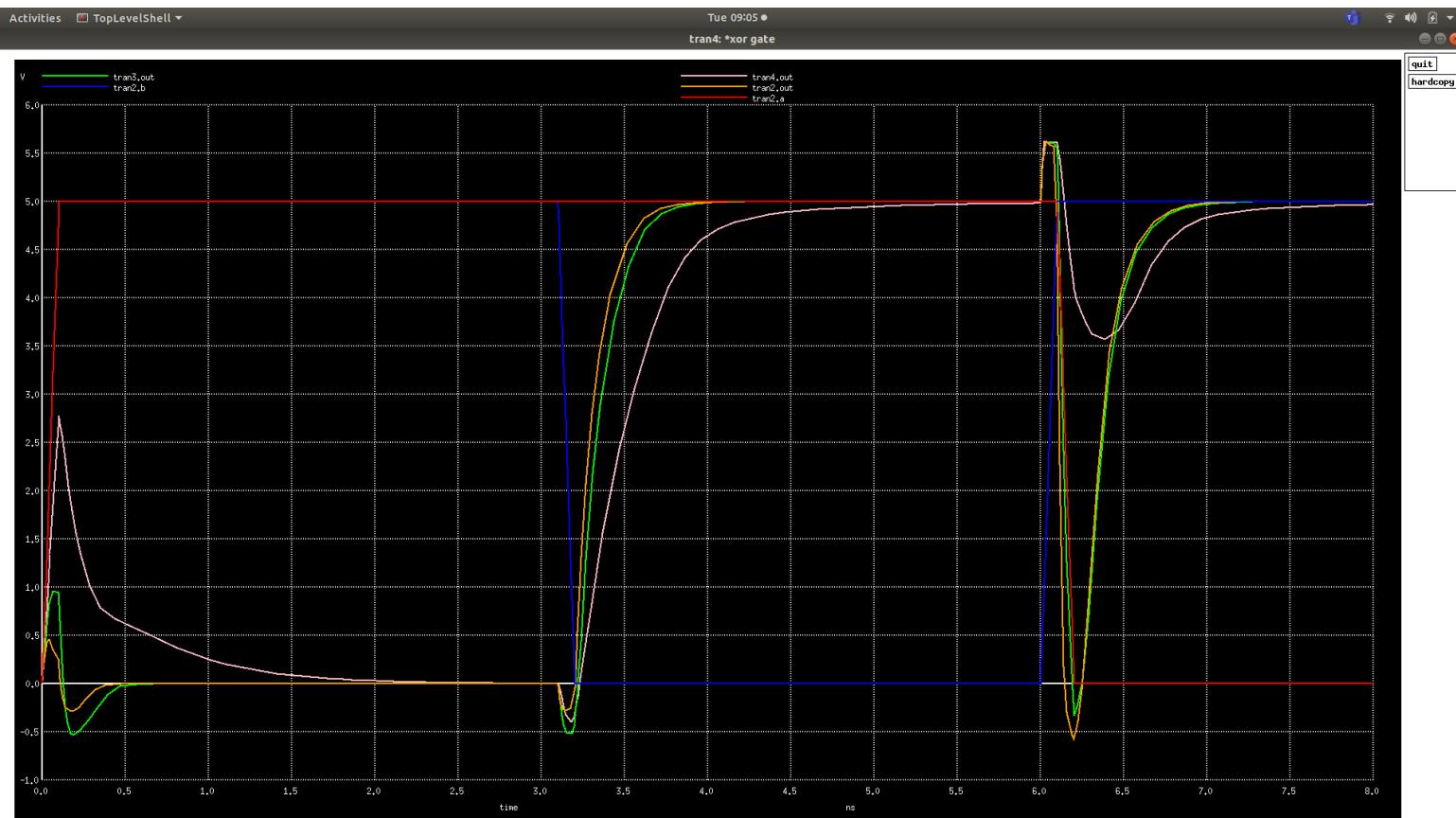


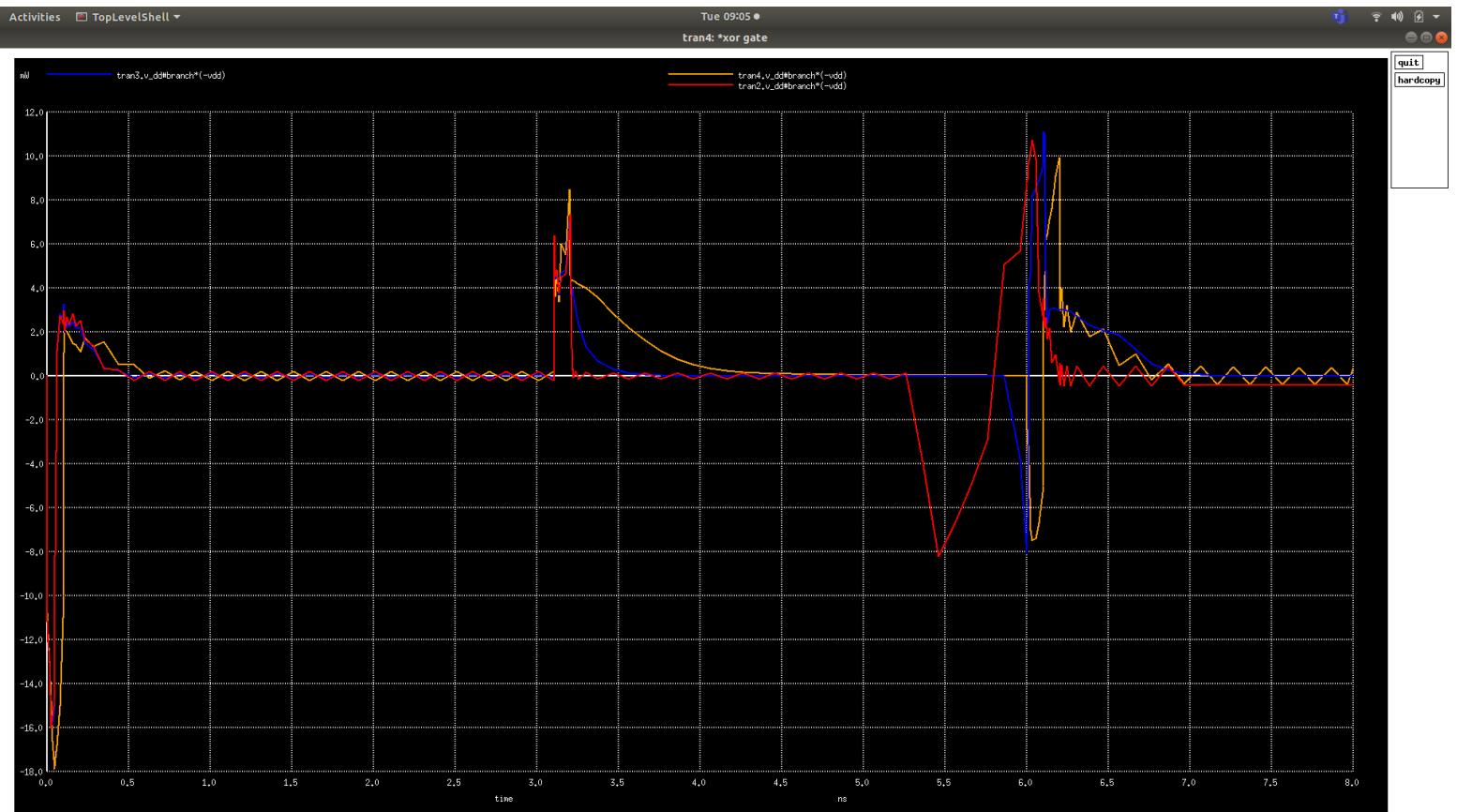
These are the results obtained when we vary the **width of the Top Mosfets** the first graph is the dc output vs the dc input after doing dc analysis the Noise Margin as we increase the width-the noise margin decreases and those not in the range do not act as an gate, Looking at second graph the rise time deceases, but fall time increases, Looking at the third graph the power consumed increases as the resistance decreases and the current increases the energy consumed also increase, and power is consumed in steady state due to sub threshold current.

## Varying the Length of Both the NMOS:-

```
*Transfer function and transient response on varying LENGTH of all the NMOS
.control
foreach len 0.5u 1u 5u
alter m4 l=$len
alter m5 l=$len
alter m6 l=$len
alter m7 l=$len
tran 0.1n 8ns
end
alter m4 l=1u
alter m5 l=1u
alter m6 l=1u
alter m7 l=1u
.endc

.control
plot tran2.a tran2.b tran2.out tran3.out tran4.out
plot tran2.v_dd#branch*(-vdd) tran3.v_dd#branch*(-vdd) tran4.v_dd#branch*(-vdd)
.endc
```



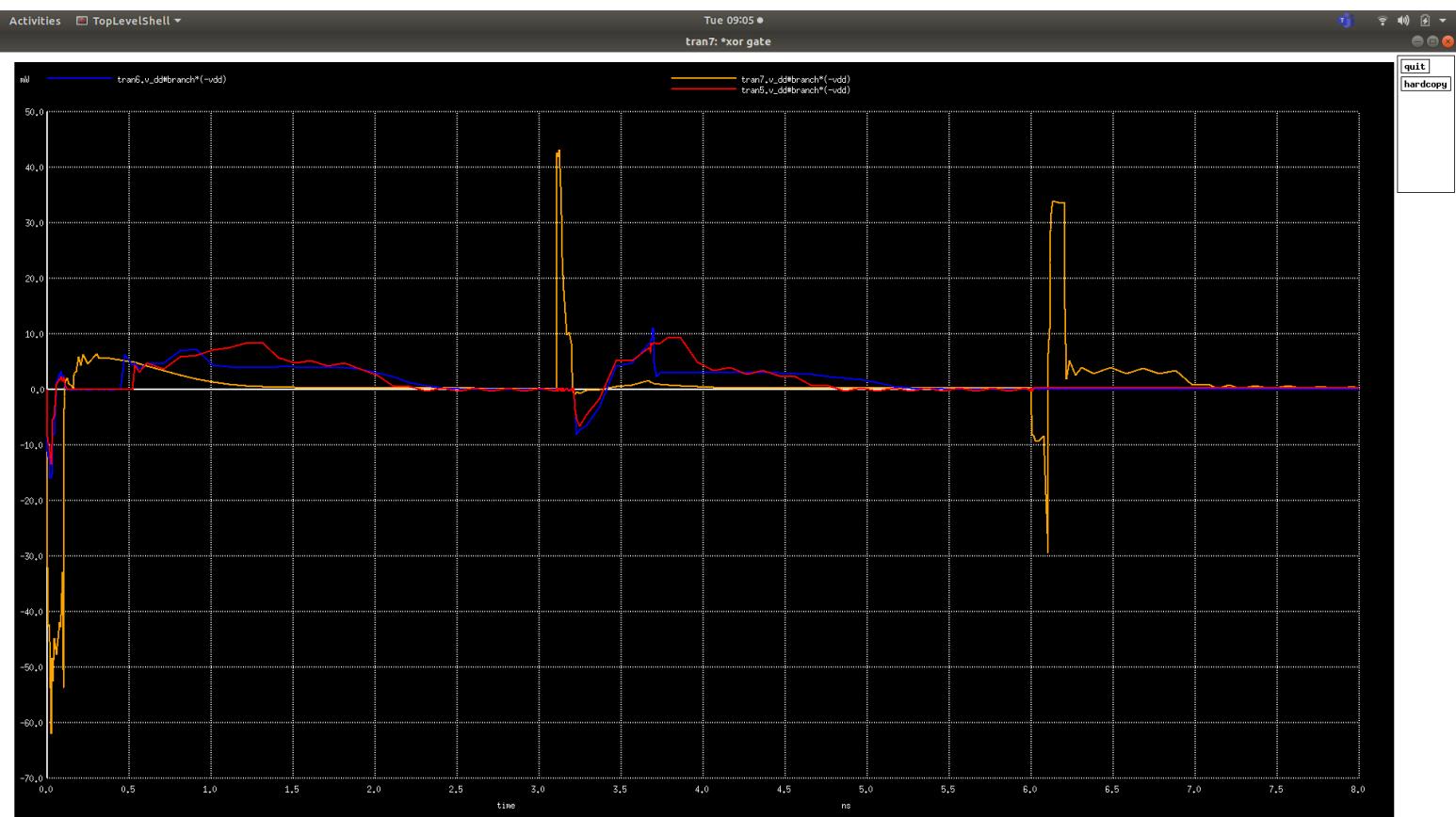
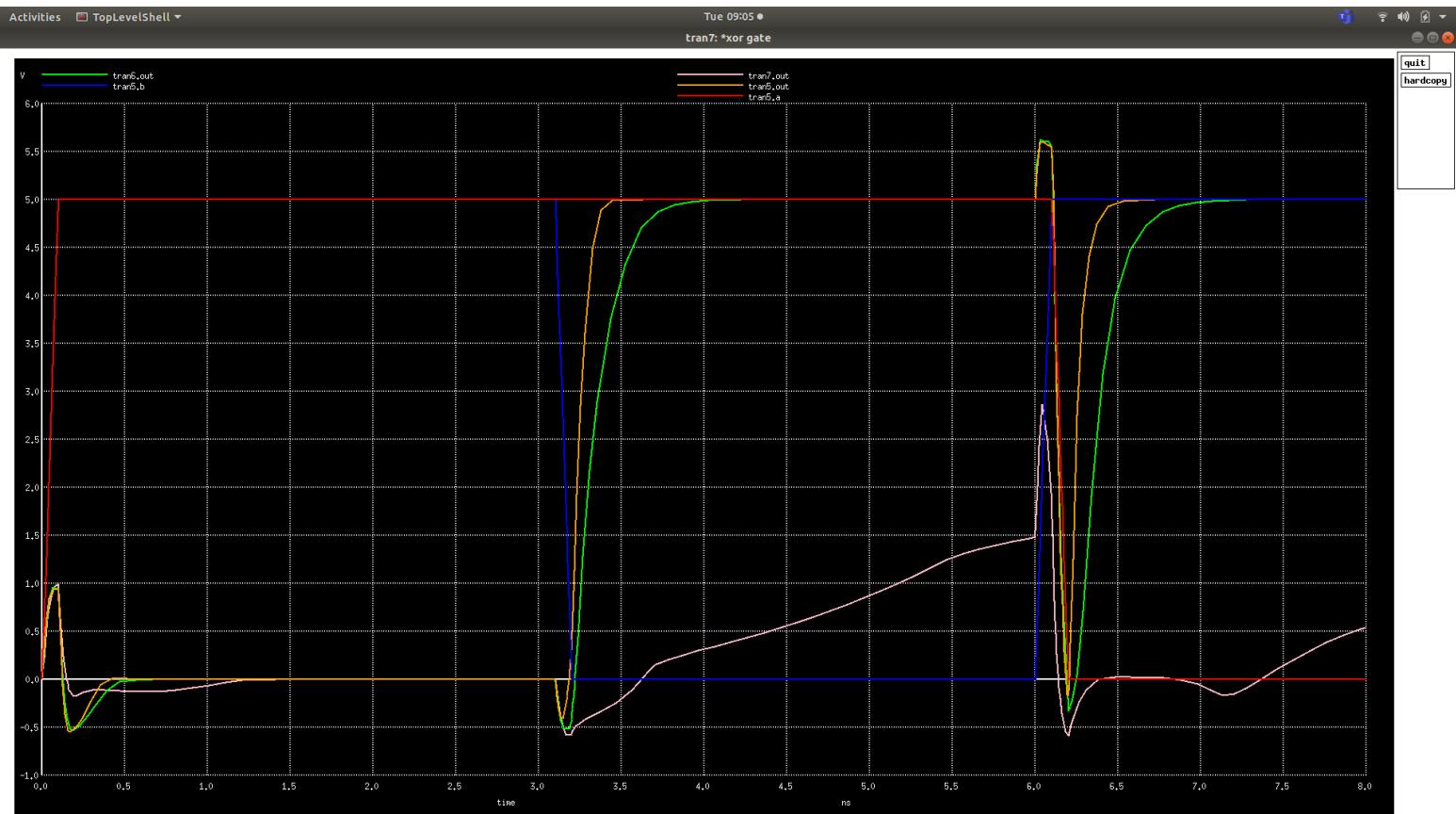


These are the results obtained when we vary the **length of the bottom Mosfets** the first graph is the dc output vs the dc input after doing dc analysis the Noise Margin as we increase the length-the noise margin increases and those not in the range do not act as an gate, Looking at second graph the rise time increase, also fall time increases, Looking at the third graph the power consumed increases, and the amount of energy consumed is more, and power is consumed in steady state due to sub threshold current.

### Varying the Length of Both the PMOS:-

```
*Transfer function and transient response on varying LENGTH of all the PMOS
.control
foreach len 0.5u 1u 10u
alter m8 l=$len
alter m9 l=$len
alter m10 l=$len
alter m11 l=$len
tran 0.1n 8ns
end
.endc

.control
plot tran5.a tran5.b tran5.out tran6.out tran7.out
plot tran5.v_dd#branch*(-vdd) tran6.v_dd#branch*(-vdd) tran7.v_dd#branch*(-vdd)
.endc
```

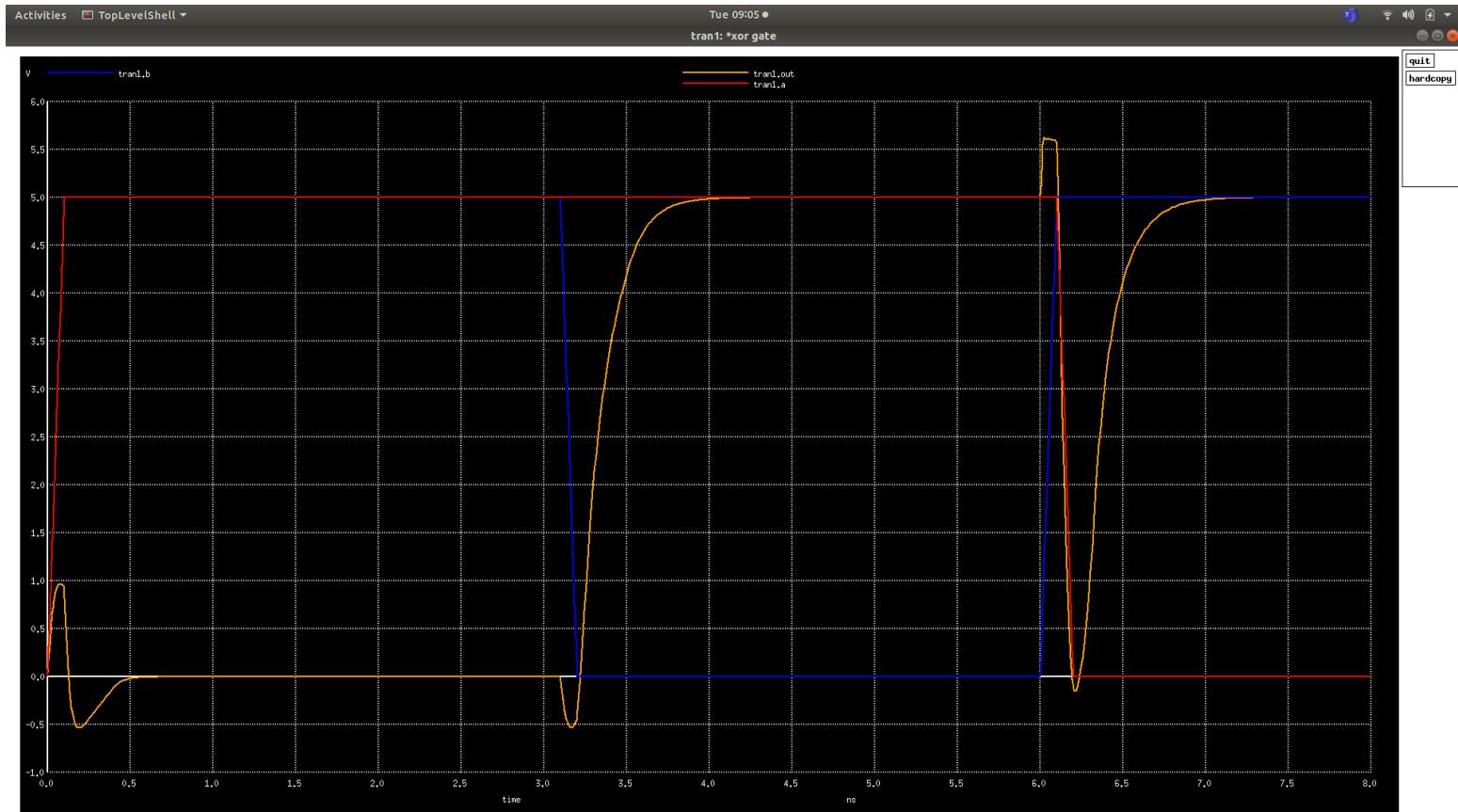


These are the results obtained when we vary the **length of the Top Mosfets** the first graph is the dc output vs the dc input after doing dc analysis for Noise Margin as we increase the length-the noise margin decreases and those not in the range do not act as an gate, Looking at second graph the rise time increase, but fall time increases, Looking at the third graph the power consumed increases as the resistance increase the energy consumed also increase, and power is consumed in steady state due to sub threshold current.

### Regular Response:-

```
.control
  tran 0.01n 8n
  run
.endc

.control
  plot tran1.a tran1.b tran1.out
.endc
.end
```



### Conclusion:-

The experiment was performed, and all graphs were analysed. The obtained graphs movements agreed with theory, and hence simulations were verified. NGSPICE was the simulator used for this task.

# 6. Study of CMOS Inverter Magic

## Objectives:-

To Learn layout,extract and characterization process in the design flow with CMOS inverter as an Example.

## Introduction:-

Inverter is one that inverts the signal supplied at its input. If input is made high or logic level is 1, then the output has logic level 0 and vice-versa. A CMOS inverter is characterised by a PMOs between the pull down transistor and the voltage source the input is fed to the Pull up network also. The output is taken at the junction of the Pmos and the pull down transistor. The pull-up circuit is constituted by the PMOS and pull-down resistor by the NMOS. When the input is low, the NMOS is open circuited and the output capacitance is charged to VDD through Pmos.

## Magic code:

```
magic
tech scmos
timestamp 1602950087
<< pwell >>
rect -3 -9 12 3
<< nwell >>
rect -4 18 11 31
<< polysilicon >>
rect 2 23 4 25
rect 2 10 4 13
rect 0 6 4 10
rect 2 3 4 6
rect 2 -2 4 0
<< ndiffusion >>
rect 1 0 2 3
rect 4 0 5 3
<< pdiffusion >>
rect -1 22 2 23
rect 1 18 2 22
rect -1 13 2 18
rect 4 22 7 23
rect 4 18 5 22
rect 4 13 7 18
<< metal1 >>
rect -4 27 -3 31
rect 1 27 9 31
rect -3 22 1 27
rect 6 3 9 18
rect -3 -5 0 -1
rect 1 -9 10 -5
```

```

<< ntransistor >>
rect 2 0 4 3
<< ptransistor >>
rect 2 13 4 23
<< polycontact >>
rect -4 6 0 10
<< ndcontact >>
rect -3 -1 1 3
rect 5 -1 9 3
rect -3 -9 1 -5
<< nsubstratencontact >>
rect -3 27 1 31
<< labels >>
rlabel metal1 3 29 3 29 5 vdd
rlabel metal1 4 -7 4 -7 1 Gnd
rlabel polycontact -2 8 -2 8 3 in
rlabel metal1 7 10 7 10 7 out
<< end >>
<< pdcontact >>
rect -3 18 1 22
rect 5 18 9 22
<< psubstratepcontact >>

```

## Spice file:

```

.option scale=1u

M1000 vdd in out vdd pfet w=10 l=2
+ ad=38 pd=30 as=38 ps=30
M1001 out in Gnd Gnd nfet w=3 l=2
+ ad=19 pd=18 as=19 ps=18
C0 in 0 4.4fF

```

## Ngspice simulation:

```

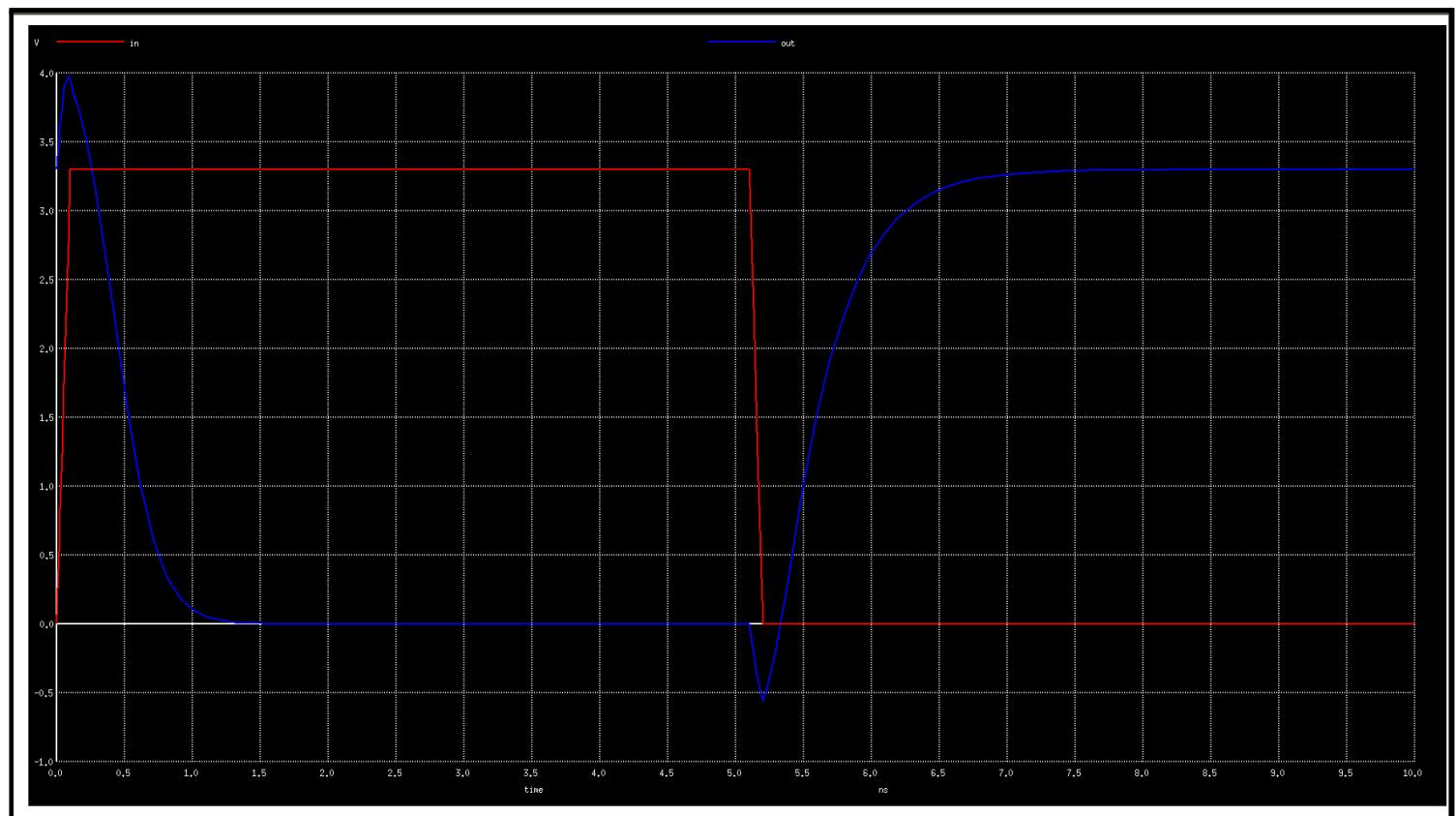
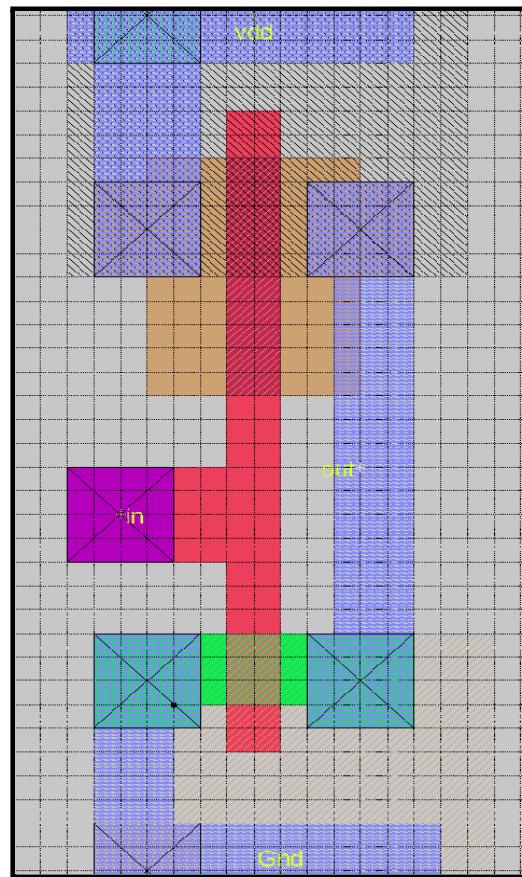
.include "t14y_tsmc_025_level3.txt"
.include "Inverter_6"

va in 0 pulse(0 3.3 0 On 5n 10n)
vdd vdd 0 3.3

.control
tran 0.1n 20n
setplot tran1
plot in out
.endc

.end

```



## 7. Study of CMOS Inverter Magic

To create a standard cell library of CMOS Gates -

Two and Three input-

- Nand
- Nor
- And
- Or,
- AOI for Two products of Two variables
- D-latch and a D-Flipflop

### **Introduction:-**

Logic gates are the basic building blocks of any digital system. It is an electronic circuit having one or more than one input and only one output. The relationship between the input and the output is based on a certain logic. Based on this, logic gates are named as AND gate, OR gate, NOT gate etc.

### **Nand Gate:-**

### **Magic code:**

```
magic
tech scmos
timestamp 1602503095
<< pwell >>
rect -5 -43 6 -31
rect 15 -43 28 -31
<< nwell >>
rect -6 -14 28 1
<< polysilicon >>
rect 0 -8 2 -6
rect 20 -8 22 -6
rect 0 -22 2 -14
rect 20 -22 22 -14
rect -1 -26 2 -22
rect 19 -26 22 -22
rect 0 -31 2 -26
rect 20 -31 22 -26
rect 0 -37 2 -35
rect 20 -37 22 -35
<< ndiffusion >>
rect -1 -35 0 -31
rect 2 -35 15 -31
rect 19 -35 20 -31
rect 22 -35 24 -31
<< pdiffusion >>
```

```
rect -3 -9 0 -8
rect -2 -13 0 -9
rect -3 -14 0 -13
rect 2 -9 5 -8
rect 17 -9 20 -8
rect 2 -13 4 -9
rect 18 -13 20 -9
rect 2 -14 5 -13
rect 17 -14 20 -13
rect 22 -9 25 -8
rect 22 -13 24 -9
rect 22 -14 25 -13
<< metal1 >>
rect -2 -3 14 1
rect -6 -9 -2 -3
rect 14 -9 18 -3
rect 4 -16 8 -13
rect 24 -16 28 -13
rect 4 -19 28 -16
rect 24 -31 28 -19
rect -5 -39 -1 -35
rect 15 -39 19 -35
<< ntransistor >>
rect 0 -35 2 -31
rect 20 -35 22 -31
<< ptransistor >>
rect 0 -14 2 -8
rect 20 -14 22 -8
<< polycontact >>
rect -5 -26 -1 -22
rect 15 -26 19 -22
<< ndcontact >>
rect -5 -35 -1 -31
rect 15 -35 19 -31
rect 24 -35 28 -31
<< pdcontact >>
rect -6 -13 -2 -9
rect 4 -13 8 -9
rect 14 -13 18 -9
rect 24 -13 28 -9
<< psubstratepcontact >>
rect -5 -43 -1 -39
rect 15 -43 19 -39
<< nsubstratencontact >>
rect -6 -3 -2 1
rect 14 -3 18 1
<< labels >>
rlabel polycontact -3 -24 -3 -24 3 a
rlabel polycontact 17 -24 17 -24 1 b
rlabel metal1 5 -1 5 -1 5 vdd
rlabel metal1 26 -18 26 -18 7 out
rlabel psubstratepcontact -3 -41 -3 -41 2 gng
rlabel psubstratepcontact -3 -41 -3 -41 2 Gnd
<< end >>
```

**Spice file:**

```
.option scale=1u

M1000 out a vdd 5 pfet w=6 l=2
+ ad=60 pd=48 as=60 ps=48
M1001 out b vdd 5 pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1002 w_15_n43# a 0 0 nfet w=4 l=2
+ ad=72 pd=44 as=20 ps=18
M1003 out b w_15_n43# 0 nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
C0 out 0 6.1fF
C1 b 0 5.6fF
C2 a 0 5.6fF
```

**Ngspice simulation:**

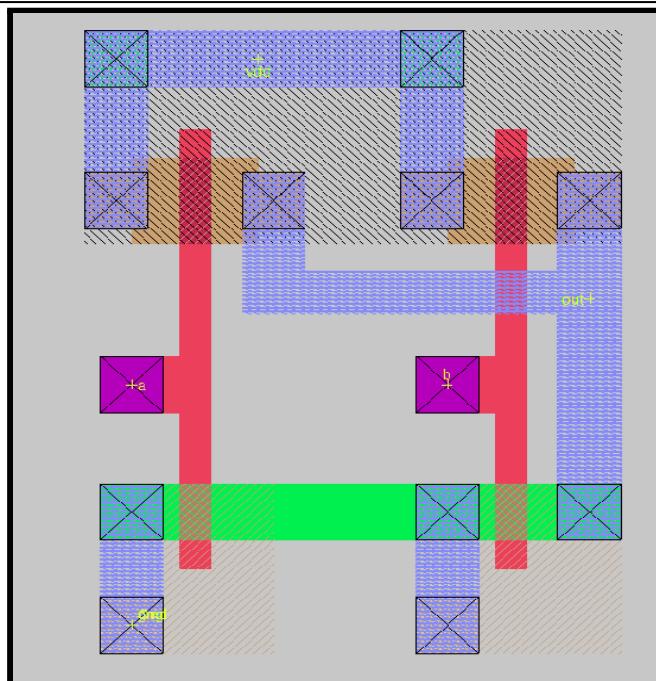
```
*layout of Nand_2

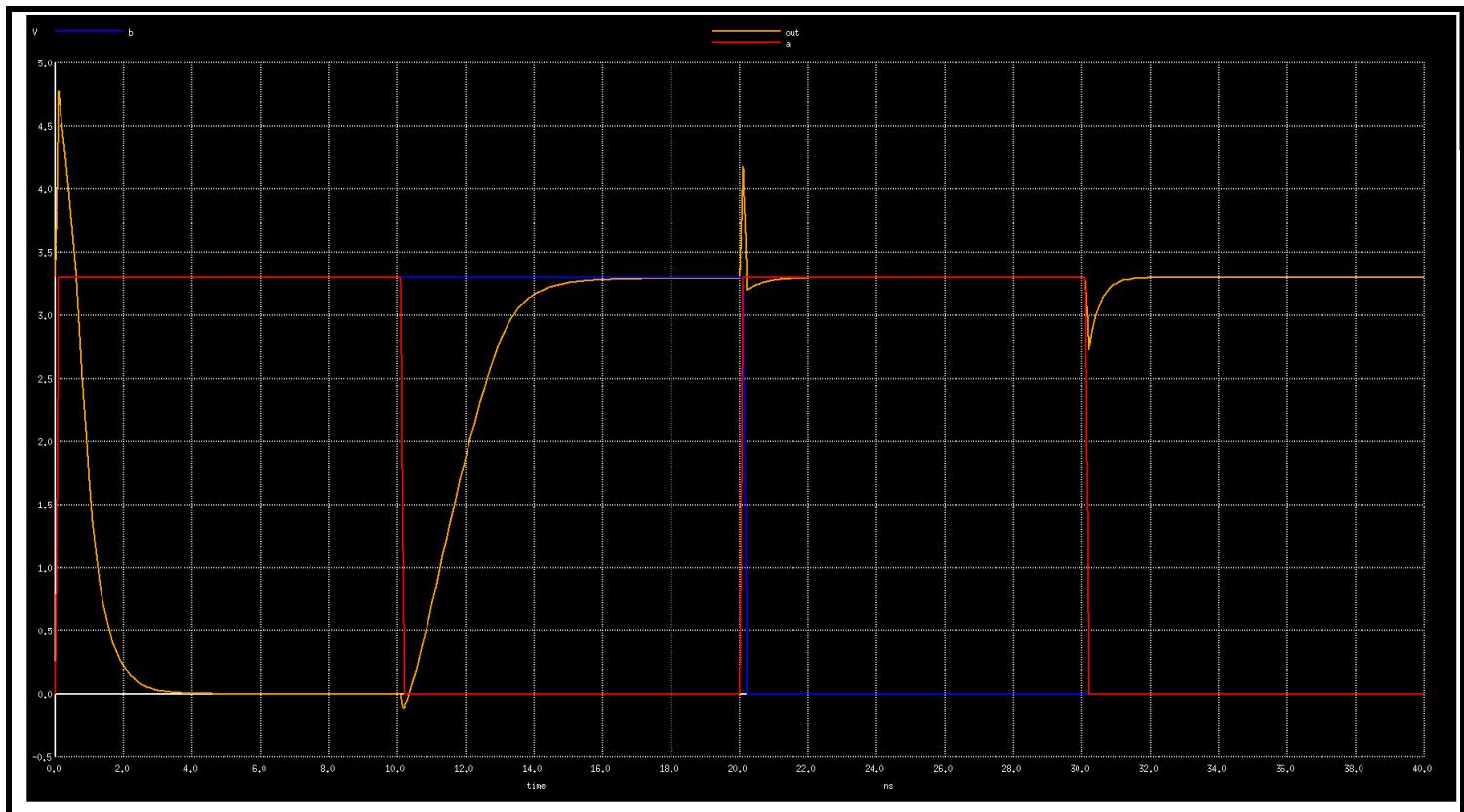
.include "t14y_tsmc_025_level3.txt"
.include "nand_2_7.spice"

va a 0 3.3 pulse(0 3.3 0 0n 10n 20n)
vb b 0 3.3 pulse(0 3.3 0 0n 20n 40n)
vdd vdd 0 3.3

.control
tran 0.1n 20n
setplot tran1
plot a b out
.endc

.end
```





## Nor\_2\_Input:

### Magic File:

```
magic
tech scmos
timestamp 1602509924
<< pwell >>
rect -6 -14 24 0
<< nwell >>
rect -7 15 25 37
<< polysilicon >>
rect -1 28 1 30
rect 17 28 19 30
rect -1 13 1 15
rect 17 13 19 15
rect -2 9 1 13
rect 16 9 19 13
rect -1 0 1 9
rect 17 0 19 9
rect -1 -5 1 -3
rect 17 -5 19 -3
<< ndiffusion >>
rect -6 -1 -1 0
rect -2 -3 -1 -1
rect 1 -2 2 0
rect 1 -3 6 -2
```

```

rect 11 -1 17 0
rect 15 -3 17 -1
rect 19 -2 20 0
rect 19 -3 24 -2
<< pdiffusion >>
rect -3 25 -1 28
rect -6 15 -1 25
rect 1 15 17 28
rect 19 19 24 28
rect 19 15 20 19
<< metal1 >>
rect -3 33 4 37
rect -7 29 -3 33
rect 20 5 24 15
rect 2 2 24 5
rect -6 -10 -2 -5
rect 11 -10 15 -5
rect -2 -14 11 -10
<< ntransistor >>
rect -1 -3 1 0
rect 17 -3 19 0
<< ptransistor >>
rect -1 15 1 28
rect 17 15 19 28
<< polycontact >>
rect -6 9 -2 13
rect 12 9 16 13
<< ndcontact >>
rect -6 -5 -2 -1
rect 2 -2 6 2
rect 11 -5 15 -1
rect 20 -2 24 2
<< pdcontact >>
rect -7 25 -3 29
rect 20 15 24 19
<< psubstratecontact >>
rect -6 -14 -2 -10
rect 11 -14 15 -10
<< nsubstratencontact >>
rect -7 33 -3 37
<< labels >>
rlabel polycontact -4 11 -4 11 3 a
rlabel polycontact 14 11 14 11 1 b
rlabel psubstratecontact 12 -12 12 -12 1 Gnd
rlabel metal1 22 8 22 8 7 out
rlabel metal1 0 35 0 35 5 vdd
<< end >>

```

**Spice file:**

```

.option scale=1u
M1000 a_1_15# a vdd vdd pfet w=13 l=2
+ ad=208 pd=58 as=72 ps=40
M1001 out b a_1_15# vdd pfet w=13 l=2
+ ad=65 pd=36 as=0 ps=0
M1002 out a Gnd Gnd nfet w=3 l=2
+ ad=46 pd=40 as=49 ps=42
M1003 out b Gnd Gnd nfet w=3 l=2
+ ad=0 pd=0 as=0 ps=0
C0 out 0 4.7fF
C1 b 0 5.2fF
C2 a 0 5.2fF

```

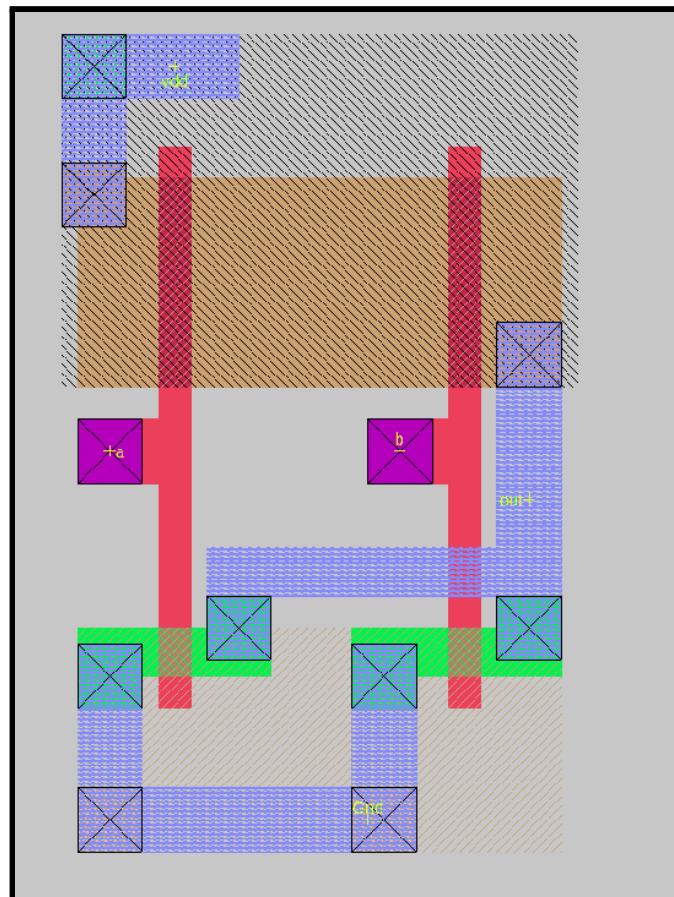
**Ngspice simulation:**

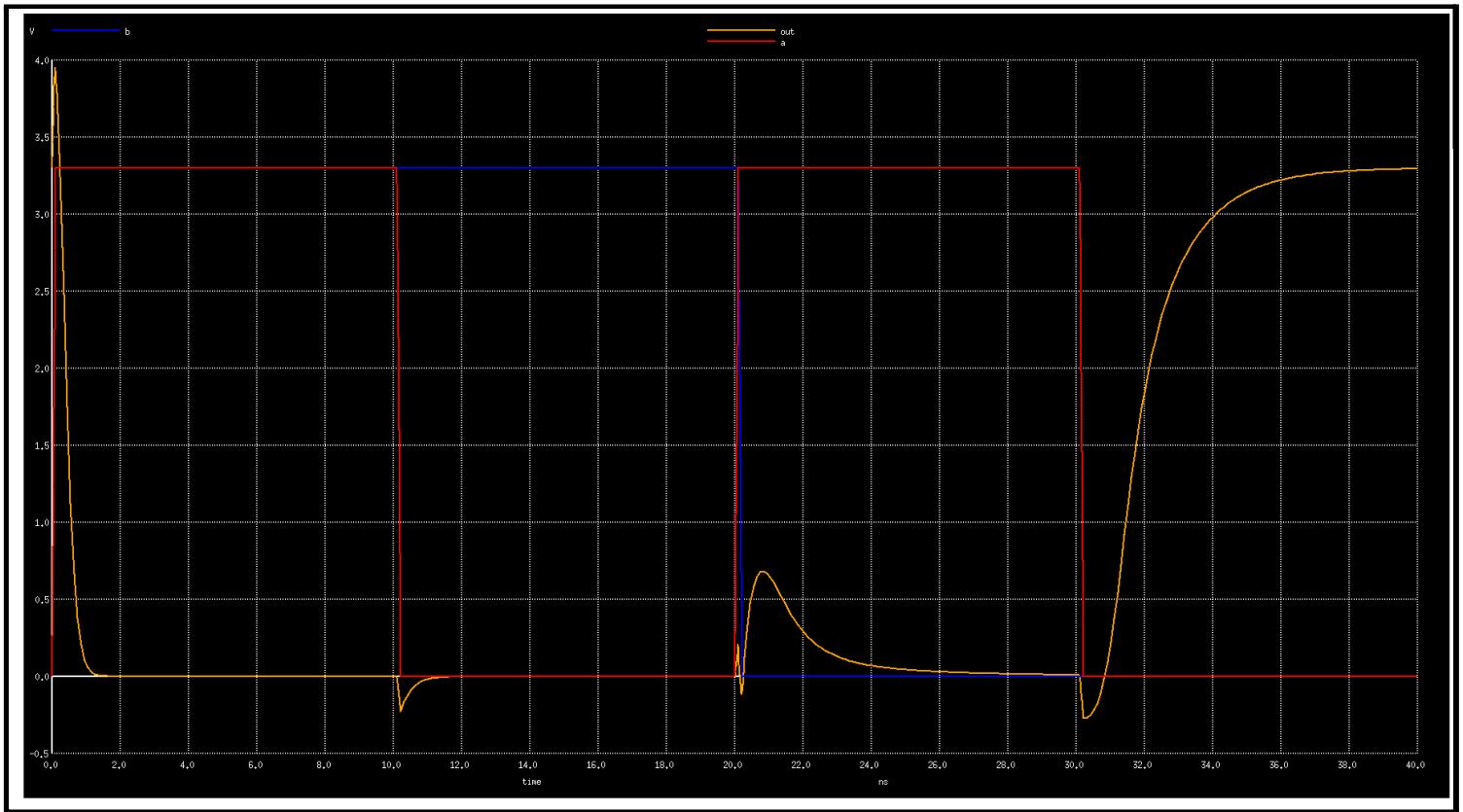
```
*layout of Nor_2
.include "t14y_tsmc_025_level3.txt"
.include "nor_2_7.spice"

va a 0 3.3 pulse(0 3.3 0 On 0n 10n 20n)
vb b 0 3.3 pulse(0 3.3 0 On 0n 20n 40n)
vdd vdd 0 3.3

.control
tran 0.1n 20n
setplot tran1
plot a b out
.endc

.end
```





## And\_2\_Input:

### Magic File:

```

magic
tech scmos
timestamp 1602567432
<< pwell >>
rect -5 -43 6 -31
rect 19 -43 29 -31
rect 38 -44 55 -32
<< nwell >>
rect -6 -14 29 1
rect 38 -14 51 1
<< polysilicon >>
rect 0 -8 2 -6
rect 21 -8 23 -6
rect 43 -8 45 -6
rect 0 -22 2 -14
rect 21 -22 23 -14
rect 43 -22 45 -14
rect -1 -26 2 -22
rect 20 -26 23 -22
rect 42 -26 45 -22
rect 0 -31 2 -26
rect 21 -31 23 -26
rect 43 -32 45 -26
rect 0 -37 2 -35
rect 21 -37 23 -35
rect 43 -37 45 -35

```

```
<< ndiffusion >>
rect -1 -35 0 -31
rect 2 -35 21 -31
rect 23 -35 25 -31
rect 42 -35 43 -32
rect 45 -35 47 -32
<< pdiffusion >>
rect -6 -9 0 -8
rect -2 -13 0 -9
rect -6 -14 0 -13
rect 2 -9 8 -8
rect 2 -13 4 -9
rect 2 -14 8 -13
rect 15 -9 21 -8
rect 19 -13 21 -9
rect 15 -14 21 -13
rect 23 -9 29 -8
rect 23 -13 25 -9
rect 23 -14 29 -13
rect 38 -9 43 -8
rect 42 -13 43 -9
rect 38 -14 43 -13
rect 45 -9 51 -8
rect 45 -13 47 -9
rect 45 -14 51 -13
<< metal1 >>
rect -2 -3 15 1
rect 19 -3 38 1
rect -6 -9 -2 -3
rect 15 -9 19 -3
rect 38 -9 41 -3
rect 4 -16 8 -13
rect 25 -16 29 -13
rect 4 -19 29 -16
rect 25 -22 29 -19
rect 25 -26 38 -22
rect 25 -31 29 -26
rect 47 -31 51 -13
rect -5 -39 -1 -35
rect 38 -39 42 -36
rect -1 -40 42 -39
rect -1 -43 38 -40
<< ntransistor >>
rect 0 -35 2 -31
rect 21 -35 23 -31
rect 43 -35 45 -32
<< ptransistor >>
rect 0 -14 2 -8
rect 21 -14 23 -8
rect 43 -14 45 -8
<< polycontact >>
rect -5 -26 -1 -22
rect 16 -26 20 -22
rect 38 -26 42 -22
<< ndcontact >>
rect -5 -35 -1 -31
rect 25 -35 29 -31
rect 38 -36 42 -32
rect 47 -35 51 -31
<< pdcontact >>
rect -6 -13 -2 -9
```

```

rect 4 -13 8 -9
rect 15 -13 19 -9
rect 25 -13 29 -9
rect 38 -13 42 -9
rect 47 -13 51 -9
<< psubstratecontact >>
rect -5 -43 -1 -39
rect 38 -44 42 -40
<< nsubstratencontact >>
rect -6 -3 -2 1
rect 15 -3 19 1
rect 38 -3 42 1
<< labels >>
rlabel polycontact -3 -24 -3 -24 3 a
rlabel metal1 5 -1 5 -1 5 vdd
rlabel polycontact 18 -24 18 -24 1 b
rlabel metal1 49 -18 49 -18 7 out
rlabel psubstratecontact -3 -41 -3 -41 2 Gnd
<< end >>

```

**Spice file:**

```

.option scale=1u

M1000 a_2_n14# a vdd vdd pfet w=6 l=2
+ ad=72 pd=48 as=102 ps=70
M1001 a_2_n14# b vdd vdd pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1002 out a_2_n14# vdd vdd pfet w=6 l=2
+ ad=36 pd=24 as=0 ps=0
M1003 a_2_n35# a Gnd Gnd nfet w=4 l=2
+ ad=76 pd=46 as=39 ps=36
M1004 a_2_n14# b a_2_n35# w_19_n43# nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
M1005 out a_2_n14# Gnd Gnd nfet w=3 l=2
+ ad=22 pd=20 as=0 ps=0
C0 out 0 3.2fF
C1 a_2_n14# 0 13.8fF
C2 b 0 5.6fF
C3 a 0 5.6fF
C4 Gnd 0 4.1fF

```

**Ngspice simulation:**

```

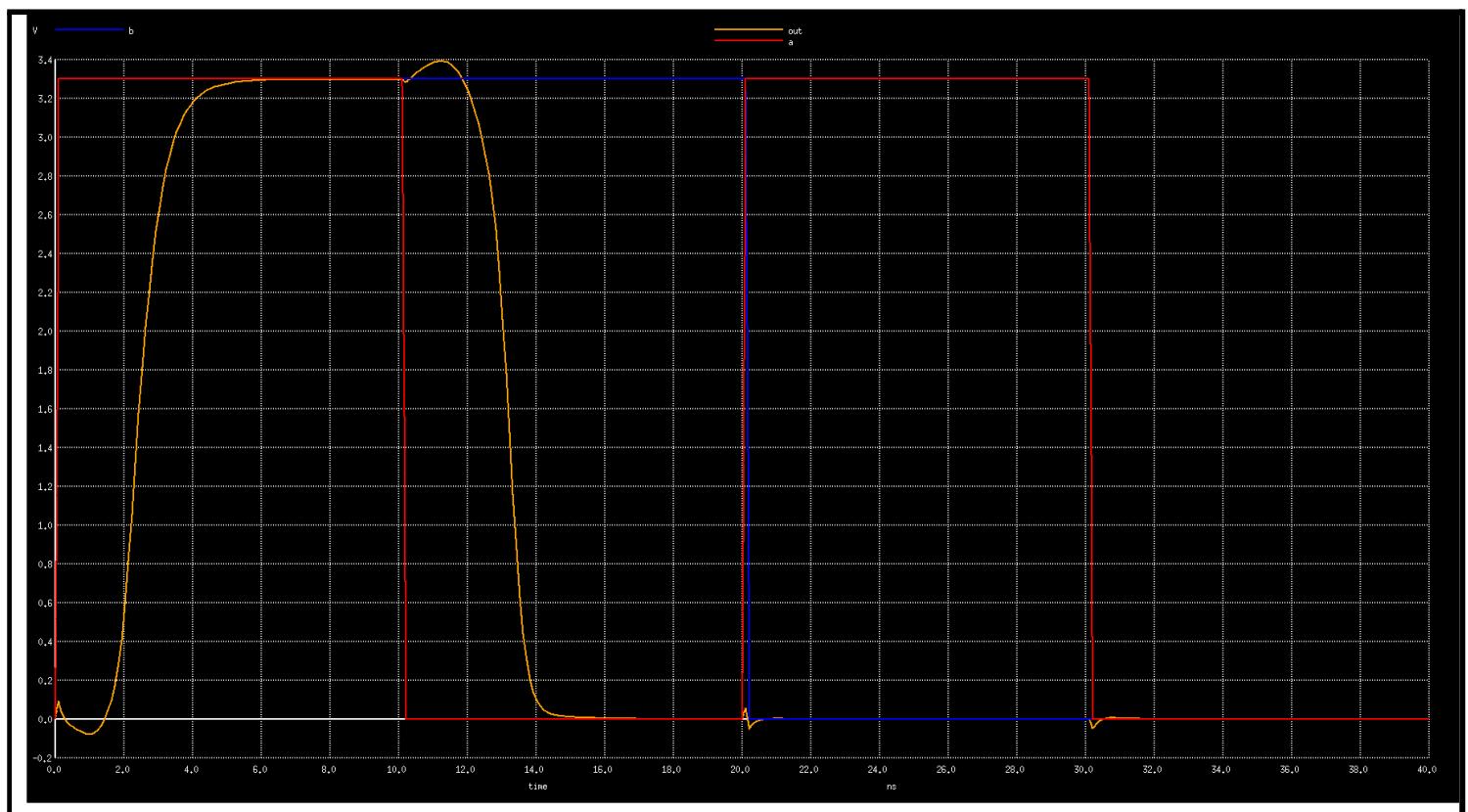
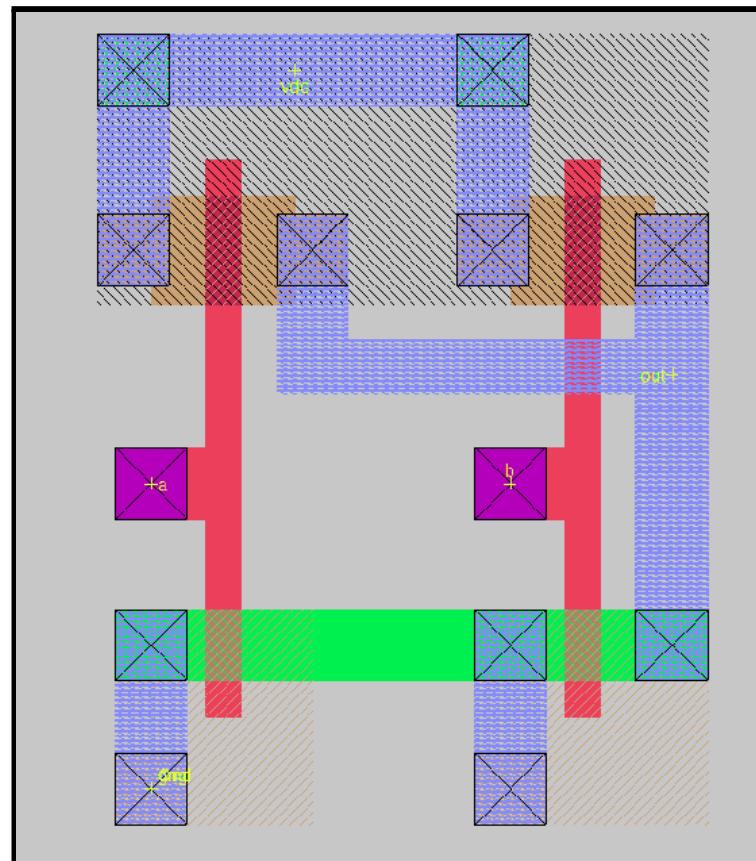
*layout of And_2

.include "t14y_tsmc_025_level3.txt"
.include "and_2_7.spice"

va a 0 3.3 pulse(0 3.3 0 On 0n 10n 20n)
vb b 0 3.3 pulse(0 3.3 0 On 0n 20n 40n)
vdd vdd 0 3.3

.control
tran 0.1n 20n
setplot tran1
plot a b out
.endc

```



**Or\_2\_Input:****Magic File:**

```
magic
tech scmos
timestamp 1602515974
<< pwell >>
rect -6 -14 24 0
rect 33 -14 46 0
<< nwell >>
rect -7 15 24 37
rect 33 15 47 26
<< polysilicon >>
rect -1 28 1 30
rect 17 28 19 30
rect 39 21 41 23
rect -1 13 1 15
rect 17 13 19 15
rect 39 13 41 15
rect -2 9 1 13
rect 16 9 19 13
rect 38 9 41 13
rect -1 0 1 9
rect 17 0 19 9
rect -1 -5 1 -3
rect 39 0 41 9
rect 17 -5 19 -3
rect 39 -5 41 -3
<< ndiffusion >>
rect -6 -1 -1 0
rect -2 -3 -1 -1
rect 1 -2 2 0
rect 1 -3 6 -2
rect 11 -1 17 0
rect 15 -3 17 -1
rect 19 -2 20 0
rect 19 -3 24 -2
rect 33 -1 39 0
rect 37 -3 39 -1
rect 41 -2 42 0
rect 41 -3 46 -2
<< pdiffusion >>
rect -3 25 -1 28
rect -6 15 -1 25
rect 1 15 17 28
rect 19 19 24 28
rect 19 15 20 19
rect 37 18 39 21
rect 34 15 39 18
rect 41 19 46 21
rect 41 15 42 19
<< metal1 >>
rect -3 33 37 37
rect -7 29 -3 33
```

```
rect 33 22 37 33
rect 20 13 24 15
rect 20 9 34 13
rect 20 5 24 9
rect 2 2 24 5
rect -6 -10 -2 -5
rect 42 2 46 15
rect 11 -10 15 -5
rect 33 -10 37 -5
rect -2 -14 11 -10
rect 15 -14 33 -10
<< ntransistor >>
rect -1 -3 1 0
rect 17 -3 19 0
rect 39 -3 41 0
<< ptransistor >>
rect -1 15 1 28
rect 17 15 19 28
rect 39 15 41 21
<< polycontact >>
rect -6 9 -2 13
rect 12 9 16 13
rect 34 9 38 13
<< ndcontact >>
rect -6 -5 -2 -1
rect 2 -2 6 2
rect 11 -5 15 -1
rect 20 -2 24 2
rect 33 -5 37 -1
rect 42 -2 46 2
<< pdcontact >>
rect -7 25 -3 29
rect 20 15 24 19
rect 33 18 37 22
rect 42 15 46 19
<< psubstratecontact >>
rect -6 -14 -2 -10
rect 11 -14 15 -10
rect 33 -14 37 -10
<< nsubstratencontact >>
rect -7 33 -3 37
<< labels >>
rlabel polycontact -4 11 -4 11 3 a
rlabel polycontact 14 11 14 11 1 b
rlabel psubstratecontact 12 -12 12 -12 1 Gnd
rlabel metal1 0 35 0 35 5 vdd
rlabel metal1 44 8 44 8 7 out
<< end >>
```

**Spice file:**

```
.option scale=1u

M1000 a_1_15# a vdd vdd pfet w=13 l=2
+ ad=208 pd=58 as=109 ps=66
M1001 a_1_n3# b a_1_15# vdd pfet w=13 l=2
+ ad=65 pd=36 as=0 ps=0
M1002 out a_1_n3# vdd w_33_15# pfet w=6 l=2
+ ad=30 pd=22 as=0 ps=0
M1003 a_1_n3# a Gnd Gnd nfet w=3 l=2
+ ad=46 pd=40 as=75 ps=64
M1004 a_1_n3# b Gnd Gnd nfet w=3 l=2
+ ad=0 pd=0 as=0 ps=0
M1005 out a_1_n3# Gnd Gnd nfet w=3 l=2
+ ad=23 pd=20 as=0 ps=0
C0 out 0 2.4fF
C1 a_1_n3# gnd! 11.7fF
C2 b 0 5.2fF
C3 a 0! 5.2fF
C4 vdd 0 3.8fF
```

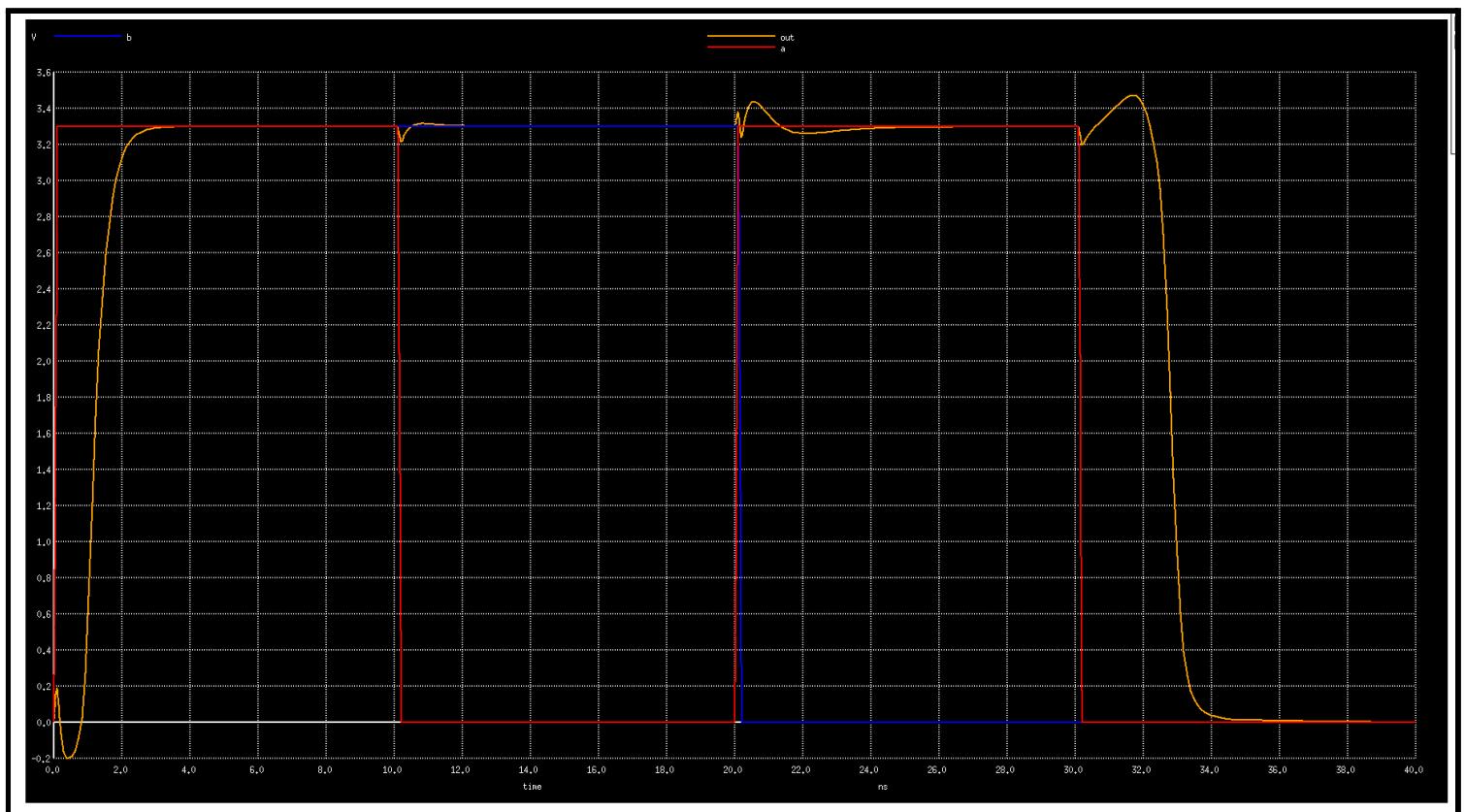
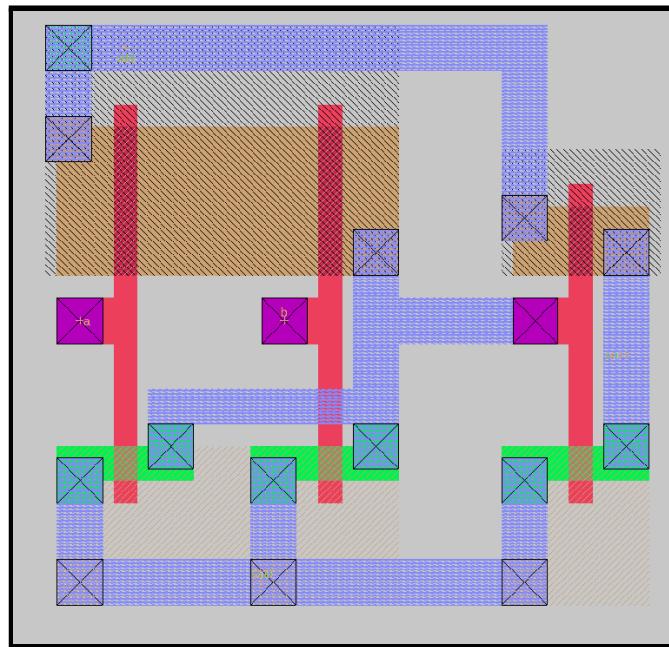
**Ngspice simulation:**

```
*layout of Or_2

.include "t14y_tsmc_025_level3.txt"
.include "nor_2_7.spice"

va a 0 3.3 pulse(0 3.3 0 0n 10n 20n)
vb b 0 3.3 pulse(0 3.3 0 0n 0n 40n)
vdd vdd 0 3.3

.control
tran 0.1n 20n
setplot tran1
plot a b out
.endc
```



## Nand\_3\_Input:

### Magic File:

```
magic
tech scmos
timestamp 1602503684
<< pwell >>
rect -5 -43 6 -31
rect 15 -43 28 -31
rect 37 -43 50 -31
<< nwell >>
rect -6 -14 50 1
<< polysilicon >>
rect 0 -8 2 -6
rect 20 -8 22 -6
rect 42 -8 44 -6
rect 0 -22 2 -14
rect 20 -22 22 -14
rect 42 -22 44 -14
rect -1 -26 2 -22
rect 19 -26 22 -22
rect 41 -26 44 -22
rect 0 -31 2 -26
rect 20 -31 22 -26
rect 42 -31 44 -26
rect 0 -37 2 -35
rect 20 -37 22 -35
rect 42 -37 44 -35
<< ndiffusion >>
rect -1 -35 0 -31
rect 2 -35 15 -31
rect 19 -35 20 -31
rect 22 -35 37 -31
rect 41 -35 42 -31
rect 44 -35 46 -31
<< pdiffusion >>
rect -3 -9 0 -8
rect -2 -13 0 -9
rect -3 -14 0 -13
rect 2 -9 5 -8
rect 17 -9 20 -8
rect 2 -13 4 -9
rect 18 -13 20 -9
rect 2 -14 5 -13
rect 17 -14 20 -13
rect 22 -9 25 -8
rect 39 -9 42 -8
rect 22 -13 24 -9
rect 40 -13 42 -9
rect 22 -14 25 -13
rect 39 -14 42 -13
rect 44 -9 47 -8
rect 44 -13 46 -9
rect 44 -14 47 -13
```

```
<< metal1 >>
rect -2 -3 14 1
rect 18 -3 36 1
rect -6 -9 -2 -3
rect 14 -9 18 -3
rect 36 -9 40 -3
rect 4 -16 8 -13
rect 24 -16 28 -13
rect 46 -16 50 -13
rect 4 -19 50 -16
rect 46 -31 50 -19
rect -5 -39 -1 -35
rect 15 -39 19 -35
rect 37 -39 41 -35
<< ntransistor >>
rect 0 -35 2 -31
rect 20 -35 22 -31
rect 42 -35 44 -31
<< ptransistor >>
rect 0 -14 2 -8
rect 20 -14 22 -8
rect 42 -14 44 -8
<< polycontact >>
rect -5 -26 -1 -22
rect 15 -26 19 -22
rect 37 -26 41 -22
<< ndcontact >>
rect -5 -35 -1 -31
rect 15 -35 19 -31
rect 37 -35 41 -31
rect 46 -35 50 -31
<< pdcontact >>
rect -6 -13 -2 -9
rect 4 -13 8 -9
rect 14 -13 18 -9
rect 24 -13 28 -9
rect 36 -13 40 -9
rect 46 -13 50 -9
<< psubstratepcontact >>
rect -5 -43 -1 -39
rect 15 -43 19 -39
rect 37 -43 41 -39
<< nsubstratencontact >>
rect -6 -3 -2 1
rect 14 -3 18 1
rect 36 -3 40 1
<< labels >>
rlabel polycontact -3 -24 -3 -24 3 a
rlabel polycontact 17 -24 17 -24 1 b
rlabel metal1 5 -1 5 -1 5 vdd
rlabel metal1 26 -18 26 -18 7 out
rlabel psubstratepcontact -3 -41 -3 -41 2 gng
rlabel psubstratepcontact -3 -41 -3 -41 2 Gnd
rlabel polycontact 39 -24 39 -24 1 c
<< end >>
```

**Spice file:**

```
.option scale=1u
```

```

M1000 out a vdd vdd pfet w=6 l=2
+ ad=90 pd=72 as=90 ps=72
M1001 out b vdd vdd pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1002 out c vdd vdd pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1003 w_15_n43# a gng gng nfet w=4 l=2
+ ad=72 pd=44 as=20 ps=18
M1004 w_37_n43# b w_15_n43# w_15_n43# nfet w=4 l=2
+ ad=80 pd=48 as=0 ps=0
M1005 out c w_37_n43# w_37_n43# nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
C0 out gnd! 9.3fF
C1 c 0 5.6fF
C2 b 0 5.6fF
C3 a 0 5.6fF

```

### **Ngspice simulation:**

```

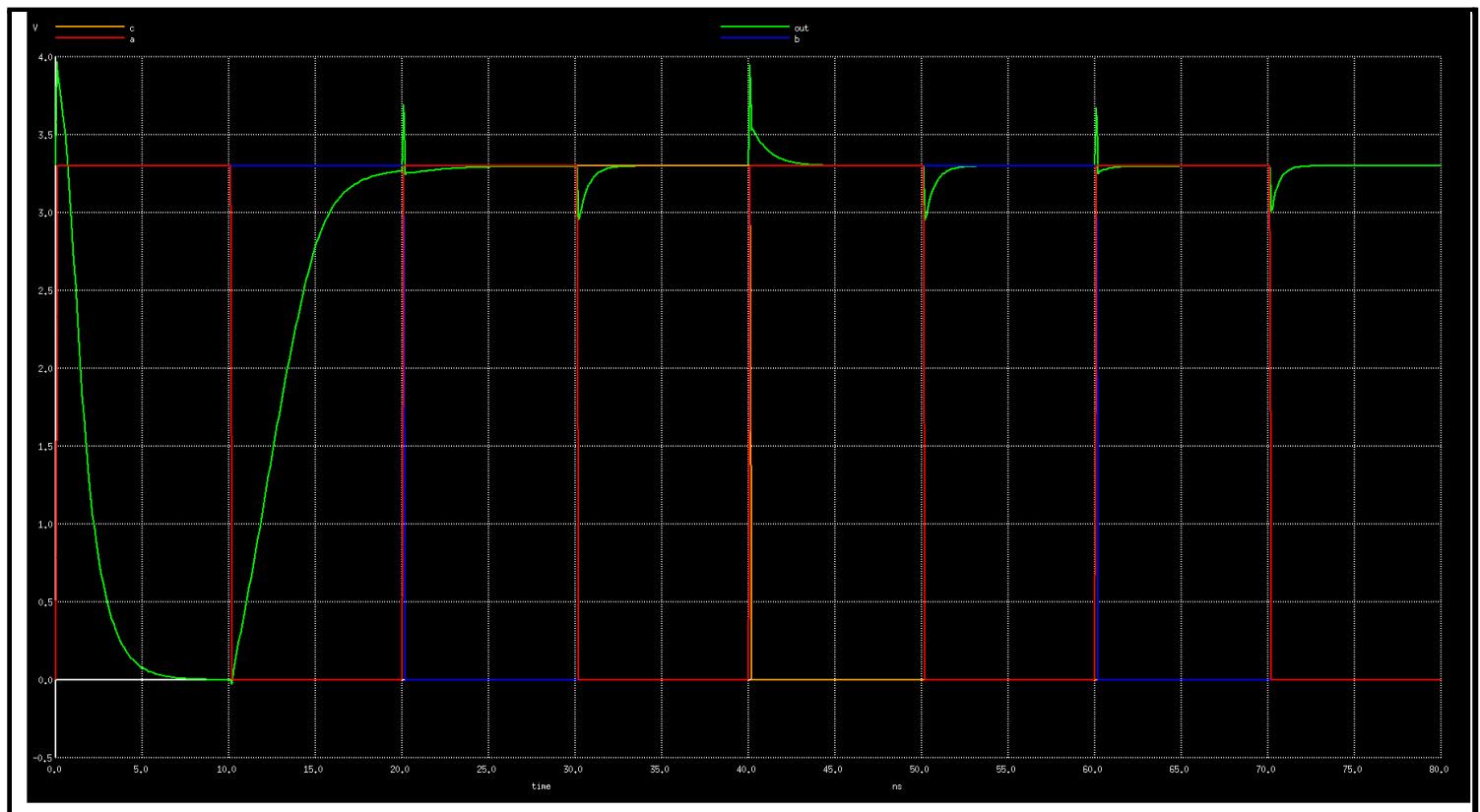
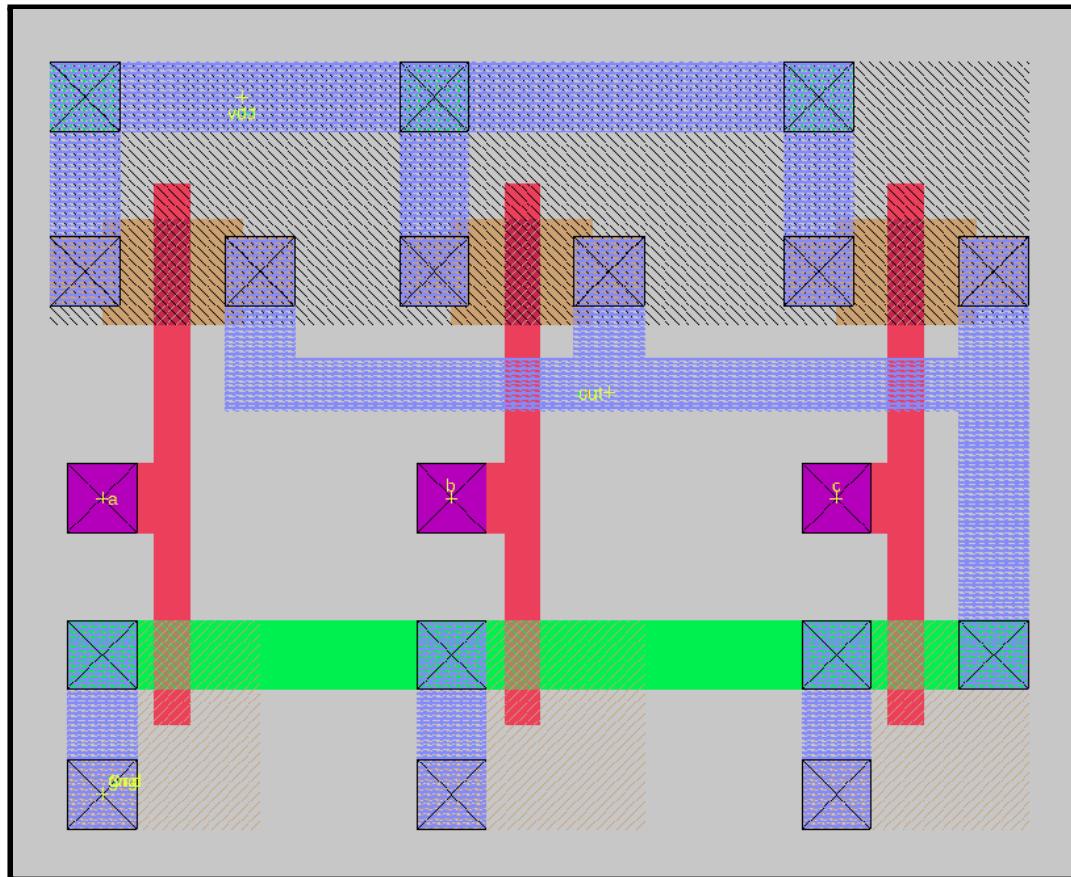
*layout of Nand_3
.include "t14y_tsmc_025_level3.txt"
.include "Or_3_7.spice"

va a 0 3.3 pulse(0 3.3 0 0n 0n 10n 20n)
vb b 0 3.3 pulse(0 3.3 0 0n 0n 20n 40n)
vc c 0 3.3 pulse(0 3.3 0 0n 0n 40n 80n)
vdd vdd 0 3.3

.control
tran 0.1n 80n
setplot tran1
plot a b c out
.endc

.end

```



**Nor\_3\_Input:****Magic File:**

```
magic
tech scmos
timestamp 1602513605
<< pwell >>
rect -6 -14 49 0
<< nwell >>
rect -7 15 50 44
<< polysilicon >>
rect -1 33 1 35
rect 22 33 24 35
rect 42 33 44 35
rect -1 13 1 15
rect 22 13 24 15
rect 42 13 44 15
rect -2 9 1 13
rect 21 9 24 13
rect 41 9 44 13
rect -1 0 1 9
rect 22 0 24 9
rect -1 -5 1 -3
rect 42 0 44 9
rect 22 -5 24 -3
rect 42 -5 44 -3
<< ndiffusion >>
rect -6 -1 -1 0
rect -2 -3 -1 -1
rect 1 -2 2 0
rect 1 -3 6 -2
rect 16 -1 22 0
rect 20 -3 22 -1
rect 24 -2 25 0
rect 24 -3 29 -2
rect 36 -1 42 0
rect 40 -3 42 -1
rect 44 -2 45 0
rect 44 -3 49 -2
<< pdiffusion >>
rect -3 30 -1 33
rect -6 15 -1 30
rect 1 15 22 33
rect 24 15 42 33
rect 44 19 49 33
rect 44 15 45 19
<< metal1 >>
rect -3 40 4 44
rect -7 34 -3 40
rect 45 5 49 15
rect 2 2 49 5
rect -6 -10 -2 -5
rect 16 -10 20 -5
rect 36 -10 40 -5
```

```

rect -2 -14 16 -10
rect 20 -14 36 -10
<< ntransistor >>
rect -1 -3 1 0
rect 22 -3 24 0
rect 42 -3 44 0
<< ptransistor >>
rect -1 15 1 33
rect 22 15 24 33
rect 42 15 44 33
<< polycontact >>
rect -6 9 -2 13
rect 17 9 21 13
rect 37 9 41 13
<< ndcontact >>
rect -6 -5 -2 -1
rect 2 -2 6 2
rect 16 -5 20 -1
rect 25 -2 29 2
rect 36 -5 40 -1
rect 45 -2 49 2
<< pdcontact >>
rect -7 30 -3 34
rect 45 15 49 19
<< psubstratecontact >>
rect -6 -14 -2 -10
rect 16 -14 20 -10
rect 36 -14 40 -10
<< nsubstratencontact >>
rect -7 40 -3 44
<< labels >>
rlabel polycontact -4 11 -4 11 3 a
rlabel metal1 47 8 47 8 7 out
rlabel psubstratecontact 17 -12 17 -12 1 Gnd
rlabel polycontact 19 11 19 11 1 b
rlabel polycontact 39 11 39 11 1 c
rlabel metal1 0 42 0 42 5 vdd
<< end >>

```

## Spice file:

```

.option scale=1u

M1000 a_1_15# a vdd vdd pfet w=18 l=2
+ ad=378 pd=78 as=97 ps=50
M1001 a_24_15# b a_1_15# vdd pfet w=18 l=2
+ ad=324 pd=72 as=0 ps=0
M1002 out c a_24_15# vdd pfet w=18 l=2
+ ad=90 pd=46 as=0 ps=0
M1003 out a Gnd Gnd nfet w=3 l=2
+ ad=69 pd=60 as=75 ps=64
M1004 out b Gnd Gnd nfet w=3 l=2
+ ad=0 pd=0 as=0 ps=0
M1005 out c Gnd Gnd nfet w=3 l=2
+ ad=0 pd=0 as=0 ps=0
C0 out 0 7.9fF
C1 c 0 5.2fF
C2 b 0 5.2fF
C3 a 0 5.2fF

```

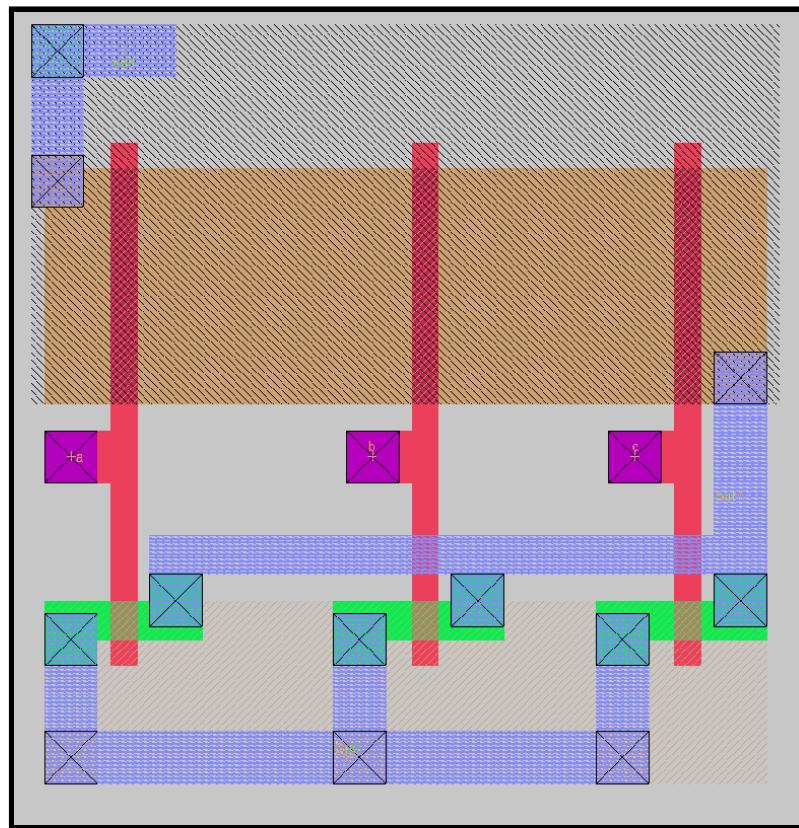
**Ngspice simulation:**

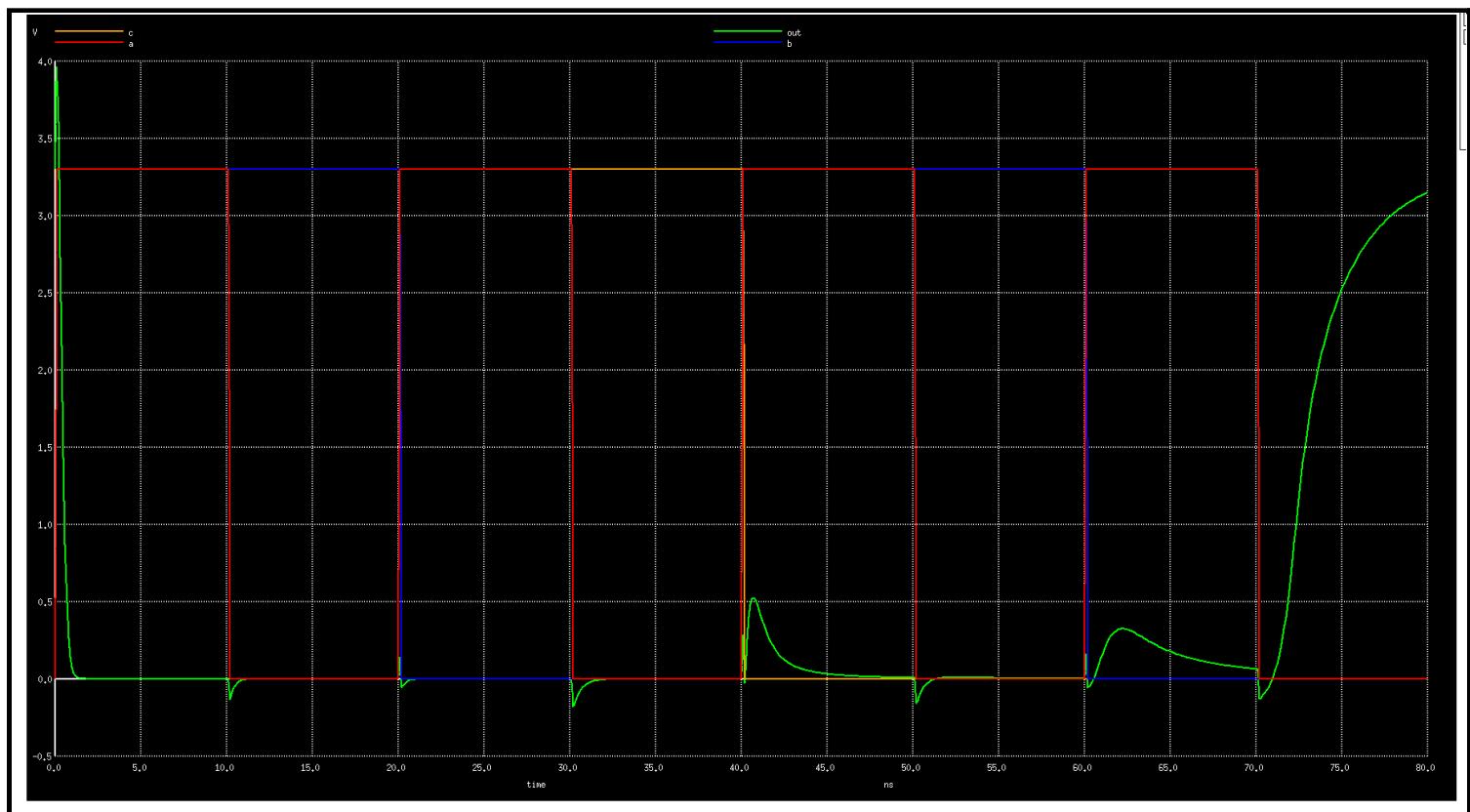
```
*layout of Nor_3
.include "t14y_tsmc_025_level3.txt"
.include "Or_3_7.spice"

va a 0 3.3 pulse(0 3.3 0 On 0n 10n 20n)
vb b 0 3.3 pulse(0 3.3 0 On 0n 20n 40n)
vc c 0 3.3 pulse(0 3.3 0 On 0n 40n 80n)
vdd vdd 0 3.3

.control
tran 0.1n 80n
setplot tran1
plot a b c out
.endc

.end
```





## And\_3\_Input:

### Magic File:

```
magic
tech scmos
timestamp 1602515327
<< pwell >>
rect -5 -43 6 -31
rect 63 -43 76 -31
<< nwell >>
rect -6 -14 50 1
rect 62 -14 76 1
<< polysilicon >>
rect 0 -8 2 -6
rect 20 -8 22 -6
rect 42 -8 44 -6
rect 68 -8 70 -6
rect 0 -22 2 -14
rect 20 -22 22 -14
rect 42 -22 44 -14
rect 68 -22 70 -14
rect -1 -26 2 -22
```

```
rect 19 -26 22 -22
rect 41 -26 44 -22
rect 67 -26 70 -22
rect 0 -31 2 -26
rect 20 -31 22 -26
rect 42 -31 44 -26
rect 68 -31 70 -26
rect 0 -37 2 -35
rect 20 -37 22 -35
rect 42 -37 44 -35
rect 68 -37 70 -35
<< ndiffusion >>
rect -1 -35 0 -31
rect 2 -35 20 -31
rect 22 -35 42 -31
rect 44 -35 46 -31
rect 67 -35 68 -31
rect 70 -35 72 -31
<< pdiffusion >>
rect -3 -9 0 -8
rect -2 -13 0 -9
rect -3 -14 0 -13
rect 2 -9 5 -8
rect 17 -9 20 -8
rect 2 -13 4 -9
rect 18 -13 20 -9
rect 2 -14 5 -13
rect 17 -14 20 -13
rect 22 -9 25 -8
rect 39 -9 42 -8
rect 22 -13 24 -9
rect 40 -13 42 -9
rect 22 -14 25 -13
rect 39 -14 42 -13
rect 44 -9 47 -8
rect 65 -9 68 -8
rect 44 -13 46 -9
rect 66 -13 68 -9
rect 44 -14 47 -13
rect 65 -14 68 -13
rect 70 -9 73 -8
rect 70 -13 72 -9
rect 70 -14 73 -13
<< metal1 >>
rect -2 -3 14 1
rect 18 -3 36 1
rect 40 -3 62 1
rect -6 -9 -2 -3
rect 14 -9 18 -3
rect 36 -9 40 -3
rect 62 -9 66 -3
rect 4 -16 8 -13
rect 24 -16 28 -13
rect 46 -16 50 -13
rect 4 -19 50 -16
rect 46 -22 50 -19
rect 46 -26 63 -22
rect 46 -31 50 -26
rect 72 -31 76 -13
rect -5 -39 -1 -35
rect 63 -39 67 -35
```

```

rect -1 -43 63 -39
<< ntransistor >>
rect 0 -35 2 -31
rect 20 -35 22 -31
rect 42 -35 44 -31
rect 68 -35 70 -31
<< ptransistor >>
rect 0 -14 2 -8
rect 20 -14 22 -8
rect 42 -14 44 -8
rect 68 -14 70 -8
<< polycontact >>
rect -5 -26 -1 -22
rect 15 -26 19 -22
rect 37 -26 41 -22
rect 63 -26 67 -22
<< ndcontact >>
rect -5 -35 -1 -31
rect 46 -35 50 -31
rect 63 -35 67 -31
rect 72 -35 76 -31
<< pdcontact >>
rect -6 -13 -2 -9
rect 4 -13 8 -9
rect 14 -13 18 -9
rect 24 -13 28 -9
rect 36 -13 40 -9
rect 46 -13 50 -9
rect 62 -13 66 -9
rect 72 -13 76 -9
<< psubstratepcontact >>
rect -5 -43 -1 -39
rect 63 -43 67 -39
<< nsubstratencontact >>
rect -6 -3 -2 1
rect 14 -3 18 1
rect 36 -3 40 1
rect 62 -3 66 1
<< labels >>
rlabel polycontact -3 -24 -3 -24 3 a
rlabel polycontact 17 -24 17 -24 1 b
rlabel metal1 5 -1 5 -1 5 vdd
rlabel polycontact 39 -24 39 -24 1 c
rlabel psubstratepcontact -3 -41 -3 -41 2 Gnd
rlabel metal1 74 -22 74 -22 7 out
<< end >>

```

**Spice file:**

```

.option scale=1u

M1000 a_2_n14# a vdd vdd pfet w=6 l=2
+ ad=90 pd=72 as=120 ps=96
M1001 a_2_n14# b vdd vdd pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1002 a_2_n14# c vdd vdd pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1003 out a_2_n14# vdd vdd pfet w=6 l=2
+ ad=30 pd=24 as=0 ps=0

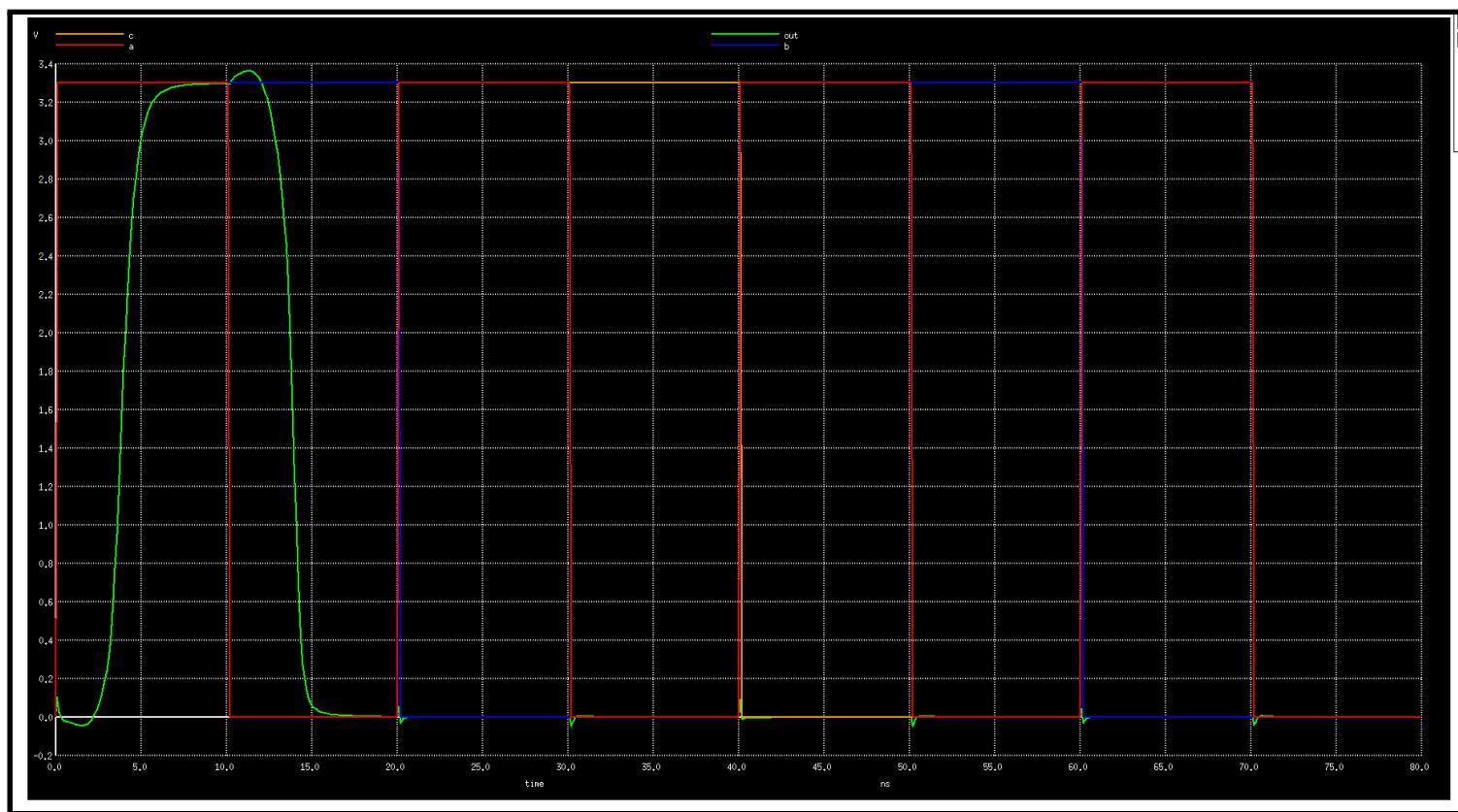
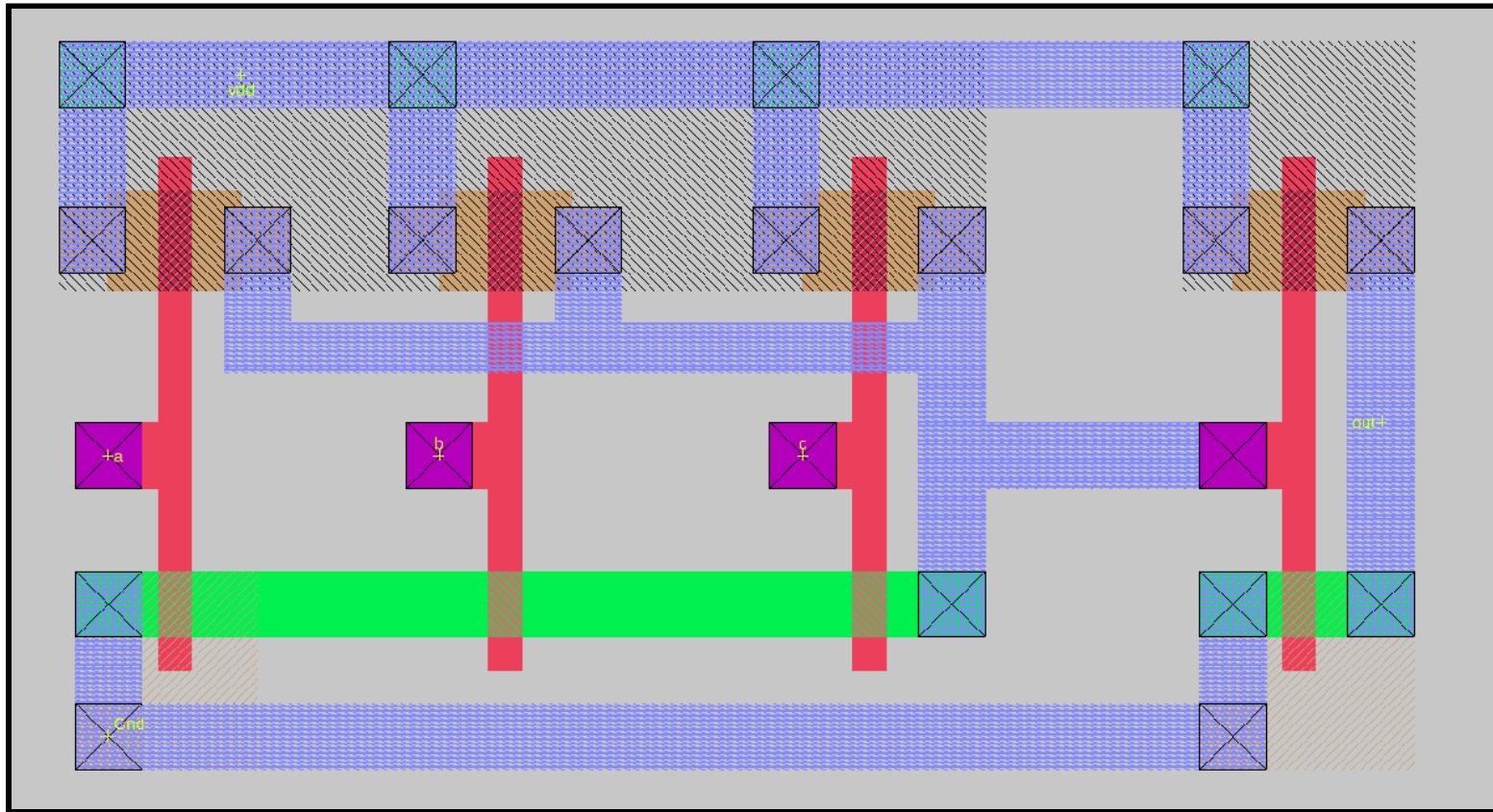
```

```
M1004 a_2_n35# a Gnd Gnd nfet w=4 l=2
+ ad=72 pd=44 as=40 ps=36
M1005 a_22_n35# b a_2_n35# Gnd nfet w=4 l=2
+ ad=80 pd=48 as=0 ps=0
M1006 a_2_n14# c a_22_n35# Gnd nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
M1007 out a_2_n14# Gnd Gnd nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
C0 out 0 3.2fF
C1 a_2_n14# 0 17.4fF
C2 c 0 6.6fF
C3 b 0 6.6fF
C4 a 0 5.6fF
C5 Gnd 0 10.7fF
C6 vdd 0 2.3fF
```

### Ngspice simulation:

```
*layout of And_3
.include "t14y_tsmc_025_level3.txt"
.include "Or_3_7.spice"

va a 0 3.3 pulse(0 3.3 0 On 0n 10n 20n)
vb b 0 3.3 pulse(0 3.3 0 On 0n 20n 40n)
vc c 0 3.3 pulse(0 3.3 0 On 0n 40n 80n)
vdd vdd 0 3.3
.control
tran 0.1n 80n
setplot tran1
plot a b c out
.endc
.end
```



**Or\_3\_Input:****Magic file:**

```
magic
tech scmos
timestamp 1602514500
<< pwell >>
rect -6 -14 49 0
rect 60 -14 76 0
<< nwell >>
rect -7 15 50 44
rect 59 15 77 29
<< polysilicon >>
rect -1 33 1 35
rect 22 33 24 35
rect 42 33 44 35
rect 69 21 71 23
rect -1 13 1 15
rect 22 13 24 15
rect 42 13 44 15
rect 69 13 71 15
rect -2 9 1 13
rect 21 9 24 13
rect 41 9 44 13
rect 68 9 71 13
rect -1 0 1 9
rect 22 0 24 9
rect -1 -5 1 -3
rect 42 0 44 9
rect 22 -5 24 -3
rect 69 0 71 9
rect 42 -5 44 -3
rect 69 -5 71 -3
<< ndiffusion >>
rect -6 -1 -1 0
rect -2 -3 -1 -1
rect 1 -2 2 0
rect 1 -3 6 -2
rect 16 -1 22 0
rect 20 -3 22 -1
rect 24 -2 25 0
rect 24 -3 29 -2
rect 36 -1 42 0
rect 40 -3 42 -1
rect 44 -2 45 0
rect 44 -3 49 -2
rect 63 -1 69 0
rect 67 -3 69 -1
rect 71 -2 72 0
rect 71 -3 76 -2
<< pdiffusion >>
rect -3 30 -1 33
rect -6 15 -1 30
rect 1 15 22 33
rect 24 15 42 33
rect 44 19 49 33
rect 44 15 45 19
```

```
rect 63 17 69 21
rect 60 15 69 17
rect 71 19 76 21
rect 71 15 72 19
<< metal1 >>
rect -3 40 63 44
rect -7 34 -3 40
rect 59 29 63 40
rect 59 21 63 25
rect 45 13 49 15
rect 45 9 64 13
rect 45 5 49 9
rect 2 2 49 5
rect -6 -10 -2 -5
rect 16 -10 20 -5
rect 72 2 76 15
rect 36 -10 40 -5
rect 63 -10 67 -5
rect -2 -14 16 -10
rect 20 -14 36 -10
rect 40 -14 63 -10
rect 67 -14 71 -10
<< ntransistor >>
rect -1 -3 1 0
rect 22 -3 24 0
rect 42 -3 44 0
rect 69 -3 71 0
<< ptransistor >>
rect -1 15 1 33
rect 22 15 24 33
rect 42 15 44 33
rect 69 15 71 21
<< polycontact >>
rect -6 9 -2 13
rect 17 9 21 13
rect 37 9 41 13
rect 64 9 68 13
<< ndcontact >>
rect -6 -5 -2 -1
rect 2 -2 6 2
rect 16 -5 20 -1
rect 25 -2 29 2
rect 36 -5 40 -1
rect 45 -2 49 2
rect 63 -5 67 -1
rect 72 -2 76 2
<< pdcontact >>
rect -7 30 -3 34
rect 45 15 49 19
rect 59 17 63 21
rect 72 15 76 19
<< psubstratepcontact >>
rect -6 -14 -2 -10
rect 16 -14 20 -10
rect 36 -14 40 -10
rect 63 -14 67 -10
<< nsubstratencontact >>
rect -7 40 -3 44
rect 59 25 63 29
<< labels >>
rlabel polycontact -4 11 -4 11 3 a
```

```
rlabel psubstratecontact 17 -12 17 -12 1 Gnd
rlabel polycontact 19 11 19 11 1 b
rlabel polycontact 39 11 39 11 1 c
rlabel metal1 0 42 0 42 5 vdd
rlabel metal1 74 8 74 8 7 out
<< end >>
```

**Spice file:**

```
.option scale=1u

M1000 a_1_15# a vdd vdd pfet w=18 l=2
+ ad=378 pd=78 as=155 ps=82
M1001 a_24_15# b a_1_15# vdd vdd pfet w=18 l=2
+ ad=324 pd=72 as=0 ps=0
M1002 a_1_n3# c a_24_15# vdd vdd pfet w=18 l=2
+ ad=90 pd=46 as=0 ps=0
M1003 out a_1_n3# vdd vdd pfet w=6 l=2
+ ad=30 pd=22 as=0 ps=0
M1004 a_1_n3# a Gnd Gnd nfet w=3 l=2
+ ad=69 pd=60 as=101 ps=86
M1005 a_1_n3# b Gnd Gnd nfet w=3 l=2
+ ad=0 pd=0 as=0 ps=0
M1006 a_1_n3# c Gnd Gnd nfet w=3 l=2
+ ad=0 pd=0 as=0 ps=0
M1007 out a_1_n3# Gnd Gnd nfet w=3 l=2
+ ad=23 pd=20 as=0 ps=0
C0 out 0 2.4fF
C1 a_1_n3# 0 15.9fF
C2 c 0 5.2fF
C3 b 0 5.2fF
C4 a 0 5.2fF
C5 Gnd 0 2.1fF
C6 vdd 0 4.5fF
```

**Ngspice simulation:**

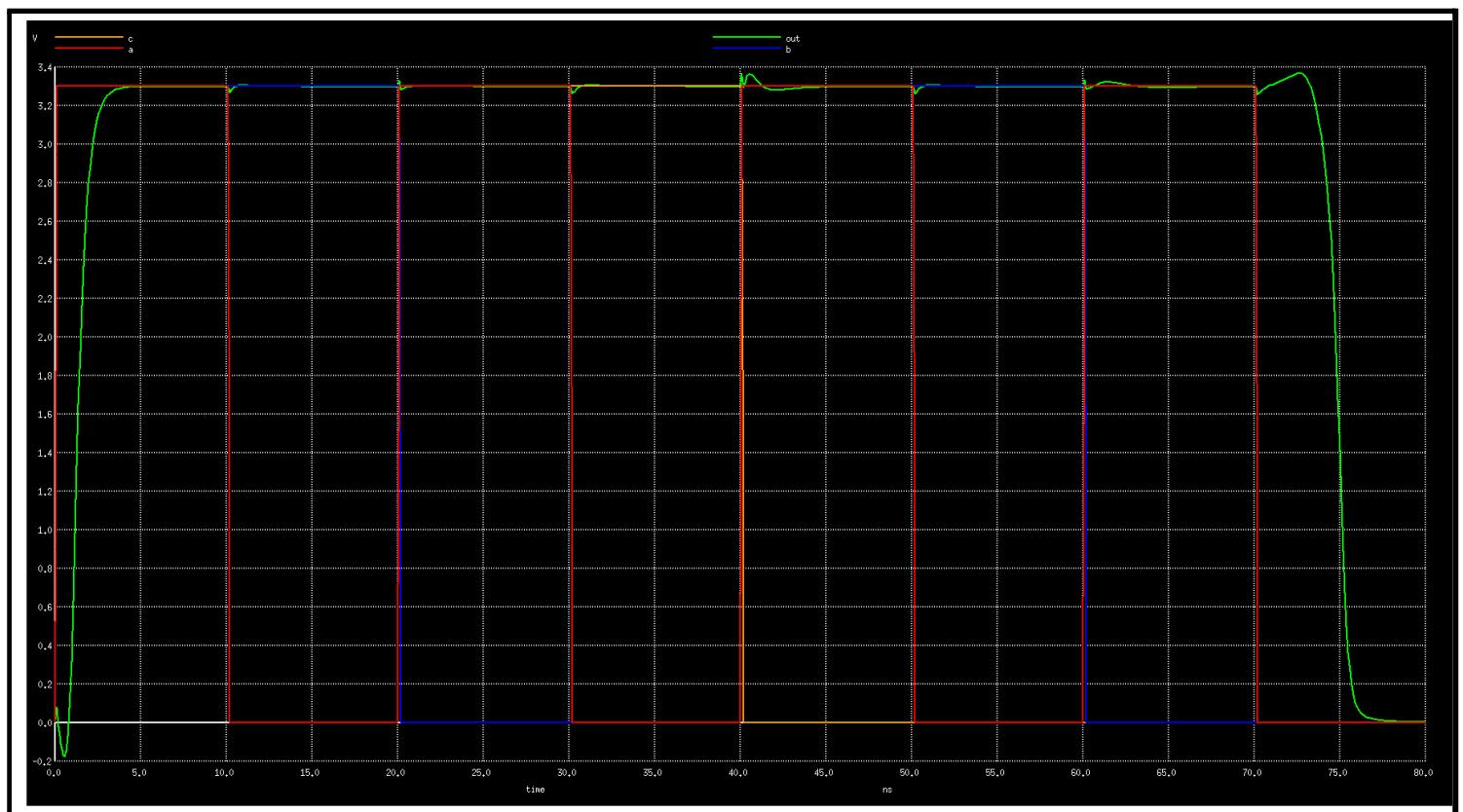
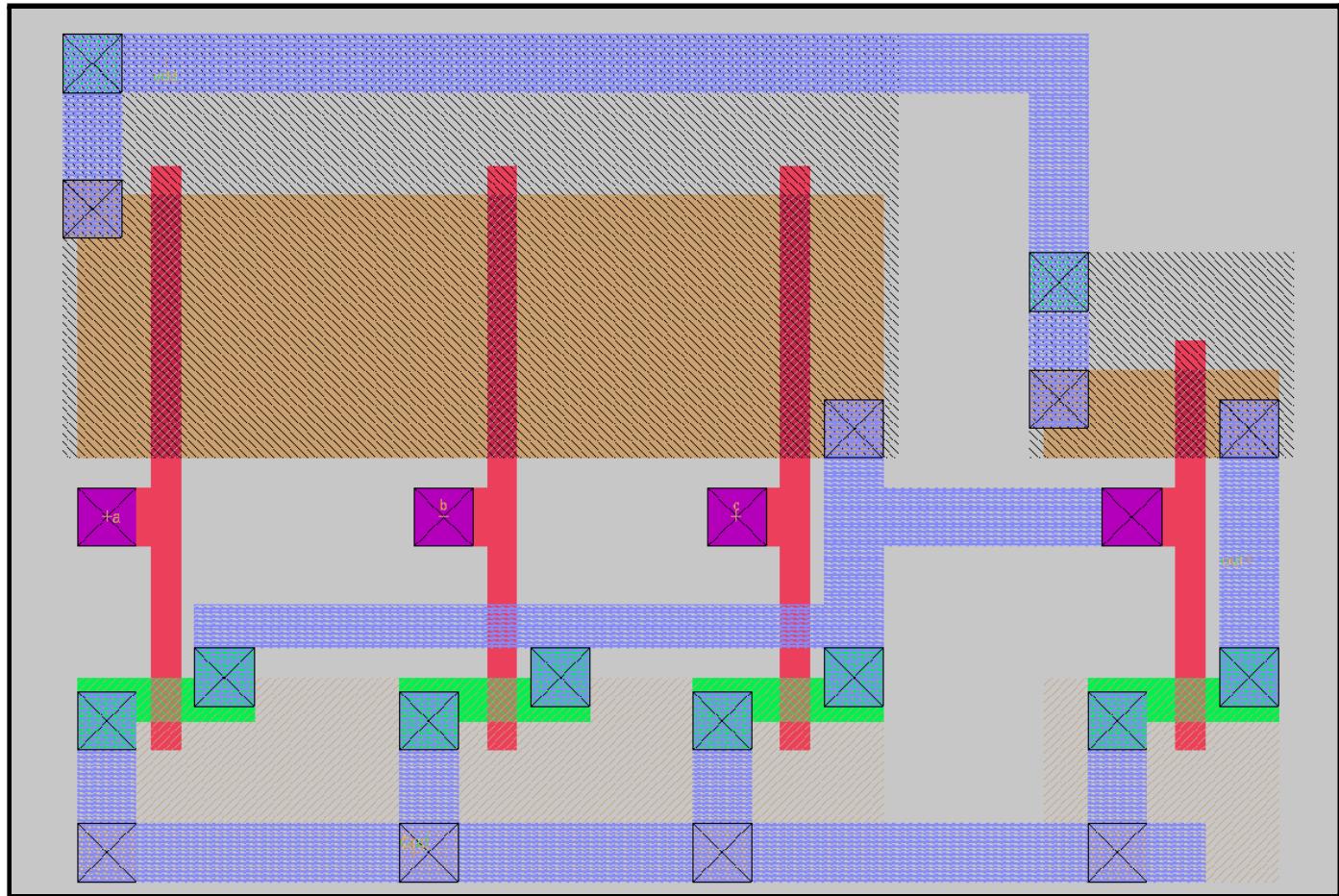
```
*layout of Or_3

.include "t14y_tsmc_025_level3.txt"
.include "Or_3_7.spice"

va a 0 3.3 pulse(0 3.3 0 0n 10n 20n)
vb b 0 3.3 pulse(0 3.3 0 0n 0n 20n 40n)
vc c 0 3.3 pulse(0 3.3 0 0n 0n 40n 80n)
vdd vdd 0 3.3

.control
tran 0.1n 80n
setplot tran1
plot a b c out
.endc

.end
```



**D\_latch:****Spice file:****Using Nand gates:**

```
.option scale=1u

M1000 a_2_n14# D w_n6_n14# w_n6_n14# pfet w=6 l=2
+ ad=72 pd=48 as=72 ps=48
M1001 a_2_n14# Clk w_n6_n14# w_n6_n14# pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1002 Q a_2_n14# w_63_n12# w_63_n12# pfet w=6 l=2
+ ad=72 pd=48 as=72 ps=48
M1003 Q Qbar w_63_n12# w_63_n12# pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1004 a_2_n35# D w_n5_n43# w_n5_n43# nfet w=4 l=2
+ ad=76 pd=46 as=20 ps=18
M1005 a_2_n14# Clk a_2_n35# w_19_n43# nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
M1006 a_71_n33# a_2_n14# w_64_n41# w_64_n41# nfet w=4 l=2
+ ad=76 pd=46 as=20 ps=18
M1007 Q Qbar a_71_n33# w_88_n41# nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
M1008 a_n25_n93# D w_n32_n72# w_n32_n72# pfet w=6 l=2
+ ad=36 pd=24 as=30 ps=22
M1009 a_2_n73# Clk w_n6_n73# w_n6_n73# pfet w=6 l=2
+ ad=72 pd=48 as=72 ps=48
M1010 a_2_n73# a_n25_n93# w_n6_n73# w_n6_n73# pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1011 Qbar Q w_63_n73# w_63_n73# pfet w=6 l=2
+ ad=72 pd=48 as=72 ps=48
M1012 Qbar a_2_n73# w_63_n73# w_63_n73# pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1013 a_n25_n93# D w_n32_n102# w_n32_n102# nfet w=3 l=2
+ ad=22 pd=20 as=19 ps=18
M1014 a_2_n94# Clk w_n5_n102# w_n5_n102# nfet w=4 l=2
+ ad=76 pd=46 as=20 ps=18
M1015 a_2_n73# a_n25_n93# a_2_n94# w_19_n102# nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
M1016 a_71_n94# Q w_64_n102# w_64_n102# nfet w=4 l=2
+ ad=76 pd=46 as=20 ps=18
M1017 Qbar a_2_n73# a_71_n94# w_88_n102# nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
C0 a_2_n73# 0 22.9fF
C1 a_n25_n93# 0 15.3fF
C2 Q 0 47.6fF
C3 Qbar 0 48.0fF
C4 a_2_n14# 0 19.6fF
```

## Using Transmission gates

```
.option scale=1u

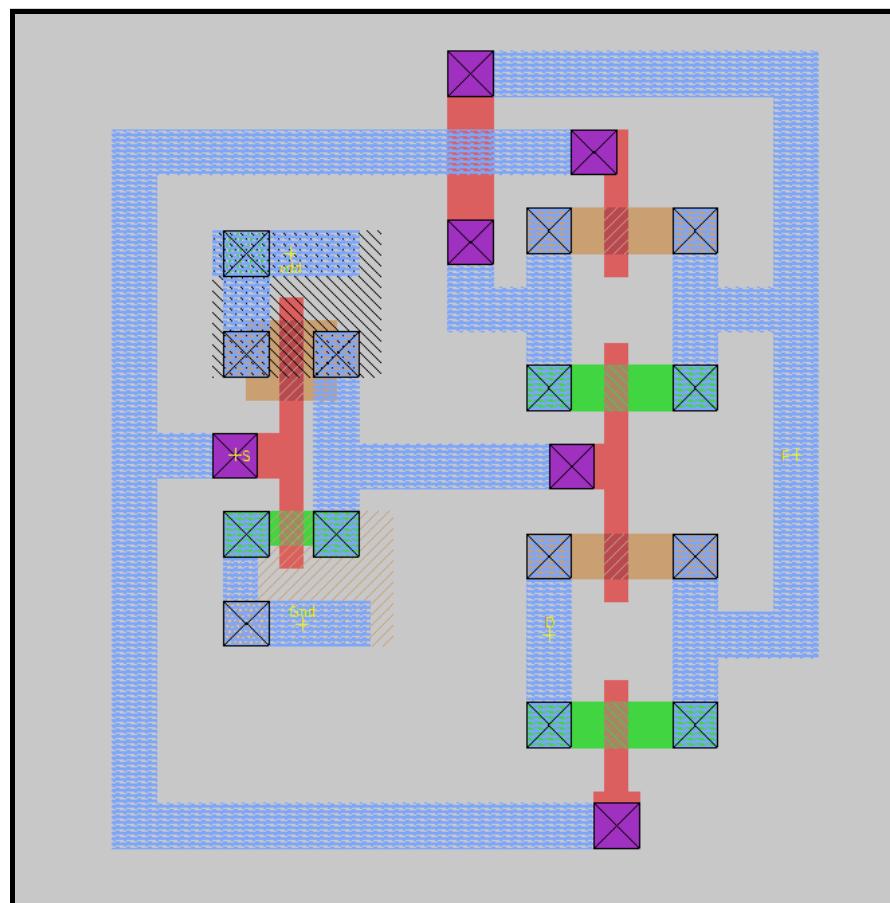
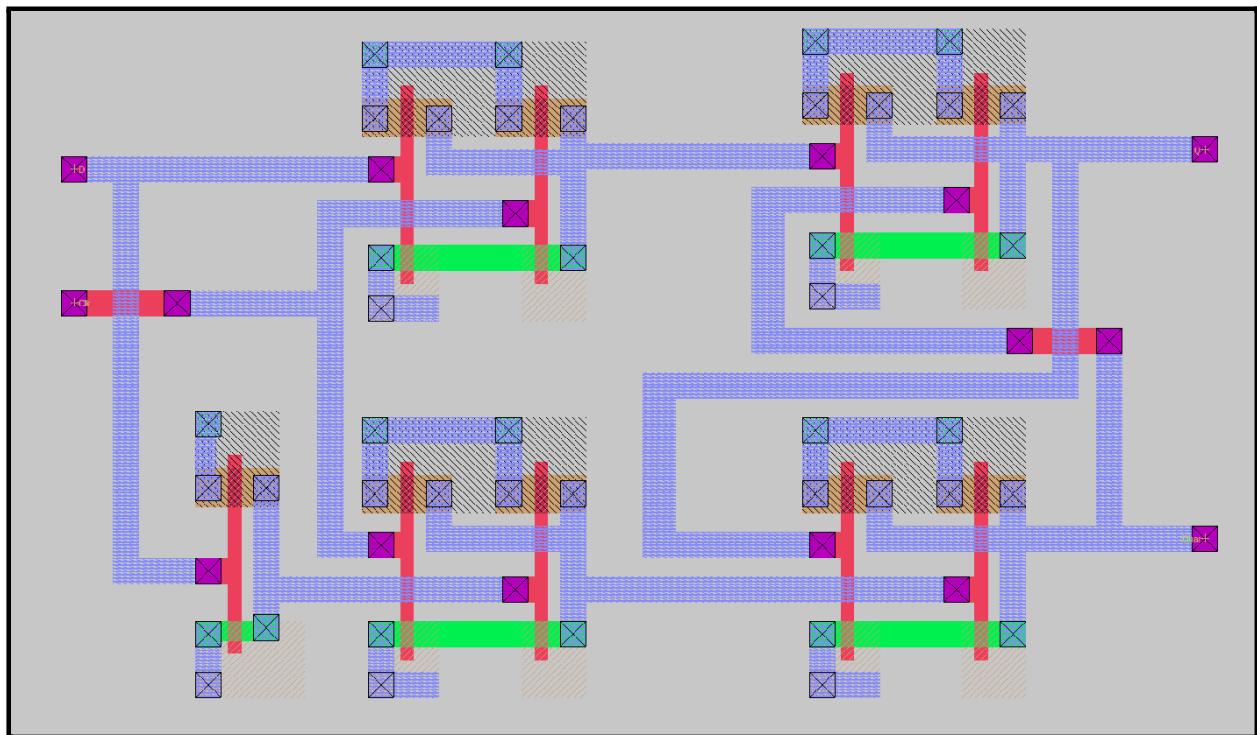
M1000 F S F w_35_58# pfet w=4 l=2
+ ad=92 pd=70 as=0 ps=0
M1001 a_15_33# S vdd vdd pfet w=7 l=2
+ ad=29 pd=24 as=29 ps=24
M1002 F a_15_33# F Gnd nfet w=4 l=2
+ ad=92 pd=70 as=0 ps=0
M1003 a_15_33# S Gnd Gnd nfet w=3 l=2
+ ad=19 pd=18 as=19 ps=18
M1004 F a_15_33# D w_35_26# pfet w=4 l=2
+ ad=0 pd=0 as=28 ps=22
M1005 F S D Gnd nfet w=4 l=2
+ ad=0 pd=0 as=28 ps=22
C0 w_35_58# S 3.7fF
C1 a_15_33# 0 9.9fF
C2 S 0 35.4fF
```

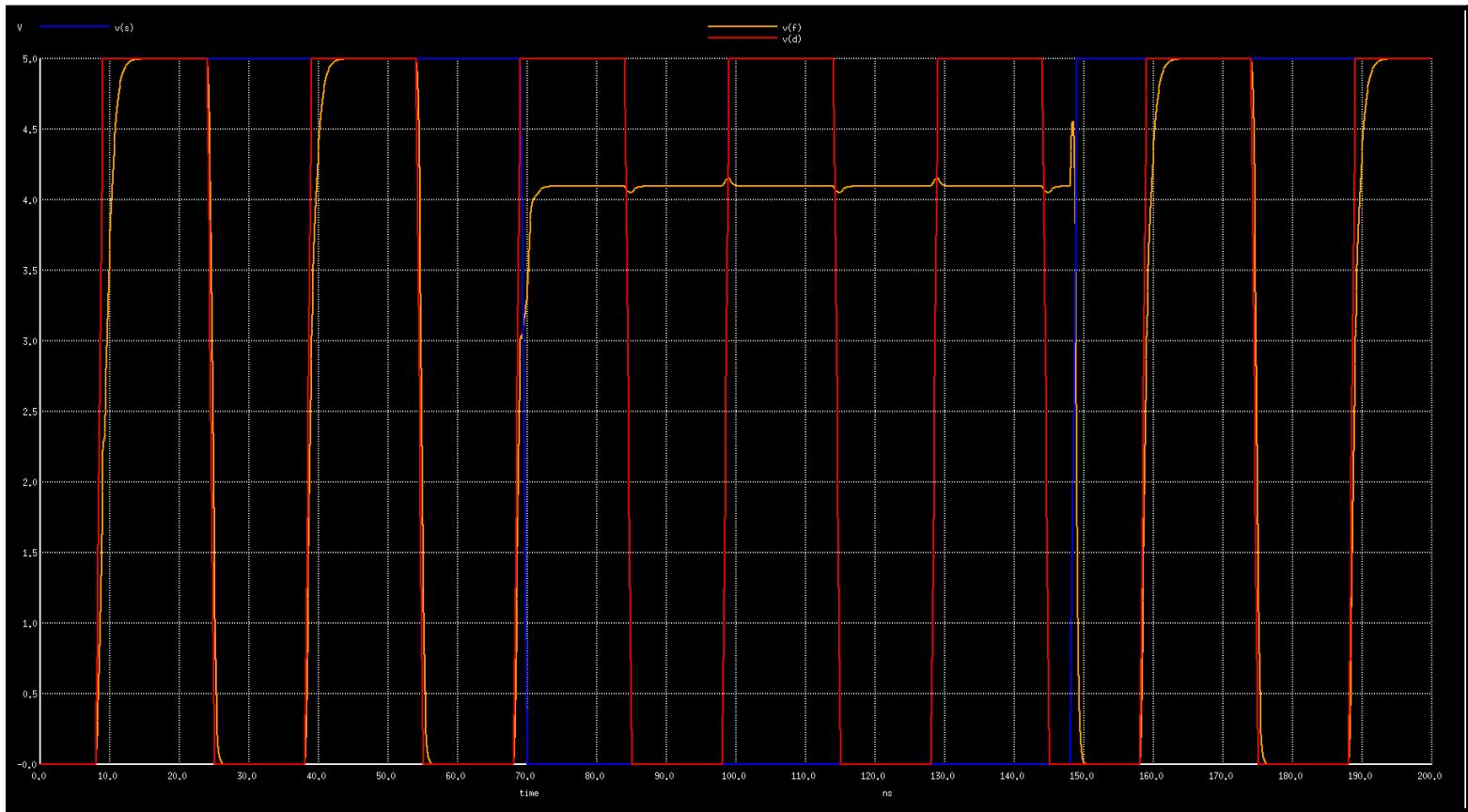
## Ngspice simulation:

```
.include ./t14y_tsmc_025_level3.txt
.include ./D_latch_7_new.spice

v_dd vdd 0 5
v_d S 0 dc 2.5 pulse(0 5 8n 1n 1n 60n 140n)
v_e D 0 dc 2.5 pulse(0 5 8n 1n 1n 15n 30n)

.control
  tran 0.1n 200n
  plot V(D), V(S), V(F)
.endc
```





## D\_FF:

### Magic File:

Due to the huge file size I am not including the magic file.

### Spice file:

### Using Nand gates:

```
.option scale=1u

M1000 a_2_n14# D w_n6_n14# w_n6_n14# pfet w=6 l=2
+ ad=72 pd=48 as=72 ps=48
M1001 a_2_n14# Clk w_n6_n14# w_n6_n14# pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1002 a_64_n80# a_2_n14# w_63_n12# w_63_n12# pfet w=6 l=2
+ ad=72 pd=48 as=72 ps=48
M1003 a_64_n80# a_71_n73# w_63_n12# w_63_n12# pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
```

```

M1004 a_171_n11# a_64_n80# w_163_n11# w_163_n11# pfet w=6 l=2
+ ad=72 pd=48 as=72 ps=48
M1005 a_171_n11# a_115_n121# w_163_n11# w_163_n11# pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1006 Q a_171_n11# w_232_n9# w_232_n9# pfet w=6 l=2
+ ad=72 pd=48 as=72 ps=48
M1007 Q Qbar w_232_n9# w_232_n9# pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1008 a_2_n35# D w_n5_n43# w_n5_n43# nfet w=4 l=2
+ ad=76 pd=46 as=20 ps=18
M1009 a_2_n14# Clk a_2_n35# w_19_n43# nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
M1010 a_71_n33# a_2_n14# w_64_n41# w_64_n41# nfet w=4 l=2
+ ad=76 pd=46 as=20 ps=18
M1011 a_64_n80# a_71_n73# a_71_n33# w_88_n41# nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
M1012 a_171_n32# a_64_n80# w_164_n40# w_164_n40# nfet w=4 l=2
+ ad=76 pd=46 as=20 ps=18
M1013 a_171_n11# a_115_n121# a_171_n32# w_188_n40# nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
M1014 a_240_n30# a_171_n11# w_233_n38# w_233_n38# nfet w=4 l=2
+ ad=76 pd=46 as=20 ps=18
M1015 Q Qbar a_240_n30# w_257_n38# nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
M1016 a_n25_n93# D w_n32_n72# w_n32_n72# pfet w=6 l=2
+ ad=36 pd=24 as=30 ps=22
M1017 a_171_n67# a_115_n121# w_163_n67# w_163_n67# pfet w=6 l=2
+ ad=72 pd=48 as=72 ps=48
M1018 a_171_n67# a_71_n73# w_163_n67# w_163_n67# pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1019 a_2_n73# Clk w_n6_n73# w_n6_n73# pfet w=6 l=2
+ ad=72 pd=48 as=72 ps=48
M1020 a_2_n73# a_n25_n93# w_n6_n73# w_n6_n73# pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1021 a_71_n73# a_64_n80# w_63_n73# w_63_n73# pfet w=6 l=2
+ ad=72 pd=48 as=72 ps=48
M1022 a_71_n73# a_2_n73# w_63_n73# w_63_n73# pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1023 a_n25_n93# D w_n32_n102# w_n32_n102# nfet w=3 l=2
+ ad=22 pd=20 as=19 ps=18
M1024 Qbar Q w_232_n70# w_232_n70# pfet w=6 l=2
+ ad=72 pd=48 as=72 ps=48
M1025 Qbar a_171_n67# w_232_n70# w_232_n70# pfet w=6 l=2
+ ad=0 pd=0 as=0 ps=0
M1026 a_171_n88# a_115_n121# w_164_n96# w_164_n96# nfet w=4 l=2
+ ad=76 pd=46 as=20 ps=18
M1027 a_171_n67# a_71_n73# a_171_n88# w_188_n96# nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
M1028 a_2_n94# Clk w_n5_n102# w_n5_n102# nfet w=4 l=2
+ ad=76 pd=46 as=20 ps=18
M1029 a_2_n73# a_n25_n93# a_2_n94# w_19_n102# nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
M1030 a_71_n94# a_64_n80# w_64_n102# w_64_n102# nfet w=4 l=2
+ ad=76 pd=46 as=20 ps=18
M1031 a_71_n73# a_2_n73# a_71_n94# w_88_n102# nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
M1032 a_240_n91# Q w_233_n99# w_233_n99# nfet w=4 l=2
+ ad=76 pd=46 as=20 ps=18
M1033 Qbar a_171_n67# a_240_n91# w_257_n99# nfet w=4 l=2
+ ad=24 pd=20 as=0 ps=0
M1034 a_115_n121# Clk w_108_n100# w_108_n100# pfet w=6 l=2

```

```
+ ad=36 pd=24 as=30 ps=22
M1035 a_115_n121# Clk w_108_n130# w_108_n130# nfet w=3 l=2
+ ad=22 pd=20 as=19 ps=18
C0 a_171_n67# 0 22.9fF
C1 a_2_n73# 0 22.9fF
C2 a_n25_n93# 0 15.3fF
C3 Q 0 47.6fF
C4 a_115_n121# 0 46.7fF
C5 a_64_n80# 0 58.9fF
C6 a_71_n73# 0 62.4fF
C7 a_2_n14# 0 19.6fF
C8 Qbar 0 48.0fF
C9 a_171_n11# 0 19.4fF
```

## Using Transmission gates

```
.option scale=1u

M1000 a_28_58# S a_28_58# w_35_58# pfet w=4 l=2
+ ad=120 pd=92 as=0 ps=0
M1001 F S a_28_58# w_123_59# pfet w=4 l=2
+ ad=92 pd=70 as=0 ps=0
M1002 a_15_33# S vdd vdd pfet w=7 l=2
+ ad=29 pd=24 as=29 ps=24
M1003 a_28_58# a_15_33# a_28_58# Gnd nfet w=4 l=2
+ ad=120 pd=92 as=0 ps=0
M1004 a_103_34# S vdd1 vdd1 pfet w=7 l=2
+ ad=29 pd=24 as=29 ps=24
M1005 F a_103_34# a_28_58# Gnd nfet w=4 l=2
+ ad=92 pd=70 as=0 ps=0
M1006 a_15_33# S Gnd Gnd nfet w=3 l=2
+ ad=19 pd=18 as=19 ps=18
M1007 a_28_58# a_15_33# D w_35_26# pfet w=4 l=2
+ ad=0 pd=0 as=28 ps=22
M1008 a_103_34# S Gnd1 Gnd1 nfet w=3 l=2
+ ad=19 pd=18 as=19 ps=18
M1009 F a_103_34# F w_123_27# pfet w=4 l=2
+ ad=0 pd=0 as=0 ps=0
M1010 a_28_58# S D Gnd nfet w=4 l=2
+ ad=0 pd=0 as=28 ps=22
M1011 F S F Gnd nfet w=4 l=2
+ ad=0 pd=0 as=0 ps=0
C0 S w_123_59# 2.9fF
```

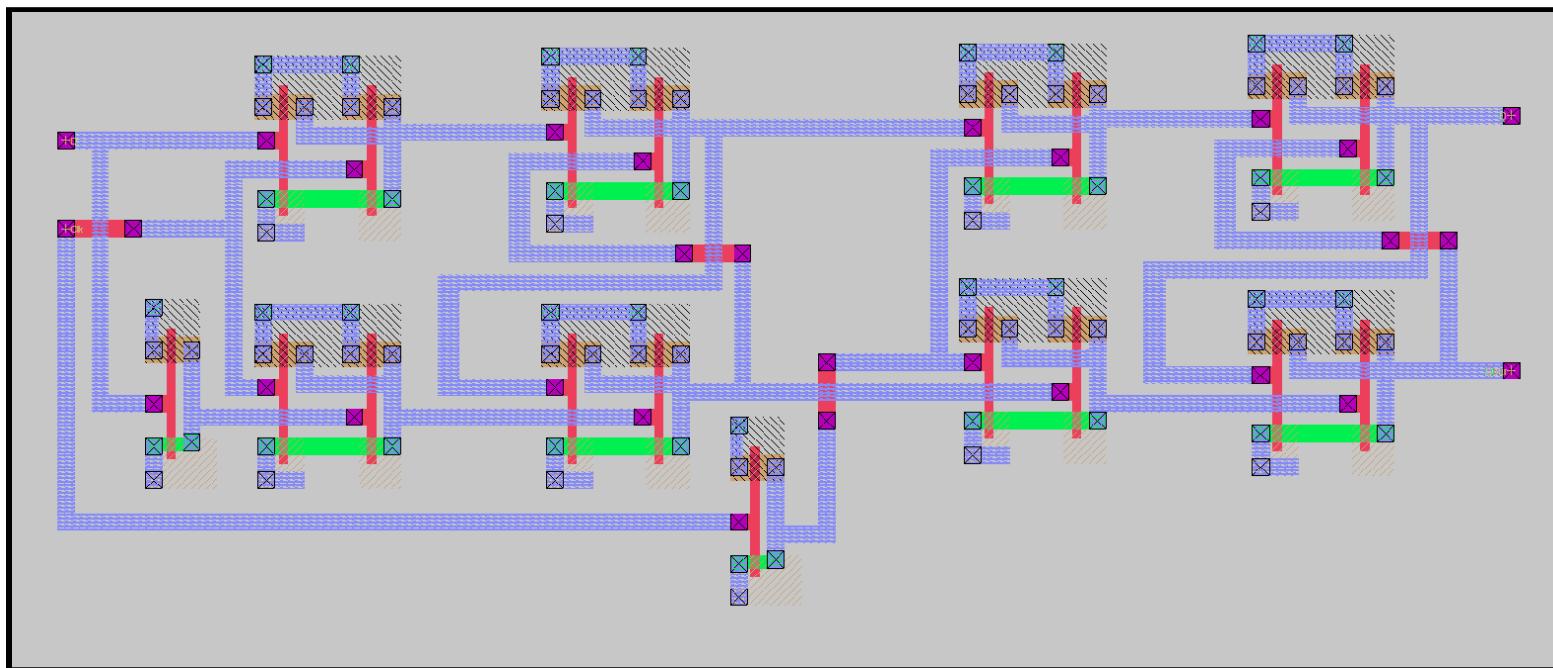
C1 S w\_35\_58# 3.7fF  
C2 a\_103\_34# 0 9.9fF  
C3 a\_15\_33# 0 9.9fF  
C4 S 0 82.5fF  
C5 a\_28\_58# 0 48.8fF

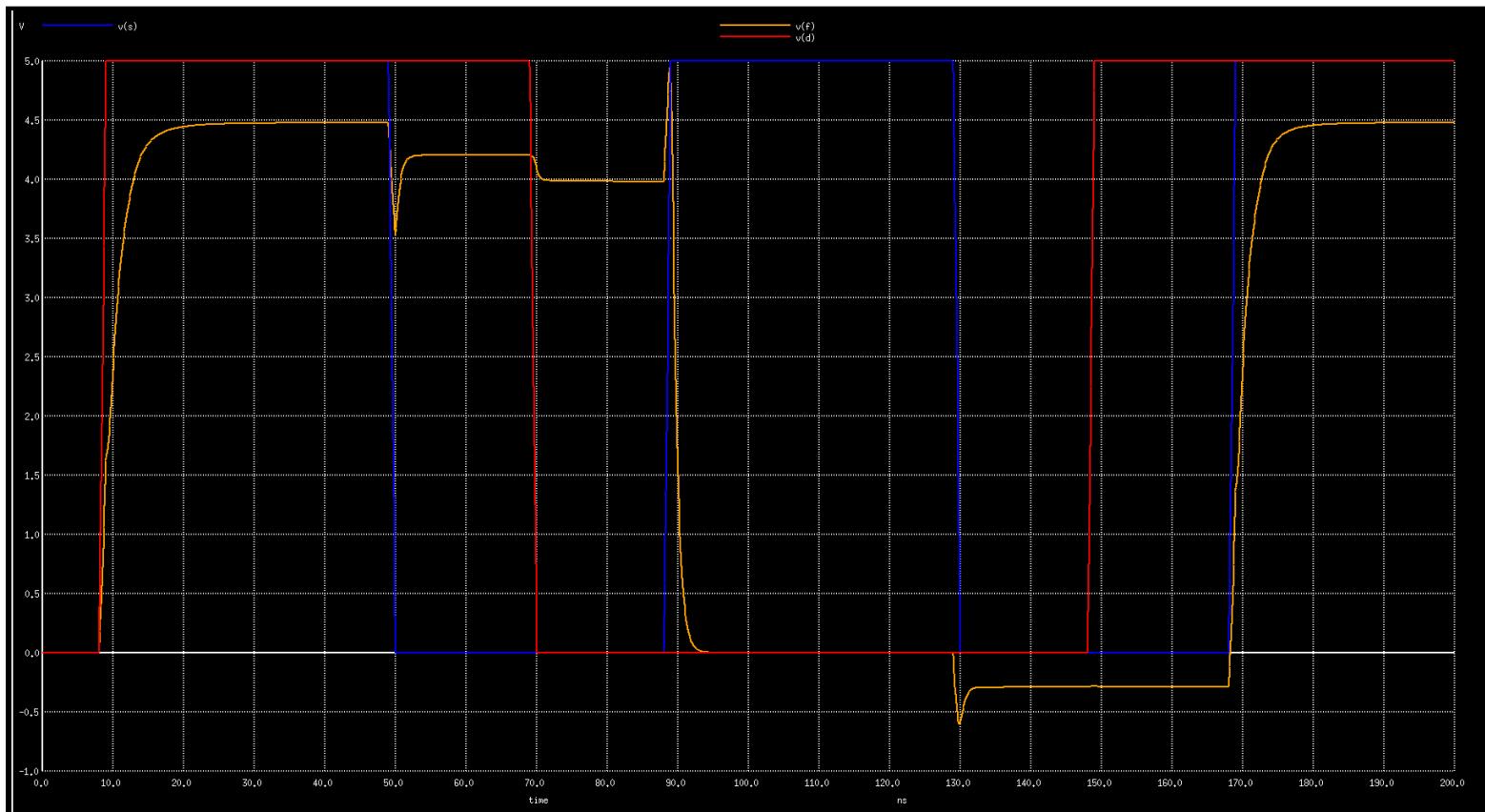
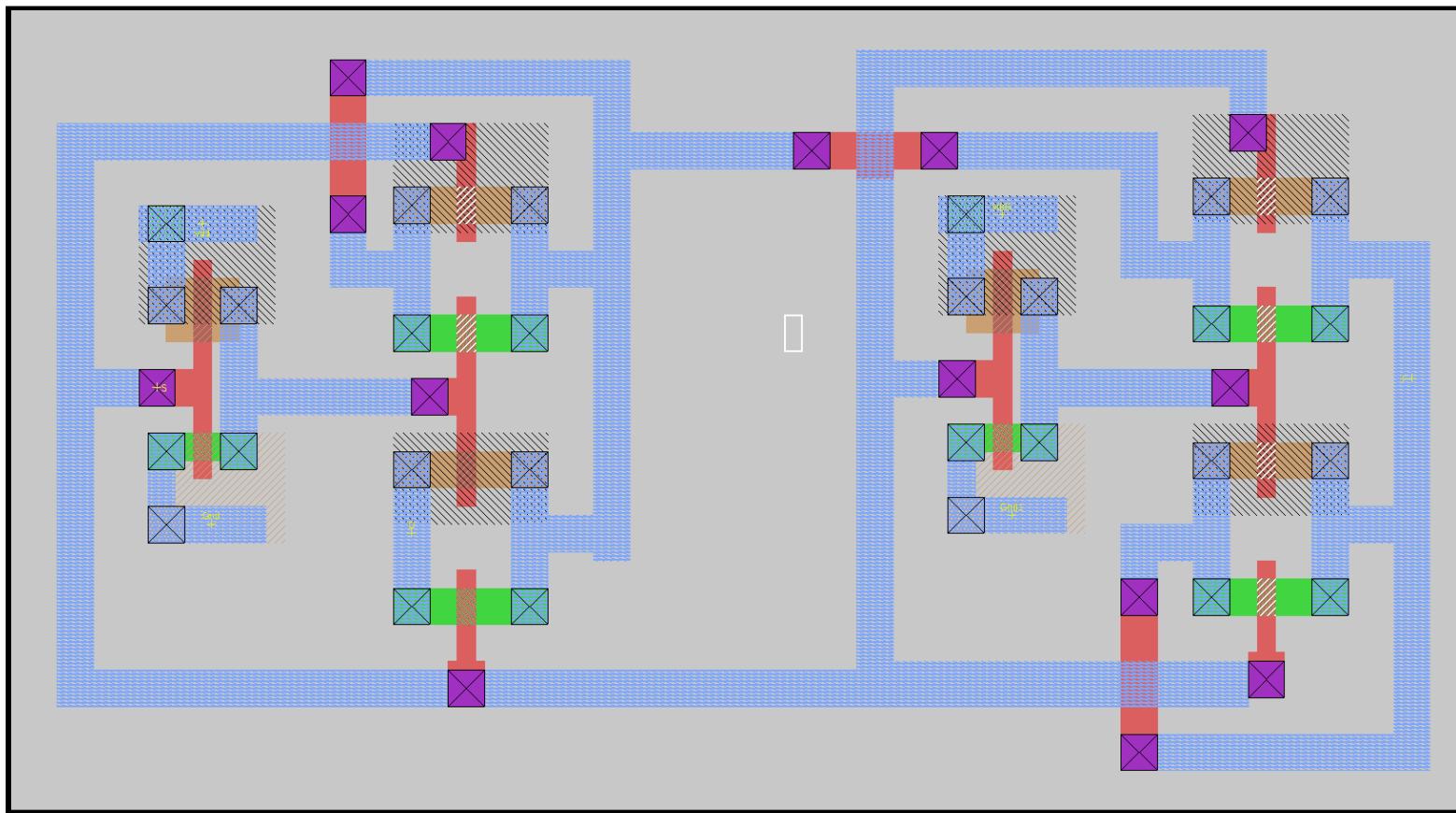
### Ngspice simulation:

```
.include ./t14y_tsmc_025_level3.txt
.include ./D_gate_new1.spice

v_dd vdd 0 5
v_dd1 vdd1 0 5
v_d S 0 dc 2.5 pulse(0 5 8n 1n 1n 60n 140n)
v_e D 0 dc 2.5 pulse(0 5 8n 1n 1n 15n 30n)

.control
  tran 0.1n 200n
  plot V(D), V(S), V(F)
.endc
```





**AOI:****Magic File:**

```
magic
tech scmos
timestamp 1603307216
<< nwell >>
rect -16 35 70 48
rect 74 14 86 24
<< polysilicon >>
rect -11 39 -9 41
rect -1 39 1 41
rect 16 39 18 41
rect 26 39 28 41
rect 46 39 48 41
rect 63 39 65 41
rect -11 12 -9 35
rect -1 12 1 35
rect 16 12 18 35
rect 26 12 28 35
rect 32 13 35 22
rect -12 8 -9 12
rect -2 8 1 12
rect 15 8 18 12
rect 25 8 28 12
rect 46 12 48 35
rect 51 19 54 29
rect 63 26 65 35
rect 62 22 65 26
rect 79 24 81 27
rect 45 8 48 12
rect -11 5 -9 8
rect -1 5 1 8
rect 16 5 18 8
rect 26 5 28 8
rect 46 5 48 8
rect 63 5 65 22
rect 79 12 81 16
rect 78 8 81 12
rect 79 5 81 8
rect -11 -1 -9 1
rect -1 -1 1 1
rect 16 -1 18 1
rect 26 -1 28 1
rect 46 -1 48 1
rect 63 -1 65 1
rect 79 -1 81 1
<< ndiffusion >>
rect -12 1 -11 5
rect -9 1 -1 5
rect 1 1 2 5
rect 15 1 16 5
rect 18 1 26 5
```

```
rect 28 1 31 5
rect 45 1 46 5
rect 48 1 63 5
rect 65 1 66 5
rect 78 1 79 5
rect 81 1 82 5
<< pdiffusion >>
rect -12 35 -11 39
rect -9 35 -7 39
rect -3 35 -1 39
rect 1 35 2 39
rect 15 35 16 39
rect 18 35 20 39
rect 24 35 26 39
rect 28 35 31 39
rect 45 35 46 39
rect 48 35 50 39
rect 62 35 63 39
rect 65 35 66 39
rect 76 22 79 24
rect 78 18 79 22
rect 76 16 79 18
rect 81 22 84 24
rect 81 18 82 22
rect 81 16 84 18
<< metal1 >>
rect -7 43 77 46
rect -7 39 -3 43
rect 20 39 24 43
rect 41 39 44 43
rect 58 39 61 43
rect -16 26 -13 35
rect 3 26 6 35
rect -16 23 6 26
rect 11 26 14 35
rect 32 26 35 35
rect 51 33 54 35
rect 11 23 31 26
rect 3 19 6 23
rect 35 23 58 26
rect 3 16 44 19
rect 3 5 6 16
rect 32 5 35 9
rect 41 12 44 16
rect 67 18 70 35
rect 74 22 77 43
rect 55 15 70 18
rect 67 11 70 15
rect 83 12 86 18
rect 67 8 74 11
rect 83 9 87 12
rect 67 5 70 8
rect 83 5 86 9
rect -16 -3 -13 1
rect 11 -3 14 1
rect 41 -3 44 1
rect 74 -3 77 1
rect -16 -6 77 -3
<< ntransistor >>
rect -11 1 -9 5
rect -1 1 1 5
```

```
rect 16 1 18 5
rect 26 1 28 5
rect 46 1 48 5
rect 63 1 65 5
rect 79 1 81 5
<< ptransistor >>
rect -11 35 -9 39
rect -1 35 1 39
rect 16 35 18 39
rect 26 35 28 39
rect 46 35 48 39
rect 63 35 65 39
rect 79 16 81 24
<< polycontact >>
rect 31 22 35 26
rect -16 8 -12 12
rect -6 8 -2 12
rect 11 8 15 12
rect 21 8 25 12
rect 31 9 35 13
rect 51 29 55 33
rect 58 22 62 26
rect 51 15 55 19
rect 41 8 45 12
rect 74 8 78 12
<< ndcontact >>
rect -16 1 -12 5
rect 2 1 6 5
rect 11 1 15 5
rect 31 1 35 5
rect 41 1 45 5
rect 66 1 70 5
rect 74 1 78 5
rect 82 1 86 5
<< pdcontact >>
rect -16 35 -12 39
rect -7 35 -3 39
rect 2 35 6 39
rect 11 35 15 39
rect 20 35 24 39
rect 31 35 35 39
rect 41 35 45 39
rect 50 35 54 39
rect 58 35 62 39
rect 66 35 70 39
rect 74 18 78 22
rect 82 18 86 22
<< labels >>
rlabel polycontact -14 10 -14 10 3 a
rlabel polycontact -4 10 -4 10 3 b
rlabel polycontact 13 10 13 10 3 c
rlabel polycontact 23 10 23 10 3 d
rlabel metal1 85 11 85 11 3 out
rlabel metal1 35 -4 35 -4 3 0
rlabel metal1 37 45 37 45 3 vdd
<< end >>
```

**Spice file:**

```
.option scale=1u
M1000 vdd a a_n16_35# w_n16_35# pfet w=5 l=2
+ ad=136 pd=110 as=40 ps=36
M1001 a_n16_35# b vdd w_n16_35# pfet w=5 l=2
+ ad=0 pd=0 as=0 ps=0
M1002 vdd c a_11_35# w_n16_35# pfet w=5 l=2
+ ad=0 pd=0 as=48 ps=40
M1003 a_11_35# d vdd w_n16_35# pfet w=45l=2
+ ad=0 pd=0 as=0 ps=0
M1004 a_48_35# a_n16_35# vdd w_n16_35# pfet w=5 l=2
+ ad=44 pd=38 as=0 ps=0
M1005 a_48_35# a_11_35# vdd w_n16_35# pfet w=5 l=2
+ ad=0 pd=0 as=0 ps=0
M1006 out a_48_35# vdd w_74_14# pfet w=8 l=2
+ ad=32 pd=26 as=0 ps=0
M1007 a_n9_1# a 0 Gnd nfet w=4 l=2
+ ad=32 pd=24 as=80 ps=72
M1008 a_n16_35# b a_n9_1# Gnd nfet w=4 l=2
+ ad=20 pd=18 as=0 ps=0
M1009 a_18_1# c 0 Gnd nfet w=4 l=2
+ ad=32 pd=24 as=0 ps=0
M1010 a_11_35# d a_18_1# Gnd nfet w=4 l=2
+ ad=28 pd=22 as=0 ps=0
M1011 a_48_1# a_n16_35# 0 Gnd nfet w=4 l=2
+ ad=60 pd=38 as=0 ps=0
M1012 a_48_35# a_11_35# a_48_1# Gnd nfet w=4 l=2
+ ad=20 pd=18 as=0 ps=0
M1013 out a_48_35# 0 Gnd nfet w=4 l=2
+ ad=20 pd=18 as=0 ps=0
C0 vdd w_n16_35# 13.5fF
C1 a_48_35# Gnd 18.1fF
C2 vdd 0 3.7fF
C3 a_11_35# 0 23.4fF
C4 a_n16_35# 0 22.2fF
C5 d 0 9.7fF
C6 c 0 9.7fF
C7 b 0 9.7fF
C8 a 0 9.7fF
```

**Simulation File:**

```
.include ./t14y_tsmc_025_level3.txt
.include ./AOI.spice
v_dd vdd 0 5
v_a a 0 dc 2.5 pulse(0 5 0.1n 0.1n 0.1n 40n 80n)
v_b b 0 dc 2.5 pulse(0 5 0.1n 0.1n 0.1n 20n 40n)
v_c c 0 dc 2.5 pulse(0 5 0.1n 0.1n 0.1n 10n 20n)
v_d d 0 dc 2.5 pulse(0 5 0.1n 0.1n 0.1n 20n 40n)
.control
    tran 0.1n 80ns
    plot tran1.a, tran1.b, tran1.c, tran1.d, tran1.out
    plot tran1.out
end
.endc
```

