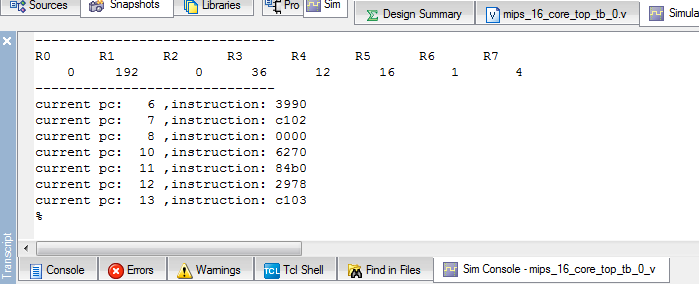
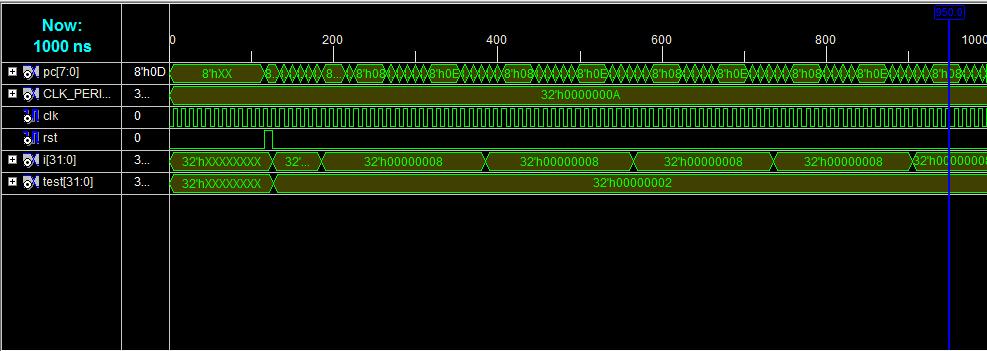
**STEPWISE RESULTS and LVS-DRC reports:**

Xilinx Results:

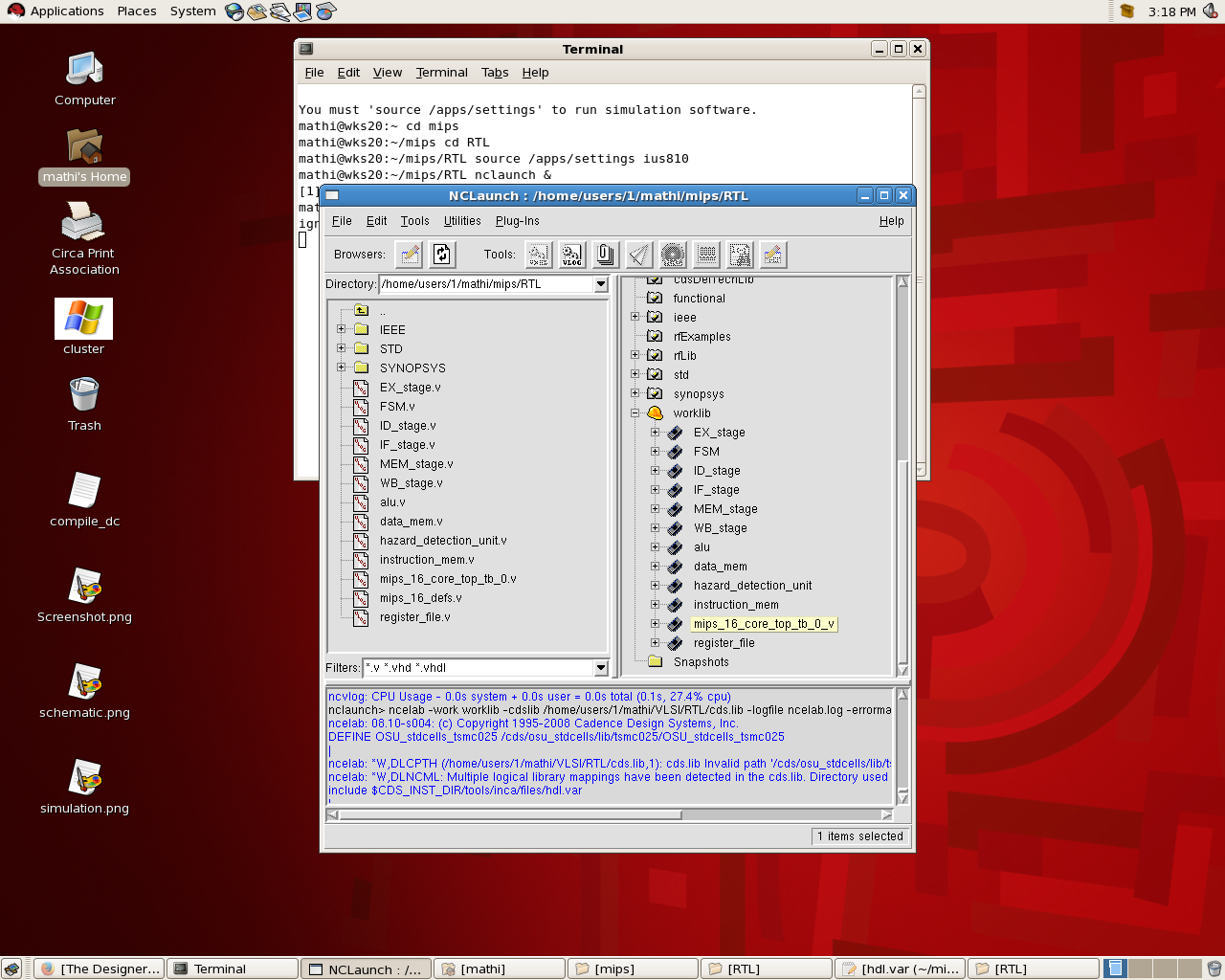


Simulation

For multiply operation 12 \* 3=36( Stored in R3)



RTL:



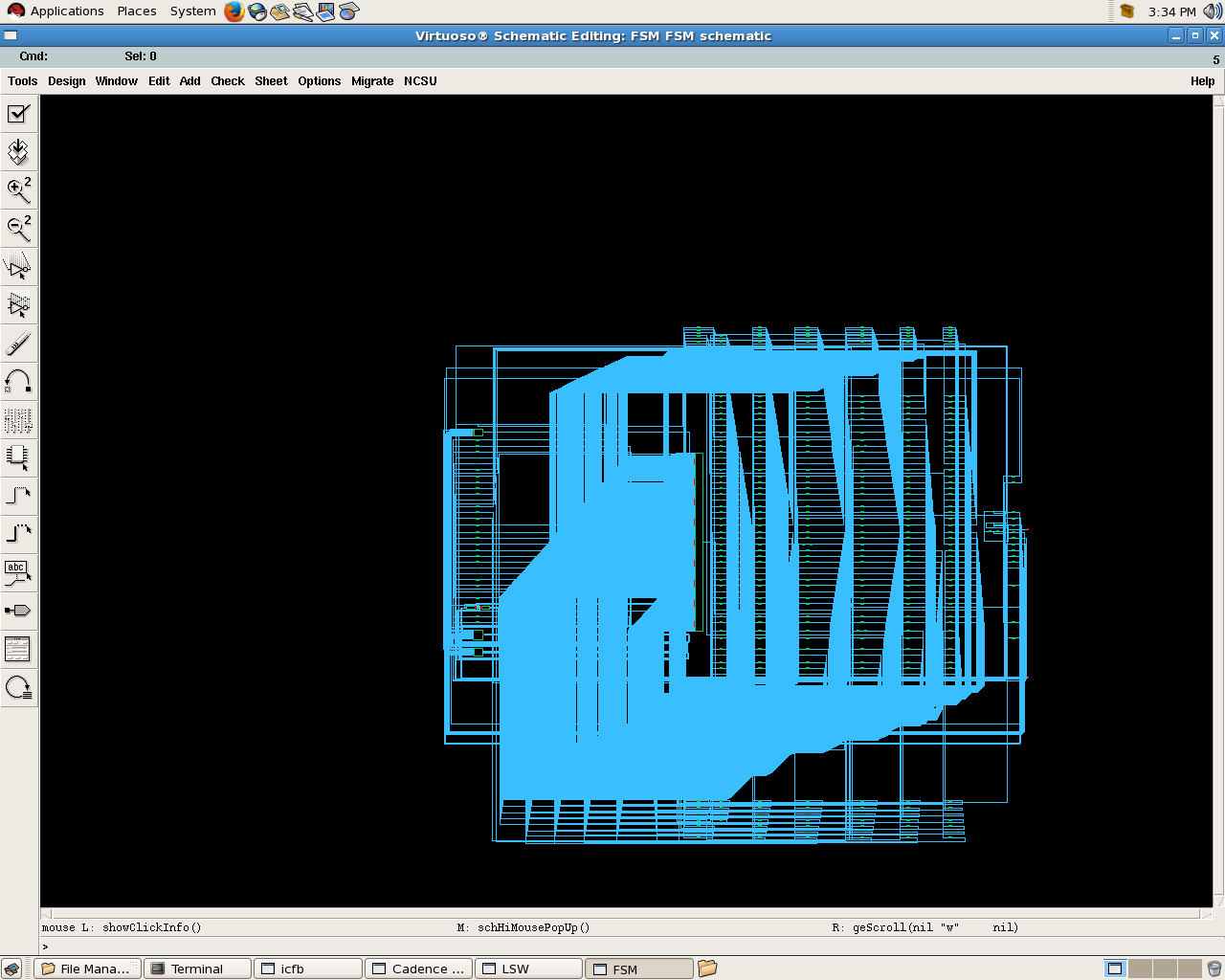
SYN:

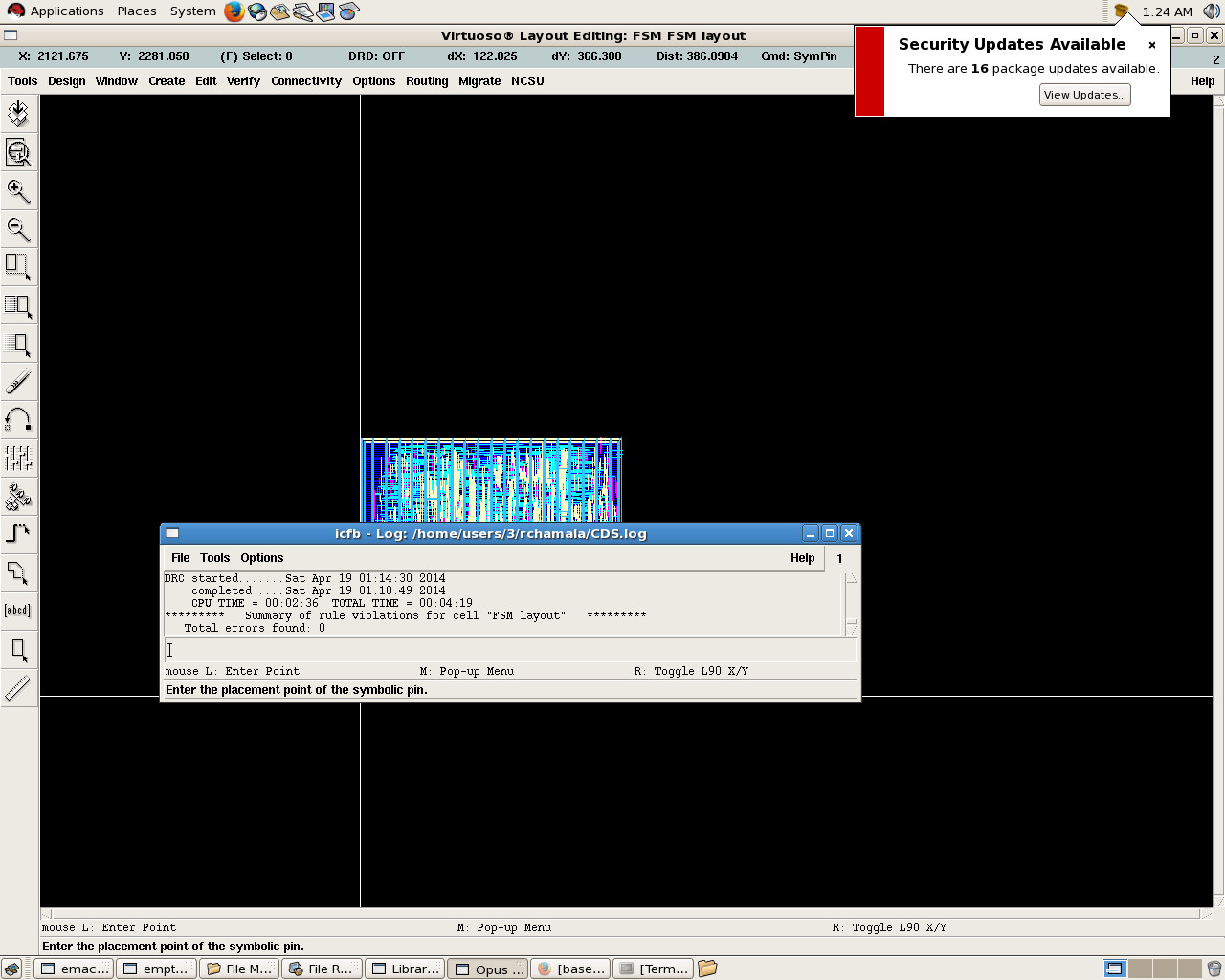
After Synthesis we get the netlist FSM.v

We also get timing.rep; power.rep; area.rep; cell.rep for both optimized and unoptimized codes.

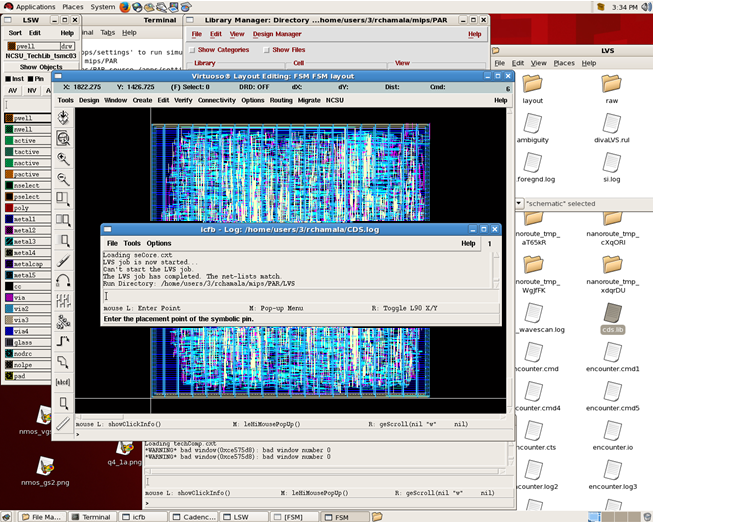
PAR:

**UNOPTIMIZED:**

Schematic of unoptimised:

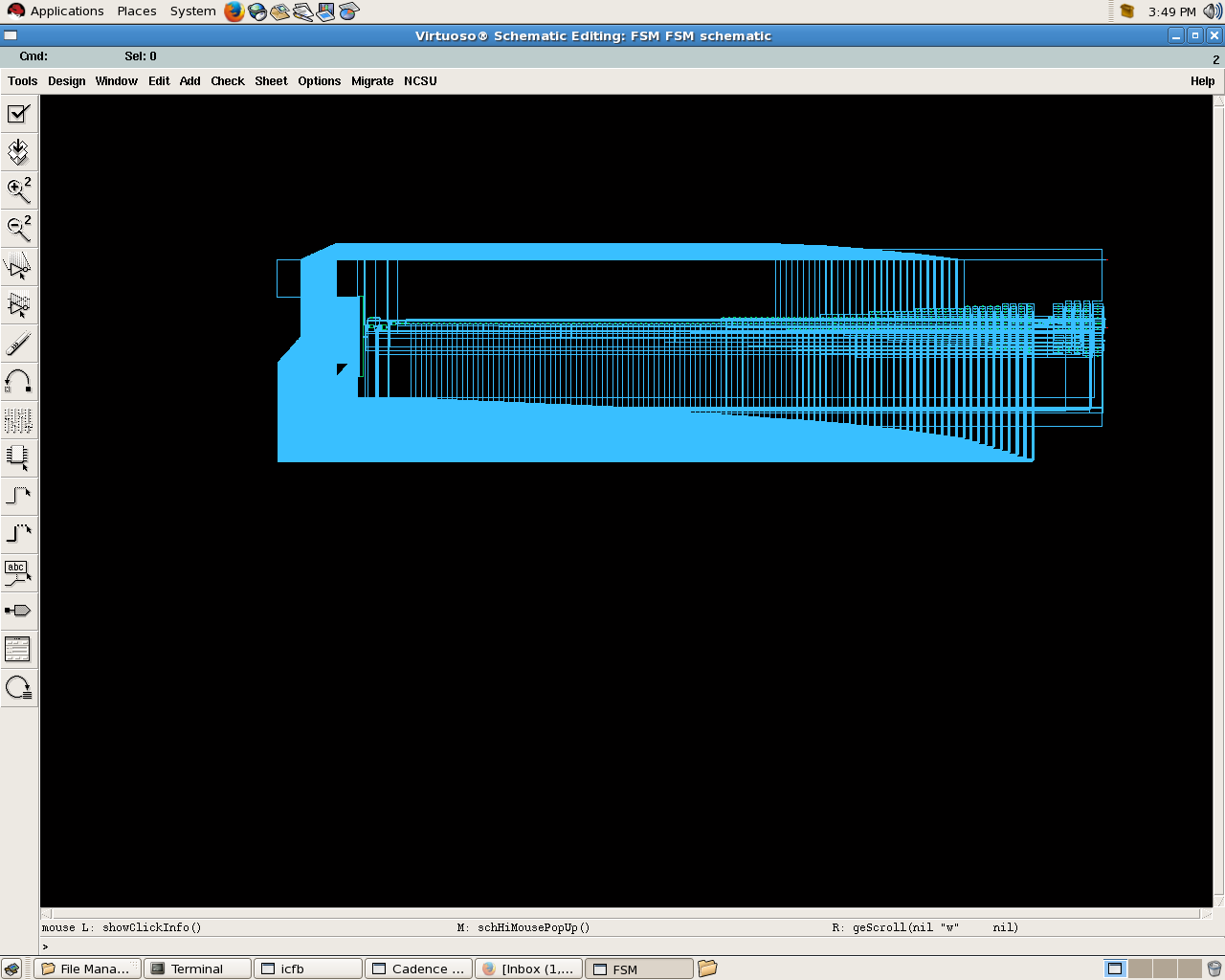
DRC 

LVS

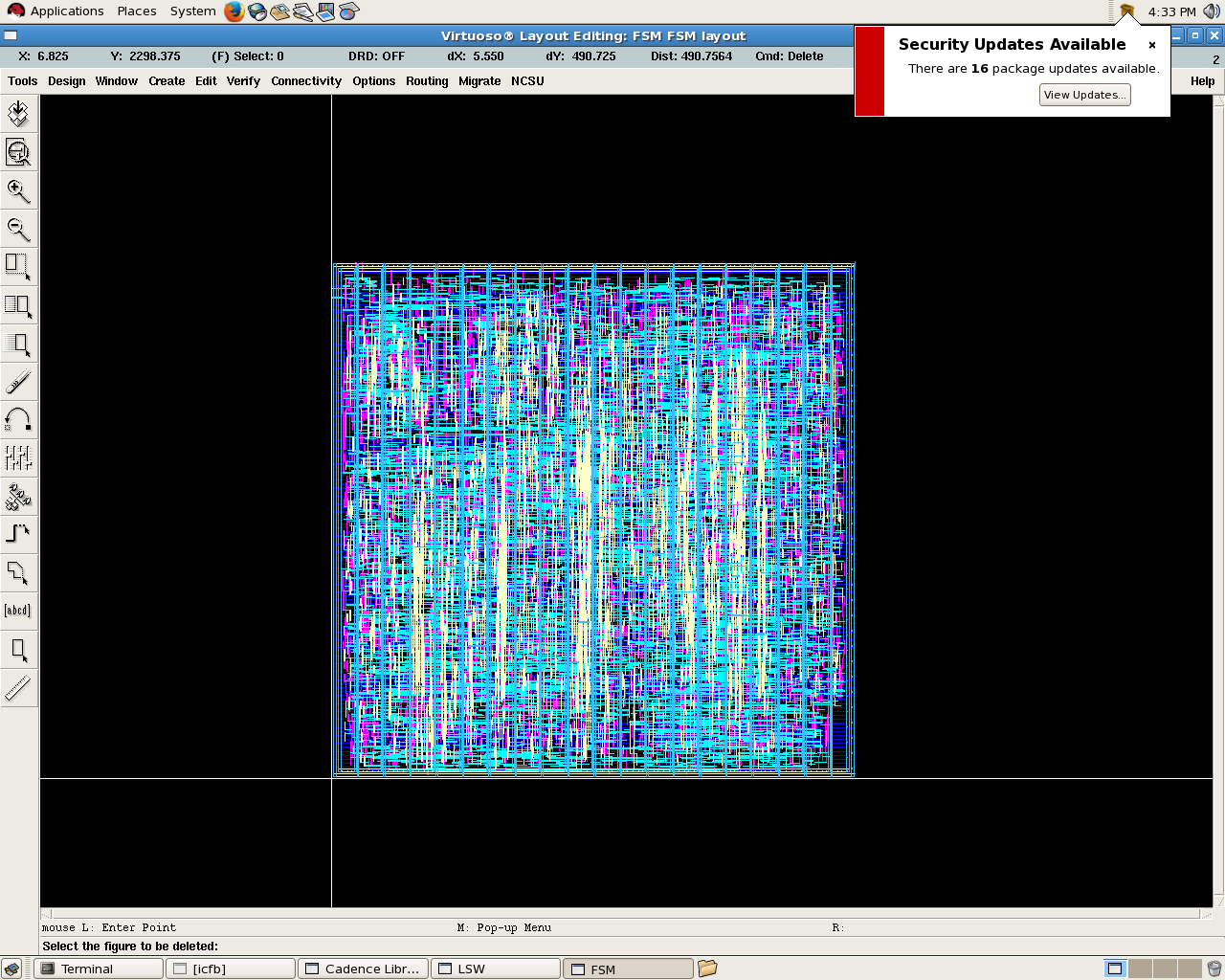


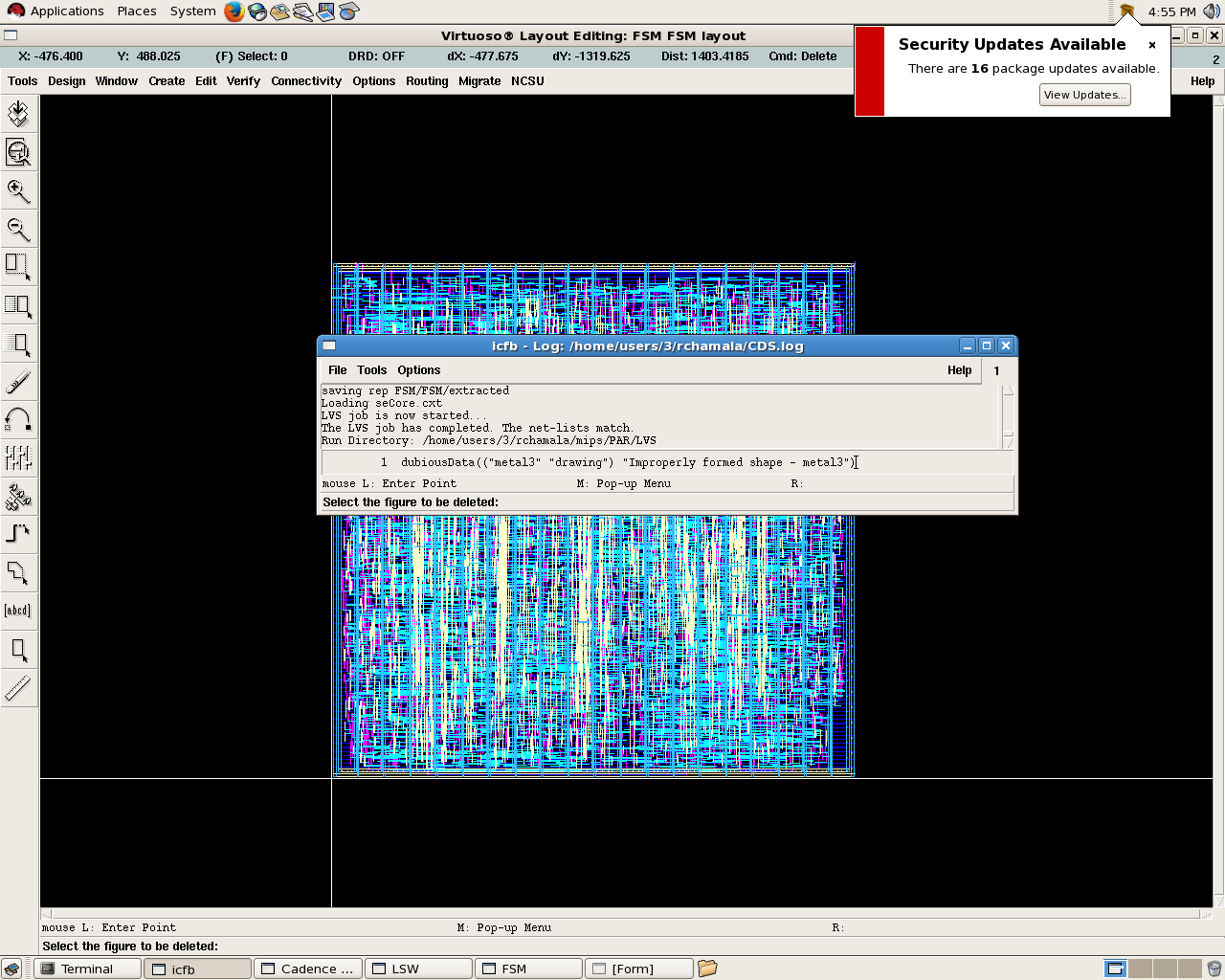
**OPTIMIZED**

Schematic for optimized code:

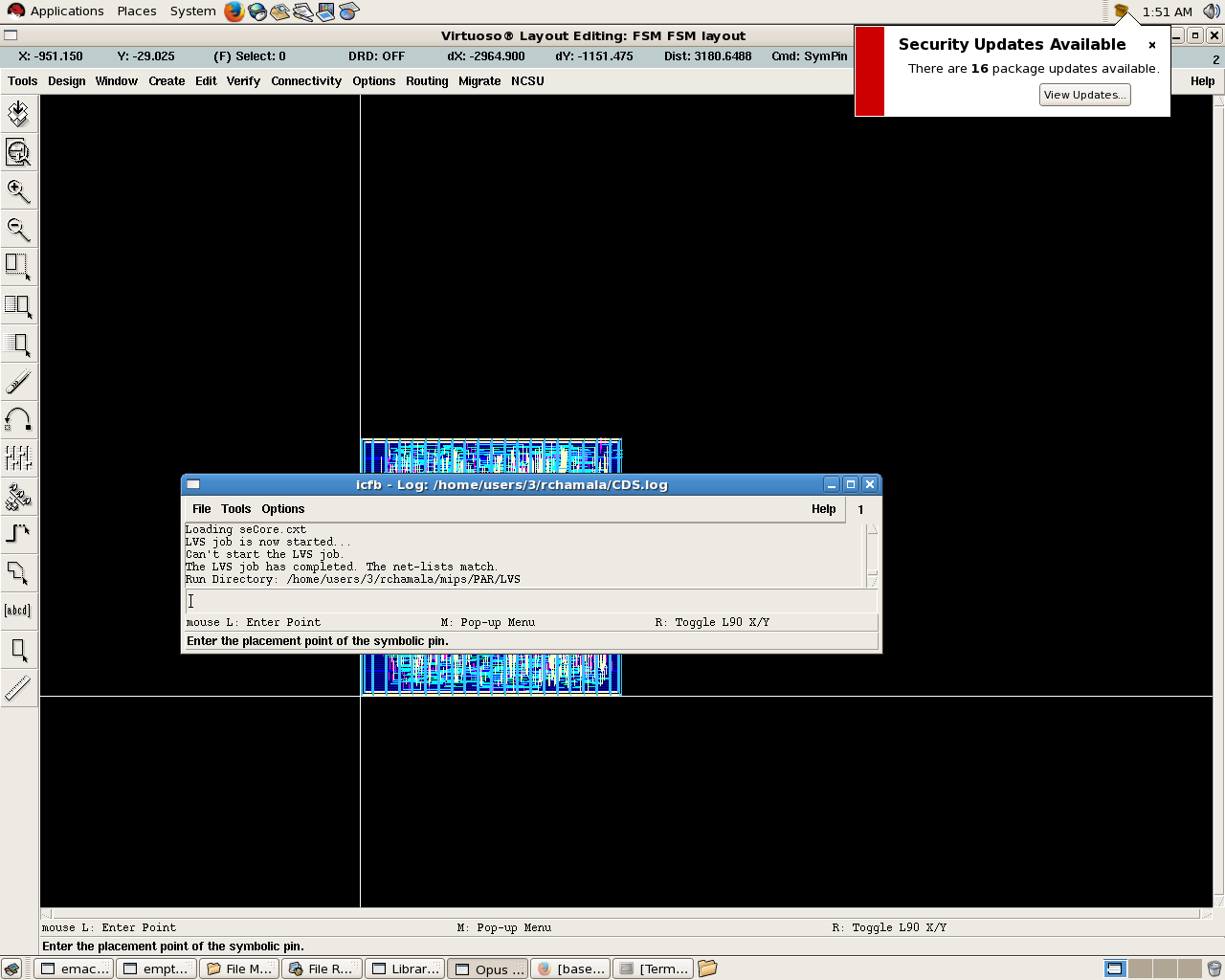


Layout for Optimised without IO pads



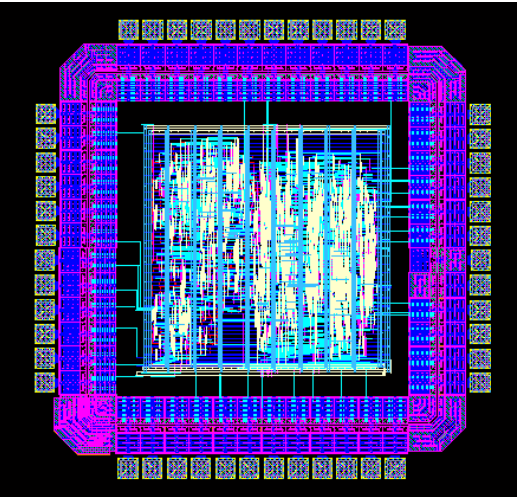
DRC check: 

LVS check:



Si.out file has been included.

Layout with I/O pads



|  |  |  |
| --- | --- | --- |
| Area | Unoptimised | Optimised |
|  | 1956471 | 2597156 |

|  |  |  |
| --- | --- | --- |
| Clock Period nS | Total Power mW Unoptimised | Total Power mW Optimised |
| 30 | 74.74 | 47.09 |
| 40 | 56.06 | 35.32 |
| 50 | 44.84 | 28.25 |
| 60 | 37.36 | 23.54 |
| 100 | 21.73 | 14.13 |