Design of 4 bit SRAM using 6T SRAM Cell

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***Abstract*—This paper deals with the design and implementation of 4-bit SRAM using 6T SRAM cell. The SRAM is designed so that it covers a minimum area in layout and the transistors are sized properly for an efficient design. The paper also presents the results about read and write access times and it also shows stable noise margins which are plotted in MATLAB. This 6T SRAM cell can be further extended to form large arrays of memory**

Index Terms—SRAM, Sense Amplifier, Noise Margins

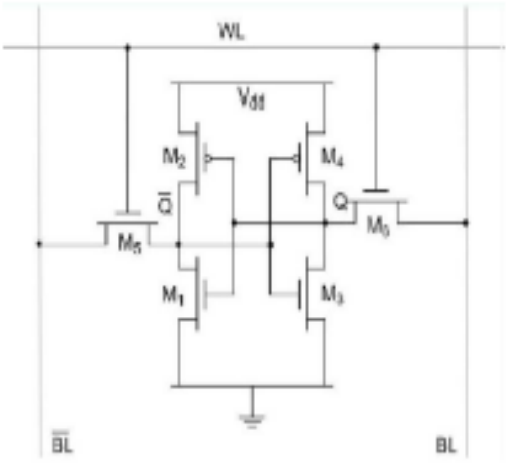
I INTRODUCTION

Memory arrays are an essential part of circuit system. They occupy more space in an IC chip. Therefore space utilization is extremely important for higher efficiency. We chose a 6T SRAM cell which is manufactured using CMOS technology .SRAM cells are fast and are used as caches in computer memory. One bit is stored in 6 transistors of SRAM. There are other components like tristate-buffer, pre charge circuitry and sense amplifier which are also part of the circuit

II MATERIALS AND DESIGN CONSIDERATIONS

A *Cell Operation*

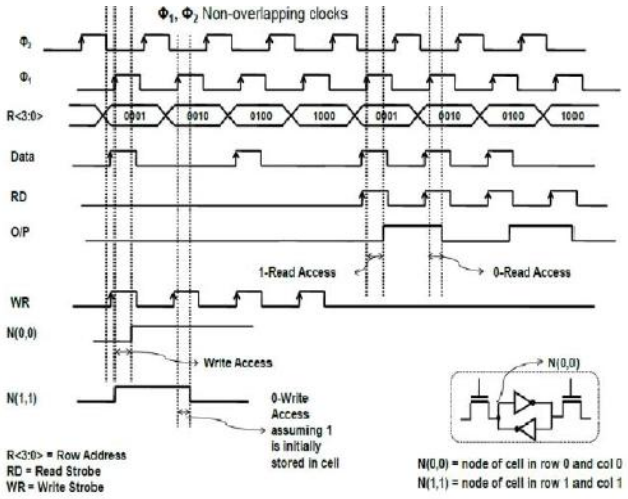
A basic 6T SRAM cell can be shown as follows:



There are two access transistors and 4 other transistors form two inverters which are used to hold the bit information which can be obtained through BL and BL_bar. The access transistors are controlled with a line which is known as Word Line. Consider a series of SRAM cells in both X and Y dimensions. The Word lines come from the output of a row decoder which takes the address as input and sets one of its output lines high. This means all of the cells in one row are selected after the row decoder output in the memory array. The Bit Lines are outputs of a Column Decoder circuit which selects a particular cell in a column.

The BL and WL combined can therefore select a particular cell in a memory array. The bit lines BL and BL_bar are precharged to VDD/2 before read and write. The charge is stored in the respective capacitances. In the figure, M5 and M6 transistors are turned whenever WL is high which selects that particular row. Initially BL and BL_bar are set to one as mentioned before. Whenever a write occurs, either BL is discharged to ground(when ‘0’ is written) or BL_bar is discharged to ground(when ‘1’ is written).Whenever a read signal is given, the two bit lines are fed into the sense amplifier which amplifies the difference between the signals and detects whether the bit is ‘1’ or ‘0’ .

A read is always succeeded by a write. The read and write operations can be shown in the diagram as follows:



Transistor Sizes and Reasoning:

There are some sizing constraints for a reliable cell operation. The voltage rise in one transistor must be low enough so that it does not cause a very high current during write or read operation which can change the information of the bit in the worst case. Hence Cell Ratio is defined to prevent a mishap in read operation which is mathematically given by

CR=(W1/L1)/(W5/L5)

Cell ratio has to greater than 1.2 to prevent read upset. Hence we chose the width and length of the transistors of M1 and M5 are 480nm,240nm ad 360nm,240nm to achieve a cell ratio of 1.33.One more advantage of this cell it that adds less capacitance and provides cell ratio as well. Similarly pull up ratio is defined between M4 and M 6 transistors. It is used to prevent write upset in an operation.

PR= (W4/L4)/(W6/L6)

For the 240nm technology, PR has to be less than 1.8.Therefore the width and lengths of transistors M4 and M6 were chosen as

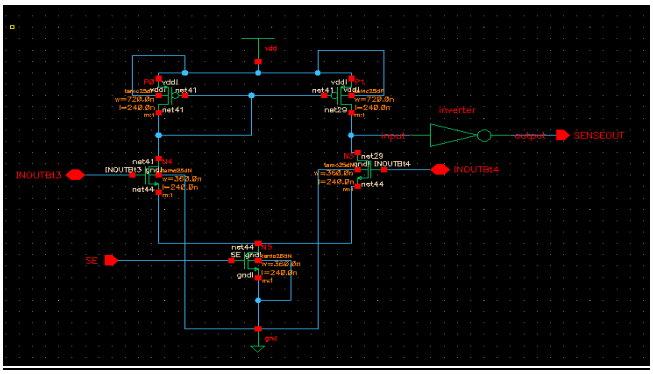
W4=W6=360nm and L4=L6=240nm

III PERIPHERALS PRESENT

Sense Amplifier:

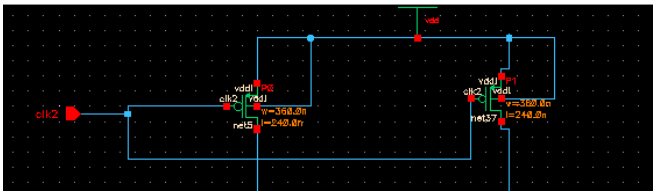
They play an important role in the functionality, performance and reliability of memory circuits. It allows resolving of data with small bit line swings and reduces the delay and power required while driving the signal range of bit line to high. Here full swing(0-2.5V) and read strobe is enabled by the input clock(Φ1).

Figure 3 below shows the schematic of a sense amplifier. It represents the circuit of a differential amplifier.



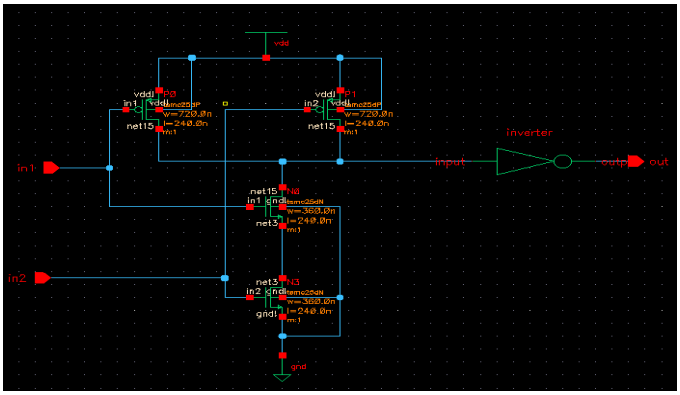
Precharge circuit:

The pre-charge circuit pre-charges the value held in the SRAM cell every clock cycle. It raises both BL and BL_bar to VDD or high at the rising edge of every clock cycle(Φ2). It has a non-overlapping clock with the input clock(Φ1). Figure.4 below shows the schematic of precharge circuitry.



Tristate Buffer:

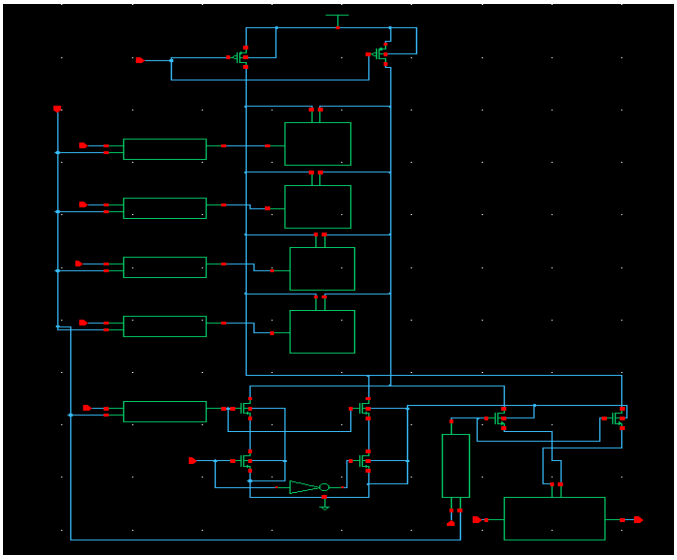
To differentiate the cell from the inputs, tri-state buffer or clock driver circuit is built to be a buffer whenever the conditional input (Φ1) is high. The width and lengths of transistors M4 and M6 were chosen as W=360nm and L=240nm. The circuit is as shown in Figure.5.



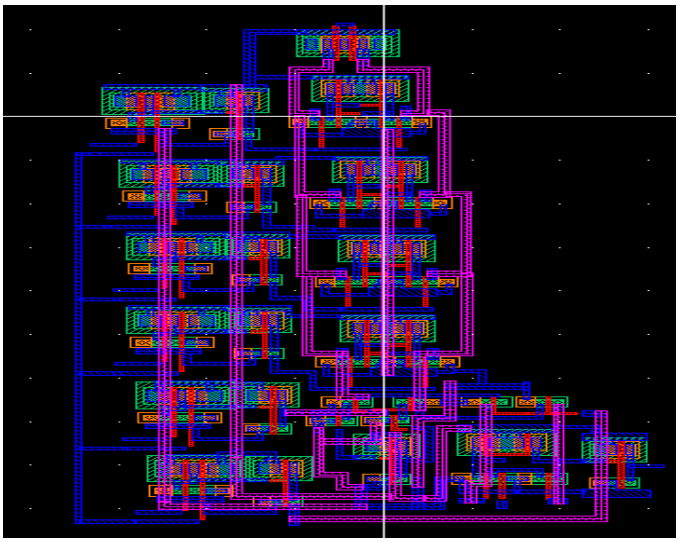
IV SCHEMATIC AND LAYOUT

The final Schematic and Layout of the complete circuit of the 4-bit SRAM is as shown below .

*Schematic:*Figure 6



*Layout:*Figure 7

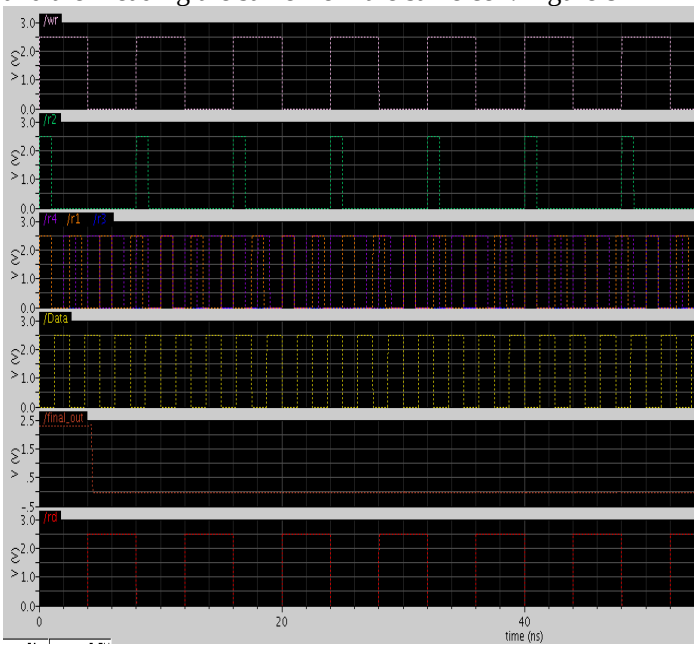


Overall Area of the 6T RAM cell is found to be 1600.25 um^2

V. RESULTS

A. Delay Calculations :

The timing diagram for the write operation followed by the read is shown in Figure 8. A '0' is written into the first cell and then reading the same from the same cell. Figure 8



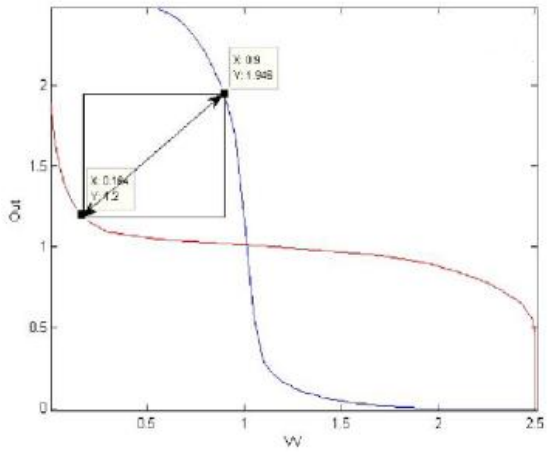
A1.Read access time: estimate the 50% delay from clock phase Φ1 to the output data (O/P) transitions for both 1 and 0 reads. It is about 0.998 ns for the first read transition for considered inputs of 10ns clock cycles.

A2. Write access time: estimate the 50% delay from the rising edge of Φ1 to the final writing of the input data into the memory. It is around 0.348 ns for the first write transition for considered inputs of 10ns clock cycles.

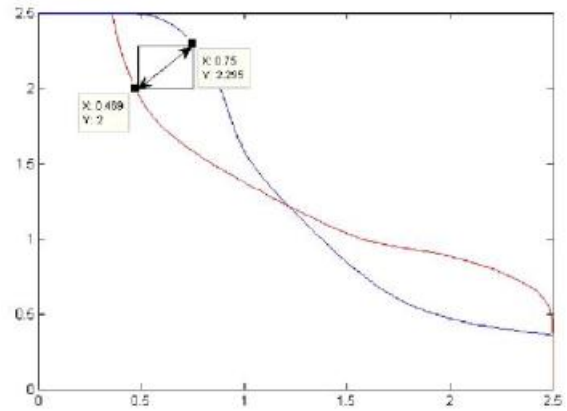
B.*Signal Noise Margin Analysis*

The Noise Margin for the Read, Write and Hold stability are calculated by sweeping the input values and output values of the inverter. The values are plotted in the MATLAB and the SNM is calculated (Figure.9, 10 & 11). The SNM is calculated as the length of the smallest square that can be drawn between the curves.

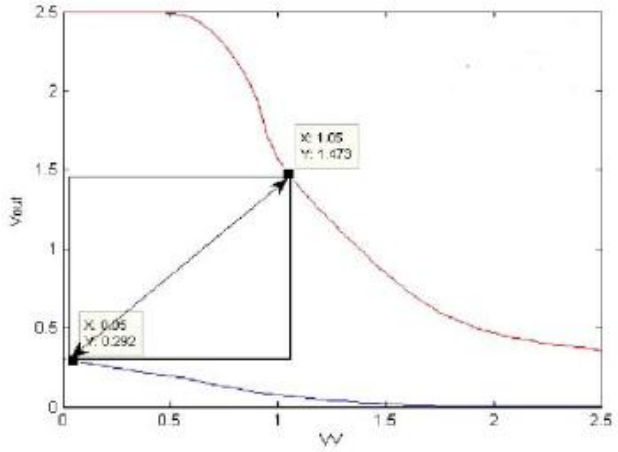
B1.Hold SNM: 0.736V



B2.Read SNM: 0.281V



B3.Write SNM:1.00V



C. Capacitance Calculations

The pass transistors, M5 and M6 from Figure 1. The diffusion capacitance of these transistors is defined in [1] as

Cdiff = Cj * Area + Cjsw * Perimeter

For the 0.24 um technology,

Cj = 2 fF/um2

Cjsw = 0.28 fF/um

The width and lengths of transistors M5 and M6 were chosen as W=360nm and L=240nm.

Thus diffusion capacitance is 0.4152fF.

The gate capacitance of pass transistors is defined as,

CG = COX * W * L + 2 * C0 * W

For 0.24 um technology,

Cox = 6 fF / um2,

C0 = 0.31 fF /um

This gives us 0.7632fF gate capacitance. The capacitance added to the word-line per 6T SRAM cell is twice the gate capacitance of the pass transistors.

VI CONCLUSION

The design of a 4 bit SRAM is completed and the results are recorded in table below.

PARAMETERS	**VALUE**
Write Access Time	998ps
Read Access Time	348ps
Diffusion Capacitance	0.4152fF
Gate Capacitance	0.7632fF
Capacitance added to 6T cell	1.5264fF
SNM(Read)	0.281V
SNM (Write)	1.000V
SNM (Hold)	0.736V
Total Area	1600.25um^2

REFERENCES

[1] J. Rabaey, A. Chandrakasan, B Nikolic, "Digital Int egrated Circuits a Design Perspective." Second Edition, Pearson Prentice Hall, 2003.

[2] Neil H. E. Weste, David Harris, "CMOS VLSI Design, A Circuits and Systems Perspective," Third Edition, Pearson, Addison-Wesley, 2005

BIO

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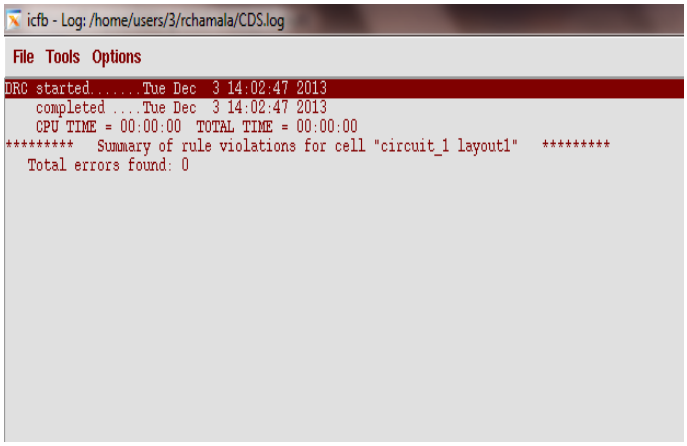
DRC AND LVS REPORT

DRC



LVS