CO224 – Lab 06 Part 02

Data Cache

Group 09

Case 1: Read hit

Part 1:

In a cache less implementation, when you read data from a memory address, it will take 5 clock cycles to complete the operation. This is because the system needs to access the main memory, which takes longer compared to accessing data from a cache.

Part 2:

The state remains unchanged as the hit signal is asserted 2 time units after receiving the CPU's address. When the hit signal is high, the data in READDATA is sent to the CPU and written to the register on the next clock edge. Hence, a cache read hit takes only 1 clock cycle.

Case 2: Write hit

Part 1:

In a cache less implementation, when you write data to a memory address, it will take 5 clock cycles to complete the operation. This is because the system needs to access the main memory, which takes longer compared to writing data to a cache.

Part 2:

The state remains unchanged as the hit signal is asserted 2 time units after receiving the CPU's address. When the hit signal is high, the data in WRITEDATA is written to memory with a 1 time unit delay. The CPU can proceed to the next instruction without stalling. Hence, a write hit to the cache takes only 1 clock cycle.

Case 3: Read miss and dirty

Part 1:

In a cache less implementation, retrieving data from a memory address takes a fixed time of 5 clock cycles. This is true regardless of the size of the data being read.

Part 2:

Considering the dirty bit is set to 1, a write back to memory will occur, taking 20 clock cycles (5 cycles per byte). Then, the memory block related to the read address must be fetched, consuming another 20 cycles (5 cycles per byte). After fetching, at the 41st cycle, the hit signal is asserted, allowing data to be read from the cache and written to a register on the next clock edge. Due to race conditions, an extra cycle is needed for writing and reading from memory. Thus, the total number of clock cycles consumed after instruction fetching is 42.

Case 4: Read miss and not dirty

Part 1:

In a cache less implementation, when reading data from a memory address, it consistently takes 5 clock cycles regardless of the data size.

Part 2:

With a dirty bit of 0, no write back to memory occurs. However, the memory block related to the read address is fetched, taking 20 cycles for 4 bytes (5 cycles per byte). After fetching, at the 21st cycle, the hit signal is asserted, allowing data to be read from the cache and sent to the CPU. The data is then written to a register on the next clock edge. A race condition causes an additional cycle to be consumed for memory reading, resulting in a total of 22 cycles after instruction fetching.

Case 5: Write miss and dirty

Part 1:

In a cache less implementation, when writing data from a memory address, it consistently takes 5 clock cycles regardless of the data size.

Part 2:

When the dirty bit is set to 1, a write back to memory occurs, taking 20 cycles (5 cycles per byte). Following this, the memory block associated with the write address is fetched, consuming 20 cycles (5 cycles per byte). After fetching, at the 41st cycle, the hit signal is asserted, allowing data to be written to the relevant cache address with a 1-time unit delay. Due to race conditions, an extra cycle is used for writing and reading from memory. Consequently, a total of 42 cycles are consumed after instruction fetching.

Case 6: Write miss and not dirty

Part 1:

In a cache less implementation, when writing data from a memory address, it consistently takes 5 clock cycles regardless of the data size.

Part 2:

With a dirty bit of 0, no write back to memory is performed. However, the memory block associated with the write address must be fetched, taking 20 cycles for 4 bytes (5 cycles per byte). After fetching, at the 21st cycle, the hit signal is asserted, allowing data to be written to the relevant cache address with a 1-time unit delay. Due to a race condition, an additional cycle is consumed for reading. Therefore, the total number of clock cycles consumed after instruction fetching is 22.

Summary

In a read hit,

- Part 2 – Instruction completes in one clock cycle.
- Part 1– Instruction completes during 5 clock cycles.

In a write hit,

- Part 2 – Instruction completes in one clock cycle.
- Part 1– Instruction completes during 5 clock cycles.

In a read miss and dirty,

- Part 2 – Instruction completes in 42 clock cycles.
- Part 1– Instruction completes during 5 clock cycles.

In a read miss and not dirty,

- Part 2 – Instruction completes in 22 clock cycles.
- Part 1– Instruction completes during 5 clock cycles.

In a write miss and dirty,

- Part 2 – Instruction completes in 42 clock cycles.
- Part 1– Instruction completes during 5 clock cycles.

In a write miss and not dirty,

- Part 2 – Instruction completes in 22 clock cycles.
- Part 1– Instruction completes during 5 clock cycles.