Design for Testability for SoC and IP's

- **SoC vs ASIC/ASSP**
  - Has both digital and analog blocks (mixed signal functions)
  - Contains many IP blocks from different suppliers
  - Contains scattered memory blocks of all sizes
  - Usually with more power gating and power island/domain partitions
  - Hierarchical mixture of processor, custom logic,, hard macro and soft core IP, peripherals, etc
- **Current Practices**
  - Test access mechanism/wrapper design (JTAG, P1500) in SoC's hierarchy
  - Leverage computation power from big server farms to generate better ATPG
    - Pattern compression by EDA tools, Sophisticated pattern and fault-grading analysis
  - Broadcasting, parallel testing, re-use or re-generate patterns on chip
  - IP sign-off requirements:
    - Virtual Component Exchange (VCX): synthesis, DFT, ATPG validated at target node.
  - Spare gates and floor-sweeping.

SoC DFT Challenges

- **Challenges from TAM wrappers:**
  - Impose restriction, overhead, timing delay, more levels of test access time
  - Block boundary optimization, scan chain re-ordering/inversion
  - More design and verification manpower.
  - More complexity added to low-power designs.
  - More difficult to debug and access failures.
- **Challenges from IP's supplied test structure and vectors:**
  - Bugs in pre-supplied vectors
  - Surrounding access mechanism
  - Timing of the logic in test mode
  - Effort in expanding the vectors to the chip level
  - Debugging efforts is fraught because of IP's different suppliers and different DFT structures
  - Low-power functions can only be verified at chip level.
- **Solutions: MBIST + LBIST + smart ATPG**

Background - Anna Chang

- **Design and Verification:**
  - SystemVerilog / UVM / OVM / OOP : 7 years
    - Microprocessor (Sun, AMD), DFT (Apple, Nvidia, TSMC, AMD),
    - JTAG (Apple, Nvidia, TSMC, AMD), MBIST (TSMC, Nvidia, Apple, AMD),
    - PCI-express (Sun), mixed Signal Audio codec (Nuvoton),
    - I2C, SPI, Ethernet, I2S, PCI/PCI-e, SLIMbus, AMBA, AXI, AHB, P1500 (in different projects)
  - Verilog / ASIC : 15 years
    - Microprocessor (Sun), and including UVM/OVM experience above.
    - Synthesis, timing analysis, micro-architecture (Sun, TSMC, Nuvoton)
    - FPGA Xilinx-Cortex M0 (Nuvoton and consulting projects, 18 months)
  - Formal Verification (Apple, 2 years)
  - Tools : VCS, NCverilog, Modelsim, Jasper, Design/DFT-Compiler, TMAX, Perforce, SVN, Git, Eclipse
- **DFT :** 12 years in JTAG, P1500, Scan-chain, MBIST, ATPG
- **Design/Project Management :** TSMC 4 years.
- **Programming Languages :** Perl, Python, Make, Tcl/tk, Java, C/C++, J2EE(Spring, Hibernate, JDBC), HTML, CSS, JavaScript (Selenium, AJAX, JQuery, Node.js), XML/JSON, Linux/Unix (bash/csh/tcsh), Apache, SQL/MySQL, PHP
- **http://github.com/changanna**