Homework 10

Problem 1: SEQ Implementation

Assume we are going to implementation the following instruction in our SEQ y68_64 processor: `iaddq V, rB`, which added value `V` to the value stored in register `rB (R[rB] <- R[rB] + V)`;
1. Try to fill in the table listed below.

Stage	`iaddq V, rB`
Fetch	
Decode	`valB <- R[rB]`
Execute	
Memory	
Write back	
PC update	

2. Please point out which logic blocks in the following ones should be modified and write the modified HCL code below.
{`need_valC, srcB, dstM, aluB, mem_data`}

Problem 2: Pipeline

Assume now we have 4 load of clothes need to wash, dry, and fold. The wash task takes 40 minutes, dry task takes 50 minutes, and fold task takes 30 minutes to deal with one load of clothes. If we do these tasks sequentially, how long would the whole process take? What if we have more resources and do these tasks using Pipeline? Please indicate the Speedup (old/new).

Problem 3: Data hazard

Is there a data hazard in the following codes in our **PIPELINE** processor **WITHOUT** forwarding? If yes, explain how the hazard happens, insert `nop`s to solve the hazard and show what value should `d_valA` and `d_valB` take if we solve this problem by forwarding. If no, explain why.

(**NOTE**: you should represent `d_valA` and `d_valB` by other HCL variables like `E_dstE`)

P1:	P2:
1 irmovq $1, %rbx 2 irmovq $2, %rcx 3 addl %rbx,, %rcx	1 rrmovq %rax, %rbx 2 irmovq $1, %rax