OVP Guide to Using Processor Models

Model Specific Information for variant powerpc_m440

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1.0 Overview

This document provides the details of an OVP Fast Processor Model variant.
OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.
The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance.
Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.
The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners.
There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

PPC32 Family Processor Model. Providing PPC 400 family variants.

1.2 Licensing

Open Source Apache 2.0

1.3 Limitations

This model is currently under development
The FPU is incomplete
FPU exceptions are not implemented
Some Single Floating Point FPU instructions are not implemented
The MMU is not implemented

1.4 Verification

Basic verification of ISA against golden reference has been performed

1.5 Features

2.0 Configuration

2.1 Location

The model source and object file is found in the VLNV tree at:
power.ovpworld.org/processor/powerpc32_400/1.0

2.2 GDB Path

The default GDB for this model is found at:
$IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/powerpc-elf-gdb

2.3 Semi-Host Library

The default semi-host library file is found in the VLNV tree at :
power.ovpworld.org/semihosting/powerpc32Newlib/1.0

2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

2.6 Processor ELF Code

The ELF code supported by this model is: 0x14

3.0 Other Variants in this Model

Table 1.

Variant
m476
m470
m460
m440

4.0 Bus Ports

Table 2.

Type	Name	Bits
master (initiator)	INSTRUCTION	32
master (initiator)	DATA	32

5.0 Net Ports

Table 3.

Name	Type
reset	input

6.0 FIFO Ports

No FIFO Ports in this model.

7.0 Parameters

Table 4.

Name	Type	Description
verbose	Boolean	Specify verbose output messages
UISA_I_B	Boolean	UISA Feature UISA_I_B
UISA_I_BCDA	Boolean	UISA Feature UISA_I_BCDA
UISA_I_S	Boolean	UISA Feature UISA_I_S
UISA_I_E	Boolean	UISA Feature UISA_I_E
UISA_I_E_PC	Boolean	UISA Feature UISA_I_E_PC
UISA_I_E_PD	Boolean	UISA Feature UISA_I_E_PD
UISA_I_EC	Boolean	UISA Feature UISA_I_EC
UISA_I_FP	Boolean	UISA Feature UISA_I_FP
UISA_I_DFP	Boolean	UISA Feature UISA_I_DFP
UISA_I_MA	Boolean	UISA Feature UISA_I_MA
UISA_I_SP	Boolean	UISA Feature UISA_I_SP
UISA_I_V	Boolean	UISA Feature UISA_I_V
UISA_I_LMA	Boolean	UISA Feature UISA_I_LMA
UISA_I_WT	Boolean	UISA Feature UISA_I_WT
UISA_I_VLE	Boolean	UISA Feature UISA_I_VLE
ENABLE_FPU	Uns32	Enable FPU At Startup
UNIMP_TO_NOP	Boolean	Map Unimplemented Instructions to NOP
WARN_NOP	Boolean	Warn when executing nop-mapped instructions

8.0 Execution Modes

No execution modes.

9.0 Exceptions

Table 5.

Name	Code
Reset	0
Undefined	1
Arith	2
RdAlign	3
WrAlign	4
RdAbort	5
WrAbort	6
RdPriv	7
WrPriv	8
Fetch	9

10.0 Hierarchy of the model

A CPU core may allow the user to configure it to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.
OVP processor models can be written to include SMP blocks and to have many levels of hierarchy.

Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

10.1 Level 1:

This level in the model hierarchy has 2 commands.

This level in the model hierarchy has 3 register groups:

Table 6.

Group name	Registers
User	32
FloatingPoint	32
System	7

This level in the model hierarchy has no children.

11.0 Model Commands

11.1 Level 1:

Table 7.

Name	Arguments
isync	specify instruction address range for synchronous execution
itrace	enable or disable instruction tracing

12.0 Registers

12.1 Level 1:

12.1.1 User

Table 8.

Name	Bits	Initial value (Hex)		Description
GPR0	32	0	rw	
GPR1	32	0	rw	
GPR2	32	0	rw	
GPR3	32	0	rw	
GPR4	32	0	rw	
GPR5	32	0	rw	
GPR6	32	0	rw	
GPR7	32	0	rw	
GPR8	32	0	rw	
GPR9	32	0	rw	
GPR10	32	0	rw	
GPR11	32	0	rw	
GPR12	32	0	rw	
GPR13	32	0	rw	
GPR14	32	0	rw	
GPR15	32	0	rw	
GPR16	32	0	rw	
GPR17	32	0	rw	
GPR18	32	0	rw	
GPR19	32	0	rw	
GPR20	32	0	rw	
GPR21	32	0	rw	
GPR22	32	0	rw	
GPR23	32	0	rw	

GPR24	32	0	rw	
GPR25	32	0	rw	
GPR26	32	0	rw	
GPR27	32	0	rw	
GPR28	32	0	rw	
GPR29	32	0	rw	
GPR30	32	0	rw	
GPR31	32	0	rw	

12.1.2 FloatingPoint

Table 9.

Name	Bits	Initial value (Hex)		Description
FPR0	64	0	rw	
FPR1	64	0	rw	
FPR2	64	0	rw	
FPR3	64	0	rw	
FPR4	64	0	rw	
FPR5	64	0	rw	
FPR6	64	0	rw	
FPR7	64	0	rw	
FPR8	64	0	rw	
FPR9	64	0	rw	
FPR10	64	0	rw	
FPR11	64	0	rw	
FPR12	64	0	rw	
FPR13	64	0	rw	
FPR14	64	0	rw	
FPR15	64	0	rw	
FPR16	64	0	rw	
FPR17	64	0	rw	
FPR18	64	0	rw	
FPR19	64	0	rw	
FPR20	64	0	rw	
FPR21	64	0	rw	
FPR22	64	0	rw	
FPR23	64	0	rw	
FPR24	64	0	rw	
FPR25	64	0	rw	
FPR26	64	0	rw	
FPR27	64	0	rw	
FPR28	64	0	rw	

FPR29	64	0	rw	
FPR30	64	0	rw	
FPR31	64	0	rw	

12.1.3 System

Table 10.

Name	Bits	Initial value (Hex)		Description
PC	32	0	rw	program counter
MSR	32	0	rw	
CR	32	0	rw	
LR	32	0	rw	
CTR	32	0	rw	
XER	32	0	rw	
FPSCR	32	0	rw	

#

