OVP Guide to Using Processor Models

Model Specific Information for variant ARM_AArch32

Imperas Software Limited
Imperas Buildings, North Weston
Thame, Oxfordshire, OX9 2HA, UK
docs@imperas.com

Author	Imperas Software Limited
Version	0.4
Filename	OVP_Model_Specific_Information_arm_AArch32.pdf
Created	25 August 2015

Copyright Notice

Right to Copy Documentation

Destination Control Statement

Disclaimer

Table of Contents

1.0 Overview

This document provides the details of an OVP Fast Processor Model variant.
OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms. The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.
The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners.
There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

ARM Processor Model

1.2 Licensing

Usage of binary model under license governing simulator usage.
Note that for models of ARM CPUs the license includes the following terms:
Licensee is granted a non-exclusive, worldwide, non-transferable, revocable licence to:
If no source is being provided to the Licensee: use and copy only (no modifications rights are granted) the model for the sole purpose of designing, developing, analyzing, debugging, testing, verifying, validating and optimizing software which: (a) (i) is for ARM based systems; and (ii) does not incorporate the ARM Models or any part thereof; and (b) such ARM Models may not be used to emulate an ARM based system to run application software in a production or live environment.
If source code is being provided to the Licensee: use, copy and modify the model for the sole purpose of designing, developing, analyzing, debugging, testing, verifying, validating and optimizing software which: (a) (i) is for ARM based systems; and (ii) does not incorporate the ARM Models or any part thereof; and (b) such ARM Models may not be used to emulate an ARM based system to run application software in a production or live environment.
In the case of any Licensee who is either or both an academic or educational institution the purposes shall be limited to internal use.
Except to the extent that such activity is permitted by applicable law, Licensee shall not reverse engineer, decompile, or disassemble this model. If this model was provided to Licensee in Europe, Licensee shall not reverse engineer, decompile or disassemble the Model for the purposes of error correction.
The License agreement does not entitle Licensee to manufacture in silicon any product based on this model.
The License agreement does not entitle Licensee to use this model for evaluating the validity of any ARM patent.
Source of model available under separate Imperas Software License Agreement.
ARMv8 architecture models additionally require a run time model license - contact Imperas for more information.

1.3 Limitations

Instruction pipelines are not modeled in any way. All instructions are assumed to complete immediately. This means that instruction barrier instructions (e.g. ISB, CP15ISB) are treated as NOPs, with the exception of any undefined instruction behavior, which is modeled. The model does not implement speculative fetch behavior. The branch cache is not modeled. Caches and write buffers are not modeled in any way. All loads, fetches and stores complete immediately and in order, and are fully synchronous (as if the memory was of Strongly

Ordered or Device-nGnRnE type). Data barrier instructions (e.g. DSB, CP15DSB) are treated as NOPs, with the exception of any undefined instruction behavior, which is modeled. Cache manipulation instructions are implemented as NOPs, with the exception of any undefined instruction behavior, which is modeled.
Real-world timing effects are not modeled: all instructions are assumed to complete in a single cycle.
Performance Monitors are implemented as a register interface only.
TLBs are architecturally-accurate but not device accurate. This means that all TLB maintenance and address translation operations are fully implemented but the cache is larger than in the real device.
Debug registers are implemented but non-functional (which is sufficient to allow operating systems such as Linux to boot). Debug state is not implemented.
This initial ARMv8 model also has the following specific limitations, which will be rectified shortly:
The model currently implements only a memory-mapped GICv2, not a register-accessible GICv3.
The optional CRC32 instructions are not supported.
The optional SIMD Cryptographic Extension instructions are not supported.

1.4 Verification

Models have been extensively tested by Imperas. ARM Cortex-A models have been successfully used by customers to simulate SMP Linux, Ubuntu Desktop, VxWorks and ThreadX on Xilinx Zynq virtual platforms.

1.5 Features

AArch32 is implemented at EL3, EL2, EL1 and EL0.
SIMD, VFP and LPA (large physical address extension) are implemented as standard in ARMv8.
Security extensions are implemented (also known as TrustZone). To make non-secure accesses visible externally, override ID_AA64MMFR0_EL1.PARange to specify the required physical bus size (32, 36, 40, 42, 44 or 48 bits) and connect the processor to a bus one bit wider (33, 37, 41, 43, 45 or 49 bits, respectively). The extra most-significant bit is the NS bit, indicating a non-secure access. If non-secure accesses are not required to be made visible externally, connect the processor to a bus of exactly the size implied by ID_AA64MMFR0_EL1.PARange.
VMSA EL1, EL2 and EL3 stage 1 address translation is implemented. VMSA stage 2 address translation is implemented.
Generic Timer is present. Use parameter override_timerScaleFactor to specify the counter rate as a fraction of the processor MIPS rate (e.g. 10 implies Generic Timer counters increment once every 10 processor instructions).

2.0 Configuration

2.1 Location

The model source and object file is found in the VLNV tree at:
    arm.ovpworld.org/processor/arm/1.0

2.2 GDB Path

The default GDB for this model is found at:
    $IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/arm-none-eabi-gdb

2.3 Semi-Host Library

The default semi-host library file is found in the VLNV tree at :
    arm.ovpworld.org/semihosting/armNewlib/1.0

2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

2.6 Processor ELF Code

The ELF code supported by this model is: 0x28

3.0 Other Variants in this Model

Table 1.

Variant
ARMv4T
ARMv4xM
ARMv4
ARMv4TxM
ARMv5xM
ARMv5
ARMv5TxM
ARMv5T
ARMv5TExP
ARMv5TE
ARMv5TEJ
ARMv6
ARMv6K
ARMv6T2
ARMv6KZ
ARMv7
ARM7TDMI
ARM7EJ-S
ARM720T
ARM920T
ARM922T
ARM926EJ-S
ARM940T
ARM946E
ARM966E
ARM968E-S
ARM1020E
ARM1022E
ARM1026EJ-S
ARM1136J-S
ARM1156T2-S
ARM1176JZ-S
Cortex-R4
Cortex-R4F
Cortex-A5UP

Cortex-A5MPx1
Cortex-A5MPx2
Cortex-A5MPx3
Cortex-A5MPx4
Cortex-A8
Cortex-A9UP
Cortex-A9MPx1
Cortex-A9MPx2
Cortex-A9MPx3
Cortex-A9MPx4
Cortex-A7UP
Cortex-A7MPx1
Cortex-A7MPx2
Cortex-A7MPx3
Cortex-A7MPx4
Cortex-A15UP
Cortex-A15MPx1
Cortex-A15MPx2
Cortex-A15MPx3
Cortex-A15MPx4
Cortex-A17MPx1
Cortex-A17MPx2
Cortex-A17MPx3
Cortex-A17MPx4
AArch32
AArch64
Cortex-A53MPx1
Cortex-A53MPx2
Cortex-A53MPx3
Cortex-A53MPx4
Cortex-A57MPx1
Cortex-A57MPx2
Cortex-A57MPx3
Cortex-A57MPx4

4.0 Bus Ports

Table 2.

Type	Name	Bits
master (initiator)	INSTRUCTION	32
master (initiator)	DATA	32

5.0 Net Ports

Table 3.

Name	Type	Description
CNTVIRQ	output	Virtual timer event (active high)
CNTPSIRQ	output	Secure physical timer event (active high)
CNTPNSIRQ	output	Non-secure physical timer event (active high)
CNTPHPIRQ	output	Hypervisor physical timer event (active high)
VINITHI	input	Configure HIVECS mode (SCTLR.V)
CFGEND	input	Configure exception endianness (SCTLR.EE)
CFGTE	input	Configure exception state at reset (SCTLR.TE)
reset	input	Processor reset, active high
fiq	input	FIQ interrupt, active high (negation of nFIQ)
irq	input	IRQ interrupt, active high (negation of nIRQ)
vfiq	input	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq	input	Virtual IRQ interrupt, active high (negation of nVIRQ)
AXI_SLVERR	input	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE	input	CP15SDISABLE (active high)

6.0 FIFO Ports

No FIFO Ports in this model.

7.0 Parameters

Table 4.

Name	Type	Description
verbose	Boolean	Specify verbosity of output
showHiddenRegs	Boolean	Show hidden registers during register tracing
UAL	Boolean	Disassemble using UAL syntax
enableVFPAtReset	Boolean	Enable vector floating point (SIMD and VFP) instructions at reset. (Enables cp10/11 in CPACR and sets FPEXC.EN)
compatibility	Enumeration	Specify compatibility mode ISA=0 gdb=1 nopSVC=2
override_debugMask	Uns32	Specifies debug mask, enabling debug output for model components
override_fcsePresent	Boolean	Specifies that FCSE is present (if true)
override_fpexcDexPresent	Boolean	Specifies that the FPEXC.DEX register field is implemented (if true)
override_advSIMDPresent	Boolean	Specifies that Advanced SIMD extensions are present (if true)
override_vfpPresent	Boolean	Specifies that VFP extensions are present (if true)
override_SCTLR_V	Boolean	Override SCTLR.V with the passed value (enables high vectors)

override_SCTLR_CP15BEN_Present	Boolean	Enable ARMv7 SCTLR.CP15BEN bit (CP15 barrier enable)
override_MIDR	Uns32	Override MIDR register
override_CTR	Uns32	Override CTR register
override_TLBTR	Uns32	Override TLBTR register
override_CLIDR	Uns32	Override CLIDR register
override_AIDR	Uns32	Override AIDR register
override_PFR0	Uns32	Override ID_PFR0 register
override_PFR1	Uns32	Override ID_PFR1 register
override_DFR0	Uns32	Override ID_DFR0 register
override_AFR0	Uns32	Override ID_AFR0 register
override_MMFR0	Uns32	Override ID_MMFR0 register
override_MMFR1	Uns32	Override ID_MMFR1 register
override_MMFR2	Uns32	Override ID_MMFR2 register
override_MMFR3	Uns32	Override ID_MMFR3 register
override_ISAR0	Uns32	Override ID_ISAR0 register
override_ISAR1	Uns32	Override ID_ISAR1 register
override_ISAR2	Uns32	Override ID_ISAR2 register
override_ISAR3	Uns32	Override ID_ISAR3 register
override_ISAR4	Uns32	Override ID_ISAR4 register
override_ISAR5	Uns32	Override ID_ISAR5 register
override_PMCR	Uns32	Override PMCR register (not functionally significant in the model)
override_PMCEID0	Uns32	Override PMCEID0 register (not functionally significant in the model)
override_PMCEID1	Uns32	Override PMCEID1 register (not functionally significant in the model)
override_FPSID	Uns32	Override SIMD/VFP FPSID register
override_MVFR0	Uns32	Override SIMD/VFP MVFR0 register
override_MVFR1	Uns32	Override SIMD/VFP MVFR1 register
override_MVFR2	Uns32	Override SIMD/VFP MVFR2 register
override_FPEXC	Uns32	Override SIMD/VFP FPEXC register
override_ERG	Uns32	Specifies exclusive reservation granule
override_RMR	Uns32	Override RMR register
override_RVBAR	Uns64	Override RVBAR register
override_AA64PFR0_EL1	Uns64	Override ID_AA64PFR0_EL1 register
override_AA64PFR1_EL1	Uns64	Override ID_AA64PFR1_EL1 register
override_AA64DFR0_EL1	Uns64	Override ID_AA64DFR0_EL1 register
override_AA64DFR1_EL1	Uns64	Override ID_AA64DFR1_EL1 register
override_AA64AFR0_EL1	Uns64	Override ID_AA64AFR0_EL1 register
override_AA64AFR1_EL1	Uns64	Override ID_AA64AFR1_EL1 register
override_AA64ISAR0_EL1	Uns64	Override ID_AA64ISAR0_EL1 register
override_AA64ISAR1_EL1	Uns64	Override ID_AA64ISAR1_EL1 register

override_AA64MMFR0_EL1	Uns64	Override ID_AA64MMFR0_EL1 register
override_AA64MMFR1_EL1	Uns64	Override ID_AA64MMFR1_EL1 register
override_DCZID_EL0	Uns32	Override DCZID_EL0 register
override_STRoffsetPC12	Boolean	Specifies that STR/STR of PC should do so with 12:byte offset from the current instruction (if true), otherwise an 8:byte offset is used
override_fcseRequiresMMU	Boolean	Specifies that FCSE is active only when MMU is enabled (if true)
override_ignoreBadCp15	Boolean	Specifies whether invalid coprocessor 15 access should be ignored (if true) or cause Invalid Instruction exceptions (if false)
override_SGIDisable	Boolean	Override whether GIC SGIs may be disabled (if true) or are permanently enabled (if false)
override_condUndefined	Boolean	Force undefined instructions to take Undefined Instruction exception even if they are conditional
override_deviceStrongAligned	Boolean	Force accesses to Device and Strongly Ordered regions to be aligned
override_Control_V	Boolean	Override SCTLR.V with the passed value (deprecated, use override_SCTLR_V)
override_MainId	Uns32	Override MIDR register (deprecated, use override_MIDR)
override_CacheType	Uns32	Override CTR register (deprecated, use override_CTR)
override_TLBType	Uns32	Override TLBTR register (deprecated, use override_TLBTR)
override_InstructionAttributes0	Uns32	Override ID_ISAR0 register (deprecated, use override_ISAR0)
override_InstructionAttributes1	Uns32	Override ID_ISAR1 register (deprecated, use override_ISAR1)
override_InstructionAttributes2	Uns32	Override ID_ISAR2 register (deprecated, use override_ISAR2)
override_InstructionAttributes3	Uns32	Override ID_ISAR3 register (deprecated, use override_ISAR3)
override_InstructionAttributes4	Uns32	Override ID_ISAR4 register (deprecated, use override_ISAR4)
override_InstructionAttributes5	Uns32	Override ID_ISAR5 register (deprecated, use override_ISAR5)

8.0 Execution Modes

Table 5.

Name	Code
User	16
FIQ	17

IRQ	18
Supervisor	19
Monitor	22
Abort	23
Hypervisor	26
Undefined	27
System	31

9.0 Exceptions

Table 6.

Name	**Code**
Reset	0
Undefined	1
SupervisorCall	2
SecureMonitorCall	3
HypervisorCall	4
PrefetchAbort	5
DataAbort	6
HypervisorTrap	7
IRQ	8
FIQ	9
IllegalState	10

10.0 Hierarchy of the model

A CPU core may allow the user to configure it to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.
OVP processor models can be written to include SMP blocks and to have many levels of hierarchy.

Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

10.1 Level 1: CPU

This level in the model hierarchy has 4 commands.

This level in the model hierarchy has 19 register groups:

Table 7.

Group name	Registers
Core	16
Control	3
User	7
FIQ	8
IRQ	3
Supervisor	3
Monitor	3
Hypervisor	3
Undefined	3
Abort	3
SIMD_VFP	32
SIMD_VFP_SYS	6
Coprocessor_32_bit	274
Coprocessor_32_bit_secure	25
Coprocessor_32_bit_non_secure	25
Coprocessor_64_bit	13
Coprocessor_64_bit_secure	3
Coprocessor_64_bit_non_secure	3
Integration_support	2

This level in the model hierarchy has no children.

11.0 Model Commands

11.1 Level 1: CPU

Table 8.

Name	Arguments
debugflags	
dumpTLB	
isync	specify instruction address range for synchronous execution
itrace	enable or disable instruction tracing

12.0 Registers

12.1 Level 1: CPU

12.1.1 Core

Table 9.

Name	Bits	Initial value (Hex)		Description
r0	32	0	rw	
r1	32	0	rw	
r2	32	0	rw	
r3	32	0	rw	
r4	32	0	rw	
r5	32	0	rw	
r6	32	0	rw	
r7	32	0	rw	
r8	32	0	rw	
r9	32	0	rw	
r10	32	0	rw	
r11	32	0	rw	frame pointer
r12	32	0	rw	
sp	32	0	rw	stack pointer
lr	32	0	rw	
pc	32	0	rw	program counter

12.1.2 Control

Table 10.

Name	Bits	Initial value (Hex)		Description
fps	32	0	rw	archaic FPSCR view (for gdb)
cpsr	32	1d3	rw	
spsr	32	0	rw	

12.1.3 User

Table 11.

Name	Bits	Initial value (Hex)		Description
r8_usr	32	0	rw	
r9_usr	32	0	rw	
r10_usr	32	0	rw	
r11_usr	32	0	rw	
r12_usr	32	0	rw	
sp_usr	32	0	rw	
lr_usr	32	0	rw	

12.1.4 FIQ

Table 12.

Name	Bits	Initial value (Hex)		Description
r8_fiq	32	0	rw	
r9_fiq	32	0	rw	
r10_fiq	32	0	rw	
r11_fiq	32	0	rw	
r12_fiq	32	0	rw	
sp_fiq	32	0	rw	
lr_fiq	32	0	rw	
spsr_fiq	32	0	rw	

12.1.5 IRQ

Table 13.

Name	Bits	Initial value (Hex)		Description
sp_irq	32	0	rw	
lr_irq	32	0	rw	
spsr_irq	32	0	rw	

12.1.6 Supervisor

Table 14.

Name	Bits	Initial value (Hex)		Description
sp_svc	32	0	rw	
lr_svc	32	0	rw	

spsr_svc	32	0	rw	

12.1.7 Monitor

Table 15.

Name	Bits	Initial value (Hex)		Description
sp_mon	32	0	rw	
lr_mon	32	0	rw	
spsr_mon	32	0	rw	

12.1.8 Hypervisor

Table 16.

Name	Bits	Initial value (Hex)		Description
sp_hyp	32	0	rw	
elr_hyp	32	0	rw	
spsr_hyp	32	0	rw	

12.1.9 Undefined

Table 17.

Name	Bits	Initial value (Hex)		Description
sp_undef	32	0	rw	
lr_undef	32	0	rw	
spsr_undef	32	0	rw	

12.1.10 Abort

Table 18.

Name	Bits	Initial value (Hex)		Description
sp_abt	32	0	rw	
lr_abt	32	0	rw	
spsr_abt	32	0	rw	

12.1.11 SIMD_VFP

Table 19.

Name	Bits	Initial value (Hex)		Description
d0	64	0	rw	
d1	64	0	rw	

d2	64	0	rw	
d3	64	0	rw	
d4	64	0	rw	
d5	64	0	rw	
d6	64	0	rw	
d7	64	0	rw	
d8	64	0	rw	
d9	64	0	rw	
d10	64	0	rw	
d11	64	0	rw	
d12	64	0	rw	
d13	64	0	rw	
d14	64	0	rw	
d15	64	0	rw	
d16	64	0	rw	
d17	64	0	rw	
d18	64	0	rw	
d19	64	0	rw	
d20	64	0	rw	
d21	64	0	rw	
d22	64	0	rw	
d23	64	0	rw	
d24	64	0	rw	
d25	64	0	rw	
d26	64	0	rw	
d27	64	0	rw	
d28	64	0	rw	
d29	64	0	rw	
d30	64	0	rw	
d31	64	0	rw	

12.1.12 SIMD_VFP_SYS

Table 20.

Name	Bits	Initial value (Hex)		Description
FPSID	32	41033092	r-	floating-point system ID
FPSCR	32	0	rw	floating-point status/control
FPEXC	32	700	rw	floating-point exception
MVFR0	32	10110222	r-	Media/VFP feature 0
MVFR1	32	12111111	r-	Media/VFP feature 1
MVFR2	32	43	r-	Media/VFP feature 2

12.1.13 Coprocessor_32_bit

Table 21.

Name	Bits	Initial value (Hex)		Description
ACTLR	32	0	rw	Auxiliary Control
ADFSR	32	0	rw	Auxilary Data Fault Status
AIDR	32	0	r-	Auxiliary ID
AIFSR	32	0	rw	Auxilary Instruction Fault Status
AMAIR0	32	0	rw	Auxilary Memory Attribute Indirection 0
AMAIR1	32	0	rw	Auxilary Memory Attribute Indirection 1
ATS1CPR	32	-	-w	Address Translate Stage 1 Current State EL1 Read
ATS1CPW	32	-	-w	Address Translate Stage 1 Current State EL1 Write
ATS1CUR	32	-	-w	Address Translate Stage 1 Current State Unprivileged Read
ATS1CUW	32	-	-w	Address Translate Stage 1 Current State Unprivileged Write
ATS1HR	32	-	-w	Address Translate Stage 1 Hyp Mode Read
ATS1HW	32	-	-w	Address Translate Stage 1 Hyp Mode Write
ATS12NSOPR	32	-	-w	Address Translate Stages 1 and 2 Non-Secure Only EL1 Read
ATS12NSOPW	32	-	-w	Address Translate Stages 1 and 2 Non-Secure Only EL1 Write
ATS12NSOUR	32	-	-w	Address Translate Stages 1 and 2 Non-Secure Only Unprivileged Read
ATS12NSOUW	32	-	-w	Address Translate Stages 1 and 2 Non-Secure Only Unprivileged Write
BPIALL	32	-	-w	Branch Predictor Invalidate All
BPIALLIS	32	-	-w	Branch Predictor Invalidate All (IS)
BPIMVA	32	-	-w	Branch Predictor Invalidate by VA
CCSIDR	32	701fe00a	r-	Cache Size ID
CLIDR	32	a000023	r-	Cache Level ID
CNTFRQ	32	4c4b40	rw	Counter Frequency
CNTHCTL	32	3	rw	Timer EL2 Control
CNTHP_CTL	32	0	rw	Counter-Timer Hyp Physical Timer Control
CNTHP_TVAL	32	0	rw	Counter-Timer Hyp Physical Timer TimerValue
CNTKCTL	32	0	rw	Timer EL1 Control
CNTP_CTL	32	0	rw	Counter-Timer Physical Timer Control
CNTP_TVAL	32	0	rw	Counter-Timer Physical Timer TimerValue
CNTV_CTL	32	0	rw	Counter-Timer Virtual Timer Control
CNTV_TVAL	32	0	rw	Counter-Timer Virtual Timer TimerValue
CONTEXTIDR	32	0	rw	Context ID
CP15DMB	32	-	-w	CP15 Data Memory Barrier
CP15DSB	32	-	-w	CP15 Data Synchronization Barrier

CP15ISB	32	-	-w	CP15 Instruction Synchronization Barrier
CPACR	32	0	rw	Coprocessor Access Control
CSSELR	32	0	rw	Cache Size Selection
CTR	32	8404c004	r-	Cache Type
DACR	32	0	rw	Domain Access Control
DBGAUTHSTATUS	32	aa	r-	Debug Authentication Status
DBGBCR0	32	0	rw	Debug Breakpoint Control 0
DBGBCR1	32	0	rw	Debug Breakpoint Control 1
DBGBCR2	32	0	rw	Debug Breakpoint Control 2
DBGBCR3	32	0	rw	Debug Breakpoint Control 3
DBGBCR4	32	0	rw	Debug Breakpoint Control 4
DBGBCR5	32	0	rw	Debug Breakpoint Control 5
DBGBCR6	32	0	rw	Debug Breakpoint Control 6
DBGBCR7	32	0	rw	Debug Breakpoint Control 7
DBGBCR8	32	0	rw	Debug Breakpoint Control 8
DBGBCR9	32	0	rw	Debug Breakpoint Control 9
DBGBCR10	32	0	rw	Debug Breakpoint Control 10
DBGBCR11	32	0	rw	Debug Breakpoint Control 11
DBGBCR12	32	0	rw	Debug Breakpoint Control 12
DBGBCR13	32	0	rw	Debug Breakpoint Control 13
DBGBCR14	32	0	rw	Debug Breakpoint Control 14
DBGBCR15	32	0	rw	Debug Breakpoint Control 15
DBGBVR0	32	0	rw	Debug Breakpoint Value 0
DBGBVR1	32	0	rw	Debug Breakpoint Value 1
DBGBVR2	32	0	rw	Debug Breakpoint Value 2
DBGBVR3	32	0	rw	Debug Breakpoint Value 3
DBGBVR4	32	0	rw	Debug Breakpoint Value 4
DBGBVR5	32	0	rw	Debug Breakpoint Value 5
DBGBVR6	32	0	rw	Debug Breakpoint Value 6
DBGBVR7	32	0	rw	Debug Breakpoint Value 7
DBGBVR8	32	0	rw	Debug Breakpoint Value 8
DBGBVR9	32	0	rw	Debug Breakpoint Value 9
DBGBVR10	32	0	rw	Debug Breakpoint Value 10
DBGBVR11	32	0	rw	Debug Breakpoint Value 11
DBGBVR12	32	0	rw	Debug Breakpoint Value 12
DBGBVR13	32	0	rw	Debug Breakpoint Value 13
DBGBVR14	32	0	rw	Debug Breakpoint Value 14
DBGBVR15	32	0	rw	Debug Breakpoint Value 15
DBGBXVR0	32	0	rw	Debug Breakpoint Extended Value 0
DBGBXVR1	32	0	rw	Debug Breakpoint Extended Value 1
DBGBXVR2	32	0	rw	Debug Breakpoint Extended Value 2
DBGBXVR3	32	0	rw	Debug Breakpoint Extended Value 3

DBGBXVR4	32	0	rw	Debug Breakpoint Extended Value 4
DBGBXVR5	32	0	rw	Debug Breakpoint Extended Value 5
DBGBXVR6	32	0	rw	Debug Breakpoint Extended Value 6
DBGBXVR7	32	0	rw	Debug Breakpoint Extended Value 7
DBGBXVR8	32	0	rw	Debug Breakpoint Extended Value 8
DBGBXVR9	32	0	rw	Debug Breakpoint Extended Value 9
DBGBXVR10	32	0	rw	Debug Breakpoint Extended Value 10
DBGBXVR11	32	0	rw	Debug Breakpoint Extended Value 11
DBGBXVR12	32	0	rw	Debug Breakpoint Extended Value 12
DBGBXVR13	32	0	rw	Debug Breakpoint Extended Value 13
DBGBXVR14	32	0	rw	Debug Breakpoint Extended Value 14
DBGBXVR15	32	0	rw	Debug Breakpoint Extended Value 15
DBGCLAIMCLR	32	0	rw	Debug Claim Tag Clear
DBGCLAIMSET	32	0	rw	Debug Claim Tag Set
DBGDCCINT	32	0	rw	DCC Interrupt Enable
DBGDIDR	32	0	r-	Debug ID
DBGDRAR	32	0	r-	Debug ROM Address (32-bit)
DBGDSCRext	32	0	rw	Debug Status and Control
DBGDSCRint	32	0	r-	Debug Status and Control, Internal View
DBGDTRRXext	32	0	rw	Debug Data Transfer, Receive, External View
DBGDTRTRXint	32	0	rw	Debug Data Transfer, Transmit/Receive
DBGDTRTXext	32	0	rw	Debug Data Transfer, Transmit, External View
DBGOSDLR	32	0	rw	Debug OS Double Lock
DBGOSECCR	32	0	rw	Debug OS Lock Exception Catch Control
DBGOSLAR	32	-	-w	Debug OS Lock Access
DBGOSLSR	32	a	r-	Debug OS Lock Status
DBGPRCR	32	0	rw	Debug Power Control
DBGVCR	32	0	rw	Debug Vector Catch
DBGWCR0	32	0	rw	Debug Watchpoint Control 0
DBGWCR1	32	0	rw	Debug Watchpoint Control 1
DBGWCR2	32	0	rw	Debug Watchpoint Control 2
DBGWCR3	32	0	rw	Debug Watchpoint Control 3
DBGWCR4	32	0	rw	Debug Watchpoint Control 4
DBGWCR5	32	0	rw	Debug Watchpoint Control 5
DBGWCR6	32	0	rw	Debug Watchpoint Control 6
DBGWCR7	32	0	rw	Debug Watchpoint Control 7
DBGWCR8	32	0	rw	Debug Watchpoint Control 8
DBGWCR9	32	0	rw	Debug Watchpoint Control 9
DBGWCR10	32	0	rw	Debug Watchpoint Control 10
DBGWCR11	32	0	rw	Debug Watchpoint Control 11
DBGWCR12	32	0	rw	Debug Watchpoint Control 12
DBGWCR13	32	0	rw	Debug Watchpoint Control 13

DBGWCR14	32	0	rw	Debug Watchpoint Control 14
DBGWCR15	32	0	rw	Debug Watchpoint Control 15
DBGWVR0	32	0	rw	Debug Watchpoint Value 0
DBGWVR1	32	0	rw	Debug Watchpoint Value 1
DBGWVR2	32	0	rw	Debug Watchpoint Value 2
DBGWVR3	32	0	rw	Debug Watchpoint Value 3
DBGWVR4	32	0	rw	Debug Watchpoint Value 4
DBGWVR5	32	0	rw	Debug Watchpoint Value 5
DBGWVR6	32	0	rw	Debug Watchpoint Value 6
DBGWVR7	32	0	rw	Debug Watchpoint Value 7
DBGWVR8	32	0	rw	Debug Watchpoint Value 8
DBGWVR9	32	0	rw	Debug Watchpoint Value 9
DBGWVR10	32	0	rw	Debug Watchpoint Value 10
DBGWVR11	32	0	rw	Debug Watchpoint Value 11
DBGWVR12	32	0	rw	Debug Watchpoint Value 12
DBGWVR13	32	0	rw	Debug Watchpoint Value 13
DBGWVR14	32	0	rw	Debug Watchpoint Value 14
DBGWVR15	32	0	rw	Debug Watchpoint Value 15
DCCIMVAC	32	-	-w	Data Cache Line Clean and Invalidate by VA to PoC
DCCISW	32	-	-w	Data Cache Line Clean and Invalidate by Set/Way
DCCMVAC	32	-	-w	Data Cache Line Clean by VA to PoC
DCCMVAU	32	-	-w	Data Cache Line Clean by VA to PoU
DCCSW	32	-	-w	Data Cache Line Clean by Set/Way
DCIMVAC	32	-	-w	Data Cache Line Invalidate by VA to PoC
DCISW	32	-	-w	Data Cache Line Invalidate by Set/Way
DFAR	32	0	rw	Data Fault Address
DFSR	32	0	rw	Data Fault Status
DLR	32	0	rw	Debug Link
DSPSR	32	0	rw	Debug Saved Program Status
DTLBIALL	32	-	-w	Invalidate Entire Data TLB
DTLBIASID	32	-	-w	Invalidate Data TLB by ASID
DTLBIMVA	32	-	-w	Invalidate Data TLB by VA
HACR	32	0	rw	Hyp Auxiliary Configuration
HACTLR	32	0	rw	Hyp Auxiliary Control
HADFSR	32	0	rw	Hyp Auxiliary Data Fault Status
HAIFSR	32	0	rw	Hyp Auxiliary Instruction Fault Status
HAMAIR0	32	0	rw	Hyp Auxiliary Memory Attribute Indirection 0
HAMAIR1	32	0	rw	Hyp Auxiliary Memory Attribute Indirection 1
HCPTR	32	33ff	rw	Hyp Coprocessor Trap
HCR	32	0	rw	Hyp Configuration
HCR2	32	0	rw	Hyp Configuration 2
HDCR	32	6	rw	Hyp Debug Configuration

HDFAR	32	0	rw	Hyp Data Fault Address
HIFAR	32	0	rw	Hyp Instruction Fault Address
HMAIR0	32	0	rw	Hyp Memory Attribute Indirection 0
HMAIR1	32	0	rw	Hyp Memory Attribute Indirection 1
HPFAR	32	0	rw	Hyp IPA Fault Address
HSCTLR	32	30c50838	rw	Hyp System Control
HSR	32	0	rw	Hyp Syndrome
HSTR	32	0	rw	Hyp System Trap
HTCR	32	80800000	rw	Hyp Translation Control
HTPIDR	32	0	rw	Hyp Thread and Process ID
HVBAR	32	0	rw	Hyp Vector Base Address
ICIALLU	32	-	-w	Instruction Cache Invalidate All
ICIALLUIS	32	-	-w	Instruction Cache Invalidate All (IS)
ICIMVAU	32	-	-w	Instruction Cache Invalidate by VA
ID_AFR0	32	0	r-	Auxiliary Feature 0
ID_DFR0	32	3010066	r-	Debug Feature 0
ID_ISAR0	32	2101110	r-	Instruction Set Attribute 0
ID_ISAR1	32	13112111	r-	Instruction Set Attribute 1
ID_ISAR2	32	21232042	r-	Instruction Set Attribute 2
ID_ISAR3	32	1112131	r-	Instruction Set Attribute 3
ID_ISAR4	32	11142	r-	Instruction Set Attribute 4
ID_ISAR5	32	1	r-	Instruction Set Attribute 5
ID_MMFR0	32	10101105	r-	Memory Model Feature 0
ID_MMFR1	32	40000000	r-	Memory Model Feature 1
ID_MMFR2	32	1260000	r-	Memory Model Feature 2
ID_MMFR3	32	2102211	r-	Memory Model Feature 3
ID_PFR0	32	131	r-	Processor Feature 0
ID_PFR1	32	11011	r-	Processor Feature 1
IFAR	32	0	rw	Instruction Fault Address
IFSR	32	0	rw	Instruction Fault Status
ISR	32	0	r-	Interrupt Status
ITLBIALL	32	-	-w	Invalidate Entire Instruction TLB
ITLBIASID	32	-	-w	Invalidate Instruction TLB by ASID
ITLBIMVA	32	-	-w	Invalidate Instruction TLB by VA
JIDR	32	0	rw	Jazelle ID
JMCR	32	0	rw	Jazelle Main Configuration
JOSCR	32	0	rw	Jazelle OS Control
MAIR0	32	98aa4	rw	Memory Attribute Indirection 0
MAIR1	32	44e048e0	rw	Memory Attribute Indirection 1
MIDR	32	410fd000	r-	Main ID
MPIDR	32	c0000000	r-	Multiprocessor Affinity
MVBAR	32	0	rw	Monitor Vector Base Address

NMRR	32	44e048e0	rw	Normal Memory Remap
NSACR	32	0	rw	Non-Secure Access Control
PAR	32	0	rw	Physical Address
PMCCFILTR	32	0	rw	Performance Monitors Cycle Count Filter
PMCCNTR	32	0	rw	Performance Monitors Cycle Count
PMCEID0	32	3fff0f3f	r-	Performance Monitors Common Event ID 0
PMCEID1	32	0	r-	Performance Monitors Common Event ID 1
PMCNTENCLR	32	0	rw	Performance Monitors Count Enable Clear
PMCNTENSET	32	0	rw	Performance Monitors Count Enable Set
PMCR	32	410f3000	rw	Performance Monitors Control
PMEVCNTR0	32	0	rw	Performance Monitors Event Count 0
PMEVCNTR1	32	0	rw	Performance Monitors Event Count 1
PMEVCNTR2	32	0	rw	Performance Monitors Event Count 2
PMEVCNTR3	32	0	rw	Performance Monitors Event Count 3
PMEVCNTR4	32	0	rw	Performance Monitors Event Count 4
PMEVCNTR5	32	0	rw	Performance Monitors Event Count 5
PMEVTYPER0	32	0	rw	Performance Monitors Event Type 0
PMEVTYPER1	32	0	rw	Performance Monitors Event Type 1
PMEVTYPER2	32	0	rw	Performance Monitors Event Type 2
PMEVTYPER3	32	0	rw	Performance Monitors Event Type 3
PMEVTYPER4	32	0	rw	Performance Monitors Event Type 4
PMEVTYPER5	32	0	rw	Performance Monitors Event Type 5
PMINTENCLR	32	0	rw	Performance Monitors Interrupt Enable Clear
PMINTENSET	32	0	rw	Performance Monitors Interrupt Enable Set
PMOVSR	32	0	rw	Performance Monitors Overflow Flag Status
PMOVSSET	32	0	rw	Performance Monitors Overflow Flag Status Set
PMSELR	32	0	rw	Performance Monitors Event Counter Selection
PMSWINC	32	-	-w	Performance Monitors Software Increment
PMUSERENR	32	0	rw	Performance Monitors User Enable
PMXEVCNTR	32	0	rw	Performance Monitors Selected Event Count
PMXEVTYPER	32	0	rw	Performance Monitors Selected Event Type
PRRR	32	98aa4	rw	Primary Region Remap
REVIDR	32	0	r-	Revision ID
SCR	32	0	rw	Secure Configuration
SCTLR	32	c50838	rw	System Control
SDCR	32	0	rw	Secure Debug Configuration
SDER	32	0	rw	Secure Debug Enable
TCMTR	32	0	r-	TCM Type
TLBIALL	32	-	-w	Invalidate Entire Unified TLB
TLBIALLH	32	-	-w	Invalidate Entire Hyp Unified TLB
TLBIALLHIS	32	-	-w	Invalidate Entire Hyp TLB (IS)
TLBIALLIS	32	-	-w	Invalidate Entire Unified TLB (IS)

TLBIALLNSNH	32	-	-w	Invalidate Entire Non-Secure Non-Hyp Unified TLB
TLBIALLNSNHIS	32	-	-w	Invalidate Entire Non-Secure Non-Hyp Unified TLB (IS)
TLBIASID	32	-	-w	Invalidate Unified TLB by ASID
TLBIASIDIS	32	-	-w	Invalidate Unified TLB by ASID (IS)
TLBIIPAS2	32	-	-w	Invalidate by IPA, Stage 2
TLBIIPAS2IS	32	-	-w	Invalidate by IPA, Stage 2 (IS)
TLBIIPAS2L	32	-	-w	Invalidate by IPA, Stage 2, Last level
TLBIIPAS2LIS	32	-	-w	Invalidate by IPA, Stage 2, Last level (IS)
TLBIMVA	32	-	-w	Invalidate Unified TLB by VA
TLBIMVAA	32	-	-w	Invalidate Unified TLB by VA, all ASID
TLBIMVAAIS	32	-	-w	Invalidate Unified TLB by VA, all ASID (IS)
TLBIMVAAL	32	-	-w	Invalidate Unified TLB by VA, all ASID, Last level
TLBIMVAALIS	32	-	-w	Invalidate Unified TLB by VA, all ASID, Last level (IS)
TLBIMVAH	32	-	-w	Invalidate Hyp Unified TLB by VA
TLBIMVAHIS	32	-	-w	Invalidate Hyp Unified TLB by VA (IS)
TLBIMVAIS	32	-	-w	Invalidate Unified TLB by VA (IS)
TLBIMVAL	32	-	-w	Invalidate Unified TLB by VA, Last level
TLBIMVALH	32	-	-w	Invalidate Hyp Unified TLB by VA, Last level
TLBIMVALHIS	32	-	-w	Invalidate Hyp Unified TLB by VA, Last level (IS)
TLBIMVALIS	32	-	-w	Invalidate Unified TLB by VA, Last level (IS)
TLBTR	32	0	r-	TLB Type
TPIDRPRW	32	0	rw	PL0 Read/Write Software Thread ID
TPIDRURO	32	0	rw	PL0 Read-Only Software Thread ID
TPIDRURW	32	0	rw	PL1 Software Thread ID
TTBCR	32	0	rw	Translation Table Base Control
TTBR0	32	0	rw	Translation Table Base 0
TTBR1	32	0	rw	Translation Table Base 1
VBAR	32	0	rw	Vector Base Address
VMPIDR	32	c0000000	rw	Virtualization Multirocessor ID
VPIDR	32	410fd000	rw	Virtualization Processor ID
VTCR	32	80000000	rw	Virtualization Translation Control

12.1.14 Coprocessor_32_bit_secure

Table 22.

Name	Bits	Initial value (Hex)		Description
ACTLR_S	32	0	rw	Auxiliary Control
ADFSR_S	32	0	rw	Auxilary Data Fault Status
AIFSR_S	32	0	rw	Auxilary Instruction Fault Status
AMAIR0_S	32	0	rw	Auxilary Memory Attribute Indirection 0
AMAIR1_S	32	0	rw	Auxilary Memory Attribute Indirection 1

CONTEXTIDR_S	32	0	rw	Context ID
CSSELR_S	32	0	rw	Cache Size Selection
DACR_S	32	0	rw	Domain Access Control
DFAR_S	32	0	rw	Data Fault Address
DFSR_S	32	0	rw	Data Fault Status
IFAR_S	32	0	rw	Instruction Fault Address
IFSR_S	32	0	rw	Instruction Fault Status
MAIR0_S	32	98aa4	rw	Memory Attribute Indirection 0
MAIR1_S	32	44e048e0	rw	Memory Attribute Indirection 1
NMRR_S	32	44e048e0	rw	Normal Memory Remap
PAR_S	32	0	rw	Physical Address
PRRR_S	32	98aa4	rw	Primary Region Remap
SCTLR_S	32	c50838	rw	System Control
TPIDRPRW_S	32	0	rw	PL0 Read/Write Software Thread ID
TPIDRURO_S	32	0	rw	PL0 Read-Only Software Thread ID
TPIDRURW_S	32	0	rw	PL1 Software Thread ID
TTBCR_S	32	0	rw	Translation Table Base Control
TTBR0_S	32	0	rw	Translation Table Base 0
TTBR1_S	32	0	rw	Translation Table Base 1
VBAR_S	32	0	rw	Vector Base Address

12.1.15 Coprocessor_32_bit_non_secure

Table 23.

Name	Bits	Initial value (Hex)		Description
ACTLR_NS	32	0	rw	Auxiliary Control
ADFSR_NS	32	0	rw	Auxilary Data Fault Status
AIFSR_NS	32	0	rw	Auxilary Instruction Fault Status
AMAIR0_NS	32	0	rw	Auxilary Memory Attribute Indirection 0
AMAIR1_NS	32	0	rw	Auxilary Memory Attribute Indirection 1
CONTEXTIDR_NS	32	0	rw	Context ID
CSSELR_NS	32	0	rw	Cache Size Selection
DACR_NS	32	0	rw	Domain Access Control
DFAR_NS	32	0	rw	Data Fault Address
DFSR_NS	32	0	rw	Data Fault Status
IFAR_NS	32	0	rw	Instruction Fault Address
IFSR_NS	32	0	rw	Instruction Fault Status
MAIR0_NS	32	98aa4	rw	Memory Attribute Indirection 0
MAIR1_NS	32	44e048e0	rw	Memory Attribute Indirection 1
NMRR_NS	32	44e048e0	rw	Normal Memory Remap
PAR_NS	32	0	rw	Physical Address
PRRR_NS	32	98aa4	rw	Primary Region Remap

SCTLR_NS	32	c50838	rw	System Control
TPIDRPRW_NS	32	0	rw	PL0 Read/Write Software Thread ID
TPIDRURO_NS	32	0	rw	PL0 Read-Only Software Thread ID
TPIDRURW_NS	32	0	rw	PL1 Software Thread ID
TTBCR_NS	32	0	rw	Translation Table Base Control
TTBR0_NS	32	0	rw	Translation Table Base 0
TTBR1_NS	32	0	rw	Translation Table Base 1
VBAR_NS	32	0	rw	Vector Base Address

12.1.16 Coprocessor_64_bit

Table 24.

Name	Bits	Initial value (Hex)		Description
CNTHP_CVAL	64	0	rw	Counter-Timer Hyp Physical Timer CompareValue
CNTPCT	64	0	r-	Counter-Timer Physical Count
CNTP_CVAL	64	0	rw	Counter-Timer Physical Timer CompareValue
CNTVCT	64	0	r-	Counter-Timer Virtual Count
CNTVOFF	64	0	rw	Virtual Offset
CNTV_CVAL	64	0	rw	Counter-Timer Virtual Timer CompareValue
DBGDRAR64	64	0	r-	Debug ROM Address (64-bit)
HTTBR	64	0	rw	Hyp Translation Table Base
PARLPA	64	0	rw	Physical Address
PMCCNTR64	64	0	rw	Performance Monitors Cycle Count (64-bit)
TTBR0LPA	64	0	rw	Translation Table Base 0
TTBR1LPA	64	0	rw	Translation Table Base 1
VTTBR	64	0	rw	Virtualization Translation Table Base

12.1.17 Coprocessor_64_bit_secure

Table 25.

Name	Bits	Initial value (Hex)		Description
PARLPA_S	64	0	rw	Physical Address
TTBR0LPA_S	64	0	rw	Translation Table Base 0
TTBR1LPA_S	64	0	rw	Translation Table Base 1

12.1.18 Coprocessor_64_bit_non_secure

Table 26.

Name	Bits	Initial value (Hex)		Description
PARLPA_NS	64	0	rw	Physical Address

TTBR0LPA_NS	64	0	rw	Translation Table Base 0
TTBR1LPA_NS	64	0	rw	Translation Table Base 1

12.1.19 Integration_support

Table 27.

Name	Bits	Initial value (Hex)		Description
transactPL	32	1	r-	privilege level of current memory transaction
transactAT	32	0	r-	current memory transaction type: PA=1, VA=0

#

