OVP Guide to Using Processor Models

Model Specific Information for variant Renesas_r8c

Imperas Software Limited
Imperas Buildings, North Weston
Thame, Oxfordshire, OX9 2HA, UK
docs@imperas.com

Author	Imperas Software Limited
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1.0 Overview

This document provides the details of an OVP Fast Processor Model variant.
OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.
The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance.
Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.
The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners.
There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

M16c Family 16Bit CISC processor model.

1.2 Licensing

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1.3 Limitations

Core Instruction Set Architecture only.
Interrupt and Reset Signals are TBD.

1.4 Verification

Model has been validated correct by running through extensive instruction level tests

2.0 Configuration

2.1 Location

The model source and object file is found in the VLNV tree at:
posedgesoft.ovpworld.org/processor/m16c/1.0

2.2 GDB Path

The default GDB for this model is found at:
$IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/m32c-elf-gdb

2.3 Semi-Host Library

The default semi-host library file is found in the VLNV tree at :
posedgesoft.ovpworld.org/semihosting/m16cNewlib/1.0

2.4 Processor Endian-ness

This is a LITTLE endian model.

2.5 QuantumLeap Support

A simulator using this processor will not be able to use QuantumLeap.

2.6 Processor ELF Code

ELF codes supported by this model are: , 0x75 and 0x78.

3.0 Other Variants in this Model

Table 1.

Variant
m16c
r8c

4.0 Bus Ports

Table 2.

Type	Name	Bits
master (initiator)	INSTRUCTION	32
master (initiator)	DATA	32

5.0 Net Ports

Table 3.

Name	Type
reset	input
nmi	input
int_per	input
int_ack	output

6.0 FIFO Ports

No FIFO Ports in this model.

7.0 Parameters

Table 4.

Name	Type	Description
compatibility	Enumeration	Specify compatibility mode isa=0 gdb=1

verbose	Boolean	Specify verbose output messages

8.0 Execution Modes

No execution modes.

9.0 Exceptions

Table 5.

Name	Code
Undefined	0
Overflow	1
BRK	2
AddressMatch	3
SingleStep	4
Watchdog	5
DBC	6
NMI	7
Reset	8
Fetch	9

10.0 Hierarchy of the model

A CPU core may allow the user to configure it to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.
OVP processor models can be written to include SMP blocks and to have many levels of hierarchy.

Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

10.1 Level 1:

This level in the model hierarchy has 2 commands.

This level in the model hierarchy has no register groups.

This level in the model hierarchy has no children.

11.0 Model Commands

11.1 Level 1:

Table 6.

Name	Arguments
isync	specify instruction address range for synchronous execution
itrace	enable or disable instruction tracing

12.0 Registers

12.1 Level 1:

Table 7.

Name	Bits	Initial value (Hex)		Description
R0	16	0	rw	
R1	16	0	rw	
R2	16	0	rw	
R3	16	0	rw	
A0	16	0	rw	
A1	16	0	rw	
FB	16	0	rw	
R0B	16	0	rw	
R1B	16	0	rw	
R2B	16	0	rw	
R3B	16	0	rw	
A0B	16	0	rw	
A1B	16	0	rw	
FBB	16	0	rw	
SB	16	0	rw	
USP	16	0	rw	
ISP	16	0	rw	
INTB	20	0	rw	
PC	20	0	rw	program counter
FLG	16	0	rw	

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