

# OVP Guide to Using Processor Models Model Specific Information for variant MIPS32\_M5150

# Imperas Software Limited

Împeras Buildings, North Weston Thame, Oxfordshire, OX9 2HA, UK docs@imperas.com



Author	Imperas Software Limited
Version	0.4
Filename	OVP_Model_Specific_Information_mips32_M5150.pdf
Created	25 August 2015

# **Copyright Notice**

Copyright © 2015 Imperas Software Limited. All rights reserved. This software and documentation contain information that is the property of Imperas Software Limited. The software and documentation are furnished under a license agreement and may be used or copied only in accordance with the terms of the license agreement. No part of the software and documentation may be reproduced, transmitted, or translated, in any form or by any means, electronic, mechanical, manual, optical, or otherwise, without prior written permission of Imperas Software Limited, or as expressly provided by the license agreement.

## **Right to Copy Documentation**

The license agreement with Imperas permits licensee to make copies of the documentation for its internal use only. Each copy shall include all copyrights, trademarks, service marks, and proprietary rights notices, if any.

#### **Destination Control Statement**

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the reader's responsibility to determine the applicable regulations and to comply with them.

#### **Disclaimer**

IMPERAS SOFTWARE LIMITED., AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

# Table of Contents

1.0 Overview	4
1.1 Description	4
1.2 Licensing.	4
1.3 Limitations	4
1.4 Verification	4
1.5 Features	4
2.0 Configuration	4
2.1 Location	4
2.2 GDB Path	4
2.3 Semi-Host Library	4
2.4 Processor Endian-ness	4
2.5 QuantumLeap Support	4
2.6 Processor ELF Code	5
3.0 Other Variants in this Model	5
4.0 Bus Ports	5
5.0 Net Ports	5
6.0 FIFO Ports	6
7.0 Parameters	6
8.0 Execution Modes	18
9.0 Exceptions	18
10.0 Hierarchy of the model	20
10.1 Level 1: CPU	20
11.0 Model Commands	21
11.1 Level 1: CPU	21
12.0 Registers	21
12.1 Level 1: CPU	21
12.1.1 Core	21
12.1.2 FPU	22
12.1.3 DSP	23
12.1.4 Shadow	23
12.1.5 COP0	36
12.1.6 SPRAM	39
12.1.7 Integration support	30

#### 1.0 Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms. The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners.

There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

#### 1.1 Description

MIPS32 Configurable Processor Model

If you need other variants, these models can be obtained from www.OVPworld.org/MIPSuser.

#### 1.2 Licensing

Usage of binary model under license governing simulator usage. Source of model available under Imperas Software License Agreement.

#### 1.3 Limitations

If this model is not part of your installation, then it is available for download from www.OVPworld.org/MIPSuser.

#### 1.4 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

#### 1.5 Features

Both MIPS32 and microMIPS32 Instruction sets implemented

MMU Type: Standard TLB

FPU implemented

L1 I and D cache model in either full or tag-only mode implemented (disabled by default)

Vectored interrupts implemented

MCU ASE implemented

DSP ASE Rev 2 implemented

# 2.0 Configuration

#### 2.1 Location

The model source and object file is found in the VLNV tree at: imgtec.ovpworld.org/processor/mips32/1.0

#### 2.2 GDB Path

The default GDB for this model is found at:

\$IMPERAS\_HOME/lib/\$IMPERAS\_ARCH/gdb/mips-sde-elf-gdb

#### 2.3 Semi-Host Library

The default semi-host library file is found in the VLNV tree at : mips.ovpworld.org/semihosting/mips32SDE/1.0

#### 2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

#### 2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

## 2.6 Processor ELF Code

The ELF code supported by this model is: 0x8

# 3.0 Other Variants in this Model

## Table 1.

Variant	
M5100	
.M5100Guest	
M5150	
.M5150Guest	
P5600	
.P5600Guest	

## 4.0 Bus Ports

#### Table 2.

Туре	Name	Bits	Description
master (initiator)	ISPRAM	32	instruction scratchpad RAM
master (initiator)	DSPRAM	32	data scratchpad RAM
master (initiator)	INSTRUCTION	32	
master (initiator)	DATA	32	

## **5.0 Net Ports**

## Table 3.

Name	Туре	Description
reset	input	Core reset
dint	input	Debug external interrupt
hwint0	input	External interrupt
hwint1	input	External interrupt
hwint2	input	External interrupt
hwint3	input	External interrupt
hwint4	input	External interrupt
hwint5	input	External interrupt
hwint6	input	External interrupt
hwint7	input	External interrupt
nmi	input	Non-maskable external interrupt
EICPresent	input	Input signal SI_EICPresent per VPE
EIC_RIPL	input	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS	input	External interrupt controller EICSS
EIC_VectorNum	input	External interrupt controller vector number
EIC_VectorOffset	input	External interrupt controller vector offset

EIC_GID	input	External interrupt controller guest ID
intISS	output	True when interrupt request is serviced
causeTI	output	True when timer interrupt expires
causeIP0	output	Raised for software interrupt request IP0
causeIP1	output	Raised for software interrupt request IP1
Guest.EIC_RIPL	input	Guest External interrupt controller RIPL
Guest.EIC_EICSS	input	Guest External interrupt controller EICSS
Guest.EIC_VectorNum	input	Guest External interrupt controller vector number
Guest.EIC_VectorOffset	input	Guest External interrupt controller vector offset
Guest.EIC_GID	input	Guest External interrupt controller guest ID
Guest.intISS	output	True when Guest interrupt request is serviced
Guest.causeTI	output	True when Guest timer interrupt expires
Guest.causeIP0	output	Raised for Guest software interrupt request IP0
Guest.causeIP1	output	Raised for Guest software interrupt request IP1

# **6.0 FIFO Ports**

No FIFO Ports in this model.

# 7.0 Parameters

Table 4.

Name	Туре	Description
cacheenable	Enumeration	Select cache model mode default=0 tag=1 full=2
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info structure
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
supervisorMode	Boolean	Override whether processor implements supervisor mode
busErrors	Boolean	Override bus error exception behavior. When true, accesses of memory not defined by platform will cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when true (sets Config.MT=3, Config.KU/K23=2 and Config1.MMUSizeM1=0)
removeDSP	Boolean	Override the DSP-present configuration when true (sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true (sets Config3.CMGCR and GCR_BASE to 0)

removeFP	Boolean	Override the FP-Present configuration when true (sets Config1.FP to 0)
removeFTLB	Boolean	Override the FTLBEn configuration when true (disable FTLB)
isISA	Boolean	Enable to specify ISA model (reset address from ELF, all coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to maximum value to improve performance
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores only)
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC implementation (MT cores only)
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior)
supportDenormals	Boolean	Enable to specify that the FPU supports denormal operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0
mpuRegions	Uns32	Number of regions for memory protection unit
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
MIPS_UHI	Boolean	Enable MIPS-Unified Hosting interface
mipsUhiArgs	String	Specifies UHI arguments string seperated by spaces
mipsUhiJail	String	Specifies UHI jailroot
MIPS_DV_MODE	Boolean	Enable Design Verification mode
MIPS_MAGIC_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes
enableTrickbox	Boolean	Enable trickbox addresses (specific for AVP)
fpuexcdisable	Boolean	Disable FPU exceptions
cop2Bits	Uns32	Specifies width in bits of COP2 registers (32 or 64)
cop2FileName	String	Specifies COP2 dynamically-loaded object (.so/.dll) defining COP2 instructions
udiConfig	Int32	Specifies UDI configuration attribute
udiFileName	String	Specifies UDI dynamically-loaded object (.so/.dll) defining UDI instructions
vectoredinterrupt	Boolean	Enables vectored interrupts (sets Config3 VInt)
externalinterrupt	Boolean	Enables the use of an external interrupt controller (sets Config3 VEIC)
rootFixedMMU	Boolean	Override the root MMU type to fixed mapping when true (sets Config.MT=3 and Config.KU/K23=2)

rootMMUSizeM1	Uns32	Override the root MMUSizeM1 field in Config1 register (number of MMU entries-1)
srsctIHSS	Uns32	Override the HSS field in SRSCtl register (number of shadow register sets)
firPS	Uns32	Override the PS field in FIR register
firHas2008	Uns32	Override the Has2008 field in FIR register
pridCompanyOptions	Uns32	Override the Company Options field in PRId register
pridRevision	Uns32	Override the Revision field in PRId register
intctlIPTI	Uns32	Override the IPTI field in IntCtl register
intctllPFDC	Uns32	Override the IPFDC field in IntCtl register
intctllPPCI	Uns32	Override the IPPCI field in IntCtl register
numWatch	Uns32	Specify number of WatchLo/WatchHi register pairs
numVC	Uns32	Specify number of Virtual Cores to be present
numVCtoStart	Uns32	Specify number of Virtual Cores to be running
sharedTLBindex	Uns32	Specify first shared TLB Index between Virtual Cores
hasFDC	Boolean	Specify Fast Debug Channel (dummy implementation)
intctlIPTI_CPU0_VC0	Uns32	Override the IPTI field in IntCtl register for CPU0/VC0
intctlIPTI_CPU0_VC1	Uns32	Override the IPTI field in IntCtl register for CPU0/VC1
intctlIPTI_CPU0_VC2	Uns32	Override the IPTI field in IntCtl register for CPU0/VC2
intctlIPTI_CPU0_VC3	Uns32	Override the IPTI field in IntCtl register for CPU0/VC3
intctlIPTI_CPU1_VC0	Uns32	Override the IPTI field in IntCtl register for CPU1/VC0
intctlIPTI_CPU1_VC1	Uns32	Override the IPTI field in IntCtl register for CPU1/VC1
intctlIPTI_CPU1_VC2	Uns32	Override the IPTI field in IntCtl register for CPU1/VC2
intctlIPTI_CPU1_VC3	Uns32	Override the IPTI field in IntCtl register for CPU1/VC3
intctlIPTI_CPU2_VC0	Uns32	Override the IPTI field in IntCtl register for CPU2/VC0
intctlIPTI_CPU2_VC1	Uns32	Override the IPTI field in IntCtl register for CPU2/VC1
intctlIPTI_CPU2_VC2	Uns32	Override the IPTI field in IntCtl register for CPU2/VC2
intetlIPTI_CPU2_VC3	Uns32	Override the IPTI field in IntCtl register for CPU2/VC3
intetlIPTI_CPU3_VC0	Uns32	Override the IPTI field in IntCtl register for CPU3/VC0

intctllPTI_CPU3_VC1	Uns32	Override the IPTI field in IntCtl register for CPU3/VC1
intctlIPTI_CPU3_VC2	Uns32	Override the IPTI field in IntCtl register for CPU3/VC2
intctllPTI_CPU3_VC3	Uns32	Override the IPTI field in IntCtl register for CPU3/VC3
intctllPFDC_CPU0_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC0
intctllPFDC_CPU0_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC1
intctllPFDC_CPU0_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC2
intctlIPFDC_CPU0_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC3
intctllPFDC_CPU1_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC0
intctllPFDC_CPU1_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC1
intctllPFDC_CPU1_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC2
intctllPFDC_CPU1_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC3
intctllPFDC_CPU2_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC0
intctllPFDC_CPU2_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC1
intctllPFDC_CPU2_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC2
intctllPFDC_CPU2_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC3
intctllPFDC_CPU3_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC0
intctllPFDC_CPU3_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC1
intctlIPFDC_CPU3_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC2
intctllPFDC_CPU3_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC3
intctlIPPCI_CPU0_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC0
intctllPPCI_CPU0_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC1
intctllPPCI_CPU0_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC2
intctlIPPCI_CPU0_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC3
		01 00/ 100

intctllPPCI_CPU1_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC0
intctllPPCI_CPU1_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC1
intctlIPPCI_CPU1_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC2
intctllPPCI_CPU1_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC3
intctlIPPCI_CPU2_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC0
intctllPPCI_CPU2_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC1
intctlIPPCI_CPU2_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC2
intctlIPPCI_CPU2_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC3
intctlIPPCI_CPU3_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC0
intctlIPPCI_CPU3_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC1
intctlIPPCI_CPU3_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC2
intctlIPPCI_CPU3_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC3
configAR	Uns32	Enables R6 support
configBM	Uns32	Override the BM field in Config register (burst mode)
configDSP	Boolean	Override Config.DSP (data scratchpad RAM present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0 cacheability)
configKU	Uns32	Override power on value of Config.KU (set Useg cacheability)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23 cacheability)
configMDU	Boolean	Override Config.MDU (iterative multiply/divide unit)
configMM	Boolean	Override Config.MM (merging mode for write)
configMT	Uns32	Override Config.MT
configSB	Boolean	Override Config.SB (simple bus transfers only)
MIPS16eASE	Boolean	Override Config1.CA (enables the MIPS16e ASE)
config1DA	Uns32	Override Config1.DA (Dcache associativity)

config1DL	Uns32	Override Config1.DL (Dcache line size)
config1DS	Uns32	Override Config1.DS (Dcache sets per way)
config1EP	Boolean	Override Config1.EP (EJTag present)
config1IA	Uns32	Override Config1.IA (Icache associativity)
config1IL	Uns32	Override Config1.IL (Icache line size)
config1IS	Uns32	Override Config1.IS (Icache sets per way)
config1MMUSizeM1	Uns32	Override Config1.MMUSizeM1 (number of
		MMU entries-1)
config1WR	Boolean	Override Config1.WR (watchpoint registers
, oou		present)
config2SU	Uns32	Override the SU field in Config2 register
config2SS	Uns32	Override the SS field in Config2 register
config2SL	Uns32	Override the SL field in Config2 register
config2SA	Uns32	Override the SA field in Config2 register
config3BI	Boolean	Override Config3.Bl
config3BP	Boolean	Override Config3.BP
config3CDMM	Boolean	Override Config3.CDMM
config3CTXTC	Boolean	Override Config3.CTXTC
config3DSPP	Boolean	Override Config3.DSPP
config3DSP2P	Boolean	Override Config3.DSP2P
config3IPLW	Uns32	Override Config3.IPLW
config3ISA	Uns32	Override Config3.ISA
config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3LPA	Boolean	Override Config3.LPA
config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
config3SC	Boolean	Override Config3.SC
config3ULRI	Boolean	Override Config3.ULRI
config3VZ	Boolean	Override Config3.VZ
config3MSAP	Boolean	Override Config3.MSAP
config3CMGCR	Boolean	Override the CMGCR field in Config3 register
config3SP	Boolean	Override the SP field in Config3 register
config3TL	Uns32	Override the TL field in Config3 register
config3PW	Boolean	Override the PW field in Config3 register
config4AE	Boolean	Override Config4.AE
config4IE	Uns32	Override Config4.IE
config4MMUConfig	Uns32	Override Config4.MMUConfig field
		(interpretation depends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.VTLBSizeExt
config5EVA	Boolean	Override Config5.EVA

config5LLB	Boolean	Override Config5.LLB (LLAddr supports LLbit)
config5MRP	Boolean	Override Config5.MRP (MaaR Present)
config5NFExists	Boolean	Override Config5.NFExists
config5MSAEn	Boolean	Override Config5.MSAEn
config5MVH	Boolean	Override Config5.MVH (enable MTHC0 and MFHC0 instructions)
config6FTLBEn	Boolean	Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE
config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initialization)
config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
config7ES	Uns32	Override the ES field in Config7 register (Externalize sync)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant with IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/ SNaN encodings match IEEE 754-2008 recommendation)
numMaarRegs	Uns32	Override number of MAAR registers (must be even)
wiredLimit	Uns32	Override Limit field of the Wired register
cdmmBaseCI	Boolean	Override CDMMBase.CI
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the corresponding BEV address bits
firstBEVExceptionBaseMaskBit	Uns32	Specify LSB position of GCR_Cx_RESET_EXT_BASE.BEVExceptionBaseM field. Only used when SegCtl present
EVAReset	Boolean	Set to one to reset into non-legacy address map and BEV location. Only used when non-CMP and SegCtl present
ExceptionBaseMask	Uns32	Specify the ExceptionBaseMask value used for bits [27:firstBEVExceptionBaseMaskBit]. Only used when non-CMP and SegCtl present
ExceptionBasePA	Uns32	Bits [35:29] of the physical address for the BEV overlays. Only used when non-CMP and SegCtl present
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present

TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable within cluster
GCR_PCORES	Uns32	CMP system only: override GCR_CONFIG.PCORES (number of cores-1)
GCR_BASE	Uns32	CMP system only: override GCR_BASE.GCR_BASE (default GCR register address)
GCR_MINOR_REV	Uns32	CMP system only: override GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MAJOR_REV
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MAJOR_REV
GIC_NUMINTERRUPTS	Uns32	CMP system only: override GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MAJOR_REV
GIC_NUM_TEAMS	Uns32	CMP system only: override GIC_SH_DBG_CONFIG.NUM_TEAMS
GIC_TRIG_RESET	Uns32	CMP system only: Zero value of GIC_SH_TRIG_[31_0, 63_32]
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPE
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override CPC_REVISION.MAJOR_REV
GIC_SH_GID_CONFIG31_0	Uns32	CMP system only: override GIC_SH_GID_CONFIG[31_0]

GIC_SH_GID_CONFIG63_32	Uns32	CMP system only: override GIC_SH_GID_CONFIG[63_32]
GIC_SH_GID_CONFIG95_64	Uns32	CMP system only: override GIC_SH_GID_CONFIG[95_64]
GIC_SH_GID_CONFIG127_96	Uns32	CMP system only: override GIC_SH_GID_CONFIG[127_96]
GIC_SH_GID_CONFIG159_128	Uns32	CMP system only: override GIC_SH_GID_CONFIG[159_128]
GIC_SH_GID_CONFIG191_160	Uns32	CMP system only: override GIC_SH_GID_CONFIG[191_160]
GIC_SH_GID_CONFIG223_192	Uns32	CMP system only: override GIC_SH_GID_CONFIG[223_192]
GIC_SH_GID_CONFIG255_224	Uns32	CMP system only: override GIC_SH_GID_CONFIG[255_224]
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 0
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 1
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 2
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 3
GCR_C0_V0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core0/vc0
GCR_C0_V1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core0/vc1
GCR_C0_V2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core0/vc2
GCR_C0_V3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core0/vc3
GCR_C1_V0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core1/vc0
GCR_C1_V1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core1/vc1
GCR_C1_V2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core1/vc2
GCR_C1_V3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core1/vc3

GCR_C2_V0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core2/vc0
GCR_C2_V1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core2/vc1
GCR_C2_V2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core2/vc2
GCR_C2_V3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core2/vc3
GCR_C3_V0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core3/vc0
GCR_C3_V1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core3/vc1
GCR_C3_V2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core3/vc2
GCR_C3_V3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core3/vc3
CPC_C0_VC_EN	Uns32	CMP system only: CPC_VC_EN for core 0
CPC_C1_VC_EN	Uns32	CMP system only: CPC_VC_EN for core 1
CPC_C2_VC_EN	Uns32	CMP system only: CPC_VC_EN for core 2
CPC_C3_VC_EN	Uns32	CMP system only: CPC_VC_EN for core 3
EIC_OPTION	Uns32	Override the external interrupt controller EIC_OPTION
guestVariant	Enumeration	Guest processor variant (same as Root if not specified) M5100=0 .M5100Guest=1 M5150=2 .M5150Guest=3 P5600=4 .P5600Guest=5
guestCtl0RI	Uns32	Override the RI field in GuestCtI0 register
guestCtl0MC	Uns32	Override the MC field in GuestCtl0 register
guestCtl0CP0	Uns32	Override the CP0 field in GuestCtl0 register
guestCtl0AT	Uns32	Override the AT field in GuestCtl0 register
guestCtl0GT	Uns32	Override the GT field in GuestCtl0 register
guestCtl0CG	Uns32	Override the CG field in GuestCtl0 register
guestCtl0CF	Uns32	Override the CF field in GuestCtl0 register
guestCtl0G1	Uns32	Override the G1 field in GuestCtl0 register
guestCtl0RAD	Uns32	Override the RAD field in GuestCtl0 register
guestCtl0DRG	Uns32	Override the DRG field in GuestCtl0 register
hasImpl17	Boolean	Enable read/write of Impl17 bit in Status register
hasImpl16	Boolean	Enable read/write of Impl16 bit in Status register
guestintctlIPTI	Uns32	Override the Guest IPTI field in IntCtl register
guestintctllPFDC	Uns32	Override the Guest IPFDC field in IntCtl register
guestintctllPPCI	Uns32	Override the Guest IPPCI field in IntCtl register

guestintctllPTI_CPU0_VC0	Uns32	Override the IPTI field in IntCtl register for CPU0/VC0
guestintctllPTI_CPU0_VC1	Uns32	Override the IPTI field in IntCtl register for CPU0/VC1
guestintctllPTI_CPU0_VC2	Uns32	Override the IPTI field in IntCtl register for CPU0/VC2
guestintctIIPTI_CPU0_VC3	Uns32	Override the IPTI field in IntCtl register for CPU0/VC3
guestintctlIPTI_CPU1_VC0	Uns32	Override the IPTI field in IntCtl register for CPU1/VC0
guestintctlIPTI_CPU1_VC1	Uns32	Override the IPTI field in IntCtl register for CPU1/VC1
guestintctlIPTI_CPU1_VC2	Uns32	Override the IPTI field in IntCtl register for CPU1/VC2
guestintctllPTI_CPU1_VC3	Uns32	Override the IPTI field in IntCtl register for CPU1/VC3
guestintctllPTI_CPU2_VC0	Uns32	Override the IPTI field in IntCtl register for CPU2/VC0
guestintctllPTI_CPU2_VC1	Uns32	Override the IPTI field in IntCtl register for CPU2/VC1
guestintctllPTI_CPU2_VC2	Uns32	Override the IPTI field in IntCtl register for CPU2/VC2
guestintctllPTI_CPU2_VC3	Uns32	Override the IPTI field in IntCtl register for CPU2/VC3
guestintctllPTI_CPU3_VC0	Uns32	Override the IPTI field in IntCtl register for CPU3/VC0
guestintctllPTI_CPU3_VC1	Uns32	Override the IPTI field in IntCtl register for CPU3/VC1
guestintctllPTI_CPU3_VC2	Uns32	Override the IPTI field in IntCtl register for CPU3/VC2
guestintctllPTI_CPU3_VC3	Uns32	Override the IPTI field in IntCtl register for CPU3/VC3
guestintctllPFDC_CPU0_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC0
guestintctllPFDC_CPU0_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC1
guestintctllPFDC_CPU0_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC2
guestintctllPFDC_CPU0_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC3
guestintctllPFDC_CPU1_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC0
guestintctllPFDC_CPU1_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC1
guestintctllPFDC_CPU1_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC2
-		

guestintctllPFDC_CPU1_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC3
guestintctllPFDC_CPU2_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC0
guestintctllPFDC_CPU2_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC1
guestintctllPFDC_CPU2_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC2
guestintctllPFDC_CPU2_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC3
guestintctllPFDC_CPU3_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC0
guestintctllPFDC_CPU3_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC1
guestintctllPFDC_CPU3_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC2
guestintctllPFDC_CPU3_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC3
guestintctllPPCI_CPU0_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC0
guestintctllPPCI_CPU0_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC1
guestintctllPPCI_CPU0_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC2
guestintctllPPCI_CPU0_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC3
guestintctllPPCI_CPU1_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC0
guestintctllPPCI_CPU1_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC1
guestintctllPPCI_CPU1_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC2
guestintctllPPCI_CPU1_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC3
guestintctlIPPCI_CPU2_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC0
guestintctllPPCI_CPU2_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC1
guestintctllPPCI_CPU2_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC2
guestintctllPPCI_CPU2_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC3
guestintctllPPCI_CPU3_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC0
guestintctlIPPCI_CPU3_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC1

guestintctlIPPCI_CPU3_VC2	Override the IPPCI field in IntCtl register for CPU3/VC2
guestintctlIPPCI_CPU3_VC3	Override the IPPCI field in IntCtl register for CPU3/VC3

# **8.0 Execution Modes**

Table 5.

Name	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3
GUEST_KERNEL	4
GUEST_SUPERVISOR	5
GUEST_USER	6

# 9.0 Exceptions

Table 6.

Name	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Вр	9
RI	10
СрU	11
Ov	12
Tr	13
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MDMX	22

WATCH	23
MCheck	24
Thread	25
DSPDis	26
GE	27
Prot	29
CacheErr	30

# 10.0 Hierarchy of the model

A CPU core may allow the user to configure it to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.

OVP processor models can be written to include SMP blocks and to have many levels of hierarchy.

Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

#### 10.1 Level 1: CPU

This level in the model hierarchy has 20 commands.

This level in the model hierarchy has 7 register groups:

Table 7.

Group name	Registers
Core	33
FPU	34
DSP	9
Shadow	512
COP0	124
SPRAM	15
Integration_support	1

This level in the model hierarchy has no children.

# 11.0 Model Commands

## 11.1 Level 1: CPU

## Table 8.

Name	Arguments
isync	specify instruction address range for synchronous execution
itrace	enable or disable instruction tracing
mipsCOP0	<register> <select></select></register>
mipsCacheDisable	
mipsCacheEnable	-tag -full
mipsCacheRatio	-icache -dcache
mipsCacheReport	
mipsCacheReset	
mipsCacheTrace	-on -off [-nocached -nouncached] [-noicache -nodcache] [-noartifact -notrue]
mipsDebugFlags	<value></value>
mipsReadRegister	<resource> <offset></offset></resource>
mipsReadTLBEntry	<index></index>
mipsTLBDump	
mipsTLBDumpGuest	
mipsTLBDumpRoot	
mipsTLBGetPhys	<virtual address=""> <asid></asid></virtual>
mipsTraceGuest	<bool></bool>
mipsTraceRoot	<bool></bool>
mipsWriteRegister	<resource> <offset> <value></value></offset></resource>
mipsWriteTLBEntry	<index> <lo0> <lo1> <hi0> <mask></mask></hi0></lo1></lo0></index>

# 12.0 Registers

12.1 Level 1: CPU

12.1.1 Core

## Table 9.

Name	Bits	Initial value (Hex)		Description
zero	32	0	r-	constant zero
at	32	0	rw	
v0	32	0	rw	
v1	32	0	rw	
a0	32	0	rw	
a1	32	0	rw	
a2	32	0	rw	
a3	32	0	rw	
tO	32	0	rw	
t1	32	0	rw	

40	22	10	I	
t2	32	0	rw	
t3	32	0	rw	
t4	32	0	rw	
t5	32	0	rw	
t6	32	0	rw	
t7	32	0	rw	
s0	32	0	rw	
s1	32	0	rw	
s2	32	0	rw	
s3	32	0	rw	
s4	32	0	rw	
s5	32	0	rw	
s6	32	0	rw	
s7	32	0	rw	
t8	32	0	rw	
t9	32	0	rw	
k0	32	0	rw	
k1	32	0	rw	
gp	32	0	rw	
sp	32	0	rw	stack pointer
s8	32	0	rw	frame pointer
ra	32	0	rw	
рс	32	bfc00000	rw	program counter

## 12.1.2 FPU

Table 10.

Name	Bits	Initial value (Hex)		Description
f0	32	0	rw	
f1	32	0	rw	
f2	32	0	rw	
f3	32	0	rw	
f4	32	0	rw	
f5	32	0	rw	
f6	32	0	rw	
f7	32	0	rw	
f8	32	0	rw	
f9	32	0	rw	
f10	32	0	rw	
f11	32	0	rw	
f12	32	0	rw	
f13	32	0	rw	

f14	32	0	rw	
f15	32	0	rw	
f16	32	0	rw	
f17	32	0	rw	
f18	32	0	rw	
f19	32	0	rw	
f20	32	0	rw	
f21	32	0	rw	
f22	32	0	rw	
f23	32	0	rw	
f24	32	0	rw	
f25	32	0	rw	
f26	32	0	rw	
f27	32	0	rw	
f28	32	0	rw	
f29	32	0	rw	
f30	32	0	rw	
f31	32	0	rw	
fsr	32	10c0000	rw	floating point status
fir	32	11f3a720	r-	floating point information

## 12.1.3 DSP

Table 11.

Name		Initial		Description
		value (Hex)		
lo	32	0	rw	
hi	32	0	rw	
lo1	32	0	rw	
hi1	32	0	rw	
lo2	32	0	rw	
hi2	32	0	rw	
lo3	32	0	rw	
hi3	32	0	rw	
dspctl	32	0	rw	DSP control

## 12.1.4 Shadow

Table 12.

Name		Initial value (Hex)		Description
zero[0]	32	0	r-	constant zero
at[0]	32	0	rw	
v0[0]	32	0	rw	

v1[0]	32	0	rw	
a0[0]	32	0	rw	
a1[0]	32	0	rw	
a2[0]	32	0	rw	
a3[0]	32	0	rw	
t0[0]	32	0	rw	
t1[0]	32	0	rw	
t2[0]	32	0	rw	
t3[0]	32	0	rw	
t4[0]	32	0	rw	
	32	0	_	
t5[0]	32	0	rw	
t6[0]	32	0	rw	
t7[0]	32		rw	
s0[0]		0	rw	
s1[0]	32	0	rw	
s2[0]	32	0	rw	
s3[0]	32	0	rw	
s4[0]	32	0	rw	
s5[0]	32	0	rw	
s6[0]	32	0	rw	
s7[0]	32	0	rw	
t8[0]	32	0	rw	
t9[0]	32	0	rw	
k0[0]	32	0	rw	
k1[0]	32	0	rw	
gp[0]	32	0	rw	
sp[0]	32	0		stack pointer
s8[0]	32	0	rw	frame pointer
ra[0]	32	0	rw	
zero[1]	32	0	r-	constant zero
at[1]	32	0	rw	
v0[1]	32	0	rw	
v1[1]	32	0	rw	
a0[1]	32	0	rw	
a1[1]	32	0	rw	
a2[1]	32	0	rw	
a3[1]	32	0	rw	
t0[1]	32	0	rw	
t1[1]	32	0	rw	
t2[1]	32	0	rw	
t3[1]	32	0	rw	
t4[1]	32	0	rw	

Total   Tota	(FI41	loo	Io.	1	
17[1]   32	t5[1]	32	0	rw	
s0[1]         32         0         rw           s1[1]         32         0         rw           s2[1]         32         0         rw           s4[1]         32         0         rw           s4[1]         32         0         rw           s5[1]         32         0         rw           s6[1]         32         0         rw           s7[1]         32         0         rw           s9[1]         32         0         rw           s6[1]         32         0         rw           s9[1]         32         0         rw           s6[1]         32         0         rw           s6[1]         32         0         rw           s6[1]         32         0         rw           s6[1]         32         0         rw           sp[1]         32         0         rw           s8[1]         32         0         rw           sero[2]         32         0         rw           v0[2]         32         0         rw           v1[2]         32         0         rw           s				rw	
s1[1]         32         0         rw           s2[1]         32         0         rw           s2[1]         32         0         rw           s4[1]         32         0         rw           s5[1]         32         0         rw           s6[1]         32         0         rw           sp[1]         32         0         rw           s6[1]         32         0         rw           s6[1]         32         0         rw           sero[2]         32         0         rr           constant zero         al[2]         32         0         rw           v1[2]         32         0         rw           al[2]         32         0         rw				rw	
s2[1]         32         0         rw           s3[1]         32         0         rw           s4[1]         32         0         rw           s6[1]         32         0         rw           sp[1]         32         0         rw           sp[1]         32         0         rw           sep[1]         32         0         rw           sep[1]         32         0         rw           sep[2]         32         0         rw           sep[2]         32         0         rw           sep[2]         32         0         rw           sep[2]         32         0         rw           <				rw	
s3[1]         32         0         rw           s4[1]         32         0         rw           s5[1]         32         0         rw           s6[1]         32         0         rw           s7[1]         32         0         rw           t8[1]         32         0         rw           k0[1]         32         0         rw           k0[1]         32         0         rw           k1[1]         32         0         rw           sp[1]         32         0         rw           sp[2]         32         0         rw           sp[1]         32         0         rw           sp[2]         32         0         rw           sp[				rw	
s4[1]         32         0         nw           s6[1]         32         0         nw           s6[1]         32         0         nw           s6[1]         32         0         nw           s6[1]         32         0         nw           s8[1]         32         0         nw           k0[1]         32         0         nw           k1[1]         32         0         nw           sp[1]         32         0         nw           sp[2]         32         0         nw           sp[2]         32         0         nw           sp[			!	rw	
SS[1]         32         0         rw           s6[1]         32         0         rw           s7[1]         32         0         rw           l8[1]         32         0         rw           l9[1]         32         0         rw           k0[1]         32         0         rw           k1[1]         32         0         rw           sp[1]         32         0         rw           sp[2]         32         0         rw           sp[2]         32         0         rw           sp[2]         32         0         rw           sp[		32	0	rw	
s6[1]         32         0         rw           s7[1]         32         0         rw           t8[1]         32         0         rw           t9[1]         32         0         rw           k1[1]         32         0         rw           k1[1]         32         0         rw           sp[1]         32         0         rw           sp[2]         32         0         rw           sp[				rw	
87[1]         32         0         rw           18[1]         32         0         rw           19[1]         32         0         rw           K0[1]         32         0         rw           K1[1]         32         0         rw           sp[1]         32         0         rw           ra[1]         32         0         rw           ra[1]         32         0         rw           ra[2]         32         0         rw           v0[2]         32         0         rw           v1[2]         32         0         rw           a1[2]         32         0         rw           a2[2]         32         0         rw           a3[2]         32         0         rw           t1[2]         32         0         rw           t2[2]         32         0         rw           t2[		32	0	rw	
18[1]         32         0         rw           19[1]         32         0         rw           K0[1]         32         0         rw           K1[1]         32         0         rw           sp[1]         32         0         rw           sp[2]         32         0         rw           sp[				rw	
t9[1]         32         0         rw           k0[1]         32         0         rw           k1[1]         32         0         rw           sp[1]         32         0         rw           ra[1]         32         0         rw           at[2]         32         0         rw           v0[2]         32         0         rw           v1[2]         32         0         rw           a1[2]         32         0         rw           a2[2]         32         0         rw           a3[2]         32         0         rw           t1[2]         32         0         rw           t2[2]         32         0         rw           t4[2]         32         0         rw           t5[	s7[1]	32	0	rw	
k0[1]         32         0         rw           k1[1]         32         0         rw           gp[1]         32         0         rw           sp[1]         32         0         rw           sp[1]         32         0         rw           sp[1]         32         0         rw           ra[1]         32         0         rw           zero[2]         32         0         rw           v0[2]         32         0         rw           v0[2]         32         0         rw           v1[2]         32         0         rw           a0[2]         32         0         rw           a1[2]         32         0         rw           a2[2]         32         0         rw           a3[2]         32         0         rw           t1[2]         32         0         rw           t	t8[1]	32	0	rw	
k1[1]         32         0         rw           gp[1]         32         0         rw           sp[1]         32         0         rw           sp[1]         32         0         rw           s8[1]         32         0         rw           ra[1]         32         0         rw           zero[2]         32         0         rw           v0[2]         32         0         rw           v1[2]         32         0         rw           v1[2]         32         0         rw           a0[2]         32         0         rw           a1[2]         32         0         rw           a2[2]         32         0         rw           a3[2]         32         0         rw           a3[2]         32         0         rw           t1[2]         32         0         rw           t1[2]         32         0         rw           t2[2]         32         0         rw           t4[2]         32         0         rw           t6[2]         32         0         rw           s	t9[1]	32	0	rw	
gp[1]         32         0         rw         stack pointer           s8[1]         32         0         rw         stack pointer           ra[1]         32         0         rw         rmme pointer           ra[1]         32         0         rw         constant zero           at[2]         32         0	k0[1]	32	0	rw	
sp[1]         32         0         rw         stack pointer           s8[1]         32         0         rw         frame pointer           ra[1]         32         0         rw         rw           zero[2]         32         0         rw         constant zero           at[2]         32         0         rw         constant zero           v0[2]         32         0         rw         constant zero           v1[2]         32         0         rw         constant zero           v1[2]         32         0         rw         constant zero           a1[2]         32         0	k1[1]	32	0	rw	
s8[1]       32       0       rw       frame pointer         ra[1]       32       0       rw       reconstant zero         at[2]       32       0       rw       rw         v0[2]       32       0       rw       rw         a0[2]       32       0       rw       rw         a1[2]       32       0       rw       rw         a2[2]       32       0       rw       rw         a3[2]       32       0       rw       rw         t0[2]       32       0       rw       rw         t1[2]       32       0       rw       rw         t2[2]       32       0       rw       rw         t4[2]       32       0       rw       rw         t5[2]       32       0       rw       rw         t6[2]       32       0       rw       rw         s0[2]       32       0       rw       rw         s1[2]       32       0       rw       rw         s1[2]       32       0       rw       rw         s2[2]       32       0       rw       rw	gp[1]	32	0	rw	
ra[1] 32 0 rw   zero[2] 32 0 rv   constant zero   at[2] 32 0 rw   v0[2] 32 0 rw   v0[2] 32 0 rw   a0[2] 32 0 rw   a0[2] 32 0 rw   a1[2] 32 0 r	sp[1]	32	0	rw	stack pointer
zero[2]         32         0         r-         constant zero           at[2]         32         0         rw         rw           v0[2]         32         0         rw         rw           a1[2]         32         0         rw         and           a1[2]         32         0         rw         and           a2[2]         32         0         rw         and           a3[2]         32         0         rw         and           a4[2]         32         0         rw         and           a4[2]         32         0         rw         and           a5[2]         32         0         rw         and           a5[2]         32         0         rw         and           a5[2]         32         0 <td< td=""><td>s8[1]</td><td>32</td><td>0</td><td>rw</td><td>frame pointer</td></td<>	s8[1]	32	0	rw	frame pointer
at[2] 32 0 rw	ra[1]	32	0	rw	
V0[2]         32         0         rw           V1[2]         32         0         rw           a0[2]         32         0         rw           a1[2]         32         0         rw           a2[2]         32         0         rw           a3[2]         32         0         rw           t0[2]         32         0         rw           t1[2]         32         0         rw           t3[2]         32         0         rw           t4[2]         32         0         rw           t5[2]         32         0         rw           t6[2]         32         0         rw           t7[2]         32         0         rw           s0[2]         32         0         rw           s1[2]         32         0         rw           s2[2]         32         0         rw           s3[2]         32         0         rw           s4[2]         32         0         rw           s5[2]         32         0         rw	zero[2]	32	0	r-	constant zero
v1[2]         32         0         rw           a0[2]         32         0         rw           a1[2]         32         0         rw           a2[2]         32         0         rw           a3[2]         32         0         rw           t0[2]         32         0         rw           t1[2]         32         0         rw           t3[2]         32         0         rw           t4[2]         32         0         rw           t5[2]         32         0         rw           t6[2]         32         0         rw           s0[2]         32         0         rw           s1[2]         32         0         rw           s2[2]         32         0         rw           s3[2]         32         0         rw           s4[2]         32         0         rw           s5[2]         32         0         rw	at[2]	32	0	rw	
a0[2]       32       0       rw         a1[2]       32       0       rw         a2[2]       32       0       rw         a3[2]       32       0       rw         t0[2]       32       0       rw         t1[2]       32       0       rw         t2[2]       32       0       rw         t3[2]       32       0       rw         t5[2]       32       0       rw         t6[2]       32       0       rw         s0[2]       32       0       rw         s1[2]       32       0       rw         s1[2]       32       0       rw         s2[2]       32       0       rw         s4[2]       32       0       rw         s5[2]       32       0       rw	v0[2]	32	0	rw	
a1[2]       32       0       rw         a2[2]       32       0       rw         a3[2]       32       0       rw         t0[2]       32       0       rw         t1[2]       32       0       rw         t2[2]       32       0       rw         t3[2]       32       0       rw         t4[2]       32       0       rw         t5[2]       32       0       rw         t6[2]       32       0       rw         s0[2]       32       0       rw         s1[2]       32       0       rw         s2[2]       32       0       rw         s4[2]       32       0       rw         s4[2]       32       0       rw         s5[2]       32       0       rw	v1[2]	32	0	rw	
a2[2]       32       0       rw         a3[2]       32       0       rw         t0[2]       32       0       rw         t1[2]       32       0       rw         t2[2]       32       0       rw         t3[2]       32       0       rw         t4[2]       32       0       rw         t6[2]       32       0       rw         t7[2]       32       0       rw         s1[2]       32       0       rw         s1[2]       32       0       rw         s2[2]       32       0       rw         s4[2]       32       0       rw         s4[2]       32       0       rw         s5[2]       32       0       rw	a0[2]	32	0	rw	
a3[2]       32       0       rw         t0[2]       32       0       rw         t1[2]       32       0       rw         t2[2]       32       0       rw         t3[2]       32       0       rw         t4[2]       32       0       rw         t5[2]       32       0       rw         t6[2]       32       0       rw         s0[2]       32       0       rw         s1[2]       32       0       rw         s2[2]       32       0       rw         s3[2]       32       0       rw         s4[2]       32       0       rw         s5[2]       32       0       rw	a1[2]	32	0	rw	
t0[2] 32 0 rw	a2[2]	32	0	rw	
t0[2] 32 0 rw t1[2] 32 0 rw t2[2] 32 0 rw t3[2] 32 0 rw t4[2] 32 0 rw t5[2] 32 0 rw t5[2] 32 0 rw t5[2] 32 0 rw t6[2] 32 0 rw t7[2] 32 0 rw t7	a3[2]	32	0	rw	
t1[2]       32       0       rw         t2[2]       32       0       rw         t3[2]       32       0       rw         t4[2]       32       0       rw         t5[2]       32       0       rw         t6[2]       32       0       rw         s0[2]       32       0       rw         s1[2]       32       0       rw         s2[2]       32       0       rw         s4[2]       32       0       rw         s5[2]       32       0       rw	t0[2]	32	0	rw	
t2[2] 32 0 rw t3[2] 32 0 rw t4[2] 32 0 rw t5[2] 32 0 rw t6[2] 32 0 rw t6[2] 32 0 rw t7[2] 32 0 rw t7	t1[2]	32	0	rw	
t3[2]       32       0       rw         t4[2]       32       0       rw         t5[2]       32       0       rw         t6[2]       32       0       rw         t7[2]       32       0       rw         s0[2]       32       0       rw         s1[2]       32       0       rw         s2[2]       32       0       rw         s4[2]       32       0       rw         s5[2]       32       0       rw		32	0	rw	
t4[2]       32       0       rw         t5[2]       32       0       rw         t6[2]       32       0       rw         t7[2]       32       0       rw         s0[2]       32       0       rw         s1[2]       32       0       rw         s2[2]       32       0       rw         s4[2]       32       0       rw         s5[2]       32       0       rw	t3[2]	32	0	rw	
t5[2]       32       0       rw         t6[2]       32       0       rw         t7[2]       32       0       rw         s0[2]       32       0       rw         s1[2]       32       0       rw         s2[2]       32       0       rw         s3[2]       32       0       rw         s4[2]       32       0       rw         s5[2]       32       0       rw		32	0	rw	
t6[2]       32       0       rw         t7[2]       32       0       rw         s0[2]       32       0       rw         s1[2]       32       0       rw         s2[2]       32       0       rw         s3[2]       32       0       rw         s4[2]       32       0       rw         s5[2]       32       0       rw	t5[2]	32	0	rw	
t7[2]       32       0       rw         s0[2]       32       0       rw         s1[2]       32       0       rw         s2[2]       32       0       rw         s3[2]       32       0       rw         s4[2]       32       0       rw         s5[2]       32       0       rw	t6[2]	32	0	rw	
\$0[2]       32       0       rw         \$1[2]       32       0       rw         \$2[2]       32       0       rw         \$3[2]       32       0       rw         \$4[2]       32       0       rw         \$5[2]       32       0       rw	t7[2]	32	0	rw	
\$1[2]       32       0       rw         \$2[2]       32       0       rw         \$3[2]       32       0       rw         \$4[2]       32       0       rw         \$5[2]       32       0       rw		32	0	rw	
\$2[2]     32     0     rw       \$3[2]     32     0     rw       \$4[2]     32     0     rw       \$5[2]     32     0     rw		32	0	rw	
s3[2]     32     0     rw       s4[2]     32     0     rw       s5[2]     32     0     rw		32	0	rw	
\$4[2]     32     0     rw       \$5[2]     32     0     rw		32	0	rw	
s5[2] 32 0 rw		32	0	rw	
		32	0	rw	
in the second of	s6[2]	32	0	rw	

s7[2]	32	0	rw	
t8[2]	32	0	rw	
t9[2]	32	0	rw	
k0[2]	32	0	rw	
k1[2]	32	0	rw	
gp[2]	32	0	rw	
sp[2]	32	0	rw	stack pointer
s8[2]	32	0	rw	frame pointer
ra[2]	32	0	rw	
zero[3]	32	0	r-	constant zero
at[3]	32	0	rw	
v0[3]	32	0	rw	
v1[3]	32	0	rw	
a0[3]	32	0	rw	
a1[3]	32	0	rw	
a2[3]	32	0	rw	
a3[3]	32	0	rw	
t0[3]	32	0	rw	
t1[3]	32	0	rw	
t2[3]	32	0	rw	
t3[3]	32	0	rw	
t4[3]	32	0	rw	
t5[3]	32	0	rw	
t6[3]	32	0	rw	
t7[3]	32	0	rw	
s0[3]	32	0	rw	
s1[3]	32	0	rw	
s2[3]	32	0	rw	
s3[3]	32	0	rw	
s4[3]	32	0	rw	
s5[3]	32	0	rw	
s6[3]	32	0	rw	
s7[3]	32	0	rw	
t8[3]	32	0	rw	
t9[3]	32	0	rw	
k0[3]	32	0	rw	
k1[3]	32	0	rw	
gp[3]	32	0	rw	
sp[3]	32	0	rw	stack pointer
s8[3]	32	0	rw	frame pointer
ra[3]	32	0	rw	
zero[4]	32	0	r-	constant zero

at[4]	32	О	rw	
v0[4]	32	0	├	
	32	0	rw	
v1[4]	32	0	rw	
a0[4]	32		rw	
a1[4]		0	rw	
a2[4]	32	0	rw	
a3[4]	32	0	rw	
t0[4]	32	0	rw	
t1[4]	32	0	rw	
t2[4]	32	0	rw	
t3[4]	32	0	rw	
t4[4]	32	0	rw	
t5[4]	32	0	rw	
t6[4]	32	0	rw	
t7[4]	32	0	rw	
s0[4]	32	0	rw	
s1[4]	32	0	rw	
s2[4]	32	0	rw	
s3[4]	32	0	rw	
s4[4]	32	0	rw	
s5[4]	32	0	rw	
s6[4]	32	0	rw	
s7[4]	32	0	rw	
t8[4]	32	0	rw	
t9[4]	32	0	rw	
k0[4]	32	0	rw	
k1[4]	32	0	rw	
gp[4]	32	0	rw	
sp[4]	32	0	rw	stack pointer
s8[4]	32	0	rw	frame pointer
ra[4]	32	0	rw	
zero[5]	32	0	r-	constant zero
at[5]	32	0	rw	
v0[5]	32	0	rw	
v1[5]	32	0	rw	
a0[5]	32	0	rw	
a1[5]	32	0	rw	
a2[5]	32	0	rw	
a3[5]	32	0	rw	
t0[5]	32	0	rw	
t1[5]	32	0	rw	
t2[5]	32	0	rw	

t3[5]	32	0	lrw	
t4[5]	32	0		
	32	0	rw	
t5[5]	32	0	rw	
t6[5]			rw	
t7[5]	32	0	rw	
s0[5]	32	0	rw	
s1[5]	32	0	rw	
s2[5]	32	0	rw	
s3[5]	32	0	rw	
s4[5]	32	0	rw	
s5[5]	32	0	rw	
s6[5]	32	0	rw	
s7[5]	32	0	rw	
t8[5]	32	0	rw	
t9[5]	32	0	rw	
k0[5]	32	0	rw	
k1[5]	32	0	rw	
gp[5]	32	0	rw	
sp[5]	32	0	rw	stack pointer
s8[5]	32	0	rw	frame pointer
ra[5]	32	0	rw	
zero[6]	32	0	r-	constant zero
at[6]	32	0	rw	
v0[6]	32	0	rw	
v1[6]	32	0	rw	
a0[6]	32	0	rw	
a1[6]	32	0	rw	
a2[6]	32	0	rw	
a3[6]	32	0	rw	
t0[6]	32	0	rw	
t1[6]	32	0	rw	
t2[6]	32	0	rw	
t3[6]	32	0	rw	
t4[6]	32	0	rw	
t5[6]	32	0	rw	
t6[6]	32	0	rw	
t7[6]	32	0	rw	
s0[6]	32	0	rw	
s1[6]	32	0	rw	
s2[6]	32	0	rw	
s3[6]	32	0	rw	
s4[6]	32	0	rw	
s4[b]	32	Įυ	rw	

s5[6]	32	0	lrw	
s6[6]	32	0	rw	
s7[6]	32	0	rw	
t8[6]	32	0	rw	
t9[6]	32	0	rw	
k0[6]	32	0	rw	
k1[6]	32	0	rw	
gp[6]	32	0	rw	
sp[6]	32	0	rw	stack pointer
s8[6]	32	0	rw	frame pointer
ra[6]	32	0	rw	name penner
zero[7]	32	0	r-	constant zero
at[7]	32	0	rw	
v0[7]	32	0	rw	
v1[7]	32	0	rw	
a0[7]	32	0	rw	
a1[7]	32	0	rw	
a2[7]	32	0	rw	
a3[7]	32	0	rw	
t0[7]	32	0	rw	
t1[7]	32	0	rw	
t2[7]	32	0	rw	
t3[7]	32	0	rw	
t4[7]	32	0	rw	
t5[7]	32	0	rw	
t6[7]	32	0	rw	
t7[7]	32	0	rw	
s0[7]	32	0	rw	
s1[7]	32	0	rw	
s2[7]	32	0	rw	
s3[7]	32	0	rw	
s4[7]	32	0	rw	
s5[7]	32	0	rw	
s6[7]	32	0	rw	
s7[7]	32	0	rw	
t8[7]	32	0	rw	
t9[7]	32	0	rw	
k0[7]	32	0	rw	
k1[7]	32	0	rw	
gp[7]	32	0	rw	
sp[7]	32	0	rw	stack pointer
s8[7]	32	0	rw	frame pointer

ra[7]	32	0	lrw					
zero[8]	32	0	r-	constant zero				
at[8]	32	0	rw					
v0[8]	32	0	rw					
v1[8]	32	0	rw					
a0[8]	32	0	rw					
a1[8]	32	0	rw					
a2[8]	32	0	rw					
a3[8]	32	0	rw					
t0[8]	32	0	rw					
t1[8]	32	0	rw					
t2[8]	32	0	rw					
t3[8]	32	0	rw					
t4[8]	32	0	rw					
t5[8]	32	0	rw					
t6[8]	32	0	rw					
t7[8]	32	0	rw					
s0[8]	32	0	rw					
s1[8]	32	0	rw					
s2[8]	32	0	rw					
s3[8]	32	0	rw					
s4[8]	32	0	rw					
s5[8]	32	0	rw					
s6[8]	32	0	rw					
s7[8]	32	0	rw					
t8[8]	32	0	rw					
t9[8]	32	0	rw					
k0[8]	32	0	rw					
k1[8]	32	0	rw					
gp[8]	32	0	rw					
sp[8]	32	0	rw	stack pointer				
s8[8]	32	0	rw	frame pointer				
ra[8]	32	0	rw					
zero[9]	32	0	r-	constant zero				
at[9]	32	0	rw					
v0[9]	32	0	rw					
v1[9]	32	0	rw					
a0[9]	32	0	rw					
a1[9]	32	0	rw					
a2[9]	32	0	rw					
a3[9]	32	0	rw					
t0[9]	32	0	rw					

t1[9]	32	0	rw	
t2[9]	32	0	rw	
t3[9]	32	0	rw	
t4[9]	32	0	rw	
t5[9]	32	0	rw	
t6[9]	32	0	rw	
t7[9]	32	0	rw	
s0[9]	32	0	rw	
s1[9]	32	0	rw	
s2[9]	32	0	rw	
s3[9]	32	0	rw	
s4[9]	32	0	rw	
s5[9]	32	0	rw	
s6[9]	32	0	rw	
s7[9]	32	0	rw	
t8[9]	32	0	rw	
t9[9]	32	0	rw	
k0[9]	32	0	rw	
k1[9]	32	0	├──	
	32	0	rw rw	
gp[9]	32	0	rw	stack pointer
sp[9] s8[9]	32	0		frame pointer
	32	0	_	marile pointer
ra[9] zero[10]	32	0	rw r-	constant zero
at[10]	32	0	├──	CONSTANT ZEIO
v0[10]	32	0	rw	
	32	0	rw	
v1[10] a0[10]	32	0	rw	
a1[10]	32	0	rw	
	32	0	rw rw	
a2[10] a3[10]	32	0	rw	
t0[10]	32	0	rw	
t1[10]	32	0	rw	
t2[10]	32	0	rw	
	32	0	rw	
t3[10]	32	0	├──	
t4[10]	32	0	rw	
t5[10]	32	0	rw	
t6[10]	32		rw	
t7[10]		0 0	rw	
s0[10]	32		rw	
s1[10]	32	0	rw	
s2[10]	32	0	rw	

s3[10]	32	0	rw	
s4[10]	32	0	rw	
s5[10]	32	0	rw	
s6[10]	32	0	rw	
s7[10]	32	0	rw	
t8[10]	32	0	rw	
t9[10]	32	0	rw	
k0[10]	32	0	rw	
k1[10]	32	0	rw	
	32	0	rw	
gp[10]	32	0	़—	ataak paintar
sp[10]	32	0	-	stack pointer frame pointer
s8[10]	32	0	-	Iname pointer
ra[10]	32	0	rw	constant zero
zero[11]	32	0	r-	constant zero
at[11]			rw	
v0[11]	32	0	rw	
v1[11]	32	0	rw	
a0[11]	32	0	rw	
a1[11]	32	0	rw	
a2[11]	32	0	rw	
a3[11]	32	0	rw	
t0[11]	32	0	rw	
t1[11]	32	0	rw	
t2[11]	32	0	rw	
t3[11]	32	0	rw	
t4[11]	32	0	rw	
t5[11]	32	0	rw	
t6[11]	32	0	rw	
t7[11]	32	0	rw	
s0[11]	32	0	rw	
s1[11]	32	0	rw	
s2[11]	32	0	rw	
s3[11]	32	0	rw	
s4[11]	32	0	rw	
s5[11]	32	0	rw	
s6[11]	32	0	rw	
s7[11]	32	0	rw	
t8[11]	32	0	rw	
t9[11]	32	0	rw	
k0[11]	32	0	rw	
k1[11]	32	0	rw	
gp[11]	32	0	rw	

sp[11]	32	0	rw	stack pointer				
s8[11]	32	0	rw	frame pointer				
ra[11]	32	0	rw					
zero[12]	32	0	r-	constant zero				
at[12]	32	0	rw					
v0[12]	32	0	rw					
v1[12]	32	0	rw					
a0[12]	32	0	rw					
a1[12]	32	0	rw					
a2[12]	32	0	rw					
a3[12]	32	0	rw					
t0[12]	32	0	rw					
t1[12]	32	0	rw					
t2[12]	32	0	rw					
t3[12]	32	0	rw					
t4[12]	32	0	rw					
t5[12]	32	0	rw					
t6[12]	32	0	rw					
t7[12]	32	0	rw					
s0[12]	32	0	rw					
s1[12]	32	0	rw					
s2[12]	32	0	rw					
s3[12]	32	0	rw					
s4[12]	32	0	rw					
s5[12]	32	0	rw					
s6[12]	32	0	rw					
s7[12]	32	0	rw					
t8[12]	32	0	rw					
t9[12]	32	0	rw					
k0[12]	32	0	rw					
k1[12]	32	0	rw					
gp[12]	32	0	rw					
sp[12]	32	0	rw	stack pointer				
s8[12]	32	0	rw	frame pointer				
ra[12]	32	0	rw					
zero[13]	32	0	r-	constant zero				
at[13]	32	0	rw					
v0[13]	32	0	rw					
v1[13]	32	0	rw	,				
a0[13]	32	0	rw					
a1[13]	32	0	rw					
a2[13]	32	0	rw					

a3[13] 3	32	0	rw	
		0		
		0	rw	
		0	rw	
			rw	
		0	rw	
	32	0	rw	
011		0	rw	
sp[13] 3	32	0	rw	stack pointer
s8[13] 3	32	0	rw	frame pointer
	32	0	rw	
zero[14] 3	32	0	r-	constant zero
at[14] 3	32	0	rw	
v0[14] 3	32	0	rw	
v1[14] 3	32	0	rw	
a0[14] 3	32	0	rw	
a1[14] 3	32	0	rw	
a2[14] 3	32	0	rw	
a3[14] 3	32	0	rw	
t0[14] 3	32	0	rw	
t1[14] 3	32	0	rw	
t2[14] 3	32	0	rw	
	32	0	rw	
t4[14] 3	32	0	rw	
	32	0	rw	
	32	0	rw	
	32	0	rw	
[· [· <del>-1</del> ] [∨	ا	_	' ' '	l I

s1[14]       32       0       rw         s2[14]       32       0       rw         s3[14]       32       0       rw         s4[14]       32       0       rw         s5[14]       32       0       rw         s6[14]       32       0       rw         t8[14]       32       0       rw         t9[14]       32       0       rw         k0[14]       32       0       rw         k1[14]       32       0       rw         gp[14]       32       0       rw	
s3[14]       32       0       rw         s4[14]       32       0       rw         s5[14]       32       0       rw         s6[14]       32       0       rw         s7[14]       32       0       rw         t8[14]       32       0       rw         t9[14]       32       0       rw         k0[14]       32       0       rw         k1[14]       32       0       rw	
s4[14]       32       0       rw         s5[14]       32       0       rw         s6[14]       32       0       rw         s7[14]       32       0       rw         t8[14]       32       0       rw         t9[14]       32       0       rw         k0[14]       32       0       rw         k1[14]       32       0       rw	
s5[14]       32       0       rw         s6[14]       32       0       rw         s7[14]       32       0       rw         t8[14]       32       0       rw         t9[14]       32       0       rw         k0[14]       32       0       rw         k1[14]       32       0       rw	
s6[14]     32     0     rw       s7[14]     32     0     rw       t8[14]     32     0     rw       t9[14]     32     0     rw       k0[14]     32     0     rw       k1[14]     32     0     rw	
s7[14]     32     0     rw       t8[14]     32     0     rw       t9[14]     32     0     rw       k0[14]     32     0     rw       k1[14]     32     0     rw	
t8[14] 32 0 rw t9[14] 32 0 rw k0[14] 32 0 rw k1[14] 32 0 rw	
t9[14] 32 0 rw k0[14] 32 0 rw k1[14] 32 0 rw	
k0[14]     32     0     rw       k1[14]     32     0     rw	
k1[14] 32 0 rw	
gp[14]  32  0  rw	
9.1 1	
sp[14] 32 0 rw stack pointer	
s8[14] 32 0 rw frame pointer	
ra[14] 32 0 rw	
zero[15] 32 0 r- constant zero	
at[15] 32 0 rw	
v0[15] 32 0 rw	
v1[15]   32   0   rw	
a0[15] 32 0 rw	
a1[15] 32 0 rw	
a2[15] 32 0 rw	
a3[15] 32 0 rw	
t0[15] 32 0 rw	
t1[15] 32 0 rw	
t2[15] 32 0 rw	
t3[15] 32 0 rw	
t4[15] 32 0 rw	
t5[15] 32 0 rw	
t6[15] 32 0 rw	
t7[15] 32 0 rw	
s0[15] 32 0 rw	
s1[15] 32 0 rw	
s2[15] 32 0 rw	
s3[15] 32 0 rw	
s4[15] 32 0 rw	
s5[15] 32 0 rw	
s6[15] 32 0 rw	
s7[15] 32 0 rw	
t8[15] 32 0 rw	
t9[15] 32 0 rw	
k0[15] 32 0 rw	

k1[15]	32	0	rw		
gp[15]	32	0	rw		
sp[15]	32	0	rw	stack pointer	
s8[15]	32	0	rw	frame pointer	
ra[15]	32	0	rw		

## 12.1.5 COP0

Table 13.

Name	Bits	Initial		Description
		value (Hex)		000 : 4 40/0
sr	32	400004	rw	CP0 register 12/0
bad	32	0	rw	CP0 register 8/0
cause	32	0	rw	CP0 register 13/0
index	32	0	rw	CP0 register 0/0
random	32	0	rw	CP0 register 1/0
entrylo0	32	0	rw	CP0 register 2/0
entrylo1	32	0	rw	CP0 register 3/0
context	32	0	rw	CP0 register 4/0
userlocal	32	0	rw	CP0 register 4/2
pagemask	32	0	rw	CP0 register 5/0
pagegrain	32	0	rw	CP0 register 5/1
wired	32	0	rw	CP0 register 6/0
hwrena	32	0	rw	CP0 register 7/0
badvaddr	32	0	rw	CP0 register 8/0
badinstr	32	0	rw	CP0 register 8/1
badinstrp	32	0	rw	CP0 register 8/2
count	32	0	rw	CP0 register 9/0
entryhi	32	0	rw	CP0 register 10/0
guestctl1	32	0	rw	CP0 register 10/4
guestctl2	32	0	rw	CP0 register 10/5
guestctl3	32	0	rw	CP0 register 10/6
compare	32	0	rw	CP0 register 11/0
guestctl0ext	32	40	rw	CP0 register 11/4
status	32	400004	rw	CP0 register 12/0
intctl	32	e3830000	rw	CP0 register 12/1
srsctl	32	3c000000	rw	CP0 register 12/2
srsmap	32	0	rw	CP0 register 12/3
viewipl	32	0	rw	CP0 register 12/4
srsmap2	32	0	rw	CP0 register 12/5
guestctl0	32	c4c00fc	rw	CP0 register 12/6
gtoffset	32	0	rw	CP0 register 12/7
viewripl	32	0	rw	CP0 register 13/4

epc 32 0 rw CP0 register 14/0 nestedepc 32 0 rw CP0 register 15/1 ebase 32 80000000 rw CP0 register 15/1 ebase 32 80000000 rw CP0 register 15/2 config 32 81a08482 rw CP0 register 16/1 config 32 bf1a4d03 rw CP0 register 16/1 config2 32 80000000 rw CP0 register 16/2 config3 32 8ca2bc28 rw CP0 register 16/3 config4 32 a00c0000 rw CP0 register 16/3 config5 32 1 rw CP0 register 16/3 config6 32 0 rw CP0 register 16/6 config7 32 8004000 rw CP0 register 16/6 config6 32 0 rw CP0 register 16/7 lladdr 32 0 rw CP0 register 16/7 lladdr 32 0 rw CP0 register 12/0 debug 32 2028000 rw CP0 register 23/0 depc 32 0 rw CP0 register 23/0 depc 32 0 rw CP0 register 28/0 itaglo 32 0 rw CP0 register 28/0 idatalo 32 0 rw CP0 register 28/1 ldatalo 32 0 rw CP0 register 28/2 ldatalo 32 0 rw CP0 register 28/2 ldatalo 32 0 rw CP0 register 28/1 ldatalo 32 0 rw CP0 register 28/2 ldatalo 32 0 rw CP0 register 28/1 l23datalo 32 0 rw CP0 register 28/1 l23datalo 32 0 rw CP0 register 28/5 ltaghi 32 0 rw CP0 register 29/0 idatahi 32 0 rw CP0 register 29/1 l23datahi 32 0 rw CP0 register 29/5 errorepc 32 0 rw CP0 register 31/2 kscratch1 32 0 rw CP0 register 31/3 guestindex 32 0 rw CP0 guest register 0/0 guestrandom 32 0 rw CP0 guest register 0/0	nestedexc	32	0	rw	CP0 register 13/5
nestedepc         32         0         rw         CP0 register 14/2           prid         32         1a720         rw         CP0 register 15/0           ebase         32         80000000         rw         CP0 register 15/1           cdmmbase         32         0         rw         CP0 register 15/2           config         32         81a08482         rw         CP0 register 16/0           config1         32         bf1a4d03         rw         CP0 register 16/1           config2         32         80000000         rw         CP0 register 16/2           config3         32         8ca2bc28         rw         CP0 register 16/3           config4         32         a00c0000         rw         CP0 register 16/3           config5         32         1         rw         CP0 register 16/6           config6         32         0         rw         CP0 register 16/7           laddr         32         80040000         rw         CP0 register 17/0           debug         32         2028000         rw         CP0 register 23/0           depc         32         0         rw         CP0 register 28/0           itaglo         32 <t< td=""><td></td><td></td><td>ļ</td><td>1</td><td></td></t<>			ļ	1	
prid 32 1a720 rw CP0 register 15/0 ebase 32 80000000 rw CP0 register 15/1 cdmmbase 32 0 rw CP0 register 15/2 config 32 81a08482 rw CP0 register 16/0 config1 32 bf1a4d03 rw CP0 register 16/1 config2 32 80000000 rw CP0 register 16/2 config3 32 8ca2bc28 rw CP0 register 16/3 config4 32 a00c0000 rw CP0 register 16/3 config5 32 1 rw CP0 register 16/6 config6 32 0 rw CP0 register 16/6 config7 32 80040000 rw CP0 register 16/6 config7 32 80040000 rw CP0 register 16/7 lladdr 32 0 rw CP0 register 16/7 lladdr 32 0 rw CP0 register 23/0 debug 32 2028000 rw CP0 register 24/0 errctl 32 0 rw CP0 register 24/0 errctl 32 0 rw CP0 register 28/0 idatalo 32 0 rw CP0 register 28/1 ddatalo 32 0 rw CP0 register 28/2 ddatalo 32 0 rw CP0 register 28/2 ldatalo 32 0 rw CP0 register 28/2 ldatalo 32 0 rw CP0 register 28/3 l23taglo 32 0 rw CP0 register 28/2 l23datalo 32 0 rw CP0 register 28/3 l23tagli 32 0 rw CP0 register 28/3 l23tagli 32 0 rw CP0 register 28/3 l23datalo 32 0 rw CP0 register 28/5 itaghi 32 0 rw CP0 register 29/0 idatahi 32 0 rw CP0 register 29/0 idatahi 32 0 rw CP0 register 29/0 idatahi 32 0 rw CP0 register 31/0 kscratch1 32 0 rw CP0 register 31/0 kscratch1 32 0 rw CP0 register 31/2 kscratch2 32 0 rw CP0 register 31/2 kscratch2 32 0 rw CP0 guest register 0/0 guestrandom 32 0 rw CP0 guest register 0/0	•		ļ		
ebase 32 8000000 rw CP0 register 15/1 cdmmbase 32 0 rw CP0 register 15/2 config 32 81a08482 rw CP0 register 16/0 config1 32 bf1a4d03 rw CP0 register 16/1 config2 32 80000000 rw CP0 register 16/2 config3 32 8ca2bc28 rw CP0 register 16/3 config4 32 a00c0000 rw CP0 register 16/3 config6 32 1 rw CP0 register 16/6 config6 32 0 rw CP0 register 16/6 config7 32 80040000 rw CP0 register 16/6 config7 32 80040000 rw CP0 register 16/7 lladdr 32 0 rw CP0 register 17/0 debug 32 2028000 rw CP0 register 23/0 depc 32 0 rw CP0 register 24/0 errctl 32 0 rw CP0 register 28/0 itaglo 32 0 rw CP0 register 28/0 itaglo 32 0 rw CP0 register 28/1 datalo 32 0 rw CP0 register 28/2 ddatalo 32 0 rw CP0 register 28/2 ldatalo 32 0 rw CP0 register 28/3 l/23taglo 32 0 rw CP0 register 28/3 l/23taglo 32 0 rw CP0 register 28/5 itaghi 32 0 rw CP0 register 28/5 itaghi 32 0 rw CP0 register 29/0 idatahi 32 0 rw CP0 register 29/0 idatahi 32 0 rw CP0 register 29/5 errorepc 32 0 rw CP0 register 31/0 kscratch1 32 0 rw CP0 register 31/2 kscratch2 32 0 rw CP0 register 31/2 kscratch2 32 0 rw CP0 register 31/2 guestrandom 32 0 rw CP0 register 13/0 rw CP0 register 31/2 guestrandom 32 0 rw CP0 register 13/0	· .		ļ	┼	
cdmmbase         32         0         rw         CP0 register 15/2           config         32         81a08482         rw         CP0 register 16/0           config1         32         bf1a4d03         rw         CP0 register 16/1           config2         32         80000000         rw         CP0 register 16/2           config3         32         8ca2bc28         rw         CP0 register 16/3           config4         32         a00c0000         rw         CP0 register 16/4           config5         32         1         rw         CP0 register 16/5           config6         32         0         rw         CP0 register 16/7           lladdr         32         0         rw         CP0 register 17/0           debug         32         2028000         rw         CP0 register 23/0           depc         32         0         rw         CP0 register 24/0           errctl         32         0         rw         CP0 register 28/0           idatalo         32         0         rw         CP0 register 28/1           dtaglo         32         0         rw         CP0 register 28/3           l23datalo         32         0			ļ	-	
config         32         81a08482         rw         CP0 register 16/0           config1         32         bf1a4d03         rw         CP0 register 16/1           config2         32         80000000         rw         CP0 register 16/2           config3         32         8ca2bc28         rw         CP0 register 16/3           config4         32         a00c0000         rw         CP0 register 16/4           config5         32         1         rw         CP0 register 16/5           config6         32         0         rw         CP0 register 16/6           config7         32         80040000         rw         CP0 register 16/7           lladdr         32         0         rw         CP0 register 16/7           lladdr         32         0         rw         CP0 register 24/0           debug         32         2028000         rw         CP0 register 24/0           errctl         32         0         rw         CP0 register 28/0           idatalo         32         0         rw         CP0 register 28/1           dtatalo         32         0         rw         CP0 register 28/3           l23datalo         32         0<			ļ	-	
config1         32         bf1a4d03         rw         CP0 register 16/1           config2         32         80000000         rw         CP0 register 16/2           config3         32         8ca2bc28         rw         CP0 register 16/3           config4         32         a00c0000         rw         CP0 register 16/4           config5         32         1         rw         CP0 register 16/5           config6         32         0         rw         CP0 register 16/6           config7         32         80040000         rw         CP0 register 16/7           lladdr         32         0         rw         CP0 register 17/0           debug         32         2028000         rw         CP0 register 23/0           depc         32         0         rw         CP0 register 26/0           itaglo         32         0         rw         CP0 register 28/0           idatalo         32         0         rw         CP0 register 28/1           ddatalo         32         0         rw         CP0 register 28/3           123datalo         32         0         rw         CP0 register 29/5           itaghi         32         0			ļ -	-	
config2         32         80000000         rw         CP0 register 16/2           config3         32         8ca2bc28         rw         CP0 register 16/3           config4         32         a00c0000         rw         CP0 register 16/4           config5         32         1         rw         CP0 register 16/5           config6         32         0         rw         CP0 register 16/7           lladdr         32         0         rw         CP0 register 17/0           debug         32         2028000         rw         CP0 register 23/0           depc         32         0         rw         CP0 register 24/0           errctl         32         0         rw         CP0 register 28/0           itaglo         32         0         rw         CP0 register 28/0           idatalo         32         0         rw         CP0 register 28/2           ddatalo         32         0         rw         CP0 register 28/3           l23taglo         32         0         rw         CP0 register 28/4           l23datalo         32         0         rw         CP0 register 29/0           idatahi         32         0         rw <td></td> <td></td> <td>Į</td> <td>-</td> <td></td>			Į	-	
config3         32         8ca2bc28         rw         CP0 register 16/3           config4         32         a00c0000         rw         CP0 register 16/4           config5         32         1         rw         CP0 register 16/5           config6         32         0         rw         CP0 register 16/6           config7         32         80040000         rw         CP0 register 16/7           lladdr         32         0         rw         CP0 register 17/0           debug         32         2028000         rw         CP0 register 23/0           depc         32         0         rw         CP0 register 24/0           errctl         32         0         rw         CP0 register 26/0           itaglo         32         0         rw         CP0 register 28/0           idatalo         32         0         rw         CP0 register 28/1           ddtaglo         32         0         rw         CP0 register 28/2           ddatalo         32         0         rw         CP0 register 28/3           123datalo         32         0         rw         CP0 register 28/5           itaghi         32         0         rw			Ļ	-	
config4         32         a00c0000         rw         CP0 register 16/4           config5         32         1         rw         CP0 register 16/5           config6         32         0         rw         CP0 register 16/6           config7         32         80040000         rw         CP0 register 16/7           lladdr         32         0         rw         CP0 register 23/0           debug         32         2028000         rw         CP0 register 23/0           depc         32         0         rw         CP0 register 24/0           errctl         32         0         rw         CP0 register 26/0           itaglo         32         0         rw         CP0 register 28/0           idatalo         32         0         rw         CP0 register 28/2           ddatalo         32         0         rw         CP0 register 28/3           l23taglo         32         0         rw         CP0 register 28/4           l23datalo         32         0         rw         CP0 register 29/0           idatahi         32         0         rw         CP0 register 29/1           l23datahi         32         0         rw			<u>!</u>	-	
config5         32         1         rw         CP0 register 16/5           config6         32         0         rw         CP0 register 16/6           config7         32         80040000         rw         CP0 register 16/7           lladdr         32         0         rw         CP0 register 23/0           debug         32         2028000         rw         CP0 register 24/0           depc         32         0         rw         CP0 register 26/0           itaglo         32         0         rw         CP0 register 28/0           idatalo         32         0         rw         CP0 register 28/1           dtaglo         32         0         rw         CP0 register 28/2           ddatalo         32         0         rw         CP0 register 28/3           l23taglo         32         0         rw         CP0 register 28/4           l23datalo         32         0         rw         CP0 register 28/5           itaghi         32         0         rw         CP0 register 29/0           idatahi         32         0         rw         CP0 register 29/5           errorepc         32         0         rw <td< td=""><td></td><td></td><td>ļ</td><td>-</td><td></td></td<>			ļ	-	
config6         32         0         rw         CP0 register 16/6           config7         32         80040000         rw         CP0 register 16/7           lladdr         32         0         rw         CP0 register 17/0           debug         32         2028000         rw         CP0 register 23/0           depc         32         0         rw         CP0 register 24/0           errctl         32         0         rw         CP0 register 26/0           itaglo         32         0         rw         CP0 register 28/0           idatalo         32         0         rw         CP0 register 28/1           dtaglo         32         0         rw         CP0 register 28/2           ddatalo         32         0         rw         CP0 register 28/3           l23taglo         32         0         rw         CP0 register 28/3           l23datalo         32         0         rw         CP0 register 28/5           itaghi         32         0         rw         CP0 register 29/0           idatahi         32         0         rw         CP0 register 29/1           l23datahi         32         0         rw <td< td=""><td></td><td></td><td></td><td>-</td><td></td></td<>				-	
Config7   32   80040000   rw   CP0 register 16/7     Iladdr   32   0   rw   CP0 register 17/0     debug   32   2028000   rw   CP0 register 23/0     depc   32   0   rw   CP0 register 24/0     errctl   32   0   rw   CP0 register 26/0     itaglo   32   0   rw   CP0 register 28/0     idatalo   32   0   rw   CP0 register 28/1     dtaglo   32   0   rw   CP0 register 28/2     ddatalo   32   0   rw   CP0 register 28/2     ddatalo   32   0   rw   CP0 register 28/3     i23taglo   32   0   rw   CP0 register 28/4     i23datalo   32   0   rw   CP0 register 28/5     itaghi   32   0   rw   CP0 register 29/0     idatahi   32   0   rw   CP0 register 29/1     i23datahi   32   0   rw   CP0 register 29/5     errorepc   32   0   rw   CP0 register 30/0     desave   32   0   rw   CP0 register 31/0     kscratch1   32   0   rw   CP0 register 31/3     guestindex   32   0   rw   CP0 guest register 0/0     guestrandom   32   0   rw   CP0 guest register 1/0			ļ	╄	
Iladdr				rw	
debug         32         2028000         rw         CP0 register 23/0           depc         32         0         rw         CP0 register 24/0           errctl         32         0         rw         CP0 register 26/0           itaglo         32         0         rw         CP0 register 28/0           idatalo         32         0         rw         CP0 register 28/2           ddatalo         32         0         rw         CP0 register 28/3           l23taglo         32         0         rw         CP0 register 28/4           l23datalo         32         0         rw         CP0 register 28/5           itaghi         32         0         rw         CP0 register 29/0           idatahi         32         0         rw         CP0 register 29/1           l23datahi         32         0         rw         CP0 register 30/0           desave         32         0         rw         CP0 register 31/0           kscratch1         32         0         rw         CP0 register 31/3           guestindex         32         0         rw         CP0 guest register 0/0           guestrandom         32         0         rw			Ļ	rw	
depc         32         0         rw         CP0 register 24/0           errctl         32         0         rw         CP0 register 26/0           itaglo         32         0         rw         CP0 register 28/0           idatalo         32         0         rw         CP0 register 28/1           dtaglo         32         0         rw         CP0 register 28/2           ddatalo         32         0         rw         CP0 register 28/3           l23taglo         32         0         rw         CP0 register 28/4           l23datalo         32         0         rw         CP0 register 29/0           idatahi         32         0         rw         CP0 register 29/0           idatahi         32         0         rw         CP0 register 29/1           l23datahi         32         0         rw         CP0 register 30/0           desave         32         0         rw         CP0 register 31/0           kscratch1         32         0         rw         CP0 register 31/2           kscratch2         32         0         rw         CP0 register 91/3           guestindex         32         0         rw         CP				rw	
errctl 32 0 rw CP0 register 26/0 itaglo 32 0 rw CP0 register 28/0 idatalo 32 0 rw CP0 register 28/1 dtaglo 32 0 rw CP0 register 28/2 ddatalo 32 0 rw CP0 register 28/2 ddatalo 32 0 rw CP0 register 28/3 l23taglo 32 0 rw CP0 register 28/4 l23datalo 32 0 rw CP0 register 28/5 itaghi 32 0 rw CP0 register 29/0 idatahi 32 0 rw CP0 register 29/1 l23datahi 32 0 rw CP0 register 29/1 l23datahi 32 0 rw CP0 register 29/5 errorepc 32 0 rw CP0 register 30/0 desave 32 0 rw CP0 register 31/0 kscratch1 32 0 rw CP0 register 31/2 kscratch2 32 0 rw CP0 register 31/3 guestindex 32 0 rw CP0 guest register 0/0 guestrandom 32 0 rw CP0 guest register 1/0				rw	
itaglo         32         0         rw         CP0 register 28/0           idatalo         32         0         rw         CP0 register 28/1           dtaglo         32         0         rw         CP0 register 28/2           ddatalo         32         0         rw         CP0 register 28/3           l23taglo         32         0         rw         CP0 register 28/4           l23datalo         32         0         rw         CP0 register 29/0           idatahi         32         0         rw         CP0 register 29/1           l23datahi         32         0         rw         CP0 register 29/5           errorepc         32         0         rw         CP0 register 30/0           desave         32         0         rw         CP0 register 31/0           kscratch1         32         0         rw         CP0 register 31/2           kscratch2         32         0         rw         CP0 register 0/0           guestindex         32         0         rw         CP0 guest register 1/0	·		Į	rw	
idatalo         32         0         rw         CP0 register 28/1           dtaglo         32         0         rw         CP0 register 28/2           ddatalo         32         0         rw         CP0 register 28/3           l23taglo         32         0         rw         CP0 register 28/4           l23datalo         32         0         rw         CP0 register 28/5           itaghi         32         0         rw         CP0 register 29/0           idatahi         32         0         rw         CP0 register 29/1           l23datahi         32         0         rw         CP0 register 29/5           errorepc         32         0         rw         CP0 register 30/0           desave         32         0         rw         CP0 register 31/0           kscratch1         32         0         rw         CP0 register 31/3           guestindex         32         0         rw         CP0 guest register 0/0           guestrandom         32         0         rw         CP0 guest register 1/0	errctl	32	0	rw	
dtaglo         32         0         rw         CP0 register 28/2           ddatalo         32         0         rw         CP0 register 28/3           l23taglo         32         0         rw         CP0 register 28/4           l23datalo         32         0         rw         CP0 register 28/5           itaghi         32         0         rw         CP0 register 29/0           idatahi         32         0         rw         CP0 register 29/1           l23datahi         32         0         rw         CP0 register 29/5           errorepc         32         0         rw         CP0 register 30/0           desave         32         0         rw         CP0 register 31/0           kscratch1         32         0         rw         CP0 register 31/2           kscratch2         32         0         rw         CP0 guest register 0/0           guestindex         32         0         rw         CP0 guest register 1/0	itaglo	32	0	rw	CP0 register 28/0
ddatalo         32         0         rw         CP0 register 28/3           I23taglo         32         0         rw         CP0 register 28/4           I23datalo         32         0         rw         CP0 register 28/5           itaghi         32         0         rw         CP0 register 29/0           idatahi         32         0         rw         CP0 register 29/1           I23datahi         32         0         rw         CP0 register 29/5           errorepc         32         0         rw         CP0 register 30/0           desave         32         0         rw         CP0 register 31/0           kscratch1         32         0         rw         CP0 register 31/2           kscratch2         32         0         rw         CP0 guest register 0/0           guestindex         32         0         rw         CP0 guest register 1/0	idatalo	32	0	rw	CP0 register 28/1
I23taglo	dtaglo	32	0	rw	CP0 register 28/2
I23datalo   32   0   rw   CP0 register 28/5     itaghi   32   0   rw   CP0 register 29/0     idatahi   32   0   rw   CP0 register 29/1     I23datahi   32   0   rw   CP0 register 29/5     errorepc   32   0   rw   CP0 register 30/0     desave   32   0   rw   CP0 register 31/0     kscratch1   32   0   rw   CP0 register 31/2     kscratch2   32   0   rw   CP0 register 31/3     guestindex   32   0   rw   CP0 guest register 0/0     guestrandom   32   0   rw   CP0 guest register 1/0	ddatalo	32	0	rw	CP0 register 28/3
itaghi         32         0         rw         CP0 register 29/0           idatahi         32         0         rw         CP0 register 29/1           I23datahi         32         0         rw         CP0 register 29/5           errorepc         32         0         rw         CP0 register 30/0           desave         32         0         rw         CP0 register 31/0           kscratch1         32         0         rw         CP0 register 31/2           kscratch2         32         0         rw         CP0 register 31/3           guestindex         32         0         rw         CP0 guest register 0/0           guestrandom         32         0         rw         CP0 guest register 1/0	l23taglo	32	0	rw	CP0 register 28/4
idatahi         32         0         rw         CP0 register 29/1           I23datahi         32         0         rw         CP0 register 29/5           errorepc         32         0         rw         CP0 register 30/0           desave         32         0         rw         CP0 register 31/0           kscratch1         32         0         rw         CP0 register 31/2           kscratch2         32         0         rw         CP0 register 31/3           guestindex         32         0         rw         CP0 guest register 0/0           guestrandom         32         0         rw         CP0 guest register 1/0	l23datalo	32	0	rw	CP0 register 28/5
123datahi   32   0   rw   CP0 register 29/5     errorepc   32   0   rw   CP0 register 30/0     desave   32   0   rw   CP0 register 31/0     kscratch1   32   0   rw   CP0 register 31/2     kscratch2   32   0   rw   CP0 register 31/3     guestindex   32   0   rw   CP0 guest register 0/0     guestrandom   32   0   rw   CP0 guest register 1/0	itaghi	32	0	rw	CP0 register 29/0
errorepc         32         0         rw         CP0 register 30/0           desave         32         0         rw         CP0 register 31/0           kscratch1         32         0         rw         CP0 register 31/2           kscratch2         32         0         rw         CP0 register 31/3           guestindex         32         0         rw         CP0 guest register 0/0           guestrandom         32         0         rw         CP0 guest register 1/0	idatahi	32	0	rw	CP0 register 29/1
desave         32         0         rw         CP0 register 31/0           kscratch1         32         0         rw         CP0 register 31/2           kscratch2         32         0         rw         CP0 register 31/3           guestindex         32         0         rw         CP0 guest register 0/0           guestrandom         32         0         rw         CP0 guest register 1/0	I23datahi	32	0	rw	CP0 register 29/5
kscratch1         32         0         rw         CP0 register 31/2           kscratch2         32         0         rw         CP0 register 31/3           guestindex         32         0         rw         CP0 guest register 0/0           guestrandom         32         0         rw         CP0 guest register 1/0	errorepc	32	0	rw	CP0 register 30/0
kscratch2 32 0 rw CP0 register 31/3 guestindex 32 0 rw CP0 guest register 0/0 guestrandom 32 0 rw CP0 guest register 1/0	desave	32	0	rw	CP0 register 31/0
guestindex 32 0 rw CP0 guest register 0/0 guestrandom 32 0 rw CP0 guest register 1/0	kscratch1	32	0	rw	CP0 register 31/2
guestrandom 32 0 rw CP0 guest register 1/0	kscratch2	32	0	rw	CP0 register 31/3
	guestindex	32	0	rw	CP0 guest register 0/0
guestentrylo0 32 0 rw CP0 guest register 2/0	guestrandom	32	0	rw	CP0 guest register 1/0
10 / · ·  -  -  -  -  -  -  -  -  -  -  -  -  -	guestentrylo0	32	0	rw	CP0 guest register 2/0
guestentrylo1 32 0 rw CP0 guest register 3/0	guestentrylo1	32	0	rw	CP0 guest register 3/0
guestcontext 32 0 rw CP0 guest register 4/0	guestcontext	32	0	rw	CP0 guest register 4/0
guestuserlocal 32 0 rw CP0 guest register 4/2		32	0	rw	
guestpagemask 32 0 rw CP0 guest register 5/0		32	0	rw	CP0 guest register 5/0
guestpagegrain 32 0 rw CP0 guest register 5/1	• • •	32	0	rw	
guestwired 32 0 rw CP0 guest register 6/0		1	0	rw	
guesthwrena 32 0 rw CP0 guest register 7/0	-			rw	
guestbadvaddr 32 0 rw CP0 guest register 8/0				╂	

guestocount   32	guestbadinstr	32	0	rw	CP0 guest register 8/1
guestount         32         0         rw         CPO guest register 9/0           guestguestctt1         32         0         rw         CPO guest register 10/0           guestguestctt1         32         lffffffff         rw         CPO guest register 10/6           guestguestct12         32         lffffffff         rw         CPO guest register 10/6           guestguestct0ext         32         lffffffff         rw         CPO guest register 11/0           guestguestct10ext         32         lffffffff         rw         CPO guest register 11/0           gueststratus         32         400004         rw         CPO guest register 12/0           gueststratt         32         32000000         rw         CPO guest register 12/1           gueststrsmap         32         lfffffff         rw         CPO guest register 12/2           gueststrsmap         32         lffffffff         rw         CPO guest register 12/5           guestguestct0         32         lffffffff         rw         CPO guest register 12/6           guestguestct0         32         lffffffff         rw         CPO guest register 12/7           guestguestcus         32         lfffffff         rw         CPO guest register 13/4		<u> </u>	<del> </del>	-	
guestentryhi         32         0         rw         CPO guest register 10/0           guestguestcl1         32         ffffffff         rw         CPO guest register 10/4           guestguestcl3         32         ffffffff         rw         CPO guest register 10/6           guestguestcl3         32         ffffffff         rw         CPO guest register 11/0           guestguestcl0ext         32         ffffffff         rw         CPO guest register 11/0           gueststastus         32         400004         rw         CPO guest register 12/1           guestinctl         32         3830000         rw         CPO guest register 12/2           guestsrsmap         32         ffffffff         rw         CPO guest register 12/2           guestsrsmap         32         fffffffff         rw         CPO guest register 12/2           guestviewipl         32         0         rw         CPO guest register 12/3           guestguestcl0         32         fffffffff         rw         CPO guest register 12/6           guestguestcdstase         32         0         rw         CPO guest register 12/7           guestcase         32         0         rw         CPO guest register 13/4           guestnestedexc <td></td> <td></td> <td></td> <td>┼</td> <td></td>				┼	
guestguestctl1         32         ffffffff         rw         CP0 guest register 10/4           guestguestctl2         32         ffffffff         rw         CP0 guest register 10/5           guestguestctl3         32         ffffffff         rw         CP0 guest register 10/6           guestcompare         32         0         rw         CP0 guest register 11/0           gueststrast         32         400004         rw         CP0 guest register 12/0           guestintctl         32         83000000         rw         CP0 guest register 12/1           guestsrsmap         32         36000000         rw         CP0 guest register 12/2           guestsrsmap         32         ffffffff         rw         CP0 guest register 12/3           guestyriewipl         32         0         rw         CP0 guest register 12/4           guestguestctl0         32         fffffffff         rw         CP0 guest register 12/6           guestguestguestctl0         32         ffffffff         rw         CP0 guest register 12/7           guestduested         32         0         rw         CP0 guest register 13/0           guestduestedrife         32         0         rw         CP0 guest register 13/4           guestdue		<u> </u>	<del> </del>	-	
guestguestct12         32         ffffffff         rw         CP0 guest register 10/5           guestguestct13         32         ffffffff         rw         CP0 guest register 11/0           guestguestctloext         32         ffffffff         rw         CP0 guest register 11/0           guestguestctloext         32         400004         rw         CP0 guest register 12/0           gueststatus         32         400004         rw         CP0 guest register 12/1           guestsrsctl         32         3000000         rw         CP0 guest register 12/2           guestsrsmap         32         ffffffff         rw         CP0 guest register 12/3           gueststrewipl         32         0         rw         CP0 guest register 12/3           guestytewipl         32         0         rw         CP0 guest register 12/4           guestguestct10         32         ffffffff         rw         CP0 guest register 12/6           guestguestdeffset         32         ffffffff         rw         CP0 guest register 12/7           guestguestduestcus         32         0         rw         CP0 guest register 13/0           guestduestedwer         32         0         rw         CP0 guest register 13/4	· ·	<u> </u>	<u> </u>	-	
guestguestct13         32         ffffffff         rw         CP0 guest register 10/6           guestguestct0mare         32         0         rw         CP0 guest register 11/0           guestguestct10ext         32         fffffffff         rw         CP0 guest register 11/4           gueststatus         32         400004         rw         CP0 guest register 12/0           gueststrst1         32         32000000         rw         CP0 guest register 12/2           guestsrsmap         32         ffffffff         rw         CP0 guest register 12/3           guestsviewipl         32         0         rw         CP0 guest register 12/4           guestguestct0         32         fffffffff         rw         CP0 guest register 12/5           guestguestcull         32         fffffffff         rw         CP0 guest register 12/6           guestguestdestcull         32         fffffffff         rw         CP0 guest register 12/7           guestduestcull         32         ffffffffff         rw         CP0 guest register 13/0           guestcull         32         fffffffff         rw         CP0 guest register 13/4           guestper         32         0         rw         CP0 guest register 14/2           <	<u> </u>			-	
guestcompare         32         0         rw         CP0 guest register 11/0           guestguestctlloext         32         ffffffff         rw         CP0 guest register 12/0           guestintctl         32         4000004         rw         CP0 guest register 12/0           gueststrass         32         32000000         rw         CP0 guest register 12/1           guestsrsmap         32         ifffffff         rw         CP0 guest register 12/2           gueststrewipl         32         0         rw         CP0 guest register 12/3           gueststresmap2         32         iffffffff         rw         CP0 guest register 12/4           guestguestctl0         32         iffffffff         rw         CP0 guest register 12/5           guestguestgeffset         32         iffffffff         rw         CP0 guest register 12/7           guestdeuse         32         0         rw         CP0 guest register 13/4           guestdeuses         32         0         rw         CP0 guest register 13/5           guesthepc         32         0         rw         CP0 guest register 14/0           guestbepc         32         0         rw         CP0 guest register 15/0           guestconfig1         3	<u> </u>		<u> </u>	-	
guestguestctiloext         32         ffffffff         rw         CP0 guest register 11/4           gueststatus         32         400004         rw         CP0 guest register 12/0           gueststrictt         32         e38300000         rw         CP0 guest register 12/1           guestsrscrll         32         36000000         rw         CP0 guest register 12/2           guestsrsmap         32         ffffffff         rw         CP0 guest register 12/3           guestsrsmap2         32         ffffffff         rw         CP0 guest register 12/5           guestguestctl0         32         ffffffff         rw         CP0 guest register 12/6           guestguestctl0         32         ffffffff         rw         CP0 guest register 12/7           guestguestcuse         32         0         rw         CP0 guest register 13/4           guestduestause         32         0         rw         CP0 guest register 13/4           guestduestedex         32         0         rw         CP0 guest register 13/4           guestdepc         32         0         rw         CP0 guest register 14/2           guestdepc         32         0         rw         CP0 guest register 15/0           guestdmbase		<u> </u>		-	3 3
gueststatus         32         400004         m         CPO guest register 12/0           guestsinctI         32         e3830000         m         CPO guest register 12/1           guestsrsctI         32         3c000000         m         CPO guest register 12/2           guestsrsmap         32         Iffffffff         m         CPO guest register 12/3           guestvewipl         32         0         m         CPO guest register 12/4           guestsrsmap2         32         Iffffffff         m         CPO guest register 12/6           guestguestctil0         32         Ifffffff         m         CPO guest register 12/7           guestguestguestctil0         32         Iffffffff         m         CPO guest register 13/0           guestguestguestguestguestguestguestguest				╂——	
guestintct1         32         e3830000         rw         CP0 guest register 12/1           guestsrsctl         32         3c000000         rw         CP0 guest register 12/2           guestsrsmap         32         ffffffff         rw         CP0 guest register 12/3           guestsviewipl         32         0         rw         CP0 guest register 12/4           guestguestctt0         32         ffffffff         rw         CP0 guest register 12/5           guestguestctt0         32         ffffffff         rw         CP0 guest register 12/7           guestguestcuse         32         0         rw         CP0 guest register 13/0           guestause         32         0         rw         CP0 guest register 13/4           guesterber         32         0         rw         CP0 guest register 13/5           guesterbe         32         0         rw         CP0 guest register 14/0           guestredepc         32         0         rw         CP0 guest register 14/2           guestprid         32         ffffffff         rw         CP0 guest register 15/0           guestprid         32         ffffffff         rw         CP0 guest register 15/0           guestconfig         32 <td< td=""><td></td><td></td><td></td><td>1</td><td></td></td<>				1	
guestsrsctl         32         3c000000         rw         CP0 guest register 12/2           guestsrsmap         32         ffffffff         rw         CP0 guest register 12/3           guestsrsmap2         32         ffffffff         rw         CP0 guest register 12/4           guestguestctl0         32         ffffffff         rw         CP0 guest register 12/5           guestguestctl0         32         ffffffff         rw         CP0 guest register 12/6           guestguestguestctl0         32         fffffffff         rw         CP0 guest register 12/7           guestcause         32         0         rw         CP0 guest register 13/0           guestcause         32         0         rw         CP0 guest register 13/4           guestnestedexc         32         0         rw         CP0 guest register 14/0           guestprid         32         0         rw         CP0 guest register 14/2           guestbase         32         80000000         rw         CP0 guest register 15/0           guestconfig         32         81a08482         rw         CP0 guest register 15/1           guestconfig1         32         bf1a4d01         rw         CP0 guest register 16/0           guestconfig3			ļ	-	
guestsrsmap         32         ffffffff         rw         CP0 guest register 12/3           guestviewipl         32         0         rw         CP0 guest register 12/4           guestsrsmap2         32         ffffffff         rw         CP0 guest register 12/5           guestguestct10         32         ffffffff         rw         CP0 guest register 12/6           guestguestct10         32         fffffffff         rw         CP0 guest register 12/7           guestguestcuse         32         0         rw         CP0 guest register 13/0           guestviewripl         32         0         rw         CP0 guest register 13/4           guestnestedexc         32         0         rw         CP0 guest register 13/5           guestepc         32         0         rw         CP0 guest register 14/0           guestepc         32         0         rw         CP0 guest register 14/2           guestprid         32         fffffffff         rw         CP0 guest register 15/0           guestprid         32         fffffffff         rw         CP0 guest register 15/1           guestconfig         32         810000000         rw         CP0 guest register 16/2           guestconfig         32			<u> </u>	-	
guestviewipl 32 0 rw CP0 guest register 12/4 guestsrsmap2 32 ffffffff rw CP0 guest register 12/5 guestguestctl0 32 ffffffff rw CP0 guest register 12/6 guestguestctl0 32 ffffffff rw CP0 guest register 12/7 guestcause 32 0 rw CP0 guest register 13/0 guestviewripl 32 0 rw CP0 guest register 13/4 guestnestedexc 32 0 rw CP0 guest register 13/4 guestpec 32 0 rw CP0 guest register 13/5 guestepc 32 0 rw CP0 guest register 14/0 guestrestedepc 32 0 rw CP0 guest register 14/0 guestrestedepc 32 0 rw CP0 guest register 14/0 guestprid 32 ffffffff rw CP0 guest register 14/2 guestprid 32 ffffffff rw CP0 guest register 15/0 guestedase 32 80000000 rw CP0 guest register 15/0 guestcdmmbase 32 ffffffff rw CP0 guest register 15/1 guestconfig 32 81a08482 rw CP0 guest register 16/0 guestconfig 32 81a08482 rw CP0 guest register 16/0 guestconfig 32 80000000 rw CP0 guest register 16/1 guestconfig 32 80000000 rw CP0 guest register 16/2 guestconfig 32 80000000 rw CP0 guest register 16/3 guestconfig 32 80000000 rw CP0 guest register 16/3 guestconfig 32 80000000 rw CP0 guest register 16/3 guestconfig 32 1 rw CP0 guest register 16/6 guestconfig 32 0 rw CP0 guest register 16/6 guestconfig 32 0 rw CP0 guest register 16/6 guestconfig 32 0 rw CP0 guest register 16/7 guestlladdr 32 0 rw CP0 guest register 16/7 guestlladdr 32 0 rw CP0 guest register 16/7 guestlladdr 32 ffffffff rw CP0 guest register 23/0 guestdebug 32 ffffffff rw CP0 guest register 23/0 guestdepc 32 ffffffff rw CP0 guest register 28/0 guestdatalo 32 ffffffff rw CP0 guest register 28/1 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	•		<u> </u>	rw	
guestsrsmap2         32         ffffffff         rw         CP0 guest register 12/5           guestguestct10         32         ffffffff         rw         CP0 guest register 12/6           guestguestcuse         32         ffffffff         rw         CP0 guest register 12/7           guestcause         32         0         rw         CP0 guest register 13/0           guestnestedexc         32         0         rw         CP0 guest register 13/5           guestpec         32         0         rw         CP0 guest register 14/0           guestpec         32         0         rw         CP0 guest register 14/0           guestprid         32         1fffffff         rw         CP0 guest register 14/2           guestprid         32         80000000         rw         CP0 guest register 15/0           guestprid         32         80000000         rw         CP0 guest register 15/1           guestconfig         32         81a08482         rw         CP0 guest register 16/2           guestconfig         32         81a08482         rw         CP0 guest register 16/3           guestconfig3         32         8c2bc20         rw         CP0 guest register 16/3           guestconfig3         32	-			rw	
guestguestctl0         32         ffffffff         rw         CP0 guest register 12/6           guestgtoffset         32         ffffffff         rw         CP0 guest register 13/0           guestcause         32         0         rw         CP0 guest register 13/4           guestviewripl         32         0         rw         CP0 guest register 13/5           guestnestedexc         32         0         rw         CP0 guest register 14/0           guestpec         32         0         rw         CP0 guest register 14/2           guestprid         32         ffffffff         rw         CP0 guest register 15/0           guestbase         32         80000000         rw         CP0 guest register 15/1           guestconfig         32         81a08482         rw         CP0 guest register 16/0           guestconfig         32         81a08482         rw         CP0 guest register 16/1           guestconfig         32         80000000         rw         CP0 guest register 16/2           guestconfig         32         80000000         rw         CP0 guest register 16/2           guestconfig         32         80c2bc20         rw         CP0 guest register 16/3           guestconfig         32 <td></td> <td></td> <td>ļ</td> <td>rw</td> <td></td>			ļ	rw	
guestgtoffset         32         ffffffff         rw         CP0 guest register 12/7           guestcause         32         0         rw         CP0 guest register 13/0           guestviewripl         32         0         rw         CP0 guest register 13/4           guestnestedexc         32         0         rw         CP0 guest register 13/5           guestepc         32         0         rw         CP0 guest register 14/0           guestepc         32         0         rw         CP0 guest register 14/2           guestepc         32         0         rw         CP0 guest register 15/0           guestchmeter         32         80000000         rw         CP0 guest register 15/1           guestcdmmbase         32         80000000         rw         CP0 guest register 15/2           guestconfig         32         81a08482         rw         CP0 guest register 16/0           guestconfig1         32         bf1a4d01         rw         CP0 guest register 16/1           guestconfig2         32         80000000         rw         CP0 guest register 16/3           guestconfig3         32         8c22bc20         rw         CP0 guest register 16/4           guestconfig6         32         <		<u> </u>		rw	
guestcause         32         0         rw         CP0 guest register 13/0           guestviewripl         32         0         rw         CP0 guest register 13/4           guestnestedexc         32         0         rw         CP0 guest register 13/5           guestepc         32         0         rw         CP0 guest register 14/0           guestnestedepc         32         0         rw         CP0 guest register 14/2           guestprid         32         fffffffff         rw         CP0 guest register 15/0           guestebase         32         80000000         rw         CP0 guest register 15/1           guestcdmmbase         32         81108482         rw         CP0 guest register 16/0           guestconfig         32         81408482         rw         CP0 guest register 16/0           guestconfig         32         81408482         rw         CP0 guest register 16/1           guestconfig         32         80000000         rw         CP0 guest register 16/2           guestconfig         32         80000000         rw         CP0 guest register 16/3           guestconfig         32         1         rw         CP0 guest register 16/5           guestconfig         32         <	<u> </u>			rw	
guestviewripl         32         0         rw         CP0 guest register 13/4           guestnestedexc         32         0         rw         CP0 guest register 13/5           guestepc         32         0         rw         CP0 guest register 14/0           guestnestedepc         32         0         rw         CP0 guest register 14/2           guestprid         32         ffffffff         rw         CP0 guest register 15/0           guestebase         32         80000000         rw         CP0 guest register 15/1           guestcdmmbase         32         fffffffff         rw         CP0 guest register 15/2           guestconfig         32         81a08482         rw         CP0 guest register 16/0           guestconfig1         32         bf1a4d01         rw         CP0 guest register 16/1           guestconfig2         32         80000000         rw         CP0 guest register 16/2           guestconfig3         32         8c22bc20         rw         CP0 guest register 16/3           guestconfig4         32         a00c0000         rw         CP0 guest register 16/5           guestconfig6         32         0         rw         CP0 guest register 16/6           guestdebug         32 <td>guestgtoffset</td> <td>32</td> <td>fffffff</td> <td>rw</td> <td></td>	guestgtoffset	32	fffffff	rw	
guestnestedexc         32         0         rw         CP0 guest register 13/5           guestepc         32         0         rw         CP0 guest register 14/0           guestnestedepc         32         0         rw         CP0 guest register 14/2           guestprid         32         ffffffff         rw         CP0 guest register 15/0           guestebase         32         80000000         rw         CP0 guest register 15/1           guestconfig         32         81a08482         rw         CP0 guest register 15/2           guestconfig         32         81a08482         rw         CP0 guest register 16/0           guestconfig         32         80000000         rw         CP0 guest register 16/1           guestconfig2         32         80000000         rw         CP0 guest register 16/2           guestconfig3         32         8c22bc20         rw         CP0 guest register 16/3           guestconfig4         32         a00c0000         rw         CP0 guest register 16/5           guestconfig5         32         1         rw         CP0 guest register 16/6           guestconfig6         32         0         rw         CP0 guest register 16/7           guestladdr         32	guestcause	32	0	rw	CP0 guest register 13/0
guestepc         32         0         rw         CP0 guest register 14/0           guestnestedepc         32         0         rw         CP0 guest register 14/2           guestprid         32         ffffffff         rw         CP0 guest register 15/0           guestebase         32         80000000         rw         CP0 guest register 15/1           guestcdmmbase         32         ffffffff         rw         CP0 guest register 15/2           guestconfig         32         81a08482         rw         CP0 guest register 16/0           guestconfig1         32         bf1a4d01         rw         CP0 guest register 16/1           guestconfig2         32         80000000         rw         CP0 guest register 16/2           guestconfig3         32         8c22bc20         rw         CP0 guest register 16/3           guestconfig4         32         a00c0000         rw         CP0 guest register 16/4           guestconfig5         32         1         rw         CP0 guest register 16/5           guestconfig6         32         0         rw         CP0 guest register 16/7           guestladdr         32         80040000         rw         CP0 guest register 16/7           guestdebug         32 </td <td>guestviewripl</td> <td>32</td> <td>0</td> <td>rw</td> <td>CP0 guest register 13/4</td>	guestviewripl	32	0	rw	CP0 guest register 13/4
guestnestedepc guestprid guestprid guestebase guestebase guestcommbase guestconfig guestconfig guestconfig2 guestconfig3 guestconfig3 guestconfig4 guestconfig4 guestconfig6 guestconfig6 guestconfig7 guestconfig8 guestconfig9 g	guestnestedexc	32	0	rw	CP0 guest register 13/5
guestprid 32 ffffffff rw CP0 guest register 15/0 guestebase 32 80000000 rw CP0 guest register 15/1 guestcdmmbase 32 ffffffff rw CP0 guest register 15/2 guestconfig 32 81a08482 rw CP0 guest register 16/0 guestconfig 32 bf1a4d01 rw CP0 guest register 16/1 guestconfig 32 8000000 rw CP0 guest register 16/2 guestconfig 32 8000000 rw CP0 guest register 16/3 guestconfig 32 8c22bc20 rw CP0 guest register 16/3 guestconfig 32 a00c0000 rw CP0 guest register 16/4 guestconfig 32 nw CP0 guest register 16/5 guestconfig 32 nw CP0 guest register 16/5 guestconfig 32 nw CP0 guest register 16/6 guestconfig 32 nw CP0 guest register 16/7 guest register 23/0 guestdebug 32 ffffffff rw CP0 guest register 24/0 guesterrctl 32 ffffffff rw CP0 guest register 26/0 guestiaglo 32 ffffffff rw CP0 guest register 28/0 guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	guestepc	32	0	rw	
guestebase         32         80000000         rw         CP0 guest register 15/1           guestcdmmbase         32         fffffffff         rw         CP0 guest register 15/2           guestconfig         32         81a08482         rw         CP0 guest register 16/0           guestconfig1         32         bf1a4d01         rw         CP0 guest register 16/1           guestconfig2         32         80000000         rw         CP0 guest register 16/2           guestconfig3         32         8c22bc20         rw         CP0 guest register 16/3           guestconfig4         32         a00c0000         rw         CP0 guest register 16/4           guestconfig5         32         1         rw         CP0 guest register 16/6           guestconfig6         32         0         rw         CP0 guest register 16/7           guestladdr         32         80040000         rw         CP0 guest register 16/7           guestdebug         32         fffffffff         rw         CP0 guest register 23/0           guestdepc         32         fffffffff         rw         CP0 guest register 26/0           guestidatalo         32         fffffffff         rw         CP0 guest register 28/1           guestddatalo </td <td>guestnestedepc</td> <td>32</td> <td>0</td> <td>rw</td> <td>CP0 guest register 14/2</td>	guestnestedepc	32	0	rw	CP0 guest register 14/2
guestconfig 32 81a08482 rw CP0 guest register 15/2 guestconfig 32 81a08482 rw CP0 guest register 16/0 guestconfig1 32 bf1a4d01 rw CP0 guest register 16/1 guestconfig2 32 80000000 rw CP0 guest register 16/2 guestconfig3 32 8c22bc20 rw CP0 guest register 16/3 guestconfig4 32 a00c0000 rw CP0 guest register 16/4 guestconfig5 32 1 rw CP0 guest register 16/5 guestconfig6 32 0 rw CP0 guest register 16/6 guestconfig7 32 80040000 rw CP0 guest register 16/7 guestlladdr 32 0 rw CP0 guest register 16/7 guestlladdr 32 0 rw CP0 guest register 17/0 guestdebug 32 ffffffff rw CP0 guest register 23/0 guestdepc 32 ffffffff rw CP0 guest register 24/0 guesterrctl 32 fffffff rw CP0 guest register 26/0 guestitaglo 32 ffffffff rw CP0 guest register 28/1 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	guestprid	32	fffffff	rw	CP0 guest register 15/0
guestconfig 32 81a08482 rw CP0 guest register 16/0 guestconfig1 32 bf1a4d01 rw CP0 guest register 16/1 guestconfig2 32 80000000 rw CP0 guest register 16/2 guestconfig3 32 8c22bc20 rw CP0 guest register 16/3 guestconfig4 32 a00c0000 rw CP0 guest register 16/4 guestconfig5 32 1 rw CP0 guest register 16/5 guestconfig6 32 0 rw CP0 guest register 16/6 guestconfig7 32 80040000 rw CP0 guest register 16/6 guestconfig7 32 80040000 rw CP0 guest register 16/7 guestlladdr 32 0 rw CP0 guest register 17/0 guestdebug 32 ffffffff rw CP0 guest register 23/0 guestdepc 32 ffffffff rw CP0 guest register 24/0 guesterrctl 32 ffffffff rw CP0 guest register 26/0 guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	guestebase	32	80000000	rw	CP0 guest register 15/1
guestconfig1 32 bf1a4d01 rw CP0 guest register 16/1 guestconfig2 32 80000000 rw CP0 guest register 16/2 guestconfig3 32 8c22bc20 rw CP0 guest register 16/3 guestconfig4 32 a00c0000 rw CP0 guest register 16/4 guestconfig5 32 1 rw CP0 guest register 16/5 guestconfig6 32 0 rw CP0 guest register 16/6 guestconfig7 32 80040000 rw CP0 guest register 16/7 guestlladdr 32 0 rw CP0 guest register 16/7 guestlladdr 32 0 rw CP0 guest register 17/0 guestdebug 32 ffffffff rw CP0 guest register 23/0 guestdepc 32 ffffffff rw CP0 guest register 24/0 guesterrctl 32 ffffffff rw CP0 guest register 26/0 guestidatalo 32 ffffffff rw CP0 guest register 28/0 guestddatalo 32 ffffffff rw CP0 guest register 28/2	guestcdmmbase	32	fffffff	rw	CP0 guest register 15/2
guestconfig2 32 80000000 rw CP0 guest register 16/2 guestconfig3 32 8c22bc20 rw CP0 guest register 16/3 guestconfig4 32 a00c0000 rw CP0 guest register 16/4 guestconfig5 32 1 rw CP0 guest register 16/5 guestconfig6 32 0 rw CP0 guest register 16/6 guestconfig7 32 80040000 rw CP0 guest register 16/7 guestlladdr 32 0 rw CP0 guest register 16/7 guestlladdr 32 0 rw CP0 guest register 17/0 guestdebug 32 ffffffff rw CP0 guest register 23/0 guestdepc 32 ffffffff rw CP0 guest register 24/0 guesterrctl 32 ffffffff rw CP0 guest register 26/0 guestidatalo 32 ffffffff rw CP0 guest register 28/0 guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2	guestconfig	32	81a08482	rw	CP0 guest register 16/0
guestconfig3 32 8c22bc20 rw CP0 guest register 16/3 guestconfig4 32 a00c0000 rw CP0 guest register 16/4 guestconfig5 32 1 rw CP0 guest register 16/5 guestconfig6 32 0 rw CP0 guest register 16/6 guestconfig7 32 80040000 rw CP0 guest register 16/7 guestlladdr 32 0 rw CP0 guest register 16/7 guestlladdr 32 ffffffff rw CP0 guest register 23/0 guestdebug 32 ffffffff rw CP0 guest register 23/0 guestdepc 32 ffffffff rw CP0 guest register 24/0 guesterrctl 32 ffffffff rw CP0 guest register 26/0 guestitaglo 32 ffffffff rw CP0 guest register 28/0 guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestdtaglo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	guestconfig1	32	bf1a4d01	rw	CP0 guest register 16/1
guestconfig4 32 a00c0000 rw CP0 guest register 16/4 guestconfig5 32 1 rw CP0 guest register 16/5 guestconfig6 32 0 rw CP0 guest register 16/6 guestconfig7 32 80040000 rw CP0 guest register 16/7 guestlladdr 32 0 rw CP0 guest register 17/0 guestdebug 32 ffffffff rw CP0 guest register 23/0 guestdepc 32 ffffffff rw CP0 guest register 24/0 guesterrctl 32 ffffffff rw CP0 guest register 26/0 guestitaglo 32 ffffffff rw CP0 guest register 28/0 guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestdtaglo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	guestconfig2	32	80000000	rw	CP0 guest register 16/2
guestconfig5 32 1 rw CP0 guest register 16/5 guestconfig6 32 0 rw CP0 guest register 16/6 guestconfig7 32 80040000 rw CP0 guest register 16/7 guestlladdr 32 0 rw CP0 guest register 17/0 guestdebug 32 ffffffff rw CP0 guest register 23/0 guestdepc 32 ffffffff rw CP0 guest register 24/0 guesterrctl 32 ffffffff rw CP0 guest register 26/0 guestitaglo 32 ffffffff rw CP0 guest register 28/0 guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestdtaglo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2	guestconfig3	32	8c22bc20	rw	CP0 guest register 16/3
guestconfig6 32 0 rw CP0 guest register 16/6 guestconfig7 32 80040000 rw CP0 guest register 16/7 guestlladdr 32 0 rw CP0 guest register 17/0 guestdebug 32 ffffffff rw CP0 guest register 23/0 guestdepc 32 ffffffff rw CP0 guest register 24/0 guesterrctl 32 ffffffff rw CP0 guest register 26/0 guestitaglo 32 ffffffff rw CP0 guest register 28/0 guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestdtaglo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	guestconfig4	32	a00c0000	rw	CP0 guest register 16/4
guestconfig7 32 80040000 rw CP0 guest register 16/7 guestlladdr 32 0 rw CP0 guest register 17/0 guestdebug 32 ffffffff rw CP0 guest register 23/0 guestdepc 32 ffffffff rw CP0 guest register 24/0 guesterrctl 32 ffffffff rw CP0 guest register 26/0 guestitaglo 32 ffffffff rw CP0 guest register 28/0 guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestdtaglo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	guestconfig5	32	1	rw	CP0 guest register 16/5
guestlladdr 32 0 rw CP0 guest register 17/0 guestdebug 32 ffffffff rw CP0 guest register 23/0 guestdepc 32 ffffffff rw CP0 guest register 24/0 guesterrctl 32 ffffffff rw CP0 guest register 26/0 guestitaglo 32 ffffffff rw CP0 guest register 28/0 guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestdtaglo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	guestconfig6	32	0	rw	CP0 guest register 16/6
guestdebug 32 ffffffff rw CP0 guest register 23/0 guestdepc 32 ffffffff rw CP0 guest register 24/0 guesterrctl 32 ffffffff rw CP0 guest register 26/0 guestitaglo 32 ffffffff rw CP0 guest register 28/0 guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestdtaglo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	guestconfig7	32	80040000	rw	CP0 guest register 16/7
guestdepc 32 ffffffff rw CP0 guest register 24/0 guesterrctl 32 ffffffff rw CP0 guest register 26/0 guestitaglo 32 ffffffff rw CP0 guest register 28/0 guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestdtaglo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	guestlladdr	32	0	rw	CP0 guest register 17/0
guesterrctl 32 ffffffff rw CP0 guest register 26/0 guestitaglo 32 ffffffff rw CP0 guest register 28/0 guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestdtaglo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	guestdebug	32	fffffff	rw	CP0 guest register 23/0
guestitaglo 32 ffffffff rw CP0 guest register 28/0 guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestdtaglo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	guestdepc	32	ttttttt	rw	CP0 guest register 24/0
guestitaglo 32 ffffffff rw CP0 guest register 28/0 guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestdtaglo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	guesterrctl	32	ttttttt	rw	CP0 guest register 26/0
guestidatalo 32 ffffffff rw CP0 guest register 28/1 guestdtaglo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	guestitaglo	32	ttttttt	rw	CP0 guest register 28/0
guestdtaglo 32 ffffffff rw CP0 guest register 28/2 guestddatalo 32 ffffffff rw CP0 guest register 28/3	<u> </u>		<del> </del>	rw	
guestddatalo 32 ffffffff rw CP0 guest register 28/3	<u> </u>	1	<del> </del>	rw	
	-		ļ	-	
gassanesagas per pinnin pri por o gassi rogisto EU/T	guestl23taglo	32	fffffff	rw	CP0 guest register 28/4

guestl23datalo	32	fffffff	rw	CP0 guest register 28/5
guestitaghi	32	fffffff	rw	CP0 guest register 29/0
guestidatahi	32	ffffffff	rw	CP0 guest register 29/1
guestl23datahi	32	fffffff	rw	CP0 guest register 29/5
guesterrorepc	32	0	rw	CP0 guest register 30/0
guestdesave	32	ffffffff	rw	CP0 guest register 31/0
guestkscratch1	32	0	rw	CP0 guest register 31/2
guestkscratch2	32	0	rw	CP0 guest register 31/3

## 12.1.6 SPRAM

Table 14.

Name	Bits	Initial value (Hex)		Description
ISPRAM_INDEX	8	0	rw	
ISPRAM_ENABLE	8	0	rw	
ISPRAM_SIZE	8	0	rw	
ISPRAM_BASE	32	0	rw	
ISPRAM_OFFSET	32	0	rw	
ISPRAM_FILE	32	-	-w	
ISPRAM_READ	32	-	-w	
ISPRAM_WRITE	32	-	-w	
DSPRAM_INDEX	8	0	rw	
DSPRAM_ENABLE	8	0	rw	
DSPRAM_SIZE	8	0	rw	
DSPRAM_BASE	32	0	rw	
DSPRAM_OFFSET	32	0	rw	
DSPRAM_READ	32	-	-w	
DSPRAM_WRITE	32	-	-w	

## 12.1.7 Integration\_support

Table 15.

Name	Bits	Initial		Description
		value (Hex)		
stop	32	0	rw	write with non-zero to stop processor

#