OVP Guide to Using Processor Models

Model Specific Information for variant MIPS64_MIPS64R6

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1.0 Overview

This document provides the details of an OVP Fast Processor Model variant.
OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms. The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.
The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners.
There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

MIPS64 Configurable Processor Model
If you need other variants, these models can be obtained from www.OVPworld.org/MIPSuser.

1.2 Licensing

Usage of binary model under license governing simulator usage. Source of model available under Imperas Software License Agreement.

1.3 Limitations

If this model is not part of your installation, then it is available for download from www.OVPworld.org/MIPSuser.
This model is in beta form and is not yet fully complete.Please watch for updates on the OVP World website or contact Imperas for current status and latest version.
Cache model does not implement coherency

1.4 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

1.5 Features

MIPS64 Instruction set implemented
MMU Type: Dual VTLB and FTLB
FPU implemented
L1 I and D cache model in either full or tag-only mode implemented (disabled by default)
External interrupt controller implemented
Vectored interrupts implemented

2.0 Configuration

2.1 Location

The model source and object file is found in the VLNV tree at:
    imgtec.ovpworld.org/processor/mips64/1.0

2.2 GDB Path

The default GDB for this model is found at:
    $IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/mips-sde-elf-gdb

2.3 Semi-Host Library

The default semi-host library file is found in the VLNV tree at :
    mips.ovpworld.org/semihosting/mips64Newlib/1.0

2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

2.5 QuantumLeap Support
This processor is qualified to run in a QuantumLeap enabled simulator.

2.6 Processor ELF Code
The ELF code supported by this model is: 0x8

3.0 Other Variants in this Model

Table 1.

Variant
I6400
.I6400Guest
MIPS64R6
.MIPS64R6Guest

4.0 Bus Ports

Table 2.

Type	Name	Bits
master (initiator)	INSTRUCTION	37
master (initiator)	DATA	37

5.0 Net Ports

Table 3.

Name	Type	Description
reset	input	CMP reset
dint	input	Debug external interrupt
int0	input	GIC external interrupt
int1	input	GIC external interrupt
int2	input	GIC external interrupt
int3	input	GIC external interrupt
int4	input	GIC external interrupt
int5	input	GIC external interrupt
int6	input	GIC external interrupt
int7	input	GIC external interrupt
int8	input	GIC external interrupt
int9	input	GIC external interrupt
int10	input	GIC external interrupt
int11	input	GIC external interrupt
int12	input	GIC external interrupt
int13	input	GIC external interrupt
int14	input	GIC external interrupt
int15	input	GIC external interrupt
int16	input	GIC external interrupt
int17	input	GIC external interrupt

int18	input	GIC external interrupt
int19	input	GIC external interrupt
int20	input	GIC external interrupt
int21	input	GIC external interrupt
int22	input	GIC external interrupt
int23	input	GIC external interrupt
int24	input	GIC external interrupt
int25	input	GIC external interrupt
int26	input	GIC external interrupt
int27	input	GIC external interrupt
int28	input	GIC external interrupt
int29	input	GIC external interrupt
int30	input	GIC external interrupt
int31	input	GIC external interrupt
int32	input	GIC external interrupt
int33	input	GIC external interrupt
int34	input	GIC external interrupt
int35	input	GIC external interrupt
int36	input	GIC external interrupt
int37	input	GIC external interrupt
int38	input	GIC external interrupt
int39	input	GIC external interrupt
dint_CPU0_VC0	input	Debug external interrupt
hwint0_CPU0_VC0	input	External interrupt
hwint1_CPU0_VC0	input	External interrupt
hwint2_CPU0_VC0	input	External interrupt
hwint3_CPU0_VC0	input	External interrupt
hwint4_CPU0_VC0	input	External interrupt
hwint5_CPU0_VC0	input	External interrupt
nmi_CPU0_VC0	input	Non-maskable external interrupt
EICPresent_CPU0_VC0	input	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU0_VC0	input	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU0_VC0	input	External interrupt controller EICSS
EIC_VectorNum_CPU0_VC0	input	External interrupt controller vector number
EIC_VectorOffset_CPU0_VC0	input	External interrupt controller vector offset
EIC_GID_CPU0_VC0	input	External interrupt controller guest ID
intISS_CPU0_VC0	output	True when interrupt request is serviced
causeTI_CPU0_VC0	output	True when timer interrupt expires
causeIP0_CPU0_VC0	output	Raised for software interrupt request IP0
causeIP1_CPU0_VC0	output	Raised for software interrupt request IP1
hwint0	input	External interrupt for compatibility

Guest.EIC_RIPL_CPU0_VC0	input	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0_VC0	input	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0_VC0	input	Guest External interrupt controller vector number
Guest.EIC_VectorOffset_CPU0_VC0	input	Guest External interrupt controller vector offset
Guest.EIC_GID_CPU0_VC0	input	Guest External interrupt controller guest ID
Guest.intISS_CPU0_VC0	output	True when Guest interrupt request is serviced
Guest.causeTI_CPU0_VC0	output	True when Guest timer interrupt expires
Guest.causeIP0_CPU0_VC0	output	Raised for Guest software interrupt request IP0
Guest.causeIP1_CPU0_VC0	output	Raised for Guest software interrupt request IP1
dint_CPU0_VC1	input	Debug external interrupt
hwint0_CPU0_VC1	input	External interrupt
hwint1_CPU0_VC1	input	External interrupt
hwint2_CPU0_VC1	input	External interrupt
hwint3_CPU0_VC1	input	External interrupt
hwint4_CPU0_VC1	input	External interrupt
hwint5_CPU0_VC1	input	External interrupt
nmi_CPU0_VC1	input	Non-maskable external interrupt
EICPresent_CPU0_VC1	input	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU0_VC1	input	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU0_VC1	input	External interrupt controller EICSS
EIC_VectorNum_CPU0_VC1	input	External interrupt controller vector number
EIC_VectorOffset_CPU0_VC1	input	External interrupt controller vector offset
EIC_GID_CPU0_VC1	input	External interrupt controller guest ID
intISS_CPU0_VC1	output	True when interrupt request is serviced
causeTI_CPU0_VC1	output	True when timer interrupt expires
causeIP0_CPU0_VC1	output	Raised for software interrupt request IP0
causeIP1_CPU0_VC1	output	Raised for software interrupt request IP1
Guest.EIC_RIPL_CPU0_VC1	input	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0_VC1	input	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0_VC1	input	Guest External interrupt controller vector number
Guest.EIC_VectorOffset_CPU0_VC1	input	Guest External interrupt controller vector offset
Guest.EIC_GID_CPU0_VC1	input	Guest External interrupt controller guest ID
Guest.intISS_CPU0_VC1	output	True when Guest interrupt request is serviced
Guest.causeTI_CPU0_VC1	output	True when Guest timer interrupt expires
Guest.causeIP0_CPU0_VC1	output	Raised for Guest software interrupt request IP0
Guest.causeIP1_CPU0_VC1	output	Raised for Guest software interrupt request IP1
dint_CPU0_VC2	input	Debug external interrupt
hwint0_CPU0_VC2	input	External interrupt
hwint1_CPU0_VC2	input	External interrupt
hwint2_CPU0_VC2	input	External interrupt
hwint3_CPU0_VC2	input	External interrupt

hwint4_CPU0_VC2	input	External interrupt
hwint5_CPU0_VC2	input	External interrupt
nmi_CPU0_VC2	input	Non-maskable external interrupt
EICPresent_CPU0_VC2	input	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU0_VC2	input	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU0_VC2	input	External interrupt controller EICSS
EIC_VectorNum_CPU0_VC2	input	External interrupt controller vector number
EIC_VectorOffset_CPU0_VC2	input	External interrupt controller vector offset
EIC_GID_CPU0_VC2	input	External interrupt controller guest ID
intISS_CPU0_VC2	output	True when interrupt request is serviced
causeTI_CPU0_VC2	output	True when timer interrupt expires
causeIP0_CPU0_VC2	output	Raised for software interrupt request IP0
causeIP1_CPU0_VC2	output	Raised for software interrupt request IP1
Guest.EIC_RIPL_CPU0_VC2	input	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0_VC2	input	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0_VC2	input	Guest External interrupt controller vector number
Guest.EIC_VectorOffset_CPU0_VC2	input	Guest External interrupt controller vector offset
Guest.EIC_GID_CPU0_VC2	input	Guest External interrupt controller guest ID
Guest.intISS_CPU0_VC2	output	True when Guest interrupt request is serviced
Guest.causeTI_CPU0_VC2	output	True when Guest timer interrupt expires
Guest.causeIP0_CPU0_VC2	output	Raised for Guest software interrupt request IP0
Guest.causeIP1_CPU0_VC2	output	Raised for Guest software interrupt request IP1
dint_CPU0_VC3	input	Debug external interrupt
hwint0_CPU0_VC3	input	External interrupt
hwint1_CPU0_VC3	input	External interrupt
hwint2_CPU0_VC3	input	External interrupt
hwint3_CPU0_VC3	input	External interrupt
hwint4_CPU0_VC3	input	External interrupt
hwint5_CPU0_VC3	input	External interrupt
nmi_CPU0_VC3	input	Non-maskable external interrupt
EICPresent_CPU0_VC3	input	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU0_VC3	input	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU0_VC3	input	External interrupt controller EICSS
EIC_VectorNum_CPU0_VC3	input	External interrupt controller vector number
EIC_VectorOffset_CPU0_VC3	input	External interrupt controller vector offset
EIC_GID_CPU0_VC3	input	External interrupt controller guest ID
intISS_CPU0_VC3	output	True when interrupt request is serviced
causeTI_CPU0_VC3	output	True when timer interrupt expires
causeIP0_CPU0_VC3	output	Raised for software interrupt request IP0
causeIP1_CPU0_VC3	output	Raised for software interrupt request IP1

Guest.EIC_RIPL_CPU0_VC3	input	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0_VC3	input	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0_VC3	input	Guest External interrupt controller vector number
Guest.EIC_VectorOffset_CPU0_VC3	input	Guest External interrupt controller vector offset
Guest.EIC_GID_CPU0_VC3	input	Guest External interrupt controller guest ID
Guest.intISS_CPU0_VC3	output	True when Guest interrupt request is serviced
Guest.causeTI_CPU0_VC3	output	True when Guest timer interrupt expires
Guest.causeIP0_CPU0_VC3	output	Raised for Guest software interrupt request IP0
Guest.causeIP1_CPU0_VC3	output	Raised for Guest software interrupt request IP1
dint_CPU1_VC0	input	Debug external interrupt
hwint0_CPU1_VC0	input	External interrupt
hwint1_CPU1_VC0	input	External interrupt
hwint2_CPU1_VC0	input	External interrupt
hwint3_CPU1_VC0	input	External interrupt
hwint4_CPU1_VC0	input	External interrupt
hwint5_CPU1_VC0	input	External interrupt
nmi_CPU1_VC0	input	Non-maskable external interrupt
EICPresent_CPU1_VC0	input	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU1_VC0	input	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU1_VC0	input	External interrupt controller EICSS
EIC_VectorNum_CPU1_VC0	input	External interrupt controller vector number
EIC_VectorOffset_CPU1_VC0	input	External interrupt controller vector offset
EIC_GID_CPU1_VC0	input	External interrupt controller guest ID
intISS_CPU1_VC0	output	True when interrupt request is serviced
causeTI_CPU1_VC0	output	True when timer interrupt expires
causeIP0_CPU1_VC0	output	Raised for software interrupt request IP0
causeIP1_CPU1_VC0	output	Raised for software interrupt request IP1
Guest.EIC_RIPL_CPU1_VC0	input	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1_VC0	input	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU1_VC0	input	Guest External interrupt controller vector number
Guest.EIC_VectorOffset_CPU1_VC0	input	Guest External interrupt controller vector offset
Guest.EIC_GID_CPU1_VC0	input	Guest External interrupt controller guest ID
Guest.intISS_CPU1_VC0	output	True when Guest interrupt request is serviced
Guest.causeTI_CPU1_VC0	output	True when Guest timer interrupt expires
Guest.causeIP0_CPU1_VC0	output	Raised for Guest software interrupt request IP0
Guest.causeIP1_CPU1_VC0	output	Raised for Guest software interrupt request IP1
dint_CPU1_VC1	input	Debug external interrupt
hwint0_CPU1_VC1	input	External interrupt
hwint1_CPU1_VC1	input	External interrupt
hwint2_CPU1_VC1	input	External interrupt
hwint3_CPU1_VC1	input	External interrupt

hwint4_CPU1_VC1	input	External interrupt
hwint5_CPU1_VC1	input	External interrupt
nmi_CPU1_VC1	input	Non-maskable external interrupt
EICPresent_CPU1_VC1	input	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU1_VC1	input	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU1_VC1	input	External interrupt controller EICSS
EIC_VectorNum_CPU1_VC1	input	External interrupt controller vector number
EIC_VectorOffset_CPU1_VC1	input	External interrupt controller vector offset
EIC_GID_CPU1_VC1	input	External interrupt controller guest ID
intISS_CPU1_VC1	output	True when interrupt request is serviced
causeTI_CPU1_VC1	output	True when timer interrupt expires
causeIP0_CPU1_VC1	output	Raised for software interrupt request IP0
causeIP1_CPU1_VC1	output	Raised for software interrupt request IP1
Guest.EIC_RIPL_CPU1_VC1	input	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1_VC1	input	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU1_VC1	input	Guest External interrupt controller vector number
Guest.EIC_VectorOffset_CPU1_VC1	input	Guest External interrupt controller vector offset
Guest.EIC_GID_CPU1_VC1	input	Guest External interrupt controller guest ID
Guest.intISS_CPU1_VC1	output	True when Guest interrupt request is serviced
Guest.causeTI_CPU1_VC1	output	True when Guest timer interrupt expires
Guest.causeIP0_CPU1_VC1	output	Raised for Guest software interrupt request IP0
Guest.causeIP1_CPU1_VC1	output	Raised for Guest software interrupt request IP1
dint_CPU1_VC2	input	Debug external interrupt
hwint0_CPU1_VC2	input	External interrupt
hwint1_CPU1_VC2	input	External interrupt
hwint2_CPU1_VC2	input	External interrupt
hwint3_CPU1_VC2	input	External interrupt
hwint4_CPU1_VC2	input	External interrupt
hwint5_CPU1_VC2	input	External interrupt
nmi_CPU1_VC2	input	Non-maskable external interrupt
EICPresent_CPU1_VC2	input	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU1_VC2	input	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU1_VC2	input	External interrupt controller EICSS
EIC_VectorNum_CPU1_VC2	input	External interrupt controller vector number
EIC_VectorOffset_CPU1_VC2	input	External interrupt controller vector offset
EIC_GID_CPU1_VC2	input	External interrupt controller guest ID
intISS_CPU1_VC2	output	True when interrupt request is serviced
causeTI_CPU1_VC2	output	True when timer interrupt expires
causeIP0_CPU1_VC2	output	Raised for software interrupt request IP0
causeIP1_CPU1_VC2	output	Raised for software interrupt request IP1

Guest.EIC_RIPL_CPU1_VC2	input	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1_VC2	input	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU1_VC2	input	Guest External interrupt controller vector number
Guest.EIC_VectorOffset_CPU1_VC2	input	Guest External interrupt controller vector offset
Guest.EIC_GID_CPU1_VC2	input	Guest External interrupt controller guest ID
Guest.intISS_CPU1_VC2	output	True when Guest interrupt request is serviced
Guest.causeTI_CPU1_VC2	output	True when Guest timer interrupt expires
Guest.causeIP0_CPU1_VC2	output	Raised for Guest software interrupt request IP0
Guest.causeIP1_CPU1_VC2	output	Raised for Guest software interrupt request IP1
dint_CPU1_VC3	input	Debug external interrupt
hwint0_CPU1_VC3	input	External interrupt
hwint1_CPU1_VC3	input	External interrupt
hwint2_CPU1_VC3	input	External interrupt
hwint3_CPU1_VC3	input	External interrupt
hwint4_CPU1_VC3	input	External interrupt
hwint5_CPU1_VC3	input	External interrupt
nmi_CPU1_VC3	input	Non-maskable external interrupt
EICPresent_CPU1_VC3	input	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU1_VC3	input	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU1_VC3	input	External interrupt controller EICSS
EIC_VectorNum_CPU1_VC3	input	External interrupt controller vector number
EIC_VectorOffset_CPU1_VC3	input	External interrupt controller vector offset
EIC_GID_CPU1_VC3	input	External interrupt controller guest ID
intISS_CPU1_VC3	output	True when interrupt request is serviced
causeTI_CPU1_VC3	output	True when timer interrupt expires
causeIP0_CPU1_VC3	output	Raised for software interrupt request IP0
causeIP1_CPU1_VC3	output	Raised for software interrupt request IP1
Guest.EIC_RIPL_CPU1_VC3	input	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1_VC3	input	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU1_VC3	input	Guest External interrupt controller vector number
Guest.EIC_VectorOffset_CPU1_VC3	input	Guest External interrupt controller vector offset
Guest.EIC_GID_CPU1_VC3	input	Guest External interrupt controller guest ID
Guest.intISS_CPU1_VC3	output	True when Guest interrupt request is serviced
Guest.causeTI_CPU1_VC3	output	True when Guest timer interrupt expires
Guest.causeIP0_CPU1_VC3	output	Raised for Guest software interrupt request IP0
Guest.causeIP1_CPU1_VC3	output	Raised for Guest software interrupt request IP1

6.0 FIFO Ports

No FIFO Ports in this model.

7.0 Parameters

Table 4.

Name	Type	Description
cacheenable	Enumeration	Select cache model mode default=0 tag=1 full=2
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info structure
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
supervisorMode	Boolean	Override whether processor implements supervisor mode
busErrors	Boolean	Override bus error exception behavior. When true, accesses of memory not defined by platform will cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when true (sets Config.MT=3, Config.KU/K23=2 and Config1.MMUSizeM1=0)
removeDSP	Boolean	Override the DSP-present configuration when true (sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true (sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true (sets Config1.FP to 0)
removeFTLB	Boolean	Override the FTLBEn configuration when true (disable FTLB)
isISA	Boolean	Enable to specify ISA model (reset address from ELF, all coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to maximum value to improve performance
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores only)
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC implementation (MT cores only)
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior)
supportDenormals	Boolean	Enable to specify that the FPU supports denormal operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0
segBits	Uns32	Override the number of address bits implemented for 64 bit segments (MIPS64 Only)

mpuRegions	Uns32	Number of regions for memory protection unit
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
MIPS_UHI	Boolean	Enable MIPS-Unified Hosting interface
mipsUhiArgs	String	Specifies UHI arguments string seperated by spaces
mipsUhiJail	String	Specifies UHI jailroot
MIPS_DV_MODE	Boolean	Enable Design Verification mode
MIPS_MAGIC_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes
enableTrickbox	Boolean	Enable trickbox addresses (specific for AVP)
fpuexcdisable	Boolean	Disable FPU exceptions
cop2Bits	Uns32	Specifies width in bits of COP2 registers (32 or 64)
cop2FileName	String	Specifies COP2 dynamically-loaded object (.so/.dll) defining COP2 instructions
udiConfig	Int32	Specifies UDI configuration attribute
udiFileName	String	Specifies UDI dynamically-loaded object (.so/.dll) defining UDI instructions
vectoredinterrupt	Boolean	Enables vectored interrupts (sets Config3 VInt)
externalinterrupt	Boolean	Enables the use of an external interrupt controller (sets Config3 VEIC)
rootFixedMMU	Boolean	Override the root MMU type to fixed mapping when true (sets Config.MT=3 and Config.KU/K23=2)
rootMMUSizeM1	Uns32	Override the root MMUSizeM1 field in Config1 register (number of MMU entries-1)
srsctlHSS	Uns32	Override the HSS field in SRSCtl register (number of shadow register sets)
firPS	Uns32	Override the PS field in FIR register
firHas2008	Uns32	Override the Has2008 field in FIR register
pridCompanyOptions	Uns32	Override the Company Options field in PRId register
pridRevision	Uns32	Override the Revision field in PRId register
intctlIPTI	Uns32	Override the IPTI field in IntCtl register
intctlIPFDC	Uns32	Override the IPFDC field in IntCtl register
intctlIPPCI	Uns32	Override the IPPCI field in IntCtl register
numWatch	Uns32	Specify number of WatchLo/WatchHi register pairs
numVC	Uns32	Specify number of Virtual Cores to be present
numVCtoStart	Uns32	Specify number of Virtual Cores to be running

sharedTLBindex	Uns32	Specify first shared TLB Index between Virtual Cores
hasFDC	Boolean	Specify Fast Debug Channel (dummy implementation)
intctlIPTI_CPU0_VC0	Uns32	Override the IPTI field in IntCtl register for CPU0/VC0
intctlIPTI_CPU0_VC1	Uns32	Override the IPTI field in IntCtl register for CPU0/VC1
intctlIPTI_CPU0_VC2	Uns32	Override the IPTI field in IntCtl register for CPU0/VC2
intctlIPTI_CPU0_VC3	Uns32	Override the IPTI field in IntCtl register for CPU0/VC3
intctlIPTI_CPU1_VC0	Uns32	Override the IPTI field in IntCtl register for CPU1/VC0
intctlIPTI_CPU1_VC1	Uns32	Override the IPTI field in IntCtl register for CPU1/VC1
intctlIPTI_CPU1_VC2	Uns32	Override the IPTI field in IntCtl register for CPU1/VC2
intctlIPTI_CPU1_VC3	Uns32	Override the IPTI field in IntCtl register for CPU1/VC3
intctlIPTI_CPU2_VC0	Uns32	Override the IPTI field in IntCtl register for CPU2/VC0
intctlIPTI_CPU2_VC1	Uns32	Override the IPTI field in IntCtl register for CPU2/VC1
intctlIPTI_CPU2_VC2	Uns32	Override the IPTI field in IntCtl register for CPU2/VC2
intctlIPTI_CPU2_VC3	Uns32	Override the IPTI field in IntCtl register for CPU2/VC3
intctlIPTI_CPU3_VC0	Uns32	Override the IPTI field in IntCtl register for CPU3/VC0
intctlIPTI_CPU3_VC1	Uns32	Override the IPTI field in IntCtl register for CPU3/VC1
intctlIPTI_CPU3_VC2	Uns32	Override the IPTI field in IntCtl register for CPU3/VC2
intctlIPTI_CPU3_VC3	Uns32	Override the IPTI field in IntCtl register for CPU3/VC3
intctlIPFDC_CPU0_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC0
intctlIPFDC_CPU0_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC1
intctlIPFDC_CPU0_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC2
intctlIPFDC_CPU0_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC3
intctlIPFDC_CPU1_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC0

intctlIPFDC_CPU1_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC1
intctlIPFDC_CPU1_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC2
intctlIPFDC_CPU1_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC3
intctlIPFDC_CPU2_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC0
intctlIPFDC_CPU2_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC1
intctlIPFDC_CPU2_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC2
intctlIPFDC_CPU2_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC3
intctlIPFDC_CPU3_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC0
intctlIPFDC_CPU3_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC1
intctlIPFDC_CPU3_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC2
intctlIPFDC_CPU3_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC3
intctlIPPCI_CPU0_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC0
intctlIPPCI_CPU0_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC1
intctlIPPCI_CPU0_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC2
intctlIPPCI_CPU0_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC3
intctlIPPCI_CPU1_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC0
intctlIPPCI_CPU1_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC1
intctlIPPCI_CPU1_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC2
intctlIPPCI_CPU1_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC3
intctlIPPCI_CPU2_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC0
intctlIPPCI_CPU2_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC1
intctlIPPCI_CPU2_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC2
intctlIPPCI_CPU2_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC3

intctlIPPCI_CPU3_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC0
intctlIPPCI_CPU3_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC1
intctlIPPCI_CPU3_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC2
intctlIPPCI_CPU3_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC3
configAR	Uns32	Enables R6 support
configBM	Uns32	Override the BM field in Config register (burst mode)
configDSP	Boolean	Override Config.DSP (data scratchpad RAM present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0 cacheability)
configKU	Uns32	Override power on value of Config.KU (set Useg cacheability)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23 cacheability)
configMDU	Boolean	Override Config.MDU (iterative multiply/divide unit)
configMM	Boolean	Override Config.MM (merging mode for write)
configMT	Uns32	Override Config.MT
configSB	Boolean	Override Config.SB (simple bus transfers only)
MIPS16eASE	Boolean	Override Config1.CA (enables the MIPS16e ASE)
config1DA	Uns32	Override Config1.DA (Dcache associativity)
config1DL	Uns32	Override Config1.DL (Dcache line size)
config1DS	Uns32	Override Config1.DS (Dcache sets per way)
config1EP	Boolean	Override Config1.EP (EJTag present)
config1IA	Uns32	Override Config1.IA (Icache associativity)
config1IL	Uns32	Override Config1.IL (Icache line size)
config1IS	Uns32	Override Config1.IS (Icache sets per way)
config1MMUSizeM1	Uns32	Override Config1.MMUSizeM1 (number of MMU entries-1)
config1WR	Boolean	Override Config1.WR (watchpoint registers present)
config2SU	Uns32	Override the SU field in Config2 register
config2SS	Uns32	Override the SS field in Config2 register
config2SL	Uns32	Override the SL field in Config2 register
config2SA	Uns32	Override the SA field in Config2 register
config3BI	Boolean	Override Config3.BI

config3BP	Boolean	Override Config3.BP
config3CDMM	Boolean	Override Config3.CDMM
config3CTXTC	Boolean	Override Config3.CTXTC
config3DSPP	Boolean	Override Config3.DSPP
config3DSP2P	Boolean	Override Config3.DSP2P
config3IPLW	Uns32	Override Config3.IPLW
config3ISA	Uns32	Override Config3.ISA
config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3LPA	Boolean	Override Config3.LPA
config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
config3SC	Boolean	Override Config3.SC
config3ULRI	Boolean	Override Config3.ULRI
config3VZ	Boolean	Override Config3.VZ
config3MSAP	Boolean	Override Config3.MSAP
config3CMGCR	Boolean	Override the CMGCR field in Config3 register
config3SP	Boolean	Override the SP field in Config3 register
config3TL	Uns32	Override the TL field in Config3 register
config3PW	Boolean	Override the PW field in Config3 register
config4AE	Boolean	Override Config4.AE
config4IE	Uns32	Override Config4.IE
config4MMUConfig	Uns32	Override Config4.MMUConfig field (interpretation depends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.VTLBSizeExt
config5EVA	Boolean	Override Config5.EVA
config5LLB	Boolean	Override Config5.LLB (LLAddr supports LLbit)
config5MRP	Boolean	Override Config5.MRP (MaaR Present)
config5NFExists	Boolean	Override Config5.NFExists
config5MSAEn	Boolean	Override Config5.MSAEn
config5MVH	Boolean	Override Config5.MVH (enable MTHC0 and MFHC0 instructions)
config6FTLBEn	Boolean	Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE
config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initialization)
config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)

config7ES	Uns32	Override the ES field in Config7 register (Externalize sync)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant with IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/ SNaN encodings match IEEE 754-2008 recommendation)
numMaarRegs	Uns32	Override number of MAAR registers (must be even)
wiredLimit	Uns32	Override Limit field of the Wired register
cdmmBaseCI	Boolean	Override CDMMBase.CI
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the corresponding BEV address bits
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable within cluster
GCR_PCORES	Uns32	CMP system only: override GCR_CONFIG.PCORES (number of cores-1)
GCR_BASE	Uns64	CMP system only: override GCR_BASE.GCR_BASE (default GCR register address)
GCR_MINOR_REV	Uns32	CMP system only: override GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MAJOR_REV
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MAJOR_REV
GCR_BEV_BASE	Uns32	CMP system only: override GCR_BEV_BASE
GIC_NUMINTERRUPTS	Uns32	CMP system only: override GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV

GIC_MAJOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MAJOR_REV
GIC_NUM_TEAMS	Uns32	CMP system only: override GIC_SH_DBG_CONFIG.NUM_TEAMS
GIC_TRIG_RESET	Uns32	CMP system only: Zero value of GIC_SH_TRIG_[31_0, 63_32]
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPE
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override CPC_REVISION.MAJOR_REV
GIC_SH_GID_CONFIG31_0	Uns32	CMP system only: override GIC_SH_GID_CONFIG[31_0]
GIC_SH_GID_CONFIG63_32	Uns32	CMP system only: override GIC_SH_GID_CONFIG[63_32]
GIC_SH_GID_CONFIG95_64	Uns32	CMP system only: override GIC_SH_GID_CONFIG[95_64]
GIC_SH_GID_CONFIG127_96	Uns32	CMP system only: override GIC_SH_GID_CONFIG[127_96]
GIC_SH_GID_CONFIG159_128	Uns32	CMP system only: override GIC_SH_GID_CONFIG[159_128]
GIC_SH_GID_CONFIG191_160	Uns32	CMP system only: override GIC_SH_GID_CONFIG[191_160]
GIC_SH_GID_CONFIG223_192	Uns32	CMP system only: override GIC_SH_GID_CONFIG[223_192]
GIC_SH_GID_CONFIG255_224	Uns32	CMP system only: override GIC_SH_GID_CONFIG[255_224]
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 0
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 1

GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 2
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 3
GCR_C0_V0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core0/vc0
GCR_C0_V1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core0/vc1
GCR_C0_V2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core0/vc2
GCR_C0_V3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core0/vc3
GCR_C1_V0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core1/vc0
GCR_C1_V1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core1/vc1
GCR_C1_V2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core1/vc2
GCR_C1_V3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core1/vc3
GCR_C2_V0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core2/vc0
GCR_C2_V1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core2/vc1
GCR_C2_V2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core2/vc2
GCR_C2_V3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core2/vc3
GCR_C3_V0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core3/vc0
GCR_C3_V1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core3/vc1
GCR_C3_V2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core3/vc2
GCR_C3_V3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core3/vc3
CPC_C0_VC_EN	Uns32	CMP system only: CPC_VC_EN for core 0
CPC_C1_VC_EN	Uns32	CMP system only: CPC_VC_EN for core 1
CPC_C2_VC_EN	Uns32	CMP system only: CPC_VC_EN for core 2
CPC_C3_VC_EN	Uns32	CMP system only: CPC_VC_EN for core 3
EIC_OPTION	Uns32	Override the external interrupt controller EIC_OPTION
guestVariant	Enumeration	Guest processor variant (same as Root if not specified) I6400=0 .I6400Guest=1 MIPS64R6=2 .MIPS64R6Guest=3
guestCtl0RI	Uns32	Override the RI field in GuestCtl0 register

guestCtl0MC	Uns32	Override the MC field in GuestCtl0 register
guestCtl0CP0	Uns32	Override the CP0 field in GuestCtl0 register
guestCtl0AT	Uns32	Override the AT field in GuestCtl0 register
guestCtl0GT	Uns32	Override the GT field in GuestCtl0 register
guestCtl0CG	Uns32	Override the CG field in GuestCtl0 register
guestCtl0CF	Uns32	Override the CF field in GuestCtl0 register
guestCtl0G1	Uns32	Override the G1 field in GuestCtl0 register
guestCtl0RAD	Uns32	Override the RAD field in GuestCtl0 register
guestCtl0DRG	Uns32	Override the DRG field in GuestCtl0 register
hasImpl17	Boolean	Enable read/write of Impl17 bit in Status register
hasImpl16	Boolean	Enable read/write of Impl16 bit in Status register
guestintctlIPTI	Uns32	Override the Guest IPTI field in IntCtl register
guestintctlIPFDC	Uns32	Override the Guest IPFDC field in IntCtl register
guestintctlIPPCI	Uns32	Override the Guest IPPCI field in IntCtl register
guestintctlIPTI_CPU0_VC0	Uns32	Override the IPTI field in IntCtl register for CPU0/VC0
guestintctlIPTI_CPU0_VC1	Uns32	Override the IPTI field in IntCtl register for CPU0/VC1
guestintctlIPTI_CPU0_VC2	Uns32	Override the IPTI field in IntCtl register for CPU0/VC2
guestintctlIPTI_CPU0_VC3	Uns32	Override the IPTI field in IntCtl register for CPU0/VC3
guestintctlIPTI_CPU1_VC0	Uns32	Override the IPTI field in IntCtl register for CPU1/VC0
guestintctlIPTI_CPU1_VC1	Uns32	Override the IPTI field in IntCtl register for CPU1/VC1
guestintctlIPTI_CPU1_VC2	Uns32	Override the IPTI field in IntCtl register for CPU1/VC2
guestintctlIPTI_CPU1_VC3	Uns32	Override the IPTI field in IntCtl register for CPU1/VC3
guestintctlIPTI_CPU2_VC0	Uns32	Override the IPTI field in IntCtl register for CPU2/VC0
guestintctlIPTI_CPU2_VC1	Uns32	Override the IPTI field in IntCtl register for CPU2/VC1
guestintctlIPTI_CPU2_VC2	Uns32	Override the IPTI field in IntCtl register for CPU2/VC2
guestintctlIPTI_CPU2_VC3	Uns32	Override the IPTI field in IntCtl register for CPU2/VC3
guestintctlIPTI_CPU3_VC0	Uns32	Override the IPTI field in IntCtl register for CPU3/VC0
guestintctlIPTI_CPU3_VC1	Uns32	Override the IPTI field in IntCtl register for CPU3/VC1

guestintctlIPTI_CPU3_VC2	Uns32	Override the IPTI field in IntCtl register for CPU3/VC2
guestintctlIPTI_CPU3_VC3	Uns32	Override the IPTI field in IntCtl register for CPU3/VC3
guestintctlIPFDC_CPU0_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC0
guestintctlIPFDC_CPU0_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC1
guestintctlIPFDC_CPU0_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC2
guestintctlIPFDC_CPU0_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC3
guestintctlIPFDC_CPU1_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC0
guestintctlIPFDC_CPU1_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC1
guestintctlIPFDC_CPU1_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC2
guestintctlIPFDC_CPU1_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC3
guestintctlIPFDC_CPU2_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC0
guestintctlIPFDC_CPU2_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC1
guestintctlIPFDC_CPU2_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC2
guestintctlIPFDC_CPU2_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC3
guestintctlIPFDC_CPU3_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC0
guestintctlIPFDC_CPU3_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC1
guestintctlIPFDC_CPU3_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC2
guestintctlIPFDC_CPU3_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC3
guestintctlIPPCI_CPU0_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC0
guestintctlIPPCI_CPU0_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC1
guestintctlIPPCI_CPU0_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC2
guestintctlIPPCI_CPU0_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC3
guestintctlIPPCI_CPU1_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC0

guestintctlIPPCI_CPU1_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC1
guestintctlIPPCI_CPU1_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC2
guestintctlIPPCI_CPU1_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC3
guestintctlIPPCI_CPU2_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC0
guestintctlIPPCI_CPU2_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC1
guestintctlIPPCI_CPU2_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC2
guestintctlIPPCI_CPU2_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC3
guestintctlIPPCI_CPU3_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC0
guestintctlIPPCI_CPU3_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC1
guestintctlIPPCI_CPU3_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC2
guestintctlIPPCI_CPU3_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC3

8.0 Execution Modes

Table 5.

Name	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3
GUEST_KERNEL	4
GUEST_SUPERVISOR	5
GUEST_USER	6

9.0 Exceptions

Table 6.

Name	Code
Int	0
Mod	1
TLBL	2
TLBS	3

AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Bp	9
RI	10
CpU	11
Ov	12
Tr	13
MSAFPE	14
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MSADis	21
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
GE	27
Prot	29
CacheErr	30

10.0 Hierarchy of the model

A CPU core may allow the user to configure it to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.
OVP processor models can be written to include SMP blocks and to have many levels of hierarchy.

Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

10.1 Level 1: CMP

This level in the model hierarchy has 2 commands.

This level in the model hierarchy has no register groups.

This level in the model hierarchy has 2 children:

PU0 and PU1

10.2 Level 2: CPU

This level in the model hierarchy has 2 commands.

This level in the model hierarchy has no register groups.

This level in the model hierarchy has 4 children:

PU0_VC0, PU0_VC1, PU0_VC2 and PU0_VC3

10.3 Level 3: VC

This level in the model hierarchy has 20 commands.

This level in the model hierarchy has 10 register groups:

Table 7.

Group name	Registers
Core	33
FPU	34
DSP	9
Shadow	32
COP0	170
MSA	40
CMP_GCR	28
CMP_CPC	14
CMP_GIC	594

Integration_support	1

This level in the model hierarchy has no children.

11.0 Model Commands

11.1 Level 1: CMP

Table 8.

Name	Arguments
isync	specify instruction address range for synchronous execution
itrace	enable or disable instruction tracing

11.2 Level 2: CPU

Table 9.

Name	Arguments
isync	specify instruction address range for synchronous execution
itrace	enable or disable instruction tracing

11.3 Level 3: VC

Table 10.

Name	Arguments
isync	specify instruction address range for synchronous execution
itrace	enable or disable instruction tracing
mipsCOP0	<register> <select>
mipsCacheDisable	
mipsCacheEnable	-tag|-full
mipsCacheRatio	-icache|-dcache
mipsCacheReport	
mipsCacheReset	
mipsCacheTrace	-on|-off [-nocached|-nouncached] [-noicache|-nodcache] [-noartifact|-notrue]
mipsDebugFlags	<value>
mipsReadRegister	<resource> <offset>
mipsReadTLBEntry	<index>
mipsTLBDump	
mipsTLBDumpGuest	
mipsTLBDumpRoot	
mipsTLBGetPhys	<virtual address> <ASID>
mipsTraceGuest	<bool>
mipsTraceRoot	<bool>
mipsWriteRegister	<resource> <offset> <value>
mipsWriteTLBEntry	<index> <lo0> <lo1> <hi0> <mask>

12.0 Registers

12.1 Level 1: CMP

No registers.

12.2 Level 2: CPU

No registers.

12.3 Level 3: VC

12.3.1 Core

Table 11.

Name	Bits	Initial value (Hex)		Description
zero	64	0	r-	constant zero
at	64	0	rw	
v0	64	0	rw	
v1	64	0	rw	
a0	64	0	rw	
a1	64	0	rw	
a2	64	0	rw	
a3	64	0	rw	
t0	64	0	rw	
t1	64	0	rw	
t2	64	0	rw	
t3	64	0	rw	
t4	64	0	rw	
t5	64	0	rw	
t6	64	0	rw	
t7	64	0	rw	
s0	64	0	rw	
s1	64	0	rw	
s2	64	0	rw	
s3	64	0	rw	
s4	64	0	rw	
s5	64	0	rw	
s6	64	0	rw	
s7	64	0	rw	
t8	64	0	rw	
t9	64	0	rw	
k0	64	0	rw	
k1	64	0	rw	
gp	64	0	rw	
sp	64	0	rw	stack pointer
s8	64	0	rw	frame pointer
ra	64	0	rw	
pc	64	ffffffffbfc00000	rw	program counter

12.3.2 FPU

Table 12.

Name	Bits	Initial value (Hex)		Description

f0	64	0	rw	
f1	64	0	rw	
f2	64	0	rw	
f3	64	0	rw	
f4	64	0	rw	
f5	64	0	rw	
f6	64	0	rw	
f7	64	0	rw	
f8	64	0	rw	
f9	64	0	rw	
f10	64	0	rw	
f11	64	0	rw	
f12	64	0	rw	
f13	64	0	rw	
f14	64	0	rw	
f15	64	0	rw	
f16	64	0	rw	
f17	64	0	rw	
f18	64	0	rw	
f19	64	0	rw	
f20	64	0	rw	
f21	64	0	rw	
f22	64	0	rw	
f23	64	0	rw	
f24	64	0	rw	
f25	64	0	rw	
f26	64	0	rw	
f27	64	0	rw	
f28	64	0	rw	
f29	64	0	rw	
f30	64	0	rw	
f31	64	0	rw	
fsr	64	c0000	rw	floating point status
fir	64	20f30320	r-	floating point information

12.3.3 DSP

Table 13.

Name	Bits	Initial value (Hex)		Description
lo	64	0	rw	
hi	64	0	rw	
lo1	64	0	rw	
hi1	64	0	rw	

lo2	64	0	rw	
hi2	64	0	rw	
lo3	64	0	rw	
hi3	64	0	rw	
dspctl	64	0	rw	DSP control

12.3.4 Shadow

Table 14.

Name	Bits	Initial value (Hex)		Description
zero[0]	64	0	r-	constant zero
at[0]	64	0	rw	
v0[0]	64	0	rw	
v1[0]	64	0	rw	
a0[0]	64	0	rw	
a1[0]	64	0	rw	
a2[0]	64	0	rw	
a3[0]	64	0	rw	
t0[0]	64	0	rw	
t1[0]	64	0	rw	
t2[0]	64	0	rw	
t3[0]	64	0	rw	
t4[0]	64	0	rw	
t5[0]	64	0	rw	
t6[0]	64	0	rw	
t7[0]	64	0	rw	
s0[0]	64	0	rw	
s1[0]	64	0	rw	
s2[0]	64	0	rw	
s3[0]	64	0	rw	
s4[0]	64	0	rw	
s5[0]	64	0	rw	
s6[0]	64	0	rw	
s7[0]	64	0	rw	
t8[0]	64	0	rw	
t9[0]	64	0	rw	
k0[0]	64	0	rw	
k1[0]	64	0	rw	
gp[0]	64	0	rw	
sp[0]	64	0	rw	stack pointer
s8[0]	64	0	rw	frame pointer
ra[0]	64	0	rw	

12.3.5 COP0

Table 15.

Name	Bits	Initial value (Hex)		Description
sr	64	4400004	rw	CP0 register 12/0
bad	64	0	rw	CP0 register 8/0
cause	64	0	rw	CP0 register 13/0
index	64	0	rw	CP0 register 0/0
vpcontrol	64	0	rw	CP0 register 0/4
random	64	0	rw	CP0 register 1/0
entrylo0	64	0	rw	CP0 register 2/0
entrylo1	64	0	rw	CP0 register 3/0
globalnumber	64	0	rw	CP0 register 3/1
context	64	0	rw	CP0 register 4/0
contextconfig	64	7ffff0	rw	CP0 register 4/1
userlocal	64	0	rw	CP0 register 4/2
xcontextconfig	64	7fffffff0	rw	CP0 register 4/3
pagemask	64	6000	rw	CP0 register 5/0
pagegrain	64	c8000000	rw	CP0 register 5/1
wired	64	0	rw	CP0 register 6/0
hwrena	64	0	rw	CP0 register 7/0
badvaddr	64	0	rw	CP0 register 8/0
badinstr	64	0	rw	CP0 register 8/1
badinstrp	64	0	rw	CP0 register 8/2
count	64	0	rw	CP0 register 9/0
entryhi	64	0	rw	CP0 register 10/0
guestctl1	64	0	rw	CP0 register 10/4
guestctl2	64	0	rw	CP0 register 10/5
guestctl3	64	0	rw	CP0 register 10/6
compare	64	0	rw	CP0 register 11/0
guestctl0ext	64	40	rw	CP0 register 11/4
status	64	4400004	rw	CP0 register 12/0
intctl	64	0	rw	CP0 register 12/1
srsctl	64	0	rw	CP0 register 12/2
srsmap	64	0	rw	CP0 register 12/3
guestctl0	64	c4c00fc	rw	CP0 register 12/6
gtoffset	64	0	rw	CP0 register 12/7
epc	64	0	rw	CP0 register 14/0
prid	64	1ac00	rw	CP0 register 15/0
ebase	64	ffffffff80000000	rw	CP0 register 15/1
cmgcrbase	64	1fbf800	rw	CP0 register 15/3
bevva	64	0	rw	CP0 register 15/4
config	64	8000ca02	rw	CP0 register 16/0

config1	64	9eab559b	rw	CP0 register 16/1
config2	64	80000000	rw	CP0 register 16/2
config3	64	fc8033e1	rw	CP0 register 16/3
config4	64	d0fc0227	rw	CP0 register 16/4
config5	64	98	rw	CP0 register 16/5
config6	64	0	rw	CP0 register 16/6
config7	64	80000000	rw	CP0 register 16/7
lladdr	64	0	rw	CP0 register 17/0
maar	64	0	rw	CP0 register 17/1
maari	64	0	rw	CP0 register 17/2
watchlo	64	0	rw	CP0 register 18/0
watchlo,1	64	0	rw	CP0 register 18/1
watchlo,2	64	0	rw	CP0 register 18/2
watchlo,3	64	0	rw	CP0 register 18/3
watchhi	64	80000000	rw	CP0 register 19/0
watchhi,1	64	80000000	rw	CP0 register 19/1
watchhi,2	64	80000000	rw	CP0 register 19/2
watchhi,3	64	0	rw	CP0 register 19/3
xcontext	64	0	rw	CP0 register 20/0
debug	64	2030000	rw	CP0 register 23/0
depc	64	0	rw	CP0 register 24/0
perfcnt	64	80000000	rw	CP0 register 25/0
perfcnt,1	64	0	rw	CP0 register 25/1
perfcnt,2	64	80000000	rw	CP0 register 25/2
perfcnt,3	64	0	rw	CP0 register 25/3
perfcnt,4	64	80000000	rw	CP0 register 25/4
perfcnt,5	64	0	rw	CP0 register 25/5
perfcnt,6	64	0	rw	CP0 register 25/6
perfcnt,7	64	0	rw	CP0 register 25/7
errctl	64	0	rw	CP0 register 26/0
cacheerr	64	0	rw	CP0 register 27/0
itaglo	64	0	rw	CP0 register 28/0
idatalo	64	0	rw	CP0 register 28/1
dtaglo	64	0	rw	CP0 register 28/2
ddatalo	64	0	rw	CP0 register 28/3
itaghi	64	0	rw	CP0 register 29/0
idatahi	64	0	rw	CP0 register 29/1
dtaghi	64	0	rw	CP0 register 29/2
ddatahi	64	0	rw	CP0 register 29/3
errorepc	64	0	rw	CP0 register 30/0
desave	64	0	rw	CP0 register 31/0
kscratch1	64	0	rw	CP0 register 31/2

kscratch2	64	0	rw	CP0 register 31/3
kscratch3	64	0	rw	CP0 register 31/4
kscratch4	64	0	rw	CP0 register 31/5
kscratch5	64	0	rw	CP0 register 31/6
kscratch6	64	0	rw	CP0 register 31/7
guestindex	64	0	rw	CP0 guest register 0/0
guestvpcontrol	64	ffffffffffffffff	rw	CP0 guest register 0/4
guestrandom	64	0	rw	CP0 guest register 1/0
guestentrylo0	64	0	rw	CP0 guest register 2/0
guestentrylo1	64	0	rw	CP0 guest register 3/0
guestglobalnumber	64	ffffffffffffffff	rw	CP0 guest register 3/1
guestcontext	64	0	rw	CP0 guest register 4/0
guestcontextconfig	64	7ffff0	rw	CP0 guest register 4/1
guestuserlocal	64	0	rw	CP0 guest register 4/2
guestxcontextconfig	64	7ffffff0	rw	CP0 guest register 4/3
guestpagemask	64	6000	rw	CP0 guest register 5/0
guestpagegrain	64	c8000000	rw	CP0 guest register 5/1
guestwired	64	0	rw	CP0 guest register 6/0
guesthwrena	64	0	rw	CP0 guest register 7/0
guestbadvaddr	64	0	rw	CP0 guest register 8/0
guestbadinstr	64	0	rw	CP0 guest register 8/1
guestbadinstrp	64	0	rw	CP0 guest register 8/2
guestcount	64	0	rw	CP0 guest register 9/0
guestentryhi	64	0	rw	CP0 guest register 10/0
guestguestctl1	64	ffffffffffffffff	rw	CP0 guest register 10/4
guestguestctl2	64	ffffffffffffffff	rw	CP0 guest register 10/5
guestguestctl3	64	ffffffffffffffff	rw	CP0 guest register 10/6
guestcompare	64	0	rw	CP0 guest register 11/0
guestguestctl0ext	64	ffffffffffffffff	rw	CP0 guest register 11/4
gueststatus	64	4400004	rw	CP0 guest register 12/0
guestintctl	64	0	rw	CP0 guest register 12/1
guestsrsctl	64	0	rw	CP0 guest register 12/2
guestsrsmap	64	ffffffffffffffff	rw	CP0 guest register 12/3
guestguestctl0	64	ffffffffffffffff	rw	CP0 guest register 12/6
guestgtoffset	64	ffffffffffffffff	rw	CP0 guest register 12/7
guestcause	64	0	rw	CP0 guest register 13/0
guestepc	64	0	rw	CP0 guest register 14/0
guestprid	64	ffffffffffffffff	rw	CP0 guest register 15/0
guestebase	64	ffffffff80000000	rw	CP0 guest register 15/1
guestcmgcrbase	64	ffffffffffffffff	rw	CP0 guest register 15/3
guestbevva	64	ffffffffffffffff	rw	CP0 guest register 15/4
guestconfig	64	8000ca02	rw	CP0 guest register 16/0

guestconfig1	64	9eab559b	rw	CP0 guest register 16/1
guestconfig2	64	80000000	rw	CP0 guest register 16/2
guestconfig3	64	dc0033e1	rw	CP0 guest register 16/3
guestconfig4	64	d0fc0227	rw	CP0 guest register 16/4
guestconfig5	64	98	rw	CP0 guest register 16/5
guestconfig6	64	0	rw	CP0 guest register 16/6
guestconfig7	64	80000000	rw	CP0 guest register 16/7
guestlladdr	64	0	rw	CP0 guest register 17/0
guestmaar	64	ffffffffffffffff	rw	CP0 guest register 17/1
guestmaari	64	ffffffffffffffff	rw	CP0 guest register 17/2
guestwatchlo	64	0	rw	CP0 guest register 18/0
guestwatchlo,1	64	0	rw	CP0 guest register 18/1
guestwatchlo,2	64	0	rw	CP0 guest register 18/2
guestwatchlo,3	64	0	rw	CP0 guest register 18/3
guestwatchhi	64	80000000	rw	CP0 guest register 19/0
guestwatchhi,1	64	80000000	rw	CP0 guest register 19/1
guestwatchhi,2	64	80000000	rw	CP0 guest register 19/2
guestwatchhi,3	64	0	rw	CP0 guest register 19/3
guestxcontext	64	0	rw	CP0 guest register 20/0
guestdebug	64	ffffffffffffffff	rw	CP0 guest register 23/0
guestdepc	64	ffffffffffffffff	rw	CP0 guest register 24/0
guestperfcnt	64	ffffffffffffffff	rw	CP0 guest register 25/0
guestperfcnt,1	64	ffffffffffffffff	rw	CP0 guest register 25/1
guestperfcnt,2	64	ffffffffffffffff	rw	CP0 guest register 25/2
guestperfcnt,3	64	ffffffffffffffff	rw	CP0 guest register 25/3
guestperfcnt,4	64	ffffffffffffffff	rw	CP0 guest register 25/4
guestperfcnt,5	64	ffffffffffffffff	rw	CP0 guest register 25/5
guestperfcnt,6	64	ffffffffffffffff	rw	CP0 guest register 25/6
guestperfcnt,7	64	ffffffffffffffff	rw	CP0 guest register 25/7
guesterrctl	64	ffffffffffffffff	rw	CP0 guest register 26/0
guestcacheerr	64	ffffffffffffffff	rw	CP0 guest register 27/0
guestitaglo	64	ffffffffffffffff	rw	CP0 guest register 28/0
guestidatalo	64	ffffffffffffffff	rw	CP0 guest register 28/1
guestdtaglo	64	ffffffffffffffff	rw	CP0 guest register 28/2
guestddatalo	64	ffffffffffffffff	rw	CP0 guest register 28/3
guestitaghi	64	ffffffffffffffff	rw	CP0 guest register 29/0
guestidatahi	64	ffffffffffffffff	rw	CP0 guest register 29/1
guestdtaghi	64	ffffffffffffffff	rw	CP0 guest register 29/2
guestddatahi	64	ffffffffffffffff	rw	CP0 guest register 29/3
guesterrorepc	64	0	rw	CP0 guest register 30/0
guestdesave	64	ffffffffffffffff	rw	CP0 guest register 31/0
guestkscratch1	64	0	rw	CP0 guest register 31/2

guestkscratch2	64	0	rw	CP0 guest register 31/3
guestkscratch3	64	0	rw	CP0 guest register 31/4
guestkscratch4	64	0	rw	CP0 guest register 31/5
guestkscratch5	64	0	rw	CP0 guest register 31/6
guestkscratch6	64	0	rw	CP0 guest register 31/7

12.3.6 MSA

Table 16.

Name	Bits	Initial value (Hex)		Description
w0	128	-	rw	
w1	128	-	rw	
w2	128	-	rw	
w3	128	-	rw	
w4	128	-	rw	
w5	128	-	rw	
w6	128	-	rw	
w7	128	-	rw	
w8	128	-	rw	
w9	128	-	rw	
w10	128	-	rw	
w11	128	-	rw	
w12	128	-	rw	
w13	128	-	rw	
w14	128	-	rw	
w15	128	-	rw	
w16	128	-	rw	
w17	128	-	rw	
w18	128	-	rw	
w19	128	-	rw	
w20	128	-	rw	
w21	128	-	rw	
w22	128	-	rw	
w23	128	-	rw	
w24	128	-	rw	
w25	128	-	rw	
w26	128	-	rw	
w27	128	-	rw	
w28	128	-	rw	
w29	128	-	rw	
w30	128	-	rw	
w31	128	-	rw	

msair	64	320	r-	MSA implementation
msacsr	64	0	rw	MSA control and status
msaaccess	64	-	r-	MSA access
msasave	64	-	r-	MSA save
msamodify	64	-	r-	MSA modify
msarequest	64	-	r-	MSA request
msamap	64	-	r-	MSA map
msaunmap	64	-	r-	MSA unmap

12.3.7 CMP_GCR

Table 17.

Name	Bits	Initial value (Hex)		Description
GCR_CONFIG	64	1	r-	
GCR_BASE	64	1fbf8000	rw	
GCR_BASE_UPPER	64	0	rw	
GCR_CONTROL	64	200000	rw	
GCR_ACCESS	64	3f	rw	
GCR_REV	64	0	r-	
GCR_ERROR_MASK	64	0	rw	
GCR_ERROR_CAUSE	64	0	rw	
GCR_ERROR_ADDR	64	0	r-	
GCR_ERROR_ADDR_UPPER	64	0	--	
GCR_ERROR_MULT	64	0	rw	
GCR_GIC_BASE	64	0	rw	
GCR_CPC_BASE	64	0	rw	
GCR_GIC_STATUS	64	1	r-	
GCR_CACHE_REV	64	0	r-	
GCR_CPC_STATUS	64	1	r-	
GCR_IOCU1_REV	64	500	r-	
GCR_BEV_BASE	64	bfc00000	rw	
GCR_CL_COHERENCE_L	64	0	rw	
GCR_CL_CONFIG_L	64	0	r-	
GCR_CL_OTHER_L	64	0	rw	
GCR_CL_RESET_BASE_L	64	bfc00000	rw	
GCR_CL_ID_L	64	0	r-	
GCR_CL_COHERENCE_O	64	0	rw	
GCR_CL_CONFIG_O	64	0	r-	
GCR_CL_OTHER_O	64	0	rw	
GCR_CL_RESET_BASE_O	64	bfc00000	rw	
GCR_CL_ID_O	64	0	r-	

12.3.8 CMP_CPC

Table 18.

Name	Bits	Initial value (Hex)		Description
CPC_SEQDEL	64	0	rw	
CPC_RAIL	64	0	rw	
CPC_RESETLEN	64	0	rw	
CPC_REVISION	64	0	r-	
CPC_CMD_L	64	0	rw	
CPC_STAT_CONF_L	64	300200	rw	
CPC_OTHER_L	64	0	rw	
CPC_CL_VC_RUN_L	64	f	rw	
CPC_CL_VC_SUS_L	64	0	r-	
CPC_CMD_O	64	0	rw	
CPC_STAT_CONF_O	64	300200	rw	
CPC_OTHER_O	64	0	rw	
CPC_CL_VC_RUN_O	64	f	rw	
CPC_CL_VC_SUS_O	64	0	r-	

12.3.9 CMP_GIC

Table 19.

Name	Bits	Initial value (Hex)		Description
GIC_SH_CONFIG	64	8040001	rw	
GIC_CounterLo	64	0	rw	
GIC_CounterHi	64	0	rw	
GIC_SH_REVISION	64	0	r-	
GIC_SH_POL63_0	64	0	rw	
GIC_SH_POL127_64	64	0	rw	
GIC_SH_POL191_128	64	0	rw	
GIC_SH_POL255_192	64	0	rw	
GIC_SH_TRIG63_0	64	0	rw	
GIC_SH_TRIG127_64	64	0	rw	
GIC_SH_TRIG191_128	64	0	rw	
GIC_SH_TRIG255_192	64	0	rw	
GIC_SH_DUAL63_0	64	0	rw	
GIC_SH_DUAL127_64	64	0	rw	
GIC_SH_DUAL191_128	64	0	rw	
GIC_SH_DUAL255_192	64	0	rw	
GIC_SH_WEDGE	64	0	-w	
GIC_SH_RMASK63_0	64	0	-w	
GIC_SH_RMASK127_64	64	0	-w	
GIC_SH_RMASK191_128	64	0	-w	
GIC_SH_RMASK255_192	64	0	-w	

GIC_SH_SMASK63_0	64	0	-w	
GIC_SH_SMASK127_64	64	0	-w	
GIC_SH_SMASK191_128	64	0	-w	
GIC_SH_SMASK255_192	64	0	-w	
GIC_SH_MASK63_0	64	0	r-	
GIC_SH_MASK127_64	64	0	r-	
GIC_SH_MASK191_128	64	0	r-	
GIC_SH_MASK255_192	64	0	r-	
GIC_SH_PEND63_0	64	0	r-	
GIC_SH_PEND127_64	64	0	r-	
GIC_SH_PEND191_128	64	0	r-	
GIC_SH_PEND255_192	64	0	r-	
GIC_SH_MAP000_PIN	64	80000000	rw	
GIC_SH_MAP001_PIN	64	80000000	rw	
GIC_SH_MAP002_PIN	64	80000000	rw	
GIC_SH_MAP003_PIN	64	80000000	rw	
GIC_SH_MAP004_PIN	64	80000000	rw	
GIC_SH_MAP005_PIN	64	80000000	rw	
GIC_SH_MAP006_PIN	64	80000000	rw	
GIC_SH_MAP007_PIN	64	80000000	rw	
GIC_SH_MAP008_PIN	64	80000000	rw	
GIC_SH_MAP009_PIN	64	80000000	rw	
GIC_SH_MAP010_PIN	64	80000000	rw	
GIC_SH_MAP011_PIN	64	80000000	rw	
GIC_SH_MAP012_PIN	64	80000000	rw	
GIC_SH_MAP013_PIN	64	80000000	rw	
GIC_SH_MAP014_PIN	64	80000000	rw	
GIC_SH_MAP015_PIN	64	80000000	rw	
GIC_SH_MAP016_PIN	64	80000000	rw	
GIC_SH_MAP017_PIN	64	80000000	rw	
GIC_SH_MAP018_PIN	64	80000000	rw	
GIC_SH_MAP019_PIN	64	80000000	rw	
GIC_SH_MAP020_PIN	64	80000000	rw	
GIC_SH_MAP021_PIN	64	80000000	rw	
GIC_SH_MAP022_PIN	64	80000000	rw	
GIC_SH_MAP023_PIN	64	80000000	rw	
GIC_SH_MAP024_PIN	64	80000000	rw	
GIC_SH_MAP025_PIN	64	80000000	rw	
GIC_SH_MAP026_PIN	64	80000000	rw	
GIC_SH_MAP027_PIN	64	80000000	rw	
GIC_SH_MAP028_PIN	64	80000000	rw	
GIC_SH_MAP029_PIN	64	80000000	rw	

GIC_SH_MAP030_PIN	64	80000000	rw	
GIC_SH_MAP031_PIN	64	80000000	rw	
GIC_SH_MAP032_PIN	64	80000000	rw	
GIC_SH_MAP033_PIN	64	80000000	rw	
GIC_SH_MAP034_PIN	64	80000000	rw	
GIC_SH_MAP035_PIN	64	80000000	rw	
GIC_SH_MAP036_PIN	64	80000000	rw	
GIC_SH_MAP037_PIN	64	80000000	rw	
GIC_SH_MAP038_PIN	64	80000000	rw	
GIC_SH_MAP039_PIN	64	80000000	rw	
GIC_SH_MAP040_PIN	64	80000000	rw	
GIC_SH_MAP041_PIN	64	80000000	rw	
GIC_SH_MAP042_PIN	64	80000000	rw	
GIC_SH_MAP043_PIN	64	80000000	rw	
GIC_SH_MAP044_PIN	64	80000000	rw	
GIC_SH_MAP045_PIN	64	80000000	rw	
GIC_SH_MAP046_PIN	64	80000000	rw	
GIC_SH_MAP047_PIN	64	80000000	rw	
GIC_SH_MAP048_PIN	64	80000000	rw	
GIC_SH_MAP049_PIN	64	80000000	rw	
GIC_SH_MAP050_PIN	64	80000000	rw	
GIC_SH_MAP051_PIN	64	80000000	rw	
GIC_SH_MAP052_PIN	64	80000000	rw	
GIC_SH_MAP053_PIN	64	80000000	rw	
GIC_SH_MAP054_PIN	64	80000000	rw	
GIC_SH_MAP055_PIN	64	80000000	rw	
GIC_SH_MAP056_PIN	64	80000000	rw	
GIC_SH_MAP057_PIN	64	80000000	rw	
GIC_SH_MAP058_PIN	64	80000000	rw	
GIC_SH_MAP059_PIN	64	80000000	rw	
GIC_SH_MAP060_PIN	64	80000000	rw	
GIC_SH_MAP061_PIN	64	80000000	rw	
GIC_SH_MAP062_PIN	64	80000000	rw	
GIC_SH_MAP063_PIN	64	80000000	rw	
GIC_SH_MAP064_PIN	64	80000000	rw	
GIC_SH_MAP065_PIN	64	80000000	rw	
GIC_SH_MAP066_PIN	64	80000000	rw	
GIC_SH_MAP067_PIN	64	80000000	rw	
GIC_SH_MAP068_PIN	64	80000000	rw	
GIC_SH_MAP069_PIN	64	80000000	rw	
GIC_SH_MAP070_PIN	64	80000000	rw	
GIC_SH_MAP071_PIN	64	80000000	rw	

GIC_SH_MAP072_PIN	64	80000000	rw	
GIC_SH_MAP073_PIN	64	80000000	rw	
GIC_SH_MAP074_PIN	64	80000000	rw	
GIC_SH_MAP075_PIN	64	80000000	rw	
GIC_SH_MAP076_PIN	64	80000000	rw	
GIC_SH_MAP077_PIN	64	80000000	rw	
GIC_SH_MAP078_PIN	64	80000000	rw	
GIC_SH_MAP079_PIN	64	80000000	rw	
GIC_SH_MAP080_PIN	64	80000000	rw	
GIC_SH_MAP081_PIN	64	80000000	rw	
GIC_SH_MAP082_PIN	64	80000000	rw	
GIC_SH_MAP083_PIN	64	80000000	rw	
GIC_SH_MAP084_PIN	64	80000000	rw	
GIC_SH_MAP085_PIN	64	80000000	rw	
GIC_SH_MAP086_PIN	64	80000000	rw	
GIC_SH_MAP087_PIN	64	80000000	rw	
GIC_SH_MAP088_PIN	64	80000000	rw	
GIC_SH_MAP089_PIN	64	80000000	rw	
GIC_SH_MAP090_PIN	64	80000000	rw	
GIC_SH_MAP091_PIN	64	80000000	rw	
GIC_SH_MAP092_PIN	64	80000000	rw	
GIC_SH_MAP093_PIN	64	80000000	rw	
GIC_SH_MAP094_PIN	64	80000000	rw	
GIC_SH_MAP095_PIN	64	80000000	rw	
GIC_SH_MAP096_PIN	64	80000000	rw	
GIC_SH_MAP097_PIN	64	80000000	rw	
GIC_SH_MAP098_PIN	64	80000000	rw	
GIC_SH_MAP099_PIN	64	80000000	rw	
GIC_SH_MAP100_PIN	64	80000000	rw	
GIC_SH_MAP101_PIN	64	80000000	rw	
GIC_SH_MAP102_PIN	64	80000000	rw	
GIC_SH_MAP103_PIN	64	80000000	rw	
GIC_SH_MAP104_PIN	64	80000000	rw	
GIC_SH_MAP105_PIN	64	80000000	rw	
GIC_SH_MAP106_PIN	64	80000000	rw	
GIC_SH_MAP107_PIN	64	80000000	rw	
GIC_SH_MAP108_PIN	64	80000000	rw	
GIC_SH_MAP109_PIN	64	80000000	rw	
GIC_SH_MAP110_PIN	64	80000000	rw	
GIC_SH_MAP111_PIN	64	80000000	rw	
GIC_SH_MAP112_PIN	64	80000000	rw	
GIC_SH_MAP113_PIN	64	80000000	rw	

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GIC_SH_MAP245_VPE31_0	64	0	rw	
GIC_SH_MAP246_VPE31_0	64	0	rw	
GIC_SH_MAP247_VPE31_0	64	0	rw	
GIC_SH_MAP248_VPE31_0	64	0	rw	
GIC_SH_MAP249_VPE31_0	64	0	rw	
GIC_SH_MAP250_VPE31_0	64	0	rw	
GIC_SH_MAP251_VPE31_0	64	0	rw	
GIC_SH_MAP252_VPE31_0	64	0	rw	
GIC_SH_MAP253_VPE31_0	64	0	rw	
GIC_SH_MAP254_VPE31_0	64	0	rw	
GIC_SH_MAP255_VPE31_0	64	0	rw	
GIC_SH_EJTAG_BRK	64	0	rw	
GIC_SH_TEAMID_LO	64	0	rw	
GIC_SH_TEAMID_HI	64	0	rw	
GIC_SH_TEAMID_EXT	64	0	rw	
GIC_SH_DBG_CONFIG	64	0	rw	
GIC_SH_DINT_PART	64	0	rw	
GIC_SH_DEBUGM_STATUS	64	0	r-	
GIC_VPE_CTL_L	64	2	rw	
GIC_VPE_PEND_L	64	0	r-	
GIC_VPE_MASK_L	64	3f	r-	
GIC_VPE_RMASK_L	64	0	-w	
GIC_VPE_SMASK_L	64	0	-w	
GIC_VPE_WD_MAP_L	64	40000000	rw	
GIC_VPE_COMPARE_MAP_L	64	0	rw	
GIC_VPE_TIMER_MAP_L	64	80000005	rw	
GIC_VPE_FDC_MAP_L	64	80000005	rw	
GIC_VPE_PERFCTR_MAP_L	64	80000005	rw	
GIC_VPE_SWInt0_MAP_L	64	80000000	rw	
GIC_VPE_SWInt1_MAP_L	64	80000000	rw	
GIC_VPE_OTHER_ADDRESS_L	64	0	rw	
GIC_VPE_IDENT_L	64	0	r-	
GIC_VPE_WD_CONFIG_L	64	0	rw	

GIC_VPE_WD_COUNT_L	64	0	r-	
GIC_VPE_WD_INITIAL_L	64	0	rw	
GIC_VPE_CompareLo_L	64	ffffffffffffffff	rw	
GIC_VPE_CompareHi_L	64	ffffffffffffffff	rw	
GIC_VL_COFFSET_L	64	0	rw	
GIC_VPE_CTL_O	64	2	rw	
GIC_VPE_PEND_O	64	0	r-	
GIC_VPE_MASK_O	64	3f	r-	
GIC_VPE_RMASK_O	64	0	-w	
GIC_VPE_SMASK_O	64	0	-w	
GIC_VPE_WD_MAP_O	64	40000000	rw	
GIC_VPE_COMPARE_MAP_O	64	0	rw	
GIC_VPE_TIMER_MAP_O	64	80000005	rw	
GIC_VPE_FDC_MAP_O	64	80000005	rw	
GIC_VPE_PERFCTR_MAP_O	64	80000005	rw	
GIC_VPE_SWInt0_MAP_O	64	80000000	rw	
GIC_VPE_SWInt1_MAP_O	64	80000000	rw	
GIC_VPE_OTHER_ADDRESS_O	64	0	rw	
GIC_VPE_IDENT_O	64	0	r-	
GIC_VPE_WD_CONFIG_O	64	0	rw	
GIC_VPE_WD_COUNT_O	64	0	r-	
GIC_VPE_WD_INITIAL_O	64	0	rw	
GIC_VPE_CompareLo_O	64	ffffffffffffffff	rw	
GIC_VPE_CompareHi_O	64	ffffffffffffffff	rw	
GIC_VL_COFFSET_O	64	0	rw	
GIC_CounterLoUser	64	0	r-	
GIC_CounterHiUser	64	0	r-	

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Table 20.

Name	Bits	Initial value (Hex)		Description
stop	64	0	rw	write with non-zero to stop processor

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