OVP Guide to Using Processor Models

Model Specific Information for variant MIPS32_M5100

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1.0 Overview

This document provides the details of an OVP Fast Processor Model variant.
OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms. The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.
The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners.
There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

MIPS32 Configurable Processor Model
If you need other variants, these models can be obtained from www.OVPworld.org/MIPSuser.

1.2 Licensing

Usage of binary model under license governing simulator usage. Source of model available under Imperas Software License Agreement.

1.3 Limitations

If this model is not part of your installation, then it is available for download from www.OVPworld.org/MIPSuser.

1.4 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

1.5 Features

Both MIPS32 and microMIPS32 Instruction sets implemented
MMU Type: Fixed Mapping
Vectored interrupts implemented
MCU ASE implemented

2.0 Configuration

2.1 Location

The model source and object file is found in the VLNV tree at:
imgtec.ovpworld.org/processor/mips32/1.0

2.2 GDB Path

The default GDB for this model is found at:
$IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/mips-sde-elf-gdb

2.3 Semi-Host Library

The default semi-host library file is found in the VLNV tree at :
mips.ovpworld.org/semihosting/mips32SDE/1.0

2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

2.6 Processor ELF Code

The ELF code supported by this model is: 0x8

3.0 Other Variants in this Model

Table 1.

Variant
M5100
.M5100Guest
M5150
.M5150Guest
P5600
.P5600Guest

4.0 Bus Ports

Table 2.

Type	Name	Bits
master (initiator)	INSTRUCTION	32
master (initiator)	DATA	32

5.0 Net Ports

Table 3.

Name	Type	Description
reset	input	Core reset
dint	input	Debug external interrupt
hwint0	input	External interrupt
hwint1	input	External interrupt
hwint2	input	External interrupt
hwint3	input	External interrupt
hwint4	input	External interrupt
hwint5	input	External interrupt
hwint6	input	External interrupt
hwint7	input	External interrupt
nmi	input	Non-maskable external interrupt
EICPresent	input	Input signal SI_EICPresent per VPE
EIC_RIPL	input	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS	input	External interrupt controller EICSS
EIC_VectorNum	input	External interrupt controller vector number
EIC_VectorOffset	input	External interrupt controller vector offset
EIC_GID	input	External interrupt controller guest ID
intISS	output	True when interrupt request is serviced
causeTI	output	True when timer interrupt expires
causeIP0	output	Raised for software interrupt request IP0
causeIP1	output	Raised for software interrupt request IP1

Guest.EIC_RIPL	input	Guest External interrupt controller RIPL
Guest.EIC_EICSS	input	Guest External interrupt controller EICSS
Guest.EIC_VectorNum	input	Guest External interrupt controller vector number
Guest.EIC_VectorOffset	input	Guest External interrupt controller vector offset
Guest.EIC_GID	input	Guest External interrupt controller guest ID
Guest.intISS	output	True when Guest interrupt request is serviced
Guest.causeTI	output	True when Guest timer interrupt expires
Guest.causeIP0	output	Raised for Guest software interrupt request IP0
Guest.causeIP1	output	Raised for Guest software interrupt request IP1

6.0 FIFO Ports

No FIFO Ports in this model.

7.0 Parameters

Table 4.

Name	Type	Description
cacheenable	Enumeration	Select cache model mode default=0 tag=1 full=2
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info structure
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
supervisorMode	Boolean	Override whether processor implements supervisor mode
busErrors	Boolean	Override bus error exception behavior. When true, accesses of memory not defined by platform will cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when true (sets Config.MT=3, Config.KU/K23=2 and Config1.MMUSizeM1=0)
removeDSP	Boolean	Override the DSP-present configuration when true (sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true (sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true (sets Config1.FP to 0)
removeFTLB	Boolean	Override the FTLBEn configuration when true (disable FTLB)
isISA	Boolean	Enable to specify ISA model (reset address from ELF, all coprocessors enabled)

hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to maximum value to improve performance
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores only)
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC implementation (MT cores only)
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior)
supportDenormals	Boolean	Enable to specify that the FPU supports denormal operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0
mpuRegions	Uns32	Number of regions for memory protection unit
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
MIPS_UHI	Boolean	Enable MIPS-Unified Hosting interface
mipsUhiArgs	String	Specifies UHI arguments string seperated by spaces
mipsUhiJail	String	Specifies UHI jailroot
MIPS_DV_MODE	Boolean	Enable Design Verification mode
MIPS_MAGIC_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes
enableTrickbox	Boolean	Enable trickbox addresses (specific for AVP)
fpuexcdisable	Boolean	Disable FPU exceptions
cop2Bits	Uns32	Specifies width in bits of COP2 registers (32 or 64)
cop2FileName	String	Specifies COP2 dynamically-loaded object (.so/.dll) defining COP2 instructions
udiConfig	Int32	Specifies UDI configuration attribute
udiFileName	String	Specifies UDI dynamically-loaded object (.so/.dll) defining UDI instructions
vectoredinterrupt	Boolean	Enables vectored interrupts (sets Config3 VInt)
externalinterrupt	Boolean	Enables the use of an external interrupt controller (sets Config3 VEIC)
rootFixedMMU	Boolean	Override the root MMU type to fixed mapping when true (sets Config.MT=3 and Config.KU/K23=2)
rootMMUSizeM1	Uns32	Override the root MMUSizeM1 field in Config1 register (number of MMU entries-1)
srsctlHSS	Uns32	Override the HSS field in SRSCtl register (number of shadow register sets)
firPS	Uns32	Override the PS field in FIR register
firHas2008	Uns32	Override the Has2008 field in FIR register

pridCompanyOptions	Uns32	Override the Company Options field in PRId register
pridRevision	Uns32	Override the Revision field in PRId register
intctlIPTI	Uns32	Override the IPTI field in IntCtl register
intctlIPFDC	Uns32	Override the IPFDC field in IntCtl register
intctlIPPCI	Uns32	Override the IPPCI field in IntCtl register
numWatch	Uns32	Specify number of WatchLo/WatchHi register pairs
numVC	Uns32	Specify number of Virtual Cores to be present
numVCtoStart	Uns32	Specify number of Virtual Cores to be running
sharedTLBindex	Uns32	Specify first shared TLB Index between Virtual Cores
hasFDC	Boolean	Specify Fast Debug Channel (dummy implementation)
intctlIPTI_CPU0_VC0	Uns32	Override the IPTI field in IntCtl register for CPU0/VC0
intctlIPTI_CPU0_VC1	Uns32	Override the IPTI field in IntCtl register for CPU0/VC1
intctlIPTI_CPU0_VC2	Uns32	Override the IPTI field in IntCtl register for CPU0/VC2
intctlIPTI_CPU0_VC3	Uns32	Override the IPTI field in IntCtl register for CPU0/VC3
intctlIPTI_CPU1_VC0	Uns32	Override the IPTI field in IntCtl register for CPU1/VC0
intctlIPTI_CPU1_VC1	Uns32	Override the IPTI field in IntCtl register for CPU1/VC1
intctlIPTI_CPU1_VC2	Uns32	Override the IPTI field in IntCtl register for CPU1/VC2
intctlIPTI_CPU1_VC3	Uns32	Override the IPTI field in IntCtl register for CPU1/VC3
intctlIPTI_CPU2_VC0	Uns32	Override the IPTI field in IntCtl register for CPU2/VC0
intctlIPTI_CPU2_VC1	Uns32	Override the IPTI field in IntCtl register for CPU2/VC1
intctlIPTI_CPU2_VC2	Uns32	Override the IPTI field in IntCtl register for CPU2/VC2
intctlIPTI_CPU2_VC3	Uns32	Override the IPTI field in IntCtl register for CPU2/VC3
intctlIPTI_CPU3_VC0	Uns32	Override the IPTI field in IntCtl register for CPU3/VC0
intctlIPTI_CPU3_VC1	Uns32	Override the IPTI field in IntCtl register for CPU3/VC1
intctlIPTI_CPU3_VC2	Uns32	Override the IPTI field in IntCtl register for CPU3/VC2
intctlIPTI_CPU3_VC3	Uns32	Override the IPTI field in IntCtl register for CPU3/VC3

intctlIPFDC_CPU0_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC0
intctlIPFDC_CPU0_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC1
intctlIPFDC_CPU0_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC2
intctlIPFDC_CPU0_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC3
intctlIPFDC_CPU1_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC0
intctlIPFDC_CPU1_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC1
intctlIPFDC_CPU1_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC2
intctlIPFDC_CPU1_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC3
intctlIPFDC_CPU2_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC0
intctlIPFDC_CPU2_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC1
intctlIPFDC_CPU2_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC2
intctlIPFDC_CPU2_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC3
intctlIPFDC_CPU3_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC0
intctlIPFDC_CPU3_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC1
intctlIPFDC_CPU3_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC2
intctlIPFDC_CPU3_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC3
intctlIPPCI_CPU0_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC0
intctlIPPCI_CPU0_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC1
intctlIPPCI_CPU0_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC2
intctlIPPCI_CPU0_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC3
intctlIPPCI_CPU1_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC0
intctlIPPCI_CPU1_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC1
intctlIPPCI_CPU1_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC2

intctlIPPCI_CPU1_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC3
intctlIPPCI_CPU2_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC0
intctlIPPCI_CPU2_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC1
intctlIPPCI_CPU2_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC2
intctlIPPCI_CPU2_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC3
intctlIPPCI_CPU3_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC0
intctlIPPCI_CPU3_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC1
intctlIPPCI_CPU3_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC2
intctlIPPCI_CPU3_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC3
configAR	Uns32	Enables R6 support
configBM	Uns32	Override the BM field in Config register (burst mode)
configDSP	Boolean	Override Config.DSP (data scratchpad RAM present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0 cacheability)
configKU	Uns32	Override power on value of Config.KU (set Useg cacheability)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23 cacheability)
configMDU	Boolean	Override Config.MDU (iterative multiply/divide unit)
configMM	Boolean	Override Config.MM (merging mode for write)
configMT	Uns32	Override Config.MT
configSB	Boolean	Override Config.SB (simple bus transfers only)
MIPS16eASE	Boolean	Override Config1.CA (enables the MIPS16e ASE)
config1DA	Uns32	Override Config1.DA (Dcache associativity)
config1DL	Uns32	Override Config1.DL (Dcache line size)
config1DS	Uns32	Override Config1.DS (Dcache sets per way)
config1EP	Boolean	Override Config1.EP (EJTag present)
config1IA	Uns32	Override Config1.IA (Icache associativity)
config1IL	Uns32	Override Config1.IL (Icache line size)
config1IS	Uns32	Override Config1.IS (Icache sets per way)

config1MMUSizeM1	Uns32	Override Config1.MMUSizeM1 (number of MMU entries-1)
config1WR	Boolean	Override Config1.WR (watchpoint registers present)
config2SU	Uns32	Override the SU field in Config2 register
config2SS	Uns32	Override the SS field in Config2 register
config2SL	Uns32	Override the SL field in Config2 register
config2SA	Uns32	Override the SA field in Config2 register
config3BI	Boolean	Override Config3.BI
config3BP	Boolean	Override Config3.BP
config3CDMM	Boolean	Override Config3.CDMM
config3CTXTC	Boolean	Override Config3.CTXTC
config3DSPP	Boolean	Override Config3.DSPP
config3DSP2P	Boolean	Override Config3.DSP2P
config3IPLW	Uns32	Override Config3.IPLW
config3ISA	Uns32	Override Config3.ISA
config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3LPA	Boolean	Override Config3.LPA
config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
config3SC	Boolean	Override Config3.SC
config3ULRI	Boolean	Override Config3.ULRI
config3VZ	Boolean	Override Config3.VZ
config3MSAP	Boolean	Override Config3.MSAP
config3CMGCR	Boolean	Override the CMGCR field in Config3 register
config3SP	Boolean	Override the SP field in Config3 register
config3TL	Uns32	Override the TL field in Config3 register
config3PW	Boolean	Override the PW field in Config3 register
config4AE	Boolean	Override Config4.AE
config4IE	Uns32	Override Config4.IE
config4MMUConfig	Uns32	Override Config4.MMUConfig field (interpretation depends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.VTLBSizeExt
config5EVA	Boolean	Override Config5.EVA
config5LLB	Boolean	Override Config5.LLB (LLAddr supports LLbit)
config5MRP	Boolean	Override Config5.MRP (MaaR Present)
config5NFExists	Boolean	Override Config5.NFExists
config5MSAEn	Boolean	Override Config5.MSAEn
config5MVH	Boolean	Override Config5.MVH (enable MTHC0 and MFHC0 instructions)

config6FTLBEn	Boolean	Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE
config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initialization)
config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
config7ES	Uns32	Override the ES field in Config7 register (Externalize sync)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant with IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/ SNaN encodings match IEEE 754-2008 recommendation)
numMaarRegs	Uns32	Override number of MAAR registers (must be even)
wiredLimit	Uns32	Override Limit field of the Wired register
cdmmBaseCI	Boolean	Override CDMMBase.CI
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the corresponding BEV address bits
firstBEVExceptionBaseMaskBit	Uns32	Specify LSB position of GCR_Cx_RESET_EXT_BASE.BEVExceptionBaseMask field. Only used when SegCtl present
EVAReset	Boolean	Set to one to reset into non-legacy address map and BEV location. Only used when non-CMP and SegCtl present
ExceptionBaseMask	Uns32	Specify the ExceptionBaseMask value used for bits [27:firstBEVExceptionBaseMaskBit]. Only used when non-CMP and SegCtl present
ExceptionBasePA	Uns32	Bits [35:29] of the physical address for the BEV overlays. Only used when non-CMP and SegCtl present
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable within cluster
GCR_PCORES	Uns32	CMP system only: override GCR_CONFIG.PCORES (number of cores-1)

GCR_BASE	Uns32	CMP system only: override GCR_BASE.GCR_BASE (default GCR register address)
GCR_MINOR_REV	Uns32	CMP system only: override GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MAJOR_REV
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MAJOR_REV
GIC_NUMINTERRUPTS	Uns32	CMP system only: override GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MAJOR_REV
GIC_NUM_TEAMS	Uns32	CMP system only: override GIC_SH_DBG_CONFIG.NUM_TEAMS
GIC_TRIG_RESET	Uns32	CMP system only: Zero value of GIC_SH_TRIG_[31_0, 63_32]
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPE
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override CPC_REVISION.MAJOR_REV
GIC_SH_GID_CONFIG31_0	Uns32	CMP system only: override GIC_SH_GID_CONFIG[31_0]
GIC_SH_GID_CONFIG63_32	Uns32	CMP system only: override GIC_SH_GID_CONFIG[63_32]
GIC_SH_GID_CONFIG95_64	Uns32	CMP system only: override GIC_SH_GID_CONFIG[95_64]
GIC_SH_GID_CONFIG127_96	Uns32	CMP system only: override GIC_SH_GID_CONFIG[127_96]

GIC_SH_GID_CONFIG159_128	Uns32	CMP system only: override GIC_SH_GID_CONFIG[159_128]
GIC_SH_GID_CONFIG191_160	Uns32	CMP system only: override GIC_SH_GID_CONFIG[191_160]
GIC_SH_GID_CONFIG223_192	Uns32	CMP system only: override GIC_SH_GID_CONFIG[223_192]
GIC_SH_GID_CONFIG255_224	Uns32	CMP system only: override GIC_SH_GID_CONFIG[255_224]
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 0
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 1
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 2
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 3
GCR_C0_V0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core0/vc0
GCR_C0_V1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core0/vc1
GCR_C0_V2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core0/vc2
GCR_C0_V3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core0/vc3
GCR_C1_V0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core1/vc0
GCR_C1_V1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core1/vc1
GCR_C1_V2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core1/vc2
GCR_C1_V3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core1/vc3
GCR_C2_V0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core2/vc0
GCR_C2_V1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core2/vc1
GCR_C2_V2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core2/vc2

GCR_C2_V3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core2/vc3
GCR_C3_V0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core3/vc0
GCR_C3_V1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core3/vc1
GCR_C3_V2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core3/vc2
GCR_C3_V3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core3/vc3
CPC_C0_VC_EN	Uns32	CMP system only: CPC_VC_EN for core 0
CPC_C1_VC_EN	Uns32	CMP system only: CPC_VC_EN for core 1
CPC_C2_VC_EN	Uns32	CMP system only: CPC_VC_EN for core 2
CPC_C3_VC_EN	Uns32	CMP system only: CPC_VC_EN for core 3
EIC_OPTION	Uns32	Override the external interrupt controller EIC_OPTION
guestVariant	Enumeration	Guest processor variant (same as Root if not specified) M5100=0 .M5100Guest=1 M5150=2 .M5150Guest=3 P5600=4 .P5600Guest=5
guestCtl0RI	Uns32	Override the RI field in GuestCtl0 register
guestCtl0MC	Uns32	Override the MC field in GuestCtl0 register
guestCtl0CP0	Uns32	Override the CP0 field in GuestCtl0 register
guestCtl0AT	Uns32	Override the AT field in GuestCtl0 register
guestCtl0GT	Uns32	Override the GT field in GuestCtl0 register
guestCtl0CG	Uns32	Override the CG field in GuestCtl0 register
guestCtl0CF	Uns32	Override the CF field in GuestCtl0 register
guestCtl0G1	Uns32	Override the G1 field in GuestCtl0 register
guestCtl0RAD	Uns32	Override the RAD field in GuestCtl0 register
guestCtl0DRG	Uns32	Override the DRG field in GuestCtl0 register
hasImpl17	Boolean	Enable read/write of Impl17 bit in Status register
hasImpl16	Boolean	Enable read/write of Impl16 bit in Status register
guestintctlIPTI	Uns32	Override the Guest IPTI field in IntCtl register
guestintctlIPFDC	Uns32	Override the Guest IPFDC field in IntCtl register
guestintctlIPPCI	Uns32	Override the Guest IPPCI field in IntCtl register
guestintctlIPTI_CPU0_VC0	Uns32	Override the IPTI field in IntCtl register for CPU0/VC0
guestintctlIPTI_CPU0_VC1	Uns32	Override the IPTI field in IntCtl register for CPU0/VC1
guestintctlIPTI_CPU0_VC2	Uns32	Override the IPTI field in IntCtl register for CPU0/VC2

guestintctlIPTI_CPU0_VC3	Uns32	Override the IPTI field in IntCtl register for CPU0/VC3
guestintctlIPTI_CPU1_VC0	Uns32	Override the IPTI field in IntCtl register for CPU1/VC0
guestintctlIPTI_CPU1_VC1	Uns32	Override the IPTI field in IntCtl register for CPU1/VC1
guestintctlIPTI_CPU1_VC2	Uns32	Override the IPTI field in IntCtl register for CPU1/VC2
guestintctlIPTI_CPU1_VC3	Uns32	Override the IPTI field in IntCtl register for CPU1/VC3
guestintctlIPTI_CPU2_VC0	Uns32	Override the IPTI field in IntCtl register for CPU2/VC0
guestintctlIPTI_CPU2_VC1	Uns32	Override the IPTI field in IntCtl register for CPU2/VC1
guestintctlIPTI_CPU2_VC2	Uns32	Override the IPTI field in IntCtl register for CPU2/VC2
guestintctlIPTI_CPU2_VC3	Uns32	Override the IPTI field in IntCtl register for CPU2/VC3
guestintctlIPTI_CPU3_VC0	Uns32	Override the IPTI field in IntCtl register for CPU3/VC0
guestintctlIPTI_CPU3_VC1	Uns32	Override the IPTI field in IntCtl register for CPU3/VC1
guestintctlIPTI_CPU3_VC2	Uns32	Override the IPTI field in IntCtl register for CPU3/VC2
guestintctlIPTI_CPU3_VC3	Uns32	Override the IPTI field in IntCtl register for CPU3/VC3
guestintctlIPFDC_CPU0_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC0
guestintctlIPFDC_CPU0_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC1
guestintctlIPFDC_CPU0_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC2
guestintctlIPFDC_CPU0_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VC3
guestintctlIPFDC_CPU1_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC0
guestintctlIPFDC_CPU1_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC1
guestintctlIPFDC_CPU1_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC2
guestintctlIPFDC_CPU1_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VC3
guestintctlIPFDC_CPU2_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC0
guestintctlIPFDC_CPU2_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC1

guestintctlIPFDC_CPU2_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC2
guestintctlIPFDC_CPU2_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VC3
guestintctlIPFDC_CPU3_VC0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC0
guestintctlIPFDC_CPU3_VC1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC1
guestintctlIPFDC_CPU3_VC2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC2
guestintctlIPFDC_CPU3_VC3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VC3
guestintctlIPPCI_CPU0_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC0
guestintctlIPPCI_CPU0_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC1
guestintctlIPPCI_CPU0_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC2
guestintctlIPPCI_CPU0_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VC3
guestintctlIPPCI_CPU1_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC0
guestintctlIPPCI_CPU1_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC1
guestintctlIPPCI_CPU1_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC2
guestintctlIPPCI_CPU1_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VC3
guestintctlIPPCI_CPU2_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC0
guestintctlIPPCI_CPU2_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC1
guestintctlIPPCI_CPU2_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC2
guestintctlIPPCI_CPU2_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VC3
guestintctlIPPCI_CPU3_VC0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC0
guestintctlIPPCI_CPU3_VC1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC1
guestintctlIPPCI_CPU3_VC2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC2
guestintctlIPPCI_CPU3_VC3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VC3

8.0 Execution Modes

Table 5.

Name	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3
GUEST_KERNEL	4
GUEST_SUPERVISOR	5
GUEST_USER	6

9.0 Exceptions

Table 6.

Name	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Bp	9
RI	10
CpU	11
Ov	12
Tr	13
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
GE	27
Prot	29

CacheErr	30

10.0 Hierarchy of the model

A CPU core may allow the user to configure it to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.
OVP processor models can be written to include SMP blocks and to have many levels of hierarchy.

Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

10.1 Level 1: CPU

This level in the model hierarchy has 20 commands.

This level in the model hierarchy has 5 register groups:

Table 7.

Group name	Registers
Core	33
DSP	9
Shadow	32
COP0	100
Integration_support	1

This level in the model hierarchy has no children.

11.0 Model Commands

11.1 Level 1: CPU

Table 8.

Name	Arguments
isync	specify instruction address range for synchronous execution
itrace	enable or disable instruction tracing
mipsCOP0	<register> <select>
mipsCacheDisable	
mipsCacheEnable	-tag|-full
mipsCacheRatio	-icache|-dcache
mipsCacheReport	
mipsCacheReset	
mipsCacheTrace	-on|-off [-nocached|-nouncached] [-noicache|-nodcache] [-noartifact|-notrue]
mipsDebugFlags	<value>
mipsReadRegister	<resource> <offset>
mipsReadTLBEntry	<index>
mipsTLBDump	
mipsTLBDumpGuest	
mipsTLBDumpRoot	
mipsTLBGetPhys	<virtual address> <ASID>
mipsTraceGuest	<bool>
mipsTraceRoot	<bool>
mipsWriteRegister	<resource> <offset> <value>
mipsWriteTLBEntry	<index> <lo0> <lo1> <hi0> <mask>

12.0 Registers

12.1 Level 1: CPU

12.1.1 Core

Table 9.

Name	Bits	Initial value (Hex)		Description
zero	32	0	r-	constant zero
at	32	0	rw	
v0	32	0	rw	
v1	32	0	rw	
a0	32	0	rw	
a1	32	0	rw	
a2	32	0	rw	
a3	32	0	rw	
t0	32	0	rw	
t1	32	0	rw	

t2	32	0	rw	
t3	32	0	rw	
t4	32	0	rw	
t5	32	0	rw	
t6	32	0	rw	
t7	32	0	rw	
s0	32	0	rw	
s1	32	0	rw	
s2	32	0	rw	
s3	32	0	rw	
s4	32	0	rw	
s5	32	0	rw	
s6	32	0	rw	
s7	32	0	rw	
t8	32	0	rw	
t9	32	0	rw	
k0	32	0	rw	
k1	32	0	rw	
gp	32	0	rw	
sp	32	0	rw	stack pointer
s8	32	0	rw	frame pointer
ra	32	0	rw	
pc	32	bfc00000	rw	program counter

12.1.2 DSP

Table 10.

Name	Bits	Initial value (Hex)		Description
lo	32	0	rw	
hi	32	0	rw	
lo1	32	0	rw	
hi1	32	0	rw	
lo2	32	0	rw	
hi2	32	0	rw	
lo3	32	0	rw	
hi3	32	0	rw	
dspctl	32	0	rw	DSP control

12.1.3 Shadow

Table 11.

Name	Bits	Initial value (Hex)		Description

zero[0]	32	0	r-	constant zero
at[0]	32	0	rw	
v0[0]	32	0	rw	
v1[0]	32	0	rw	
a0[0]	32	0	rw	
a1[0]	32	0	rw	
a2[0]	32	0	rw	
a3[0]	32	0	rw	
t0[0]	32	0	rw	
t1[0]	32	0	rw	
t2[0]	32	0	rw	
t3[0]	32	0	rw	
t4[0]	32	0	rw	
t5[0]	32	0	rw	
t6[0]	32	0	rw	
t7[0]	32	0	rw	
s0[0]	32	0	rw	
s1[0]	32	0	rw	
s2[0]	32	0	rw	
s3[0]	32	0	rw	
s4[0]	32	0	rw	
s5[0]	32	0	rw	
s6[0]	32	0	rw	
s7[0]	32	0	rw	
t8[0]	32	0	rw	
t9[0]	32	0	rw	
k0[0]	32	0	rw	
k1[0]	32	0	rw	
gp[0]	32	0	rw	
sp[0]	32	0	rw	stack pointer
s8[0]	32	0	rw	frame pointer
ra[0]	32	0	rw	

12.1.4 COP0

Table 12.

Name	Bits	Initial value (Hex)		Description
sr	32	400004	rw	CP0 register 12/0
bad	32	0	rw	CP0 register 8/0
cause	32	0	rw	CP0 register 13/0
index	32	0	rw	CP0 register 0/0
random	32	0	rw	CP0 register 1/0

entrylo0	32	0	rw	CP0 register 2/0
entrylo1	32	0	rw	CP0 register 3/0
context	32	0	rw	CP0 register 4/0
userlocal	32	0	rw	CP0 register 4/2
pagemask	32	0	rw	CP0 register 5/0
pagegrain	32	0	rw	CP0 register 5/1
wired	32	0	rw	CP0 register 6/0
hwrena	32	0	rw	CP0 register 7/0
badvaddr	32	0	rw	CP0 register 8/0
badinstr	32	0	rw	CP0 register 8/1
badinstrp	32	0	rw	CP0 register 8/2
count	32	0	rw	CP0 register 9/0
entryhi	32	0	rw	CP0 register 10/0
guestctl1	32	0	rw	CP0 register 10/4
guestctl2	32	0	rw	CP0 register 10/5
guestctl3	32	0	rw	CP0 register 10/6
compare	32	0	rw	CP0 register 11/0
guestctl0ext	32	40	rw	CP0 register 11/4
status	32	400004	rw	CP0 register 12/0
intctl	32	e0030000	rw	CP0 register 12/1
srsctl	32	0	rw	CP0 register 12/2
srsmap	32	0	rw	CP0 register 12/3
viewipl	32	0	rw	CP0 register 12/4
srsmap2	32	0	rw	CP0 register 12/5
guestctl0	32	c4c00fc	rw	CP0 register 12/6
gtoffset	32	0	rw	CP0 register 12/7
viewripl	32	0	rw	CP0 register 13/4
nestedexc	32	0	rw	CP0 register 13/5
epc	32	0	rw	CP0 register 14/0
nestedepc	32	0	rw	CP0 register 14/2
prid	32	1a620	rw	CP0 register 15/0
ebase	32	80000000	rw	CP0 register 15/1
config	32	a4018582	rw	CP0 register 16/0
config1	32	8e000002	rw	CP0 register 16/1
config2	32	80000000	rw	CP0 register 16/2
config3	32	8ca2b020	rw	CP0 register 16/3
config4	32	a00c0000	rw	CP0 register 16/4
config5	32	1	rw	CP0 register 16/5
config6	32	0	rw	CP0 register 16/6
config7	32	80000000	rw	CP0 register 16/7
debug	32	2028000	rw	CP0 register 23/0
depc	32	0	rw	CP0 register 24/0

errorepc	32	0	rw	CP0 register 30/0
desave	32	0	rw	CP0 register 31/0
kscratch1	32	0	rw	CP0 register 31/2
kscratch2	32	0	rw	CP0 register 31/3
guestindex	32	ffffffff	rw	CP0 guest register 0/0
guestrandom	32	ffffffff	rw	CP0 guest register 1/0
guestentrylo0	32	ffffffff	rw	CP0 guest register 2/0
guestentrylo1	32	ffffffff	rw	CP0 guest register 3/0
guestcontext	32	ffffffff	rw	CP0 guest register 4/0
guestuserlocal	32	0	rw	CP0 guest register 4/2
guestpagemask	32	ffffffff	rw	CP0 guest register 5/0
guestpagegrain	32	ffffffff	rw	CP0 guest register 5/1
guestwired	32	ffffffff	rw	CP0 guest register 6/0
guesthwrena	32	0	rw	CP0 guest register 7/0
guestbadvaddr	32	0	rw	CP0 guest register 8/0
guestbadinstr	32	0	rw	CP0 guest register 8/1
guestbadinstrp	32	0	rw	CP0 guest register 8/2
guestcount	32	0	rw	CP0 guest register 9/0
guestentryhi	32	ffffffff	rw	CP0 guest register 10/0
guestguestctl1	32	ffffffff	rw	CP0 guest register 10/4
guestguestctl2	32	ffffffff	rw	CP0 guest register 10/5
guestguestctl3	32	ffffffff	rw	CP0 guest register 10/6
guestcompare	32	0	rw	CP0 guest register 11/0
guestguestctl0ext	32	ffffffff	rw	CP0 guest register 11/4
gueststatus	32	400004	rw	CP0 guest register 12/0
guestintctl	32	e0030000	rw	CP0 guest register 12/1
guestsrsctl	32	0	rw	CP0 guest register 12/2
guestsrsmap	32	ffffffff	rw	CP0 guest register 12/3
guestviewipl	32	0	rw	CP0 guest register 12/4
guestsrsmap2	32	ffffffff	rw	CP0 guest register 12/5
guestguestctl0	32	ffffffff	rw	CP0 guest register 12/6
guestgtoffset	32	ffffffff	rw	CP0 guest register 12/7
guestcause	32	0	rw	CP0 guest register 13/0
guestviewripl	32	0	rw	CP0 guest register 13/4
guestnestedexc	32	0	rw	CP0 guest register 13/5
guestepc	32	0	rw	CP0 guest register 14/0
guestnestedepc	32	0	rw	CP0 guest register 14/2
guestprid	32	ffffffff	rw	CP0 guest register 15/0
guestebase	32	80000000	rw	CP0 guest register 15/1
guestconfig	32	a4018582	rw	CP0 guest register 16/0
guestconfig1	32	80000000	rw	CP0 guest register 16/1
guestconfig2	32	80000000	rw	CP0 guest register 16/2

guestconfig3	32	8c22a020	rw	CP0 guest register 16/3
guestconfig4	32	800c0000	rw	CP0 guest register 16/4
guestconfig5	32	1	rw	CP0 guest register 16/5
guestconfig6	32	0	rw	CP0 guest register 16/6
guestconfig7	32	80000000	rw	CP0 guest register 16/7
guestdebug	32	ffffffff	rw	CP0 guest register 23/0
guestdepc	32	ffffffff	rw	CP0 guest register 24/0
guesterrorepc	32	0	rw	CP0 guest register 30/0
guestdesave	32	ffffffff	rw	CP0 guest register 31/0
guestkscratch1	32	0	rw	CP0 guest register 31/2
guestkscratch2	32	0	rw	CP0 guest register 31/3

12.1.5 Integration_support

Table 13.

Name	Bits	Initial value (Hex)		Description
stop	32	0	rw	write with non-zero to stop processor

#

