Imperas Guide to using Virtual Platforms

Platform Specific Information for imperas.ovpworld.org / QuadArmVersatileExpress

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Author	Imperas Software Limited
Version	20150901.0
Filename	Imperas_Platform_User_Guide_QuadArmVersatileExpress.pdf
Created	26 August 2015
Status	OVP Standard Release

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

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1.0 Virtual Platform: QuadArmVersatileExpress

This document provides the details of the usage of an Imperas OVP Virtual Platform. The first half of the document covers specifics of this particular virtual platform. For more information about Imperas OVP virtual platforms, how they are built and used, please see the later sections in this document.

1.1 Licensing

Open Source Apache 2.0

1.2 Description

This platform models the ARM Versatile Express development board with a CoreTile Express A15x2 (V2P-CA15) Daughterboard.
See the ARM documents DUI0447G_v2m_p1_trm.pdf and DUI0604E_v2p_ca15_tc1_trm.pdf for details of the hardware being modeled.
Note this platform implements the motherboard's 'Cortex-A Series' memory map.

The default processor is an ARM Cortex-A15MPx2, which may be changed.

1.3 Limitations

This platform provides the peripherals required to boot and run Operating Systems such as Linux or Android.
Some of the peripherals are register-only, non-functional models. See the individual peripheral model documentation for details.

CoreSight software debug and trace ports are not modeled.

Remap option not modeled.

The CLCD does not work in Linux

1.4 Location

The QuadArmVersatileExpress virtual platform is located in an Imperas/OVP installation at the VLNV: imperas.ovpworld.org / platform / QuadArmVersatileExpress / 1.0.

2.0 Command Line Control of the Platform

2.1 Built-in Arguments

Table 1. Platform Built-in Arguments

Attribute	Value	Description
allargs	allargs	The Command line parser will accept the complete imperas argument set. Note that this option is ignored in some Imperas products

When running a platform in a Windows or Linux shell several command arguments can be specified.
Typically there is a '-help' command which lists the commands available in the platforms. For example:

```
myplatform.exe -help
```

Some command line arguments require a value to be provided. For example:

```
myplatform.exe -program myimagefile.elf
```

2.2 Platform Specific Command Line Arguments

Table 2. Platform Arguments

Name	Type	Description
zimage	stringvar	Linux zImage file to load using smartLoader
zimageaddr	uns64var	Physical address to load zImage file (default:physicalbase + 0x00010000)
initrd	stringvar	Linux initrd file to load using smartLoader
initrdaddr	uns64var	Physical address to load initrd file (default:physicalbase + 0x00d00000)
linuxsym	stringvar	Linux ELF file with symbolic debug info (CpuManger only)
linuxcmd	stringvar	Linux command line (default: 'mem=2G@0x80000000 raid=noautodetect console=ttyAMA0,38400n8 devtmpfs.mount=0
boardid	int32var	Value to pass to Linux as the boardid (default (0x8e0)
linuxmem	uns64var	Amount of memory allocated to Linux (required in AMP mode)
boot	stringvar	Boot code object file (If specified, smartLoader will jump to this rather than zImage)
image0	stringvar	Image file to load on cpu0
image0addr	uns64var	load address for image on cpu0 (IMAGE0 must be specified)
image0sym	stringvar	Elf file with symbolic debug info for image on cpu0 (IMAGE0 must be specified, CpuManger only)
image1	stringvar	Image file to load on cpu1 to n
image1addr	uns64var	Load address for image on cpu1 to n (IMAGE1 must be specified)
image1sym	stringvar	Elf file with symbolic debug info for image on cpu1 to n (IMAGE1 must be specified, CpuManger only)
uart0port	stringvar	Uart0 port: 'auto' for automatic console, 0 for simulator chosen port #, or number of specific port
uart1port	stringvar	Uart1 port: 'auto' for automatic console, 0 for simulator chosen port #, or number of specific port
nographics	boolvar	Inhibit opening of the lcd graphics window
android	boolvar	Enable android specific configuration options

sdimage	stringvar	File containing SD Card image to load on MultiMedia Card Interace mmc1

3.0 Processor [arm.ovpworld.org/processor/arm/1.0] instance: cpu_0

3.1 Processor model type: 'arm' variant 'Cortex-A15MPx2' definition

Imperas OVP processor models support multiple variants and details of the variants implemented in this model can be found in:
- the Imperas installation located at ImperasLib/source/arm.ovpworld.org/processor/arm/1.0/doc
- the OVP website: OVP_Model_Specific_Information_arm_Cortex-A15MPx2.pdf

3.1.1 Description

ARM Processor Model

3.1.2 Licensing

Usage of binary model under license governing simulator usage.
Note that for models of ARM CPUs the license includes the following terms:
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3.1.3 Limitations

Instruction pipelines are not modeled in any way. All instructions are assumed to complete immediately. This means that instruction barrier instructions (e.g. ISB, CP15ISB) are treated as NOPs, with the exception of any undefined instruction behavior, which is modeled. The model does not implement speculative fetch behavior. The branch cache is not modeled.

Caches and write buffers are not modeled in any way. All loads, fetches and stores complete immediately and in order, and are fully synchronous (as if the memory was of Strongly Ordered or Device-nGnRnE type). Data barrier instructions (e.g. DSB, CP15DSB) are treated as NOPs, with the exception of any undefined instruction behavior, which is modeled. Cache manipulation instructions are implemented as NOPs, with the exception of any undefined instruction behavior, which is modeled.
Real-world timing effects are not modeled: all instructions are assumed to complete in a single cycle.
Performance Monitors are implemented as a register interface only.
TLBs are architecturally-accurate but not device accurate. This means that all TLB maintenance and address translation operations are fully implemented but the cache is larger than in the real device.

3.1.4 Verification

Models have been extensively tested by Imperas. ARM Cortex-A models have been successfully used by customers to simulate SMP Linux, Ubuntu Desktop, VxWorks and ThreadX on Xilinx Zynq virtual platforms.

3.1.5 Features

Large physical address extension is implemented.
Thumb-2 instructions are supported.
Trivial Jazelle extension is implemented.
SIMD instructions are implemented.
NEON is implemented.
VFP is implemented.
Security extensions are implemented (also known as TrustZone). Non-secure accesses can be made visible externally by connecting the processor to a 41-bit physical bus, in which case bits 39..0 give the true physical address and bit 40 is the NS bit.
Virtualization extensions are implemented.
VMSA stage 1 secure, non-secure and Hypervisor address translation is implemented. VMSA stage 2 address translation is implemented.
Generic Timer is present. Use parameter override_timerScaleFactor to specify the counter rate as a fraction of the processor MIPS rate (e.g. 10 implies Generic Timer counters increment once every 10 processor instructions).
GIC block is implemented (GICv2, including security extensions). Accesses to GIC registers can be viewed externally by connecting to the 32-bit GICRegisters bus port. Secure register accesses are at offset 0x0 on this bus; for example, a secure access to GIC register GICD_CTLR can be observed by monitoring address 0x00001000. Non-secure accesses are at offset 0x80000000 on this bus; for example, a non-secure access to GIC register GICD_CTLR can be observed by monitoring address 0x80001000

3.2 Instance Parameters

Several parameters can be specified when a processor is instanced in a platform. For this processor instance 'cpu_0' it has been instanced with the following parameters:

Table 3. Processor Instance 'cpu_0' Parameters (Configurations)

Parameter	Value	Description

endian	little	Select processor endian (big or little)
simulateexceptions	simulateexceptions	Causes the processor simulate exceptions instead of halting
mips	1000	The nominal MIPS for the processor

Table 4. Processor Instance 'cpu_0' Parameters (Attributes)

Parameter Name	Value	Type
variant	Cortex-A15MPx2	
compatibility	ISA	
UAL	1	
override_CBAR	0x2c000000	
override_GICD_TYPER_ITLines	4	

3.3 Memory Map for processor 'cpu_0' bus: 'pBus_0'

Processor instance 'cpu_0' is connected to bus 'pBus_0' using master port 'INSTRUCTION'.
Processor instance 'cpu_0' is connected to bus 'pBus_0' using master port 'DATA'.

Table 5. Memory Map ('cpu_0' / 'pBus_0' [width: 40])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFFF	nor0Bridge_0	bridge
remappable	remappable	clcd_0	LcdPL110
0x8000000	0xBFFFFFF	nor0Remap_0	bridge
0xC000000	0xFFFFFFF	nor1_0	ram
0x1001A000	0x1001AFFF	cf1_0	CompactFlashRegs
0x14000000	0x17FFFFF	sram1_0	ram
0x18000000	0x19FFFFF	vram1_0	ram
0x1A000000	0x1A000FFF	eth0_0	LAN9118
0x1B000000	0x1B00FFFF	usb0_0	ISP1761
0x1C010000	0x1C010FFF	sysRegs_0	VexpressSysRegs
0x1C020000	0x1C020FFF	sysCtrl_0	SysCtrlSP810
0x1C040000	0x1C040FFF	aac1_0	AaciPL041
0x1C050000	0x1C050FFF	mmc1_0	MmciPL181
0x1C060000	0x1C060FFF	kb1_0	KbPL050
0x1C070000	0x1C070FFF	ms1_0	KbPL050
0x1C090000	0x1C090FFF	uart0_0	UartPL011
0x1C0A0000	0x1C0A0FFF	uart1_0	UartPL011
0x1C0B0000	0x1C0B0FFF	uart2_0	UartPL011
0x1C0C0000	0x1C0C0FFF	uart3_0	UartPL011
0x1C0F0000	0x1C0F0FFF	wdt1_0	WdtSP805
0x1C110000	0x1C110FFF	timer01_0	TimerSP804
0x1C120000	0x1C120FFF	timer23_0	TimerSP804
0x1C160000	0x1C160FFF	dvi1_0	SerBusDviRegs
0x1C170000	0x1C170FFF	rtc1_0	RtcPL031
0x1C1B0000	0x1C1B0FFF	uart4_0	UartPL011
0x1C1F0000	0x1C1F0FFF	clcd_0	LcdPL110
0x2B060000	0x2B060FFF	wdt2_0	WdtSP805
0x2B0A0000	0x2B0A0FFF	dmc1_0	DMemCtrlPL341
0x7FFB0000	0x7FFB0FFF	dma0_0	dummyPort

0x7FFD0000	0x7FFD0FFF	smc1_0	SMemCtrlPL354
0x80000000	0xFFFFFFFF	ddr2Bridge_0	bridge
0x800000000	0x87FFFFFF	ddr2Remap1_0	bridge
0x880000000	0x8FFFFFFF	ddr2Remap2_0	bridge
0x8000000000	0x807FFFFFF	ddr2Remap3_0	bridge
0x8080000000	0x80FFFFFFF	ddr2Remap4_0	bridge

Table 6. Bridged Memory Map ('cpu_0' / 'nor0Bridge_0' / 'nor0bus_0' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFFF	nor0_0	ram

Table 7. Bridged Memory Map ('cpu_0' / 'nor0Remap_0' / 'nor0bus_0' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFFF	nor0_0	ram

Table 8. Bridged Memory Map ('cpu_0' / 'ddr2Bridge_0' / 'ddr2bus_0' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFF	ddr2ram_0	ram

Table 9. Bridged Memory Map ('cpu_0' / 'ddr2Remap1_0' / 'ddr2bus_0' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFF	ddr2ram_0	ram

Table 10. Bridged Memory Map ('cpu_0' / 'ddr2Remap2_0' / 'ddr2bus_0' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFF	ddr2ram_0	ram

Table 11. Bridged Memory Map ('cpu_0' / 'ddr2Remap3_0' / 'ddr2bus_0' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFF	ddr2ram_0	ram

Table 12. Bridged Memory Map ('cpu_0' / 'ddr2Remap4_0' / 'ddr2bus_0' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFF	ddr2ram_0	ram

3.4 Net Connections to processor: 'cpu_0'

Table 13. Processor Net Connections ('cpu_0')

Net Port	Net	Instance	Component
SPI34	ir2_0	timer01_0	TimerSP804

SPI35	ir3_0	timer23_0	TimerSP804
SPI36	ir4_0	rtc1_0	RtcPL031
SPI37	ir5_0	uart0_0	UartPL011
SPI38	ir6_0	uart1_0	UartPL011
SPI39	ir7_0	uart2_0	UartPL011
SPI40	ir8_0	uart3_0	UartPL011
SPI41	ir9_0	mmc1_0	MmciPL181
SPI42	ir10_0	mmc1_0	MmciPL181
SPI44	ir12_0	kb1_0	KbPL050
SPI45	ir13_0	ms1_0	KbPL050
SPI46	ir14_0	clcd_0	LcdPL110
SPI47	ir15_0	eth0_0	LAN9118
SPI48	ir16_0	usb0_0	ISP1761

4.0 Processor [arm.ovpworld.org/processor/arm/1.0] instance: cpu_1

4.1 Processor model type: 'arm' variant 'Cortex-A15MPx2' definition

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ARM Processor Model

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4.1.3 Limitations

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Caches and write buffers are not modeled in any way. All loads, fetches and stores complete immediately and in order, and are fully synchronous (as if the memory was of Strongly Ordered or Device-nGnRnE type). Data barrier instructions (e.g. DSB, CP15DSB) are treated as NOPs, with the exception of any undefined instruction behavior, which is modeled. Cache manipulation instructions are implemented as NOPs, with the exception of any undefined instruction behavior, which is modeled.
Real-world timing effects are not modeled: all instructions are assumed to complete in a single cycle.
Performance Monitors are implemented as a register interface only.
TLBs are architecturally-accurate but not device accurate. This means that all TLB maintenance and address translation operations are fully implemented but the cache is larger than in the real device.

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SIMD instructions are implemented.
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Security extensions are implemented (also known as TrustZone). Non-secure accesses can be made visible externally by connecting the processor to a 41-bit physical bus, in which case bits 39..0 give the true physical address and bit 40 is the NS bit.
Virtualization extensions are implemented.
VMSA stage 1 secure, non-secure and Hypervisor address translation is implemented. VMSA stage 2 address translation is implemented.
Generic Timer is present. Use parameter override_timerScaleFactor to specify the counter rate as a fraction of the processor MIPS rate (e.g. 10 implies Generic Timer counters increment once every 10 processor instructions).
GIC block is implemented (GICv2, including security extensions). Accesses to GIC registers can be viewed externally by connecting to the 32-bit GICRegisters bus port. Secure register accesses are at offset 0x0 on

this bus; for example, a secure access to GIC register GICD_CTLR can be observed by monitoring address 0x00001000. Non-secure accesses are at offset 0x80000000 on this bus; for example, a non-secure access to GIC register GICD_CTLR can be observed by monitoring address 0x80001000

4.2 Instance Parameters

Several parameters can be specified when a processor is instanced in a platform. For this processor instance 'cpu_1' it has been instanced with the following parameters:

Table 14. Processor Instance 'cpu_1' Parameters (Configurations)

Parameter	Value	Description
endian	little	Select processor endian (big or little)
simulateexceptions	simulateexceptions	Causes the processor simulate exceptions instead of halting
mips	1000	The nominal MIPS for the processor

Table 15. Processor Instance 'cpu_1' Parameters (Attributes)

Parameter Name	Value	Type
variant	Cortex-A15MPx2	
compatibility	ISA	
UAL	1	
override_CBAR	0x2c000000	
override_GICD_TYPER_ITLines	4	

4.3 Memory Map for processor 'cpu_1' bus: 'pBus_1'

Processor instance 'cpu_1' is connected to bus 'pBus_1' using master port 'INSTRUCTION'.
Processor instance 'cpu_1' is connected to bus 'pBus_1' using master port 'DATA'.

Table 16. Memory Map ('cpu_1' / 'pBus_1' [width: 40])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFFF	nor0Bridge_1	bridge
remappable	remappable	clcd_1	LcdPL110
0x8000000	0xBFFFFFF	nor0Remap_1	bridge
0xC000000	0xFFFFFFF	nor1_1	ram
0x1001A000	0x1001AFFF	cf1_1	CompactFlashRegs
0x14000000	0x17FFFFF	sram1_1	ram
0x18000000	0x19FFFFF	vram1_1	ram
0x1A000000	0x1A000FFF	eth0_1	LAN9118
0x1B000000	0x1B00FFFF	usb0_1	ISP1761
0x1C010000	0x1C010FFF	sysRegs_1	VexpressSysRegs
0x1C020000	0x1C020FFF	sysCtrl_1	SysCtrlSP810
0x1C040000	0x1C040FFF	aac1_1	AaciPL041
0x1C050000	0x1C050FFF	mmc1_1	MmciPL181
0x1C060000	0x1C060FFF	kb1_1	KbPL050
0x1C070000	0x1C070FFF	ms1_1	KbPL050
0x1C090000	0x1C090FFF	uart0_1	UartPL011
0x1C0A0000	0x1C0A0FFF	uart1_1	UartPL011
0x1C0B0000	0x1C0B0FFF	uart2_1	UartPL011

0x1C0C0000	0x1C0C0FFF	uart3_1	UartPL011
0x1C0F0000	0x1C0F0FFF	wdt1_1	WdtSP805
0x1C110000	0x1C110FFF	timer01_1	TimerSP804
0x1C120000	0x1C120FFF	timer23_1	TimerSP804
0x1C160000	0x1C160FFF	dvi1_1	SerBusDviRegs
0x1C170000	0x1C170FFF	rtc1_1	RtcPL031
0x1C1B0000	0x1C1B0FFF	uart4_1	UartPL011
0x1C1F0000	0x1C1F0FFF	clcd_1	LcdPL110
0x2B060000	0x2B060FFF	wdt2_1	WdtSP805
0x2B0A0000	0x2B0A0FFF	dmc1_1	DMemCtrlPL341
0x7FFB0000	0x7FFB0FFF	dma0_1	dummyPort
0x7FFD0000	0x7FFD0FFF	smc1_1	SMemCtrlPL354
0x80000000	0xFFFFFFFF	ddr2Bridge_1	bridge
0x800000000	0x87FFFFFF	ddr2Remap1_1	bridge
0x880000000	0x8FFFFFFF	ddr2Remap2_1	bridge
0x8000000000	0x807FFFFFF	ddr2Remap3_1	bridge
0x8080000000	0x80FFFFFFF	ddr2Remap4_1	bridge

Table 17. Bridged Memory Map ('cpu_1' / 'nor0Bridge_1' / 'nor0bus_1' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFF	nor0_1	ram

Table 18. Bridged Memory Map ('cpu_1' / 'nor0Remap_1' / 'nor0bus_1' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFF	nor0_1	ram

Table 19. Bridged Memory Map ('cpu_1' / 'ddr2Bridge_1' / 'ddr2bus_1' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFF	ddr2ram_1	ram

Table 20. Bridged Memory Map ('cpu_1' / 'ddr2Remap1_1' / 'ddr2bus_1' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFF	ddr2ram_1	ram

Table 21. Bridged Memory Map ('cpu_1' / 'ddr2Remap2_1' / 'ddr2bus_1' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFF	ddr2ram_1	ram

Table 22. Bridged Memory Map ('cpu_1' / 'ddr2Remap3_1' / 'ddr2bus_1' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFF	ddr2ram_1	ram

Table 23. Bridged Memory Map ('cpu_1' / 'ddr2Remap4_1' / 'ddr2bus_1' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFFF	ddr2ram_1	ram

4.4 Net Connections to processor: 'cpu_1'

Table 24. Processor Net Connections ('cpu_1')

Net Port	Net	Instance	Component
SPI34	ir2_1	timer01_1	TimerSP804
SPI35	ir3_1	timer23_1	TimerSP804
SPI36	ir4_1	rtc1_1	RtcPL031
SPI37	ir5_1	uart0_1	UartPL011
SPI38	ir6_1	uart1_1	UartPL011
SPI39	ir7_1	uart2_1	UartPL011
SPI40	ir8_1	uart3_1	UartPL011
SPI41	ir9_1	mmc1_1	MmciPL181
SPI42	ir10_1	mmc1_1	MmciPL181
SPI44	ir12_1	kb1_1	KbPL050
SPI45	ir13_1	ms1_1	KbPL050
SPI46	ir14_1	clcd_1	LcdPL110
SPI47	ir15_1	eth0_1	LAN9118
SPI48	ir16_1	usb0_1	ISP1761

5.0 Processor [arm.ovpworld.org/processor/arm/1.0] instance: cpu_2

5.1 Processor model type: 'arm' variant 'Cortex-A15MPx2' definition

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ARM Processor Model

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In the case of any Licensee who is either or both an academic or educational institution the purposes shall be limited to internal use.
Except to the extent that such activity is permitted by applicable law, Licensee shall not reverse engineer, decompile, or disassemble this model. If this model was provided to Licensee in Europe, Licensee shall not reverse engineer, decompile or disassemble the Model for the purposes of error correction.
The License agreement does not entitle Licensee to manufacture in silicon any product based on this model.
The License agreement does not entitle Licensee to use this model for evaluating the validity of any ARM patent.
Source of model available under separate Imperas Software License Agreement.

5.1.3 Limitations

Instruction pipelines are not modeled in any way. All instructions are assumed to complete immediately. This means that instruction barrier instructions (e.g. ISB, CP15ISB) are treated as NOPs, with the exception of any undefined instruction behavior, which is modeled. The model does not implement speculative fetch behavior. The branch cache is not modeled.
Caches and write buffers are not modeled in any way. All loads, fetches and stores complete immediately and in order, and are fully synchronous (as if the memory was of Strongly Ordered or Device-nGnRnE type). Data barrier instructions (e.g. DSB, CP15DSB) are treated as NOPs, with the exception of any undefined instruction behavior, which is modeled. Cache manipulation instructions are implemented as NOPs, with the exception of any undefined instruction behavior, which is modeled.
Real-world timing effects are not modeled: all instructions are assumed to complete in a single cycle.
Performance Monitors are implemented as a register interface only.
TLBs are architecturally-accurate but not device accurate. This means that all TLB maintenance and address translation operations are fully implemented but the cache is larger than in the real device.

5.1.4 Verification

Models have been extensively tested by Imperas. ARM Cortex-A models have been successfully used by customers to simulate SMP Linux, Ubuntu Desktop, VxWorks and ThreadX on Xilinx Zynq virtual platforms.

5.1.5 Features

Large physical address extension is implemented.
Thumb-2 instructions are supported.
Trivial Jazelle extension is implemented.
SIMD instructions are implemented.
NEON is implemented.
VFP is implemented.
Security extensions are implemented (also known as TrustZone). Non-secure accesses can be made visible

externally by connecting the processor to a 41-bit physical bus, in which case bits 39..0 give the true physical address and bit 40 is the NS bit.
Virtualization extensions are implemented.
VMSA stage 1 secure, non-secure and Hypervisor address translation is implemented. VMSA stage 2 address translation is implemented.
Generic Timer is present. Use parameter override_timerScaleFactor to specify the counter rate as a fraction of the processor MIPS rate (e.g. 10 implies Generic Timer counters increment once every 10 processor instructions).
GIC block is implemented (GICv2, including security extensions). Accesses to GIC registers can be viewed externally by connecting to the 32-bit GICRegisters bus port. Secure register accesses are at offset 0x0 on this bus; for example, a secure access to GIC register GICD_CTLR can be observed by monitoring address 0x00001000. Non-secure accesses are at offset 0x80000000 on this bus; for example, a non-secure access to GIC register GICD_CTLR can be observed by monitoring address 0x80001000

5.2 Instance Parameters

Several parameters can be specified when a processor is instanced in a platform. For this processor instance 'cpu_2' it has been instanced with the following parameters:

Table 25. Processor Instance 'cpu_2' Parameters (Configurations)

Parameter	Value	Description
endian	little	Select processor endian (big or little)
simulateexceptions	simulateexceptions	Causes the processor simulate exceptions instead of halting
mips	1000	The nominal MIPS for the processor

Table 26. Processor Instance 'cpu_2' Parameters (Attributes)

Parameter Name	Value	Type
variant	Cortex-A15MPx2	
compatibility	ISA	
UAL	1	
override_CBAR	0x2c000000	
override_GICD_TYPER_ITLines	4	

5.3 Memory Map for processor 'cpu_2' bus: 'pBus_2'

Processor instance 'cpu_2' is connected to bus 'pBus_2' using master port 'INSTRUCTION'.
Processor instance 'cpu_2' is connected to bus 'pBus_2' using master port 'DATA'.

Table 27. Memory Map ('cpu_2' / 'pBus_2' [width: 40])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFF	nor0Bridge_2	bridge
remappable	remappable	clcd_2	LcdPL110
0x8000000	0xBFFFFFF	nor0Remap_2	bridge
0xC000000	0xFFFFFFF	nor1_2	ram
0x1001A000	0x1001AFFF	cf1_2	CompactFlashRegs
0x14000000	0x17FFFFF	sram1_2	ram
0x18000000	0x19FFFFF	vram1_2	ram

0x1A000000	0x1A000FFF	eth0_2	LAN9118
0x1B000000	0x1B00FFFF	usb0_2	ISP1761
0x1C010000	0x1C010FFF	sysRegs_2	VexpressSysRegs
0x1C020000	0x1C020FFF	sysCtrl_2	SysCtrlSP810
0x1C040000	0x1C040FFF	aac1_2	AaciPL041
0x1C050000	0x1C050FFF	mmc1_2	MmciPL181
0x1C060000	0x1C060FFF	kb1_2	KbPL050
0x1C070000	0x1C070FFF	ms1_2	KbPL050
0x1C090000	0x1C090FFF	uart0_2	UartPL011
0x1C0A0000	0x1C0A0FFF	uart1_2	UartPL011
0x1C0B0000	0x1C0B0FFF	uart2_2	UartPL011
0x1C0C0000	0x1C0C0FFF	uart3_2	UartPL011
0x1C0F0000	0x1C0F0FFF	wdt1_2	WdtSP805
0x1C110000	0x1C110FFF	timer01_2	TimerSP804
0x1C120000	0x1C120FFF	timer23_2	TimerSP804
0x1C160000	0x1C160FFF	dvi1_2	SerBusDviRegs
0x1C170000	0x1C170FFF	rtc1_2	RtcPL031
0x1C1B0000	0x1C1B0FFF	uart4_2	UartPL011
0x1C1F0000	0x1C1F0FFF	clcd_2	LcdPL110
0x2B060000	0x2B060FFF	wdt2_2	WdtSP805
0x2B0A0000	0x2B0A0FFF	dmc1_2	DMemCtrlPL341
0x7FFB0000	0x7FFB0FFF	dma0_2	dummyPort
0x7FFD0000	0x7FFD0FFF	smc1_2	SMemCtrlPL354
0x80000000	0xFFFFFFFF	ddr2Bridge_2	bridge
0x800000000	0x87FFFFFF	ddr2Remap1_2	bridge
0x880000000	0x8FFFFFFF	ddr2Remap2_2	bridge
0x8000000000	0x807FFFFFF	ddr2Remap3_2	bridge
0x8080000000	0x80FFFFFFF	ddr2Remap4_2	bridge

Table 28. Bridged Memory Map ('cpu_2' / 'nor0Bridge_2' / 'nor0bus_2' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFF	nor0_2	ram

Table 29. Bridged Memory Map ('cpu_2' / 'nor0Remap_2' / 'nor0bus_2' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFF	nor0_2	ram

Table 30. Bridged Memory Map ('cpu_2' / 'ddr2Bridge_2' / 'ddr2bus_2' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFF	ddr2ram_2	ram

Table 31. Bridged Memory Map ('cpu_2' / 'ddr2Remap1_2' / 'ddr2bus_2' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFF	ddr2ram_2	ram

Table 32. Bridged Memory Map ('cpu_2' / 'ddr2Remap2_2' / 'ddr2bus_2' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFFF	ddr2ram_2	ram

Table 33. Bridged Memory Map ('cpu_2' / 'ddr2Remap3_2' / 'ddr2bus_2' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFFF	ddr2ram_2	ram

Table 34. Bridged Memory Map ('cpu_2' / 'ddr2Remap4_2' / 'ddr2bus_2' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFFF	ddr2ram_2	ram

5.4 Net Connections to processor: 'cpu_2'

Table 35. Processor Net Connections ('cpu_2')

Net Port	Net	Instance	Component
SPI34	ir2_2	timer01_2	TimerSP804
SPI35	ir3_2	timer23_2	TimerSP804
SPI36	ir4_2	rtc1_2	RtcPL031
SPI37	ir5_2	uart0_2	UartPL011
SPI38	ir6_2	uart1_2	UartPL011
SPI39	ir7_2	uart2_2	UartPL011
SPI40	ir8_2	uart3_2	UartPL011
SPI41	ir9_2	mmc1_2	MmciPL181
SPI42	ir10_2	mmc1_2	MmciPL181
SPI44	ir12_2	kb1_2	KbPL050
SPI45	ir13_2	ms1_2	KbPL050
SPI46	ir14_2	clcd_2	LcdPL110
SPI47	ir15_2	eth0_2	LAN9118
SPI48	ir16_2	usb0_2	ISP1761

6.0 Processor [arm.ovpworld.org/processor/arm/1.0] instance: cpu_3

6.1 Processor model type: 'arm' variant 'Cortex-A15MPx2' definition

Imperas OVP processor models support multiple variants and details of the variants implemented in this model can be found in:
- the Imperas installation located at ImperasLib/source/arm.ovpworld.org/processor/arm/1.0/doc
- the OVP website: OVP_Model_Specific_Information_arm_Cortex-A15MPx2.pdf

6.1.1 Description

ARM Processor Model

6.1.2 Licensing

Usage of binary model under license governing simulator usage.
Note that for models of ARM CPUs the license includes the following terms:
Licensee is granted a non-exclusive, worldwide, non-transferable, revocable licence to:
If no source is being provided to the Licensee: use and copy only (no modifications rights are granted) the model for the sole purpose of designing, developing, analyzing, debugging, testing, verifying, validating and optimizing software which: (a) (i) is for ARM based systems; and (ii) does not incorporate the ARM Models or any part thereof; and (b) such ARM Models may not be used to emulate an ARM based system to run application software in a production or live environment.
If source code is being provided to the Licensee: use, copy and modify the model for the sole purpose of designing, developing, analyzing, debugging, testing, verifying, validating and optimizing software which: (a) (i) is for ARM based systems; and (ii) does not incorporate the ARM Models or any part thereof; and (b) such ARM Models may not be used to emulate an ARM based system to run application software in a production or live environment.
In the case of any Licensee who is either or both an academic or educational institution the purposes shall be limited to internal use.
Except to the extent that such activity is permitted by applicable law, Licensee shall not reverse engineer, decompile, or disassemble this model. If this model was provided to Licensee in Europe, Licensee shall not reverse engineer, decompile or disassemble the Model for the purposes of error correction.
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The License agreement does not entitle Licensee to use this model for evaluating the validity of any ARM patent.
Source of model available under separate Imperas Software License Agreement.

6.1.3 Limitations

Instruction pipelines are not modeled in any way. All instructions are assumed to complete immediately. This means that instruction barrier instructions (e.g. ISB, CP15ISB) are treated as NOPs, with the exception of any undefined instruction behavior, which is modeled. The model does not implement speculative fetch behavior. The branch cache is not modeled.
Caches and write buffers are not modeled in any way. All loads, fetches and stores complete immediately and in order, and are fully synchronous (as if the memory was of Strongly Ordered or Device-nGnRnE type). Data barrier instructions (e.g. DSB, CP15DSB) are treated as NOPs, with the exception of any undefined instruction behavior, which is modeled. Cache manipulation instructions are implemented as NOPs, with the exception of any undefined instruction behavior, which is modeled.
Real-world timing effects are not modeled: all instructions are assumed to complete in a single cycle.
Performance Monitors are implemented as a register interface only.
TLBs are architecturally-accurate but not device accurate. This means that all TLB maintenance and address translation operations are fully implemented but the cache is larger than in the real device.

6.1.4 Verification

Models have been extensively tested by Imperas. ARM Cortex-A models have been successfully used by customers to simulate SMP Linux, Ubuntu Desktop, VxWorks and ThreadX on Xilinx Zynq virtual platforms.

6.1.5 Features

Large physical address extension is implemented.
Thumb-2 instructions are supported.
Trivial Jazelle extension is implemented.
SIMD instructions are implemented.
NEON is implemented.
VFP is implemented.
Security extensions are implemented (also known as TrustZone). Non-secure accesses can be made visible externally by connecting the processor to a 41-bit physical bus, in which case bits 39..0 give the true physical address and bit 40 is the NS bit.
Virtualization extensions are implemented.
VMSA stage 1 secure, non-secure and Hypervisor address translation is implemented. VMSA stage 2 address translation is implemented.
Generic Timer is present. Use parameter override_timerScaleFactor to specify the counter rate as a fraction of the processor MIPS rate (e.g. 10 implies Generic Timer counters increment once every 10 processor instructions).
GIC block is implemented (GICv2, including security extensions). Accesses to GIC registers can be viewed externally by connecting to the 32-bit GICRegisters bus port. Secure register accesses are at offset 0x0 on this bus; for example, a secure access to GIC register GICD_CTLR can be observed by monitoring address 0x00001000. Non-secure accesses are at offset 0x80000000 on this bus; for example, a non-secure access to GIC register GICD_CTLR can be observed by monitoring address 0x80001000

6.2 Instance Parameters

Several parameters can be specified when a processor is instanced in a platform. For this processor instance 'cpu_3' it has been instanced with the following parameters:

Table 36. Processor Instance 'cpu_3' Parameters (Configurations)

Parameter	Value	Description
endian	little	Select processor endian (big or little)
simulateexceptions	simulateexceptions	Causes the processor simulate exceptions instead of halting
mips	1000	The nominal MIPS for the processor

Table 37. Processor Instance 'cpu_3' Parameters (Attributes)

Parameter Name	Value	Type
variant	Cortex-A15MPx2	
compatibility	ISA	
UAL	1	
override_CBAR	0x2c000000	
override_GICD_TYPER_ITLines	4	

6.3 Memory Map for processor 'cpu_3' bus: 'pBus_3'

Processor instance 'cpu_3' is connected to bus 'pBus_3' using master port 'INSTRUCTION'.
Processor instance 'cpu_3' is connected to bus 'pBus_3' using master port 'DATA'.

Table 38. Memory Map ('cpu_3' / 'pBus_3' [width: 40])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFFF	nor0Bridge_3	bridge
remappable	remappable	clcd_3	LcdPL110
0x8000000	0xBFFFFFF	nor0Remap_3	bridge
0xC000000	0xFFFFFFF	nor1_3	ram
0x1001A000	0x1001AFFF	cf1_3	CompactFlashRegs
0x14000000	0x17FFFFF	sram1_3	ram
0x18000000	0x19FFFFF	vram1_3	ram
0x1A000000	0x1A000FFF	eth0_3	LAN9118
0x1B000000	0x1B00FFFF	usb0_3	ISP1761
0x1C010000	0x1C010FFF	sysRegs_3	VexpressSysRegs
0x1C020000	0x1C020FFF	sysCtrl_3	SysCtrlSP810
0x1C040000	0x1C040FFF	aac1_3	AaciPL041
0x1C050000	0x1C050FFF	mmc1_3	MmciPL181
0x1C060000	0x1C060FFF	kb1_3	KbPL050
0x1C070000	0x1C070FFF	ms1_3	KbPL050
0x1C090000	0x1C090FFF	uart0_3	UartPL011
0x1C0A0000	0x1C0A0FFF	uart1_3	UartPL011
0x1C0B0000	0x1C0B0FFF	uart2_3	UartPL011
0x1C0C0000	0x1C0C0FFF	uart3_3	UartPL011
0x1C0F0000	0x1C0F0FFF	wdt1_3	WdtSP805
0x1C110000	0x1C110FFF	timer01_3	TimerSP804
0x1C120000	0x1C120FFF	timer23_3	TimerSP804
0x1C160000	0x1C160FFF	dvi1_3	SerBusDviRegs
0x1C170000	0x1C170FFF	rtc1_3	RtcPL031
0x1C1B0000	0x1C1B0FFF	uart4_3	UartPL011
0x1C1F0000	0x1C1F0FFF	clcd_3	LcdPL110
0x2B060000	0x2B060FFF	wdt2_3	WdtSP805
0x2B0A0000	0x2B0A0FFF	dmc1_3	DMemCtrlPL341
0x7FFB0000	0x7FFB0FFF	dma0_3	dummyPort
0x7FFD0000	0x7FFD0FFF	smc1_3	SMemCtrlPL354
0x80000000	0xFFFFFFFF	ddr2Bridge_3	bridge
0x800000000	0x87FFFFFFF	ddr2Remap1_3	bridge
0x880000000	0x8FFFFFFFF	ddr2Remap2_3	bridge
0x8000000000	0x807FFFFFFF	ddr2Remap3_3	bridge
0x8080000000	0x80FFFFFFFF	ddr2Remap4_3	bridge

Table 39. Bridged Memory Map ('cpu_3' / 'nor0Bridge_3' / 'nor0bus_3' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFFF	nor0_3	ram

Table 40. Bridged Memory Map ('cpu_3' / 'nor0Remap_3' / 'nor0bus_3' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x3FFFFFF	nor0_3	ram

Table 41. Bridged Memory Map ('cpu_3' / 'ddr2Bridge_3' / 'ddr2bus_3' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFFF	ddr2ram_3	ram

Table 42. Bridged Memory Map ('cpu_3' / 'ddr2Remap1_3' / 'ddr2bus_3' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFFF	ddr2ram_3	ram

Table 43. Bridged Memory Map ('cpu_3' / 'ddr2Remap2_3' / 'ddr2bus_3' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFFF	ddr2ram_3	ram

Table 44. Bridged Memory Map ('cpu_3' / 'ddr2Remap3_3' / 'ddr2bus_3' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFFF	ddr2ram_3	ram

Table 45. Bridged Memory Map ('cpu_3' / 'ddr2Remap4_3' / 'ddr2bus_3' [width: 32])

Lo Address	Hi Address	Instance	Component
0x0	0x7FFFFFFF	ddr2ram_3	ram

6.4 Net Connections to processor: 'cpu_3'

Table 46. Processor Net Connections ('cpu_3')

Net Port	Net	Instance	Component
SPI34	ir2_3	timer01_3	TimerSP804
SPI35	ir3_3	timer23_3	TimerSP804
SPI36	ir4_3	rtc1_3	RtcPL031
SPI37	ir5_3	uart0_3	UartPL011
SPI38	ir6_3	uart1_3	UartPL011
SPI39	ir7_3	uart2_3	UartPL011
SPI40	ir8_3	uart3_3	UartPL011
SPI41	ir9_3	mmc1_3	MmciPL181
SPI42	ir10_3	mmc1_3	MmciPL181
SPI44	ir12_3	kb1_3	KbPL050
SPI45	ir13_3	ms1_3	KbPL050
SPI46	ir14_3	clcd_3	LcdPL110
SPI47	ir15_3	eth0_3	LAN9118
SPI48	ir16_3	usb0_3	ISP1761

7.0 Peripheral Instances

7.1 Peripheral [smsc.ovpworld.org/peripheral/LAN9118/1.0] instance: eth0_0

7.1.1 Description
Fully functional Model of SMSC LAN9118 for Arm Versatile Express platforms. For full details please consult README-EMAC.txt

7.1.2 Licensing
Open Source Apache 2.0

7.1.3 Limitations
See README-EMAC.txt

7.1.4 Reference
SMSC LAN9118 High Performance single-chip 10/100 Non-PCI Ethernet Controller Datasheet Revision 1.5 (07-11-08)

There are no configuration options set for this peripheral instance.

7.2 Peripheral [philips.ovpworld.org/peripheral/ISP1761/1.0] instance: usb0_0

7.2.1 Description
Functional Model of USB Phillips ISP1761 for Arm Versatile Explress platforms. For full details please consult README-OTG.txt

7.2.2 Licensing
Open Source Apache 2.0

7.2.3 Limitations
- Only host mode is supported. - DMA modes are not supported for the moment, only the mandatory slave mode is implemented. - Control and bulk transfer types are currently implemented. No interrupt and isochronous transfers yet. - Tested only the attachment of a single host device. The HSOTG controller's root hub has a single port, so only one device can be attached to it. This device could be a hub, though. Currently we support only one non-hub device. - Hot plug events are currently unsupported.

7.2.4 Reference
Philips/NXP

There are no configuration options set for this peripheral instance.

7.3 Peripheral [arm.ovpworld.org/peripheral/VexpressSysRegs/1.0] instance: sysRegs_0

7.3.1 Description
ARM Versatile Express System Registers

7.3.2 Limitations
Only select registers are modeled. See user.c for details.

7.3.3 Reference
A

7.3.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.4 Peripheral [arm.ovpworld.org/peripheral/SysCtrlSP810/1.0] instance: sysCtrl_0

7.4.1 Description
ARM SP810 System Control Registers

7.4.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.4.3 Reference
ARM PrimeCell System Controller (SP810) Technical Reference Manual (ARM DDI 0254)

7.4.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.5 Peripheral [arm.ovpworld.org/peripheral/AaciPL041/1.0] instance: aac1_0

7.5.1 Description
ARM PL041 PrimeCell Advanced Audio CODEC Interface Registers

7.5.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.5.3 Reference
ARM PrimeCell Advanced Audio CODEC Interface (PL041) Technical Reference Manual (ARM DDI 0173)

7.5.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.6 Peripheral [arm.ovpworld.org/peripheral/MmciPL181/1.0] instance: mmc1_0

7.6.1 Description
ARM PrimeCell Multimedia Card Interface (MMCI)

7.6.2 Limitations
None

7.6.3 Licensing
Open Source Apache 2.0

7.6.4 Reference
ARM PrimeCell Multimedia Card Interface (Pl180) Technical Reference Manual (ARM DDI 0172)

There are no configuration options set for this peripheral instance.

7.7 Peripheral [arm.ovpworld.org/peripheral/KbPL050/1.0] instance: kb1_0

7.7.1 Description
ARM PL050 PS2 Keyboard or mouse controller

7.7.2 Limitations
None

7.7.3 Reference
ARM PrimeCell PS2 Keyboard/Mouse Interface (PL050) Technical Reference Manual (ARM DDI 0143)

7.7.4 Licensing
Open Source Apache 2.0

Table 47. Configuration options (attributes) set for instance 'kb1_0'

Attributes	Value
isKeyboard	1
grabDisable	1

7.8 Peripheral [arm.ovpworld.org/peripheral/KbPL050/1.0] instance: ms1_0

7.8.1 Description
ARM PL050 PS2 Keyboard or mouse controller

7.8.2 Limitations
None

7.8.3 Reference
ARM PrimeCell PS2 Keyboard/Mouse Interface (PL050) Technical Reference Manual (ARM DDI 0143)

7.8.4 Licensing
Open Source Apache 2.0

Table 48. Configuration options (attributes) set for instance 'ms1_0'

Attributes	Value
isMouse	1
grabDisable	1

7.9 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart0_0

7.9.1 Description
ARM PL011 UART

7.9.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.9.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.9.4 Licensing
Open Source Apache 2.0

Table 49. Configuration options (attributes) set for instance 'uart0_0'

Attributes	Value
variant	ARM
outfile	uart0_0.log
finishOnDisconnect	1

7.10 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart1_0

7.10.1 Description
ARM PL011 UART

7.10.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as

baud rates etc.

7.10.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.10.4 Licensing
Open Source Apache 2.0

Table 50. Configuration options (attributes) set for instance 'uart1_0'

Attributes	Value
variant	ARM
outfile	uart1_0.log

7.11 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart2_0

7.11.1 Description
ARM PL011 UART

7.11.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.11.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.11.4 Licensing
Open Source Apache 2.0

Table 51. Configuration options (attributes) set for instance 'uart2_0'

Attributes	Value
variant	ARM

7.12 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart3_0

7.12.1 Description
ARM PL011 UART

7.12.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.12.3 Reference

ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.12.4 Licensing
Open Source Apache 2.0

Table 52. Configuration options (attributes) set for instance 'uart3_0'

Attributes	Value
variant	ARM

7.13 Peripheral [arm.ovpworld.org/peripheral/WdtSP805/1.0] instance: wdt1_0

7.13.1 Description
ARM SP805 Watchdog Registers.

7.13.2 Limitations
Does NOT model watchdog functionality, just provides registers to allow code to run.

7.13.3 Reference
ARM Watchdog Module (SP805) Technical Reference Manual (ARM DDI 0270)

7.13.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.14 Peripheral [arm.ovpworld.org/peripheral/TimerSP804/1.0] instance: timer01_0

7.14.1 Description
Timer SP804 Module

7.14.2 Licensing
Open Source Apache 2.0

7.14.3 Limitations
none

7.14.4 Reference
ARM Dual-Timer Module (SP804) Technical Reference Manual (ARM DDI 0271)

There are no configuration options set for this peripheral instance.

7.15 Peripheral [arm.ovpworld.org/peripheral/TimerSP804/1.0] instance: timer23_0

7.15.1 Description
Timer SP804 Module

7.15.2 Licensing
Open Source Apache 2.0

7.15.3 Limitations
none

7.15.4 Reference
ARM Dual-Timer Module (SP804) Technical Reference Manual (ARM DDI 0271)

There are no configuration options set for this peripheral instance.

7.16 Peripheral [arm.ovpworld.org/peripheral/SerBusDviRegs/1.0] instance: dvi1_0

7.16.1 Description
Versatile Express Serial Bus DVI Registers

7.16.2 Licensing
Open Source Apache 2.0

7.16.3 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.16.4 Reference
A

There are no configuration options set for this peripheral instance.

7.17 Peripheral [arm.ovpworld.org/peripheral/RtcPL031/1.0] instance: rtc1_0

7.17.1 Description
ARM PL031 Real Time Clock (RTC)

7.17.2 Limitations
none

7.17.3 Reference
ARM PrimeCell Real Time Clock (PL031) Technical Reference Manual (ARM DDI 0224)

7.17.4 Licensing

Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.18 Peripheral [arm.ovpworld.org/peripheral/CompactFlashRegs/1.0] instance: cf1_0

7.18.1 Description
ARM Versatile Express Compact Flash Interface Registers

7.18.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.18.3 Reference
ARM Motherboard Express uATX (V2M-P1) Technical Reference Manual (ARM DDI 0447)

7.18.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.19 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart4_0

7.19.1 Description
ARM PL011 UART

7.19.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.19.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.19.4 Licensing
Open Source Apache 2.0

Table 53. Configuration options (attributes) set for instance 'uart4_0'

Attributes	Value
variant	ARM

7.20 Peripheral [arm.ovpworld.org/peripheral/LcdPL110/1.0] instance: clcd_0

7.20.1 Description

ARM PL110 LCD Controller

7.20.2 Limitations

The VGA display refresh is not optimised resulting in the VGA peripheral causing a limit on the maximum performance of a platform it contains to be around 300 MIPS (actual dependent upon refresh rate of LCD).
The LCD peripheral utilises memory watchpoints to optimise display refresh. This requires the use of ICM memory for the frame buffers, which currently may stop its use in SystemC TLM2 platforms.
Interrupts are not supported

7.20.3 Reference

ARM PrimeCell Color LCD Controller (PL111) Technical Reference Manual (ARM DDI 0293)

7.20.4 Licensing

Open Source Apache 2.0

Table 54. Configuration options (attributes) set for instance 'clcd_0'

Attributes	Value
resolution	xga
noGraphics	1

7.21 Peripheral [arm.ovpworld.org/peripheral/WdtSP805/1.0] instance: wdt2_0

7.21.1 Description

ARM SP805 Watchdog Registers.

7.21.2 Limitations

Does NOT model watchdog functionality, just provides registers to allow code to run.

7.21.3 Reference

ARM Watchdog Module (SP805) Technical Reference Manual (ARM DDI 0270)

7.21.4 Licensing

Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.22 Peripheral [arm.ovpworld.org/peripheral/DMemCtrlPL341/1.0] instance: dmc1_0

7.22.1 Description

ARM PL341 Dynamic Memory Controller Registers

7.22.2 Limitations

Programmers View, register model only. Does NOT model functionality, just provides registers to allow

code to run.

7.22.3 Reference
ARM CoreLink DDR2 Dynamic Memory Controller (DMC-341) Technical Reference Manual (ARM DDI 0418)

7.22.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.23 Peripheral [ovpworld.org/peripheral/dummyPort/1.0] instance: dma0_0

7.23.1 Description
Dummy peripheral that provides an area for accesses.

7.23.2 Limitations
Has no behavior. This peripheral defines a port through which a 4k byte memory area can be read and written.

7.23.3 Licensing
Open Source Apache 2.0

7.23.4 Reference
This is not based upon a real device

There are no configuration options set for this peripheral instance.

7.24 Peripheral [arm.ovpworld.org/peripheral/SMemCtrlPL354/1.0] instance: smc1_0

7.24.1 Description
PL354 Static Memory Controller

7.24.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.24.3 Reference
ARM PrimeCell Static Memory Controller (PL350 series) Technical Reference Manual (ARM DDI 0380)

7.24.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.25 Peripheral [arm.ovpworld.org/peripheral/SmartLoaderArmLinux/1.0] instance: smartLoader_0

7.25.1 Description

Psuedo-peripheral to perform memory initialisation for an ARM based Linux kernel boot:
Loads Linux kernel image file and (optional) initial ram disk image into memory.
Writes ATAG data into memory.
Writes tiny boot code at physical memory base that configures the registers as expected by Linux Kernel and then jumps to boot address (image load address by default).

7.25.2 Licensing

Open Source Apache 2.0

7.25.3 Limitations

Only supports little endian

7.25.4 Reference

See ARM Linux boot requirements in Linux source tree at documentation/arm/Booting

Table 55. Configuration options (attributes) set for instance 'smartLoader_0'

Attributes	Value
kernel	kernel
initrd	initrd
command	mem=2G@0x80000000 raid=noautodetect console=ttyAMA0,38400n8 devtmpfs.mount=0
physicalbase	0x80000000
memsize	0x80000000
boardid	0x8e0
disable	disable

7.26 Peripheral [smsc.ovpworld.org/peripheral/LAN9118/1.0] instance: eth0_1

7.26.1 Description

Fully functional Model of SMSC LAN9118 for Arm Versatile Express platforms. For full details please consult README-EMAC.txt

7.26.2 Licensing

Open Source Apache 2.0

7.26.3 Limitations

See README-EMAC.txt

7.26.4 Reference

SMSC LAN9118 High Performance single-chip 10/100 Non-PCI Ethernet Controller Datasheet Revision 1.5 (07-11-08)

There are no configuration options set for this peripheral instance.

7.27 Peripheral [philips.ovpworld.org/peripheral/ISP1761/1.0] instance: usb0_1

7.27.1 Description
Functional Model of USB Phillips ISP1761 for Arm Versatile Explress platforms. For full details please consult README-OTG.txt

7.27.2 Licensing
Open Source Apache 2.0

7.27.3 Limitations
- Only host mode is supported. - DMA modes are not supported for the moment, only the mandatory slave mode is implemented. - Control and bulk transfer types are currently implemented. No interrupt and isochronous transfers yet. - Tested only the attachment of a single host device. The HSOTG controller's root hub has a single port, so only one device can be attached to it. This device could be a hub, though. Currently we support only one non-hub device. - Hot plug events are currently unsupported.

7.27.4 Reference
Philips/NXP

There are no configuration options set for this peripheral instance.

7.28 Peripheral [arm.ovpworld.org/peripheral/VexpressSysRegs/1.0] instance: sysRegs_1

7.28.1 Description
ARM Versatile Express System Registers

7.28.2 Limitations
Only select registers are modeled. See user.c for details.

7.28.3 Reference
A

7.28.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.29 Peripheral [arm.ovpworld.org/peripheral/SysCtrlSP810/1.0] instance: sysCtrl_1

7.29.1 Description
ARM SP810 System Control Registers

7.29.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.29.3 Reference
ARM PrimeCell System Controller (SP810) Technical Reference Manual (ARM DDI 0254)

7.29.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.30 Peripheral [arm.ovpworld.org/peripheral/AaciPL041/1.0] instance: aac1_1

7.30.1 Description
ARM PL041 PrimeCell Advanced Audio CODEC Interface Registers

7.30.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.30.3 Reference
ARM PrimeCell Advanced Audio CODEC Interface (PL041) Technical Reference Manual (ARM DDI 0173)

7.30.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.31 Peripheral [arm.ovpworld.org/peripheral/MmciPL181/1.0] instance: mmc1_1

7.31.1 Description
ARM PrimeCell Multimedia Card Interface (MMCI)

7.31.2 Limitations
None

7.31.3 Licensing
Open Source Apache 2.0

7.31.4 Reference
ARM PrimeCell Multimedia Card Interface (Pl180) Technical Reference Manual (ARM DDI 0172)

There are no configuration options set for this peripheral instance.

7.32 Peripheral [arm.ovpworld.org/peripheral/KbPL050/1.0] instance: kb1_1

7.32.1 Description
ARM PL050 PS2 Keyboard or mouse controller

7.32.2 Limitations
None

7.32.3 Reference
ARM PrimeCell PS2 Keyboard/Mouse Interface (PL050) Technical Reference Manual (ARM DDI 0143)

7.32.4 Licensing
Open Source Apache 2.0

Table 56. Configuration options (attributes) set for instance 'kb1_1'

Attributes	Value
isKeyboard	1
grabDisable	1

7.33 Peripheral [arm.ovpworld.org/peripheral/KbPL050/1.0] instance: ms1_1

7.33.1 Description
ARM PL050 PS2 Keyboard or mouse controller

7.33.2 Limitations
None

7.33.3 Reference
ARM PrimeCell PS2 Keyboard/Mouse Interface (PL050) Technical Reference Manual (ARM DDI 0143)

7.33.4 Licensing
Open Source Apache 2.0

Table 57. Configuration options (attributes) set for instance 'ms1_1'

Attributes	Value
isMouse	1
grabDisable	1

7.34 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart0_1

7.34.1 Description
ARM PL011 UART

7.34.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.34.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.34.4 Licensing
Open Source Apache 2.0

Table 58. Configuration options (attributes) set for instance 'uart0_1'

Attributes	Value
variant	ARM
outfile	uart0_1.log
finishOnDisconnect	1

7.35 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart1_1

7.35.1 Description
ARM PL011 UART

7.35.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.35.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.35.4 Licensing
Open Source Apache 2.0

Table 59. Configuration options (attributes) set for instance 'uart1_1'

Attributes	Value
variant	ARM
outfile	uart1_1.log

7.36 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart2_1

7.36.1 Description
ARM PL011 UART

7.36.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.36.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.36.4 Licensing
Open Source Apache 2.0

Table 60. Configuration options (attributes) set for instance 'uart2_1'

Attributes	Value
variant	ARM

7.37 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart3_1

7.37.1 Description
ARM PL011 UART

7.37.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.37.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.37.4 Licensing
Open Source Apache 2.0

Table 61. Configuration options (attributes) set for instance 'uart3_1'

Attributes	Value
variant	ARM

7.38 Peripheral [arm.ovpworld.org/peripheral/WdtSP805/1.0] instance: wdt1_1

7.38.1 Description
ARM SP805 Watchdog Registers.

7.38.2 Limitations

Does NOT model watchdog functionality, just provides registers to allow code to run.

7.38.3 Reference
ARM Watchdog Module (SP805) Technical Reference Manual (ARM DDI 0270)

7.38.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.39 Peripheral [arm.ovpworld.org/peripheral/TimerSP804/1.0] instance: timer01_1

7.39.1 Description
Timer SP804 Module

7.39.2 Licensing
Open Source Apache 2.0

7.39.3 Limitations
none

7.39.4 Reference
ARM Dual-Timer Module (SP804) Technical Reference Manual (ARM DDI 0271)

There are no configuration options set for this peripheral instance.

7.40 Peripheral [arm.ovpworld.org/peripheral/TimerSP804/1.0] instance: timer23_1

7.40.1 Description
Timer SP804 Module

7.40.2 Licensing
Open Source Apache 2.0

7.40.3 Limitations
none

7.40.4 Reference
ARM Dual-Timer Module (SP804) Technical Reference Manual (ARM DDI 0271)

There are no configuration options set for this peripheral instance.

7.41 Peripheral [arm.ovpworld.org/peripheral/SerBusDviRegs/1.0] instance: dvi1_1

7.41.1 Description
Versatile Express Serial Bus DVI Registers

7.41.2 Licensing
Open Source Apache 2.0

7.41.3 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.41.4 Reference
A

There are no configuration options set for this peripheral instance.

7.42 Peripheral [arm.ovpworld.org/peripheral/RtcPL031/1.0] instance: rtc1_1

7.42.1 Description
ARM PL031 Real Time Clock (RTC)

7.42.2 Limitations
none

7.42.3 Reference
ARM PrimeCell Real Time Clock (PL031) Technical Reference Manual (ARM DDI 0224)

7.42.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.43 Peripheral [arm.ovpworld.org/peripheral/CompactFlashRegs/1.0] instance: cf1_1

7.43.1 Description
ARM Versatile Express Compact Flash Interface Registers

7.43.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.43.3 Reference
ARM Motherboard Express uATX (V2M-P1) Technical Reference Manual (ARM DDI 0447)

7.43.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.44 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart4_1

7.44.1 Description
ARM PL011 UART

7.44.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.44.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.44.4 Licensing
Open Source Apache 2.0

Table 62. Configuration options (attributes) set for instance 'uart4_1'

Attributes	Value
variant	ARM

7.45 Peripheral [arm.ovpworld.org/peripheral/LcdPL110/1.0] instance: clcd_1

7.45.1 Description
ARM PL110 LCD Controller

7.45.2 Limitations
The VGA display refresh is not optimised resulting in the VGA peripheral causing a limit on the maximum performance of a platform it contains to be around 300 MIPS (actual dependent upon refresh rate of LCD).
The LCD peripheral utilises memory watchpoints to optimise display refresh. This requires the use of ICM memory for the frame buffers, which currently may stop its use in SystemC TLM2 platforms.
Interrupts are not supported

7.45.3 Reference
ARM PrimeCell Color LCD Controller (PL111) Technical Reference Manual (ARM DDI 0293)

7.45.4 Licensing
Open Source Apache 2.0

Table 63. Configuration options (attributes) set for instance 'clcd_1'

Attributes	Value
resolution	xga
noGraphics	1

7.46 Peripheral [arm.ovpworld.org/peripheral/WdtSP805/1.0] instance: wdt2_1

7.46.1 Description
ARM SP805 Watchdog Registers.

7.46.2 Limitations
Does NOT model watchdog functionality, just provides registers to allow code to run.

7.46.3 Reference
ARM Watchdog Module (SP805) Technical Reference Manual (ARM DDI 0270)

7.46.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.47 Peripheral [arm.ovpworld.org/peripheral/DMemCtrlPL341/1.0] instance: dmc1_1

7.47.1 Description
ARM PL341 Dynamic Memory Controller Registers

7.47.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.47.3 Reference
ARM CoreLink DDR2 Dynamic Memory Controller (DMC-341) Technical Reference Manual (ARM DDI 0418)

7.47.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.48 Peripheral [ovpworld.org/peripheral/dummyPort/1.0] instance: dma0_1

7.48.1 Description
Dummy peripheral that provides an area for accesses.

7.48.2 Limitations

Has no behavior. This peripheral defines a port through which a 4k byte memory area can be read and written.

7.48.3 Licensing
Open Source Apache 2.0

7.48.4 Reference
This is not based upon a real device

There are no configuration options set for this peripheral instance.

7.49 Peripheral [arm.ovpworld.org/peripheral/SMemCtrlPL354/1.0] instance: smc1_1

7.49.1 Description
PL354 Static Memory Controller

7.49.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.49.3 Reference
ARM PrimeCell Static Memory Controller (PL350 series) Technical Reference Manual (ARM DDI 0380)

7.49.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.50 Peripheral [arm.ovpworld.org/peripheral/SmartLoaderArmLinux/1.0] instance: smartLoader_1

7.50.1 Description
Psuedo-peripheral to perform memory initialisation for an ARM based Linux kernel boot:
Loads Linux kernel image file and (optional) initial ram disk image into memory.
Writes ATAG data into memory.
Writes tiny boot code at physical memory base that configures the registers as expected by Linux Kernel and then jumps to boot address (image load address by default).

7.50.2 Licensing
Open Source Apache 2.0

7.50.3 Limitations
Only supports little endian

7.50.4 Reference

See ARM Linux boot requirements in Linux source tree at documentation/arm/Booting

Table 64. Configuration options (attributes) set for instance 'smartLoader_1'

Attributes	Value
kernel	kernel
initrd	initrd
command	mem=2G@0x80000000 raid=noautodetect console=ttyAMA0,38400n8 devtmpfs.mount=0
physicalbase	0x80000000
memsize	0x80000000
boardid	0x8e0
disable	disable

7.51 Peripheral [smsc.ovpworld.org/peripheral/LAN9118/1.0] instance: eth0_2

7.51.1 Description

Fully functional Model of SMSC LAN9118 for Arm Versatile Express platforms. For full details please consult README-EMAC.txt

7.51.2 Licensing

Open Source Apache 2.0

7.51.3 Limitations

See README-EMAC.txt

7.51.4 Reference

SMSC LAN9118 High Performance single-chip 10/100 Non-PCI Ethernet Controller Datasheet Revision 1.5 (07-11-08)

There are no configuration options set for this peripheral instance.

7.52 Peripheral [philips.ovpworld.org/peripheral/ISP1761/1.0] instance: usb0_2

7.52.1 Description

Functional Model of USB Phillips ISP1761 for Arm Versatile Explress platforms. For full details please consult README-OTG.txt

7.52.2 Licensing

Open Source Apache 2.0

7.52.3 Limitations

- Only host mode is supported. - DMA modes are not supported for the moment, only the mandatory slave mode is implemented. - Control and bulk transfer types are currently implemented. No interrupt and

isochronous transfers yet. - Tested only the attachment of a single host device. The HSOTG controller's root hub has a single port, so only one device can be attached to it. This device could be a hub, though. Currently we support only one non-hub device. - Hot plug events are currently unsupported.

7.52.4 Reference
Philips/NXP

There are no configuration options set for this peripheral instance.

7.53 Peripheral [arm.ovpworld.org/peripheral/VexpressSysRegs/1.0] instance: sysRegs_2

7.53.1 Description
ARM Versatile Express System Registers

7.53.2 Limitations
Only select registers are modeled. See user.c for details.

7.53.3 Reference
A

7.53.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.54 Peripheral [arm.ovpworld.org/peripheral/SysCtrlSP810/1.0] instance: sysCtrl_2

7.54.1 Description
ARM SP810 System Control Registers

7.54.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.54.3 Reference
ARM PrimeCell System Controller (SP810) Technical Reference Manual (ARM DDI 0254)

7.54.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.55 Peripheral [arm.ovpworld.org/peripheral/AaciPL041/1.0] instance: aac1_2

7.55.1 Description
ARM PL041 PrimeCell Advanced Audio CODEC Interface Registers

7.55.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.55.3 Reference
ARM PrimeCell Advanced Audio CODEC Interface (PL041) Technical Reference Manual (ARM DDI 0173)

7.55.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.56 Peripheral [arm.ovpworld.org/peripheral/MmciPL181/1.0] instance: mmc1_2

7.56.1 Description
ARM PrimeCell Multimedia Card Interface (MMCI)

7.56.2 Limitations
None

7.56.3 Licensing
Open Source Apache 2.0

7.56.4 Reference
ARM PrimeCell Multimedia Card Interface (Pl180) Technical Reference Manual (ARM DDI 0172)

There are no configuration options set for this peripheral instance.

7.57 Peripheral [arm.ovpworld.org/peripheral/KbPL050/1.0] instance: kb1_2

7.57.1 Description
ARM PL050 PS2 Keyboard or mouse controller

7.57.2 Limitations
None

7.57.3 Reference
ARM PrimeCell PS2 Keyboard/Mouse Interface (PL050) Technical Reference Manual (ARM DDI 0143)

7.57.4 Licensing
Open Source Apache 2.0

Table 65. Configuration options (attributes) set for instance 'kb1_2'

Attributes	Value
isKeyboard	1
grabDisable	1

7.58 Peripheral [arm.ovpworld.org/peripheral/KbPL050/1.0] instance: ms1_2

7.58.1 Description
ARM PL050 PS2 Keyboard or mouse controller

7.58.2 Limitations
None

7.58.3 Reference
ARM PrimeCell PS2 Keyboard/Mouse Interface (PL050) Technical Reference Manual (ARM DDI 0143)

7.58.4 Licensing
Open Source Apache 2.0

Table 66. Configuration options (attributes) set for instance 'ms1_2'

Attributes	Value
isMouse	1
grabDisable	1

7.59 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart0_2

7.59.1 Description
ARM PL011 UART

7.59.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.59.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.59.4 Licensing
Open Source Apache 2.0

Table 67. Configuration options (attributes) set for instance 'uart0_2'

Attributes	Value
variant	ARM
outfile	uart0_2.log
finishOnDisconnect	1

7.60 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart1_2

7.60.1 Description
ARM PL011 UART

7.60.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.60.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.60.4 Licensing
Open Source Apache 2.0

Table 68. Configuration options (attributes) set for instance 'uart1_2'

Attributes	Value
variant	ARM
outfile	uart1_2.log

7.61 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart2_2

7.61.1 Description
ARM PL011 UART

7.61.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.61.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.61.4 Licensing
Open Source Apache 2.0

Table 69. Configuration options (attributes) set for instance 'uart2_2'

Attributes	Value
variant	ARM

7.62 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart3_2

7.62.1 Description
ARM PL011 UART

7.62.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.62.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.62.4 Licensing
Open Source Apache 2.0

Table 70. Configuration options (attributes) set for instance 'uart3_2'

Attributes	Value
variant	ARM

7.63 Peripheral [arm.ovpworld.org/peripheral/WdtSP805/1.0] instance: wdt1_2

7.63.1 Description
ARM SP805 Watchdog Registers.

7.63.2 Limitations
Does NOT model watchdog functionality, just provides registers to allow code to run.

7.63.3 Reference
ARM Watchdog Module (SP805) Technical Reference Manual (ARM DDI 0270)

7.63.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.64 Peripheral [arm.ovpworld.org/peripheral/TimerSP804/1.0] instance: timer01_2

7.64.1 Description
Timer SP804 Module

7.64.2 Licensing
Open Source Apache 2.0

7.64.3 Limitations
none

7.64.4 Reference
ARM Dual-Timer Module (SP804) Technical Reference Manual (ARM DDI 0271)

There are no configuration options set for this peripheral instance.

7.65 Peripheral [arm.ovpworld.org/peripheral/TimerSP804/1.0] instance: timer23_2

7.65.1 Description
Timer SP804 Module

7.65.2 Licensing
Open Source Apache 2.0

7.65.3 Limitations
none

7.65.4 Reference
ARM Dual-Timer Module (SP804) Technical Reference Manual (ARM DDI 0271)

There are no configuration options set for this peripheral instance.

7.66 Peripheral [arm.ovpworld.org/peripheral/SerBusDviRegs/1.0] instance: dvi1_2

7.66.1 Description
Versatile Express Serial Bus DVI Registers

7.66.2 Licensing
Open Source Apache 2.0

7.66.3 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.66.4 Reference
A

There are no configuration options set for this peripheral instance.

7.67 Peripheral [arm.ovpworld.org/peripheral/RtcPL031/1.0] instance: rtc1_2

7.67.1 Description
ARM PL031 Real Time Clock (RTC)

7.67.2 Limitations
none

7.67.3 Reference
ARM PrimeCell Real Time Clock (PL031) Technical Reference Manual (ARM DDI 0224)

7.67.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.68 Peripheral [arm.ovpworld.org/peripheral/CompactFlashRegs/1.0] instance: cf1_2

7.68.1 Description
ARM Versatile Express Compact Flash Interface Registers

7.68.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.68.3 Reference
ARM Motherboard Express uATX (V2M-P1) Technical Reference Manual (ARM DDI 0447)

7.68.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.69 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart4_2

7.69.1 Description
ARM PL011 UART

7.69.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.69.3 Reference

ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.69.4 Licensing
Open Source Apache 2.0

Table 71. Configuration options (attributes) set for instance 'uart4_2'

Attributes	Value
variant	ARM

7.70 Peripheral [arm.ovpworld.org/peripheral/LcdPL110/1.0] instance: clcd_2

7.70.1 Description
ARM PL110 LCD Controller

7.70.2 Limitations
The VGA display refresh is not optimised resulting in the VGA peripheral causing a limit on the maximum performance of a platform it contains to be around 300 MIPS (actual dependent upon refresh rate of LCD).
The LCD peripheral utilises memory watchpoints to optimise display refresh. This requires the use of ICM memory for the frame buffers, which currently may stop its use in SystemC TLM2 platforms.
Interrupts are not supported

7.70.3 Reference
ARM PrimeCell Color LCD Controller (PL111) Technical Reference Manual (ARM DDI 0293)

7.70.4 Licensing
Open Source Apache 2.0

Table 72. Configuration options (attributes) set for instance 'clcd_2'

Attributes	Value
resolution	xga
noGraphics	1

7.71 Peripheral [arm.ovpworld.org/peripheral/WdtSP805/1.0] instance: wdt2_2

7.71.1 Description
ARM SP805 Watchdog Registers.

7.71.2 Limitations
Does NOT model watchdog functionality, just provides registers to allow code to run.

7.71.3 Reference
ARM Watchdog Module (SP805) Technical Reference Manual (ARM DDI 0270)

7.71.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.72 Peripheral [arm.ovpworld.org/peripheral/DMemCtrlPL341/1.0] instance: dmc1_2

7.72.1 Description
ARM PL341 Dynamic Memory Controller Registers

7.72.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.72.3 Reference
ARM CoreLink DDR2 Dynamic Memory Controller (DMC-341) Technical Reference Manual (ARM DDI 0418)

7.72.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.73 Peripheral [ovpworld.org/peripheral/dummyPort/1.0] instance: dma0_2

7.73.1 Description
Dummy peripheral that provides an area for accesses.

7.73.2 Limitations
Has no behavior. This peripheral defines a port through which a 4k byte memory area can be read and written.

7.73.3 Licensing
Open Source Apache 2.0

7.73.4 Reference
This is not based upon a real device

There are no configuration options set for this peripheral instance.

7.74 Peripheral [arm.ovpworld.org/peripheral/SMemCtrlPL354/1.0] instance: smc1_2

7.74.1 Description

PL354 Static Memory Controller

7.74.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.74.3 Reference
ARM PrimeCell Static Memory Controller (PL350 series) Technical Reference Manual (ARM DDI 0380)

7.74.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.75 Peripheral [arm.ovpworld.org/peripheral/SmartLoaderArmLinux/1.0] instance: smartLoader_2

7.75.1 Description
Psuedo-peripheral to perform memory initialisation for an ARM based Linux kernel boot:
Loads Linux kernel image file and (optional) initial ram disk image into memory.
Writes ATAG data into memory.
Writes tiny boot code at physical memory base that configures the registers as expected by Linux Kernel and then jumps to boot address (image load address by default).

7.75.2 Licensing
Open Source Apache 2.0

7.75.3 Limitations
Only supports little endian

7.75.4 Reference
See ARM Linux boot requirements in Linux source tree at documentation/arm/Booting

Table 73. Configuration options (attributes) set for instance 'smartLoader_2'

Attributes	Value
kernel	kernel
initrd	initrd
command	mem=2G@0x80000000 raid=noautodetect console=ttyAMA0,38400n8 devtmpfs.mount=0
physicalbase	0x80000000
memsize	0x80000000
boardid	0x8e0
disable	disable

7.76 Peripheral [smsc.ovpworld.org/peripheral/LAN9118/1.0] instance: eth0_3

7.76.1 Description
Fully functional Model of SMSC LAN9118 for Arm Versatile Express platforms. For full details please consult README-EMAC.txt

7.76.2 Licensing
Open Source Apache 2.0

7.76.3 Limitations
See README-EMAC.txt

7.76.4 Reference
SMSC LAN9118 High Performance single-chip 10/100 Non-PCI Ethernet Controller Datasheet Revision 1.5 (07-11-08)

There are no configuration options set for this peripheral instance.

7.77 Peripheral [philips.ovpworld.org/peripheral/ISP1761/1.0] instance: usb0_3

7.77.1 Description
Functional Model of USB Phillips ISP1761 for Arm Versatile Explress platforms. For full details please consult README-OTG.txt

7.77.2 Licensing
Open Source Apache 2.0

7.77.3 Limitations
- Only host mode is supported. - DMA modes are not supported for the moment, only the mandatory slave mode is implemented. - Control and bulk transfer types are currently implemented. No interrupt and isochronous transfers yet. - Tested only the attachment of a single host device. The HSOTG controller's root hub has a single port, so only one device can be attached to it. This device could be a hub, though. Currently we support only one non-hub device. - Hot plug events are currently unsupported.

7.77.4 Reference
Philips/NXP

There are no configuration options set for this peripheral instance.

7.78 Peripheral [arm.ovpworld.org/peripheral/VexpressSysRegs/1.0] instance: sysRegs_3

7.78.1 Description
ARM Versatile Express System Registers

7.78.2 Limitations
Only select registers are modeled. See user.c for details.

7.78.3 Reference
A

7.78.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.79 Peripheral [arm.ovpworld.org/peripheral/SysCtrlSP810/1.0] instance: sysCtrl_3

7.79.1 Description
ARM SP810 System Control Registers

7.79.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.79.3 Reference
ARM PrimeCell System Controller (SP810) Technical Reference Manual (ARM DDI 0254)

7.79.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.80 Peripheral [arm.ovpworld.org/peripheral/AaciPL041/1.0] instance: aac1_3

7.80.1 Description
ARM PL041 PrimeCell Advanced Audio CODEC Interface Registers

7.80.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.80.3 Reference
ARM PrimeCell Advanced Audio CODEC Interface (PL041) Technical Reference Manual (ARM DDI 0173)

7.80.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.81 Peripheral [arm.ovpworld.org/peripheral/MmciPL181/1.0] instance: mmc1_3

7.81.1 Description
ARM PrimeCell Multimedia Card Interface (MMCI)

7.81.2 Limitations
None

7.81.3 Licensing
Open Source Apache 2.0

7.81.4 Reference
ARM PrimeCell Multimedia Card Interface (Pl180) Technical Reference Manual (ARM DDI 0172)

There are no configuration options set for this peripheral instance.

7.82 Peripheral [arm.ovpworld.org/peripheral/KbPL050/1.0] instance: kb1_3

7.82.1 Description
ARM PL050 PS2 Keyboard or mouse controller

7.82.2 Limitations
None

7.82.3 Reference
ARM PrimeCell PS2 Keyboard/Mouse Interface (PL050) Technical Reference Manual (ARM DDI 0143)

7.82.4 Licensing
Open Source Apache 2.0

Table 74. Configuration options (attributes) set for instance 'kb1_3'

Attributes	Value
isKeyboard	1
grabDisable	1

7.83 Peripheral [arm.ovpworld.org/peripheral/KbPL050/1.0] instance: ms1_3

7.83.1 Description
ARM PL050 PS2 Keyboard or mouse controller

7.83.2 Limitations
None

7.83.3 Reference
ARM PrimeCell PS2 Keyboard/Mouse Interface (PL050) Technical Reference Manual (ARM DDI 0143)

7.83.4 Licensing
Open Source Apache 2.0

Table 75. Configuration options (attributes) set for instance 'ms1_3'

Attributes	Value
isMouse	1
grabDisable	1

7.84 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart0_3

7.84.1 Description
ARM PL011 UART

7.84.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.84.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.84.4 Licensing
Open Source Apache 2.0

Table 76. Configuration options (attributes) set for instance 'uart0_3'

Attributes	Value
variant	ARM
outfile	uart0_3.log
finishOnDisconnect	1

7.85 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart1_3

7.85.1 Description
ARM PL011 UART

7.85.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as

baud rates etc.

7.85.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.85.4 Licensing
Open Source Apache 2.0

Table 77. Configuration options (attributes) set for instance 'uart1_3'

Attributes	Value
variant	ARM
outfile	uart1_3.log

7.86 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart2_3

7.86.1 Description
ARM PL011 UART

7.86.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.86.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.86.4 Licensing
Open Source Apache 2.0

Table 78. Configuration options (attributes) set for instance 'uart2_3'

Attributes	Value
variant	ARM

7.87 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart3_3

7.87.1 Description
ARM PL011 UART

7.87.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.87.3 Reference

ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.87.4 Licensing
Open Source Apache 2.0

Table 79. Configuration options (attributes) set for instance 'uart3_3'

Attributes	Value
variant	ARM

7.88 Peripheral [arm.ovpworld.org/peripheral/WdtSP805/1.0] instance: wdt1_3

7.88.1 Description
ARM SP805 Watchdog Registers.

7.88.2 Limitations
Does NOT model watchdog functionality, just provides registers to allow code to run.

7.88.3 Reference
ARM Watchdog Module (SP805) Technical Reference Manual (ARM DDI 0270)

7.88.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.89 Peripheral [arm.ovpworld.org/peripheral/TimerSP804/1.0] instance: timer01_3

7.89.1 Description
Timer SP804 Module

7.89.2 Licensing
Open Source Apache 2.0

7.89.3 Limitations
none

7.89.4 Reference
ARM Dual-Timer Module (SP804) Technical Reference Manual (ARM DDI 0271)

There are no configuration options set for this peripheral instance.

7.90 Peripheral [arm.ovpworld.org/peripheral/TimerSP804/1.0] instance: timer23_3

7.90.1 Description
Timer SP804 Module

7.90.2 Licensing
Open Source Apache 2.0

7.90.3 Limitations
none

7.90.4 Reference
ARM Dual-Timer Module (SP804) Technical Reference Manual (ARM DDI 0271)

There are no configuration options set for this peripheral instance.

7.91 Peripheral [arm.ovpworld.org/peripheral/SerBusDviRegs/1.0] instance: dvi1_3

7.91.1 Description
Versatile Express Serial Bus DVI Registers

7.91.2 Licensing
Open Source Apache 2.0

7.91.3 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.91.4 Reference
A

There are no configuration options set for this peripheral instance.

7.92 Peripheral [arm.ovpworld.org/peripheral/RtcPL031/1.0] instance: rtc1_3

7.92.1 Description
ARM PL031 Real Time Clock (RTC)

7.92.2 Limitations
none

7.92.3 Reference
ARM PrimeCell Real Time Clock (PL031) Technical Reference Manual (ARM DDI 0224)

7.92.4 Licensing

Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.93 Peripheral [arm.ovpworld.org/peripheral/CompactFlashRegs/1.0] instance: cf1_3

7.93.1 Description
ARM Versatile Express Compact Flash Interface Registers

7.93.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.93.3 Reference
ARM Motherboard Express uATX (V2M-P1) Technical Reference Manual (ARM DDI 0447)

7.93.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.94 Peripheral [arm.ovpworld.org/peripheral/UartPL011/1.0] instance: uart4_3

7.94.1 Description
ARM PL011 UART

7.94.2 Limitations
This is not a complete model of the PL011. There is no modeling of physical aspects of the UART, such as baud rates etc.

7.94.3 Reference
ARM PrimeCell UART (PL011) Technical Reference Manual (ARM DDI 0183)

7.94.4 Licensing
Open Source Apache 2.0

Table 80. Configuration options (attributes) set for instance 'uart4_3'

Attributes	Value
variant	ARM

7.95 Peripheral [arm.ovpworld.org/peripheral/LcdPL110/1.0] instance: clcd_3

7.95.1 Description

ARM PL110 LCD Controller

7.95.2 Limitations

The VGA display refresh is not optimised resulting in the VGA peripheral causing a limit on the maximum performance of a platform it contains to be around 300 MIPS (actual dependent upon refresh rate of LCD).
The LCD peripheral utilises memory watchpoints to optimise display refresh. This requires the use of ICM memory for the frame buffers, which currently may stop its use in SystemC TLM2 platforms.
Interrupts are not supported

7.95.3 Reference

ARM PrimeCell Color LCD Controller (PL111) Technical Reference Manual (ARM DDI 0293)

7.95.4 Licensing

Open Source Apache 2.0

Table 81. Configuration options (attributes) set for instance 'clcd_3'

Attributes	Value
resolution	xga
noGraphics	1

7.96 Peripheral [arm.ovpworld.org/peripheral/WdtSP805/1.0] instance: wdt2_3

7.96.1 Description

ARM SP805 Watchdog Registers.

7.96.2 Limitations

Does NOT model watchdog functionality, just provides registers to allow code to run.

7.96.3 Reference

ARM Watchdog Module (SP805) Technical Reference Manual (ARM DDI 0270)

7.96.4 Licensing

Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.97 Peripheral [arm.ovpworld.org/peripheral/DMemCtrlPL341/1.0] instance: dmc1_3

7.97.1 Description

ARM PL341 Dynamic Memory Controller Registers

7.97.2 Limitations

Programmers View, register model only. Does NOT model functionality, just provides registers to allow

code to run.

7.97.3 Reference
ARM CoreLink DDR2 Dynamic Memory Controller (DMC-341) Technical Reference Manual (ARM DDI 0418)

7.97.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.98 Peripheral [ovpworld.org/peripheral/dummyPort/1.0] instance: dma0_3

7.98.1 Description
Dummy peripheral that provides an area for accesses.

7.98.2 Limitations
Has no behavior. This peripheral defines a port through which a 4k byte memory area can be read and written.

7.98.3 Licensing
Open Source Apache 2.0

7.98.4 Reference
This is not based upon a real device

There are no configuration options set for this peripheral instance.

7.99 Peripheral [arm.ovpworld.org/peripheral/SMemCtrlPL354/1.0] instance: smc1_3

7.99.1 Description
PL354 Static Memory Controller

7.99.2 Limitations
Programmers View, register model only. Does NOT model functionality, just provides registers to allow code to run.

7.99.3 Reference
ARM PrimeCell Static Memory Controller (PL350 series) Technical Reference Manual (ARM DDI 0380)

7.99.4 Licensing
Open Source Apache 2.0

There are no configuration options set for this peripheral instance.

7.100 Peripheral [arm.ovpworld.org/peripheral/SmartLoaderArmLinux/1.0] instance: smartLoader_3

7.100.1 Description

Psuedo-peripheral to perform memory initialisation for an ARM based Linux kernel boot:
Loads Linux kernel image file and (optional) initial ram disk image into memory.
Writes ATAG data into memory.
Writes tiny boot code at physical memory base that configures the registers as expected by Linux Kernel and then jumps to boot address (image load address by default).

7.100.2 Licensing

Open Source Apache 2.0

7.100.3 Limitations

Only supports little endian

7.100.4 Reference

See ARM Linux boot requirements in Linux source tree at documentation/arm/Booting

Table 82. Configuration options (attributes) set for instance 'smartLoader_3'

Attributes	Value
kernel	kernel
initrd	initrd
command	mem=2G@0x80000000 raid=noautodetect console=ttyAMA0,38400n8 devtmpfs.mount=0
physicalbase	0x80000000
memsize	0x80000000
boardid	0x8e0
disable	disable

8.0 Overview of Imperas OVP Virtual Platforms

This document provides the details of the usage of an Imperas OVP Virtual Platform. The first half of the document covers specifics of this particular virtual platform.

This second part of the document, includes information about Imperas OVP virtual platforms, how they are built and used.

The Imperas virtual platforms are designed to provide a base for you to run high-speed software simulations of CPU-based SoCs and platforms on any suitable PC. They are typically based on the functionality of vendors fixed or evaluation platforms, enabling you to simulate software on these reference platforms. Typically virtual platforms are fixed and require the vendor to modify or extend them. Imperas virtual platforms are different in that they enable you to extend the functionality of the virtual platform, to closer reflect your own platform, by adding more component models, running different operating systems or adding additional applications.

Imperas virtual platforms are created using the Imperas iGen technology, allowing them to be used with Imperas OVP based simulators and also with Accellera/OSCI compliant SystemC simulators and commercial EDA System Design environments that use SystemC.

Virtual platforms include simulation models of the target devices, including the processor model(s) for the target device plus enough peripheral models to boot an operating system or run bare metal applications. The platform and the peripheral models used in most of the virtual platforms are open source, so that you can easily add new models to the platform as well as modify the existing models. Some models are only provided as binary, normally because the IP owner has restricted the release of the model source. In this case, please contact Imperas for more information.

There are typically several generic flavors of the virtual platforms for specific processor families, some targeting full operating systems, such as Linux, and some which focus on Real Time Operating Systems (RTOS) such as Mentor Nucleus or freeRTOS. OVP models of the processor cores are included in the virtual platforms, and for those processors which support mulitple cores SMP Linux is often supported for that virtual platform. For all of these virtual platforms, many of the peripheral components of the platform are modeled, often including the Ethernet and USB components. The semi-hosting capability of the Imperas virtual platform simulator products enables connection via the Ethernet and USB components from the virtual platform to the real world via the x86 host machine.

The Imperas OVP CPU models are written using the OVP Virtual Machine Interface (VMI) API that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. The processor models are Instruction Accurate and do not model the detailed cycle timing of the processor and they implement functionality at the level of a Programmers View of the processor and peripherals and the software running on them does not know it is not running on hardware. Many models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore

and modify the model. The models are run through an extensive QA and regression testing process and most processor model families are validated using technology provided by the processor IP owners. All the models in this platform are developed with the Open Virtual Platforms APIs and are implemented in C.

More information on modeling and APIs can be found on the www.OVPworld.org site.

9.0 Getting Started with Imperas OVP Virtual Platforms

Virtual platforms are downloadable from the OVPworld website OVPworld.org/downloads. You need to browse and look for '<platform processor name> Examples'. You do need to be registered and logged in on the OVP site to download. OVPworld currently provides 32 bit host versions of packages containing virtual platforms.

When downloading, choose, Linux or Windows host. 32 bit packages can be installed and executed on 32 bit or 64 bit hosts. If you require a 64 bit host version please contact Imperas.

For example, for the ARM Versatile Express platform booting Linux on Cortex-A15MP Single, Dual, and Quad core procesors, you would want the download package:
'OVPsim_demo_Linux_ArmVersatileExpress_arm_Cortex-A15MP'.

Most virtual platform packages contain the platform and all the processor and peripheral models needed. You will need to download a simulator to run the platform. You can use OVPsim, downloadable from OVPworld.org/downloads, or you can use one of the Imperas simulators (imperas.com/products) available commercially from Imperas.

10.0 Simulating Software

10.1 Getting a license key to run

After you have downloaded you will need a runtime license key before the simulators will run. For OVPsim please visit OVPworld.org/likey and provide the required information and an evaluation/demo license key will be automatically sent to you. If you are using Imperas, then please contact Imperas for a license key.

10.2 Normal runs

To run a platform, read the section below on command line control of the platform and the section on setting command line arguments.

10.3 Loading Software

For most virtual platforms the platform is already configured to run the default software application/program and there is normally a script to run that sets some arguments. You can then copy/edit this script to select your own applications etc.

The example application programs are typically .elf format files and are provided pre-compiled. There are normally makefiles and associated scripts to recompile the example applications.

To find more information about compiling and loading software, the following document should be looked at: Imperas_Installation_and_Getting_Started.pdf.

10.4 Semihosting

In a virtual platform, semihosting is not normally used as there is normally hardware that implements the appropriate functionality - for example I/O will be handled by UARTs etc.

10.5 Using a terminal (UART)

If the platform includes one or more UARTs you will need to connect a terminal program to it so that you can see output and type into the simulated program. Review the list of peripherals below and see what configuration options it has been set with. In most cases there is an option to set to instruct the simulator to 'pop up' a terminal window connected to the simulated UART.

10.6 Interacting with the simulation (keyboard and mouse)

If the platform has a simulated UART you can normally set a command to get the simulator to pop up a terminal window allowing you to see output from the simulated UART and also allowing you to type characters into the UART that can be processed by the simulated software.

If your simulated platform has an LCD device then you can often configure it to recognize mouse movements and mouse clicks - allowing full interaction.

To see these interactions in action, have a look at some of the available videos available at OVPworld.org/demosandvideos.

10.7 More Information (Documentation) on Simulation

To find more information about running simulations and more of the options the simulators provide, the following documents should be looked at:
Imperas_Installation_and_Getting_Started.pdf
OVPsim_and_CpuManager_User_Guide.pdf
OVP_Control_File_User_Guide.pdf

A full list of the currently available OVP documentation is available: OVPworld.org/documentation.

11.0 Debugging Software running on an Imperas OVP Virtual Platform

The Imperas and OVP simulators have several different interfaces to debuggers. These include several proprietary formats and also the standard GNU RSP format is supported allowing many compatible debuggers to be used. Below are some examples that Imperas directly support.

11.1 Debugging with GDB

A GNU debugger (GDB) can be connected to a processor in a platform using the RSP protocol. This allows the application program running on a processor to be debugged using a specific GDB for the processor selected. When using the Imperas Professional products many connections can be made allowing a GDB to

be connected to all the processors in the platform.

The use of GDB is documented: OVPsim_Debugging_Applications_with_GDB_User_Guide.pdf.

*11.2 Debugging with Imperas M*DBG*

The Imperas multi-processor debugger can be connected to a platform and through this connection you can debug application programs running on all of the processors instanced within the platform. It is also capable, within this single unified environment, to debug peripheral model behavioral code in conjunction with the processor application programs.

For more information please see the Imperas M*DBG user guide.

The Imperas multi-processor debugger is also capable of controlling the Imperas Verification Analysis aand Profiling (VAP) tools in real time, making them invaluable to application program development, debugging and analysis.

For more information please see the Imperas VAP tools user guide.

11.3 Debugging with the Imperas iGui and GDB

Imperas iGui gives a GUI front end to the use of the GDB debugger. It allows use of all the features of GDB including source level application program debugging on processors.

*11.4 Debugging with the Imperas iGui and M*DBG*

Imperas iGui gives a GUI front end to the Imperas multi-processor debugger. It provides all the features of this debugger but does so with source level application program debugging on processors and source level debugging of the behavioral code on peripheral components in the platform. A context view shows all the processor and peripheral components within the platform and allows switching between them to examine the state of each at the event at which the simulation was stopped

Imperas iGui provides a menu from which the Imperas VAP tools can be controlled.

11.5 Debugging with Eclipse

A standard Eclipse CDT development environment can be connected to one or more processors in a platform (multiple processors require an Imperas professional product). The simulation platform is started remotely or using the external tool feature in Eclipse, opens a debug port and awaits the connection with Eclipse. All features provided by the Eclipse CDT development environment are available to be used to debug software applications executing on the processors in the platform.

The use of Eclipse is documented: OVPsim_Debugging_Applications_with_Eclipse_User_Guide.pdf.

11.6 Debugging applications running under a simulated operating system

If the simulated platform is running an Operating System and the platform has a UART or Ethernet etc

connection then it is often possible to connect an external debugger and debug the applications running under the simulated operating system.

An example would be a simulated platform running the Linux operating system, such as the MIPS Malta, or ARM Versatile Express. Within the simulated Linux you can start a gdbserver that connects from within the simulation through a UART out to the host PC via a port. Within the host PC you start a terminal program and connect to the port with a debugger such as GDB and can then debug the simulated user application.

12.0 Modifying the Platform

12.1 Platforms use C/C++ and OVP APIs

The Imperas and OVP simulators execute a platform that is written in C/C++ and that makes function calls into the simulator's APIs. Thus the virtual platform is compiled from C/C++ into a binary shared object that the simulator loads and runs. OVP provides the definition and documentation that defines the C APIs for modeling the platforms, the peripherals and the processors. You can find more information about these APIs on the OVP website and in the OVP API documentation.

12.2 Platforms/Peripherals can be easily built with iGen from Imperas

Imperas provides a product 'iGen' that takes an input script file and creates the C/C++ files needed for platforms and peripherals - it creates the C/C++ file that is compiled into the platform or peripheral that is needed as an object file by the simulator. iGen creates the C/C++ files, you then need to add any necessary behaviors or further details etc. For platforms iGen creates either a C platform or a C++ SystemC TLM2 platform. For peripherals iGen creates the C files and also provides a native C++ SystemC TLM2 interface to allow the peripheral to be instantiated in SystemC TLM2 platforms.

Information on iGen is available from: imperas.com/products.

12.3 Re-configuring the platform

There will nornmally be several configuration options that you can set when running the platform without the neeed to change any source. Refer to the section above on command line arguments. If these do not allow you to make the changes you need, then you may need to edit and recompile the source of the platform.

The source of the platform and the source of the peripherals will be installed as part of the packages you are using. The sources are located in the Imperas/OVP installation VLNV source tree. The VLNV term refers to: Vendor (eg arm.ovpworld.org), Library (eg platform), Name, (eg ArmVersatileExpress-CA15), and Version (eg 1.0). To modify the platform, locate the platform source files.

If you are an Imperas user and have access to iGen, we recommend you modify the source script files and regenerate and recompile the C that makes up the platform. Refer to the Imperas iGen model generator guide and the Imperas platform generator guide.

If you are using the C or SystemC TLM2 platforms with OVPsim, then you can edit the C/C++ files, recompile the source directly using the supplied makefiles, and the run the simulator directly with the resultant shared object.

12.4 Replacing peripherals components

If you need to replace peripherals, find the appropriate place in the source of the platform, make the change you need, and recompile etc. Look in the library for documentation on available peripherals and their configuration options.

12.5 Adding new peripherals components

If you need to add peripherals, find the appropriate place in the source, make the additions you need, and recompile etc. Look in the library for documentation on available peripherals and their configuration options.

If you need to create new peripheral components then use iGen to very quickly create the necessary C/C++ files that get you started. With iGen you can create peripherals with register/memory state in a few lines of iGen source. When adding behavior to the peripherals refer to the OVP API documentation.

13.0 Available Virtual Platforms

Table 83. Imperas / OVP Extendable Platform Kits (17 available)

Platform Name	Vendor
AlteraCycloneIII_3c120	altera.ovpworld.org
AlteraCycloneV_HPS	altera.ovpworld.org
AlteraCycloneV_HPS_TLM2	altera.ovpworld.org
ARMv8-A-FMv1	arm.ovpworld.org
ArmIntegratorCP	arm.ovpworld.org
ArmIntegratorCP_TLM2.0	arm.ovpworld.org
ArmVersatileExpress	arm.ovpworld.org
ArmVersatileExpress-CA15	arm.ovpworld.org
ArmVersatileExpress-CA9	arm.ovpworld.org
ArmVersatileExpress_CA9_TLM2	arm.ovpworld.org
AtmelAT91SAM7	atmel.ovpworld.org
FreescaleKinetis60	freescale.ovpworld.org
FreescaleVybridVF5	freescale.ovpworld.org
MipsMalta	mips.ovpworld.org
MipsMaltaLinux_TLM2.0	mips.ovpworld.org
RenesasUPD70F3441	renesas.ovpworld.org
XilinxML505	xilinx.ovpworld.org

Table 84. Imperas General Virtual Platforms (6 available)

Platform Name	Vendor
arm-ti-eabi	arm.imperas.com
armm-ti-coff	arm.imperas.com
armm-ti-eabi	arm.imperas.com
HeteroAlteraCycloneV_HPS_CycloneIII_3c120	imperas.ovpworld.org
HeteroArmNucleusMIPSLinux	imperas.ovpworld.org
QuadArmVersatileExpress	imperas.ovpworld.org

Table 85. Imperas / OVP Bare Metal Virtual Platforms (39 available)

Platform Name	Vendor
BareMetalNios_IISingle	altera.ovpworld.org
BareMetalNios_IISingle_TLM2.0	altera.ovpworld.org
BareMetalArcSingle	arc.ovpworld.org
BareMetalArcSingle_TLM2.0	arc.ovpworld.org
BareMetalArm7Single	arm.ovpworld.org
BareMetalArm7Single_TLM2.0	arm.ovpworld.org
BareMetalArmAArch64Single_TLM2.0	arm.ovpworld.org
BareMetalArmCortexADual	arm.ovpworld.org
BareMetalArmCortexASingle	arm.ovpworld.org
BareMetalArmCortexASingleAngelTrap	arm.ovpworld.org
BareMetalArmCortexASingle_TLM2.0	arm.ovpworld.org
BareMetalArmCortexMSingle	arm.ovpworld.org
BareMetalArmCortexMSingle_TLM2.0	arm.ovpworld.org

ArmCortexMFreeRTOS	imperas.ovpworld.org
ArmCortexMuCOS-II	imperas.ovpworld.org
BareMetalArcManycore24_TLM2.0	imperas.ovpworld.org
BareMetalArm7Dual_TLM2.0	imperas.ovpworld.org
BareMetalArmx1Mips32x3	imperas.ovpworld.org
BareMetalMips32Multicore2_TLM2.0	imperas.ovpworld.org
Or1kUclinux_TLM2.0	imperas.ovpworld.org
BareMetalM14KSingle	mips.ovpworld.org
BareMetalM14KSingle_TLM2.0	mips.ovpworld.org
BareMetalMips32Dual	mips.ovpworld.org
BareMetalMips32Single	mips.ovpworld.org
BareMetalMips32Single_TLM2.0	mips.ovpworld.org
BareMetalMips64Single	mips.ovpworld.org
BareMetalMips64Single_TLM2.0	mips.ovpworld.org
BareMetalMipsDual	mips.ovpworld.org
BareMetalMipsSingle	mips.ovpworld.org
BareMetalMipsSingle_TLM2.0	mips.ovpworld.org
BareMetalOr1kSingle	ovpworld.org
BareMetalOr1kSingle_TLM2.0	ovpworld.org
BareMetalM16cSingle	posedgesoft.ovpworld.org
BareMetalPowerPc32Single	power.ovpworld.org
BareMetalPowerPc32Single_TLM2.0	power.ovpworld.org
BareMetalV850Single	renesas.ovpworld.org
BareMetalV850Single_TLM2.0	renesas.ovpworld.org
ghs-multi	renesas.ovpworld.org
BareMetalMicroBlazeSingle_TLM2.0	xilinx.ovpworld.org

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