Imperas Peripheral Model Guide

Model Specific Information for freescale.ovpworld.org / VybridDMA

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

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1.0 Model Specific Information

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers, other component parts, and configuration options and general information for peripheral modeling with Imperas OVP.

1.1 Description

Freescale Vybrid Direct Memory Access Controller

1.2 Limitations

Only models control register read/write - control register CX and ECX bits are modeled as RAZ/WI

1.3 Licensing

Open Source Apache 2.0

1.4 Reference

Freescale Vybrid Peripheral User Guide

1.5 Location

The VybridDMA peripheral model is located in an Imperas/OVP installation at the VLNV: freescale.ovpworld.org / peripheral / VybridDMA / 1.0.

2.0 Net Ports

This model has the following net ports:

Table 1. Net Ports

Name	Type	Must Be Connected	Description
Reset	input	F (False)	
eDMARequest	input	F (False)	
eDMADone	output	F (False)	
errorInterrupt	output	F (False)	DMA Error Interrupt port
dmaInterrupt_ch0	output	F (False)	DMA Done for channel 0 Interrupt port
dmaInterrupt_ch1	output	F (False)	DMA Done for channel 1 Interrupt port
dmaInterrupt_ch2	output	F (False)	DMA Done for channel 2 Interrupt port
dmaInterrupt_ch3	output	F (False)	DMA Done for channel 3 Interrupt port
dmaInterrupt_ch4	output	F (False)	DMA Done for channel 4 Interrupt port
dmaInterrupt_ch5	output	F (False)	DMA Done for channel 5 Interrupt port
dmaInterrupt_ch6	output	F (False)	DMA Done for channel 6 Interrupt port
dmaInterrupt_ch7	output	F (False)	DMA Done for channel 7 Interrupt port
dmaInterrupt_ch8	output	F (False)	DMA Done for channel 8 Interrupt port
dmaInterrupt_ch9	output	F (False)	DMA Done for channel 9 Interrupt port
dmaInterrupt_ch10	output	F (False)	DMA Done for channel 10 Interrupt

			port
dmaInterrupt_ch11	output	F (False)	DMA Done for channel 11 Interrupt port
dmaInterrupt_ch12	output	F (False)	DMA Done for channel 12 Interrupt port
dmaInterrupt_ch13	output	F (False)	DMA Done for channel 13 Interrupt port
dmaInterrupt_ch14	output	F (False)	DMA Done for channel 14 Interrupt port
dmaInterrupt_ch15	output	F (False)	DMA Done for channel 15 Interrupt port

3.0 Bus Master Ports

This model has the following bus master ports:

3.1 Bus Master Port: MREAD

Table 2. MREAD

Name	Address Width (bits)	Description
MREAD	32	DMA Master Read of address space

3.2 Bus Master Port: MWRITE

Table 3. MWRITE

Name	Address Width (bits)	Description
MWRITE	32	DMA Master Write of address space

4.0 Bus Slave Ports

This model has the following bus slave ports:

4.1 Bus Slave Port: bport1

Table 4. Bus Slave Port: bport1

Name	Size (bytes)	Must Be Connected	Description
bport1	0x2000	F (False)	

Table 5. Bus Slave Port: bport1 Registers:

Name	Offset	Width (bits)	Description	R/W	is Volatile
ab_CR	0x0	32	Control Register, offset: 0x0		
ab_ES	0x4	32	Error Status Register, offset: 0x4		
ab_ERQ	0xc	32	Enable Request Register, offset: 0xC		
ab_EEI	0x14	32			
ab_CS_EEI_ERC	0x18	32	Clear/Set EEI, ERC		
ab_DNE_SRT_ERR_INT	0x1c	32	Clear/Set DNE, START, ERR, INT registers		
ab_INT	0x24	32			

ab_ERR	0x2c	32	Error Register, offset: 0x2C		
ab_HRS	0x34	32			
ab_EARS	0x44	32	Enable Asyncronous Request		
ab_DCHPRI3_0	0x100	32	Channel n Priority Registers 3 to 0		
ab_DCHPRI7_4	0x104	32			
ab_DCHPRI11_8	0x108	32			
ab_DCHPRI15_12	0x10c	32			
ab_DCHPRI19_16	0x110	32			
ab_DCHPRI23_20	0x114	32			
ab_DCHPRI27_24	0x118	32			
ab_DCHPRI31_28	0x11c	32			
ab_TCD0_SADDR	0x1000	32	TCD Source Address		
ab_TCD0_SOFF_ATTR	0x1004	32	TCD Signed Source Address Offset		
ab_TCD0_NBYTES	0x1008	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD0_SLAST	0x100c	32			
ab_TCD0_DADDR	0x1010	32			
ab_TCD0_DOFF_CITER	0x1014	32			
ab_TCD0_DLASTSGA	0x1018	32			
ab_TCD0_CSR_BITER	0x101c	32			
ab_TCD1_SADDR	0x1020	32	TCD Source Address		
ab_TCD1_SOFF_ATTR	0x1024	32	TCD Signed Source Address Offset		
ab_TCD1_NBYTES	0x1028	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD1_SLAST	0x102c	32			
ab_TCD1_DADDR	0x1030	32			
ab_TCD1_DOFF_CITER	0x1034	32			
ab_TCD1_DLASTSGA	0x1038	32			
ab_TCD1_CSR_BITER	0x103c	32			
ab_TCD2_SADDR	0x1040	32	TCD Source Address		
ab_TCD2_SOFF_ATTR	0x1044	32	TCD Signed Source Address Offset		
ab_TCD2_NBYTES	0x1048	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD2_SLAST	0x104c	32			
ab_TCD2_DADDR	0x1050	32			
ab_TCD2_DOFF_CITER	0x1054	32			
ab_TCD2_DLASTSGA	0x1058	32			
ab_TCD2_CSR_BITER	0x105c	32			
ab_TCD3_SADDR	0x1060	32	TCD Source Address		
ab_TCD3_SOFF_ATTR	0x1064	32	TCD Signed Source Address Offset		
ab_TCD3_NBYTES	0x1068	32	TCD Signed Minor Loop Offset, Minor Loop		

			Disabled		
ab_TCD3_SLAST	0x106c	32			
ab_TCD3_DADDR	0x1070	32			
ab_TCD3_DOFF_CITER	0x1074	32			
ab_TCD3_DLASTSGA	0x1078	32			
ab_TCD3_CSR_BITER	0x107c	32			
ab_TCD4_SADDR	0x1080	32	TCD Source Address		
ab_TCD4_SOFF_ATTR	0x1084	32	TCD Signed Source Address Offset		
ab_TCD4_NBYTES	0x1088	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD4_SLAST	0x108c	32			
ab_TCD4_DADDR	0x1090	32			
ab_TCD4_DOFF_CITER	0x1094	32			
ab_TCD4_DLASTSGA	0x1098	32			
ab_TCD4_CSR_BITER	0x109c	32			
ab_TCD5_SADDR	0x10a0	32	TCD Source Address		
ab_TCD5_SOFF_ATTR	0x10a4	32	TCD Signed Source Address Offset		
ab_TCD5_NBYTES	0x10a8	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD5_SLAST	0x10ac	32			
ab_TCD5_DADDR	0x10b0	32			
ab_TCD5_DOFF_CITER	0x10b4	32			
ab_TCD5_DLASTSGA	0x10b8	32			
ab_TCD5_CSR_BITER	0x10bc	32			
ab_TCD6_SADDR	0x10c0	32	TCD Source Address		
ab_TCD6_SOFF_ATTR	0x10c4	32	TCD Signed Source Address Offset		
ab_TCD6_NBYTES	0x10c8	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD6_SLAST	0x10cc	32			
ab_TCD6_DADDR	0x10d0	32			
ab_TCD6_DOFF_CITER	0x10d4	32			
ab_TCD6_DLASTSGA	0x10d8	32			
ab_TCD6_CSR_BITER	0x10dc	32			
ab_TCD7_SADDR	0x10e0	32	TCD Source Address		
ab_TCD7_SOFF_ATTR	0x10e4	32	TCD Signed Source Address Offset		
ab_TCD7_NBYTES	0x10e8	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD7_SLAST	0x10ec	32			
ab_TCD7_DADDR	0x10f0	32			
ab_TCD7_DOFF_CITER	0x10f4	32			
ab_TCD7_DLASTSGA	0x10f8	32			
ab_TCD7_CSR_BITER	0x10fc	32			
ab_TCD8_SADDR	0x1100	32	TCD Source Address		

ab_TCD8_SOFF_ATTR	0x1104	32	TCD Signed Source Address Offset		
ab_TCD8_NBYTES	0x1108	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD8_SLAST	0x110c	32			
ab_TCD8_DADDR	0x1110	32			
ab_TCD8_DOFF_CITER	0x1114	32			
ab_TCD8_DLASTSGA	0x1118	32			
ab_TCD8_CSR_BITER	0x111c	32			
ab_TCD9_SADDR	0x1120	32	TCD Source Address		
ab_TCD9_SOFF_ATTR	0x1124	32	TCD Signed Source Address Offset		
ab_TCD9_NBYTES	0x1128	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD9_SLAST	0x112c	32			
ab_TCD9_DADDR	0x1130	32			
ab_TCD9_DOFF_CITER	0x1134	32			
ab_TCD9_DLASTSGA	0x1138	32			
ab_TCD9_CSR_BITER	0x113c	32			
ab_TCD10_SADDR	0x1140	32	TCD Source Address		
ab_TCD10_SOFF_ATTR	0x1144	32	TCD Signed Source Address Offset		
ab_TCD10_NBYTES	0x1148	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD10_SLAST	0x114c	32			
ab_TCD10_DADDR	0x1150	32			
ab_TCD10_DOFF_CITER	0x1154	32			
ab_TCD10_DLASTSGA	0x1158	32			
ab_TCD10_CSR_BITER	0x115c	32			
ab_TCD11_SADDR	0x1160	32	TCD Source Address		
ab_TCD11_SOFF_ATTR	0x1164	32	TCD Signed Source Address Offset		
ab_TCD11_NBYTES	0x1168	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD11_SLAST	0x116c	32			
ab_TCD11_DADDR	0x1170	32			
ab_TCD11_DOFF_CITER	0x1174	32			
ab_TCD11_DLASTSGA	0x1178	32			
ab_TCD11_CSR_BITER	0x117c	32			
ab_TCD12_SADDR	0x1180	32	TCD Source Address		
ab_TCD12_SOFF_ATTR	0x1184	32	TCD Signed Source Address Offset		
ab_TCD12_NBYTES	0x1188	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD12_SLAST	0x118c	32			

ab_TCD12_DADDR	0x1190	32			
ab_TCD12_DOFF_CITER	0x1194	32			
ab_TCD12_DLASTSGA	0x1198	32			
ab_TCD12_CSR_BITER	0x119c	32			
ab_TCD13_SADDR	0x11a0	32	TCD Source Address		
ab_TCD13_SOFF_ATTR	0x11a4	32	TCD Signed Source Address Offset		
ab_TCD13_NBYTES	0x11a8	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD13_SLAST	0x11ac	32			
ab_TCD13_DADDR	0x11b0	32			
ab_TCD13_DOFF_CITER	0x11b4	32			
ab_TCD13_DLASTSGA	0x11b8	32			
ab_TCD13_CSR_BITER	0x11bc	32			
ab_TCD14_SADDR	0x11c0	32	TCD Source Address		
ab_TCD14_SOFF_ATTR	0x11c4	32	TCD Signed Source Address Offset		
ab_TCD14_NBYTES	0x11c8	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD14_SLAST	0x11cc	32			
ab_TCD14_DADDR	0x11d0	32			
ab_TCD14_DOFF_CITER	0x11d4	32			
ab_TCD14_DLASTSGA	0x11d8	32			
ab_TCD14_CSR_BITER	0x11dc	32			
ab_TCD15_SADDR	0x11e0	32	TCD Source Address		
ab_TCD15_SOFF_ATTR	0x11e4	32	TCD Signed Source Address Offset		
ab_TCD15_NBYTES	0x11e8	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD15_SLAST	0x11ec	32			
ab_TCD15_DADDR	0x11f0	32			
ab_TCD15_DOFF_CITER	0x11f4	32			
ab_TCD15_DLASTSGA	0x11f8	32			
ab_TCD15_CSR_BITER	0x11fc	32			
ab_TCD16_SADDR	0x1200	32	TCD Source Address		
ab_TCD16_SOFF_ATTR	0x1204	32	TCD Signed Source Address Offset		
ab_TCD16_NBYTES	0x1208	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD16_SLAST	0x120c	32			
ab_TCD16_DADDR	0x1210	32			
ab_TCD16_DOFF_CITER	0x1214	32			
ab_TCD16_DLASTSGA	0x1218	32			

ab_TCD16_CSR_BITER	0x121c	32			
ab_TCD17_SADDR	0x1220	32	TCD Source Address		
ab_TCD17_SOFF_ATTR	0x1224	32	TCD Signed Source Address Offset		
ab_TCD17_NBYTES	0x1228	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD17_SLAST	0x122c	32			
ab_TCD17_DADDR	0x1230	32			
ab_TCD17_DOFF_CITER	0x1234	32			
ab_TCD17_DLASTSGA	0x1238	32			
ab_TCD17_CSR_BITER	0x123c	32			
ab_TCD18_SADDR	0x1240	32	TCD Source Address		
ab_TCD18_SOFF_ATTR	0x1244	32	TCD Signed Source Address Offset		
ab_TCD18_NBYTES	0x1248	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD18_SLAST	0x124c	32			
ab_TCD18_DADDR	0x1250	32			
ab_TCD18_DOFF_CITER	0x1254	32			
ab_TCD18_DLASTSGA	0x1258	32			
ab_TCD18_CSR_BITER	0x125c	32			
ab_TCD19_SADDR	0x1260	32	TCD Source Address		
ab_TCD19_SOFF_ATTR	0x1264	32	TCD Signed Source Address Offset		
ab_TCD19_NBYTES	0x1268	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD19_SLAST	0x126c	32			
ab_TCD19_DADDR	0x1270	32			
ab_TCD19_DOFF_CITER	0x1274	32			
ab_TCD19_DLASTSGA	0x1278	32			
ab_TCD19_CSR_BITER	0x127c	32			
ab_TCD20_SADDR	0x1280	32	TCD Source Address		
ab_TCD20_SOFF_ATTR	0x1284	32	TCD Signed Source Address Offset		
ab_TCD20_NBYTES	0x1288	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD20_SLAST	0x128c	32			
ab_TCD20_DADDR	0x1290	32			
ab_TCD20_DOFF_CITER	0x1294	32			
ab_TCD20_DLASTSGA	0x1298	32			
ab_TCD20_CSR_BITER	0x129c	32			
ab_TCD21_SADDR	0x12a0	32	TCD Source Address		
ab_TCD21_SOFF_ATTR	0x12a4	32	TCD Signed Source Address Offset		

ab_TCD21_NBYTES	0x12a8	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD21_SLAST	0x12ac	32			
ab_TCD21_DADDR	0x12b0	32			
ab_TCD21_DOFF_CITER	0x12b4	32			
ab_TCD21_DLASTSGA	0x12b8	32			
ab_TCD21_CSR_BITER	0x12bc	32			
ab_TCD22_SADDR	0x12c0	32	TCD Source Address		
ab_TCD22_SOFF_ATTR	0x12c4	32	TCD Signed Source Address Offset		
ab_TCD22_NBYTES	0x12c8	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD22_SLAST	0x12cc	32			
ab_TCD22_DADDR	0x12d0	32			
ab_TCD22_DOFF_CITER	0x12d4	32			
ab_TCD22_DLASTSGA	0x12d8	32			
ab_TCD22_CSR_BITER	0x12dc	32			
ab_TCD23_SADDR	0x12e0	32	TCD Source Address		
ab_TCD23_SOFF_ATTR	0x12e4	32	TCD Signed Source Address Offset		
ab_TCD23_NBYTES	0x12e8	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD23_SLAST	0x12ec	32			
ab_TCD23_DADDR	0x12f0	32			
ab_TCD23_DOFF_CITER	0x12f4	32			
ab_TCD23_DLASTSGA	0x12f8	32			
ab_TCD23_CSR_BITER	0x12fc	32			
ab_TCD24_SADDR	0x1300	32	TCD Source Address		
ab_TCD24_SOFF_ATTR	0x1304	32	TCD Signed Source Address Offset		
ab_TCD24_NBYTES	0x1308	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD24_SLAST	0x130c	32			
ab_TCD24_DADDR	0x1310	32			
ab_TCD24_DOFF_CITER	0x1314	32			
ab_TCD24_DLASTSGA	0x1318	32			
ab_TCD24_CSR_BITER	0x131c	32			
ab_TCD25_SADDR	0x1320	32	TCD Source Address		
ab_TCD25_SOFF_ATTR	0x1324	32	TCD Signed Source Address Offset		
ab_TCD25_NBYTES	0x1328	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD25_SLAST	0x132c	32			
ab_TCD25_DADDR	0x1330	32			

ab_TCD25_DOFF_CITER	0x1334	32			
ab_TCD25_DLASTSGA	0x1338	32			
ab_TCD25_CSR_BITER	0x133c	32			
ab_TCD26_SADDR	0x1340	32	TCD Source Address		
ab_TCD26_SOFF_ATTR	0x1344	32	TCD Signed Source Address Offset		
ab_TCD26_NBYTES	0x1348	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD26_SLAST	0x134c	32			
ab_TCD26_DADDR	0x1350	32			
ab_TCD26_DOFF_CITER	0x1354	32			
ab_TCD26_DLASTSGA	0x1358	32			
ab_TCD26_CSR_BITER	0x135c	32			
ab_TCD27_SADDR	0x1360	32	TCD Source Address		
ab_TCD27_SOFF_ATTR	0x1364	32	TCD Signed Source Address Offset		
ab_TCD27_NBYTES	0x1368	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD27_SLAST	0x136c	32			
ab_TCD27_DADDR	0x1370	32			
ab_TCD27_DOFF_CITER	0x1374	32			
ab_TCD27_DLASTSGA	0x1378	32			
ab_TCD27_CSR_BITER	0x137c	32			
ab_TCD28_SADDR	0x1380	32	TCD Source Address		
ab_TCD28_SOFF_ATTR	0x1384	32	TCD Signed Source Address Offset		
ab_TCD28_NBYTES	0x1388	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD28_SLAST	0x138c	32			
ab_TCD28_DADDR	0x1390	32			
ab_TCD28_DOFF_CITER	0x1394	32			
ab_TCD28_DLASTSGA	0x1398	32			
ab_TCD28_CSR_BITER	0x139c	32			
ab_TCD29_SADDR	0x13a0	32	TCD Source Address		
ab_TCD29_SOFF_ATTR	0x13a4	32	TCD Signed Source Address Offset		
ab_TCD29_NBYTES	0x13a8	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD29_SLAST	0x13ac	32			
ab_TCD29_DADDR	0x13b0	32			
ab_TCD29_DOFF_CITER	0x13b4	32			
ab_TCD29_DLASTSGA	0x13b8	32			
ab_TCD29_CSR_BITER	0x13bc	32			

ab_TCD30_SADDR	0x13c0	32	TCD Source Address		
ab_TCD30_SOFF_ATTR	0x13c4	32	TCD Signed Source Address Offset		
ab_TCD30_NBYTES	0x13c8	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD30_SLAST	0x13cc	32			
ab_TCD30_DADDR	0x13d0	32			
ab_TCD30_DOFF_CITER	0x13d4	32			
ab_TCD30_DLASTSGA	0x13d8	32			
ab_TCD30_CSR_BITER	0x13dc	32			
ab_TCD31_SADDR	0x13e0	32	TCD Source Address		
ab_TCD31_SOFF_ATTR	0x13e4	32	TCD Signed Source Address Offset		
ab_TCD31_NBYTES	0x13e8	32	TCD Signed Minor Loop Offset, Minor Loop Disabled		
ab_TCD31_SLAST	0x13ec	32			
ab_TCD31_DADDR	0x13f0	32			
ab_TCD31_DOFF_CITER	0x13f4	32			
ab_TCD31_DLASTSGA	0x13f8	32			
ab_TCD31_CSR_BITER	0x13fc	32			

5.0 Platforms that use this peripheral component

Peripheral components can be used in many different platforms, including those developed by Imperas or by other users of OVP. You can use this peripheral in your own platforms.

Table 6. Publicly available platforms using peripheral 'VybridDMA'

Platform Name	Vendor
FreescaleVybridVF5	freescale.ovpworld.org

6.0 Peripheral components in the library

Table 7. Publicly available Imperas/OVP peripheral models (158 models)

Peripheral	Peripheral	Peripheral
freescale.ovpworld.org/VybridGPIO	freescale.ovpworld.org/VybridI2C	freescale.ovpworld.org/VybridLCD
freescale.ovpworld.org/VybridQUADSPI	freescale.ovpworld.org/VybridSDHC	freescale.ovpworld.org/VybridSPI
freescale.ovpworld.org/VybridUART	freescale.ovpworld.org/VybridUSB	intel.ovpworld.org/82077AA
intel.ovpworld.org/82371EB	intel.ovpworld.org/8253	intel.ovpworld.org/8259A
intel.ovpworld.org/NorFlash48F4400	intel.ovpworld.org/PciIDE	intel.ovpworld.org/PciPM
intel.ovpworld.org/PciUSB	intel.ovpworld.org/Ps2Control	marvell.ovpworld.org/GT6412x
mips.ovpworld.org/16450C	mips.ovpworld.org/MaltaFPGA	mips.ovpworld.org/SmartLoaderLinux
motorola.ovpworld.org/MC146818	national.ovpworld.org/16450	national.ovpworld.org/16550
ovpworld.org/Alpha2x16Display	ovpworld.org/dummyPort	ovpworld.org/DynamicBridge
ovpworld.org/FlashDevice	ovpworld.org/ledRegister	ovpworld.org/SerInt
ovpworld.org/SimpleDma	ovpworld.org/VirtioBlkMMIO	philips.ovpworld.org/ISP1761
renesas.ovpworld.org/adc	renesas.ovpworld.org/bcu	renesas.ovpworld.org/brg
renesas.ovpworld.org/can	renesas.ovpworld.org/can	renesas.ovpworld.org/clkgen
renesas.ovpworld.org/crc	renesas.ovpworld.org/csib	renesas.ovpworld.org/csie
renesas.ovpworld.org/dma	renesas.ovpworld.org/intc	renesas.ovpworld.org/memc
renesas.ovpworld.org/rng	renesas.ovpworld.org/taa	renesas.ovpworld.org/tms
renesas.ovpworld.org/tmt	renesas.ovpworld.org/uartc	renesas.ovpworld.org/UPD70F3441Logic
smsc.ovpworld.org/LAN9118	smsc.ovpworld.org/LAN91C111	ti.ovpworld.org/UartInterface
xilinx.ovpworld.org/mdm	xilinx.ovpworld.org/mpmc	xilinx.ovpworld.org/xps-gpio
xilinx.ovpworld.org/xps-iic	xilinx.ovpworld.org/xps-intc	xilinx.ovpworld.org/xps-ll-temac
xilinx.ovpworld.org/xps-mch-emc	xilinx.ovpworld.org/xps-sysace	xilinx.ovpworld.org/xps-timer
xilinx.ovpworld.org/xps-uartlite	altera.ovpworld.org/dw-apb-timer	altera.ovpworld.org/dw-apb-uart
altera.ovpworld.org/IntervalTimer32Core	altera.ovpworld.org/IntervalTimer64Core	altera.ovpworld.org/JtagUart
altera.ovpworld.org/PerformanceCounterCore	altera.ovpworld.org/RSTMGR	altera.ovpworld.org/SystemIDCore
altera.ovpworld.org/Uart	amd.ovpworld.org/79C970	arm.ovpworld.org/AaciPL041
arm.ovpworld.org/CompactFlashRegs	arm.ovpworld.org/CoreModule9x6	arm.ovpworld.org/DebugLedAndDipSwitch
arm.ovpworld.org/DMemCtrlPL341	arm.ovpworld.org/IcpControl	arm.ovpworld.org/IcpCounterTimer
arm.ovpworld.org/IntICP	arm.ovpworld.org/IntICP	arm.ovpworld.org/KbPL050
arm.ovpworld.org/L2CachePL310	arm.ovpworld.org/LcdPL110	arm.ovpworld.org/MmciPL181
arm.ovpworld.org/RtcPL031	arm.ovpworld.org/SerBusDviRegs	arm.ovpworld.org/SmartLoaderArm64Linux
arm.ovpworld.org/SmartLoaderArmLinux	arm.ovpworld.org/SMemCtrlPL354	arm.ovpworld.org/SysCtrlSP810
arm.ovpworld.org/TimerSP804	arm.ovpworld.org/TzpcBP147	arm.ovpworld.org/UartPL011
arm.ovpworld.org/VexpressSysRegs	arm.ovpworld.org/WdtSP805	atmel.ovpworld.org/AdvancedInterruptController
atmel.ovpworld.org/ParallelIOController	atmel.ovpworld.org/PowerSaving	atmel.ovpworld.org/SpecialFunction
atmel.ovpworld.org/TimerCounter	atmel.ovpworld.org/UsartInterface	atmel.ovpworld.org/WatchdogTimer
cirrus.ovpworld.org/GD5446	freescale.ovpworld.org/KinetisADC	freescale.ovpworld.org/KinetisAIPS
freescale.ovpworld.org/KinetisAXBS	freescale.ovpworld.org/KinetisCAN	freescale.ovpworld.org/KinetisCMP
freescale.ovpworld.org/KinetisCMT	freescale.ovpworld.org/KinetisCRC	freescale.ovpworld.org/KinetisDAC
freescale.ovpworld.org/KinetisDDR	freescale.ovpworld.org/KinetisDMA	freescale.ovpworld.org/KinetisDMAC
freescale.ovpworld.org/KinetisDMAMUX	freescale.ovpworld.org/KinetisENET	freescale.ovpworld.org/KinetisEWM
freescale.ovpworld.org/KinetisFB	freescale.ovpworld.org/KinetisFMC	freescale.ovpworld.org/KinetisFTFE
freescale.ovpworld.org/KinetisFTM	freescale.ovpworld.org/KinetisGPIO	freescale.ovpworld.org/KinetisI2C
freescale.ovpworld.org/KinetisI2S	freescale.ovpworld.org/KinetisLLWU	freescale.ovpworld.org/KinetisLPTMR

freescale.ovpworld.org/KinetisMCG	freescale.ovpworld.org/KinetisMPU	freescale.ovpworld.org/KinetisNFC
freescale.ovpworld.org/KinetisOSC	freescale.ovpworld.org/KinetisPDB	freescale.ovpworld.org/KinetisPIT
freescale.ovpworld.org/KinetisPMC	freescale.ovpworld.org/KinetisPORT	freescale.ovpworld.org/KinetisRCM
freescale.ovpworld.org/KinetisRFSYS	freescale.ovpworld.org/KinetisRFVBAT	freescale.ovpworld.org/KinetisRNG
freescale.ovpworld.org/KinetisRTC	freescale.ovpworld.org/KinetisSDHC	freescale.ovpworld.org/KinetisSIM
freescale.ovpworld.org/KinetisSMC	freescale.ovpworld.org/KinetisSPI	freescale.ovpworld.org/KinetisTSI
freescale.ovpworld.org/KinetisUART	freescale.ovpworld.org/KinetisUSB	freescale.ovpworld.org/KinetisUSBDCD
freescale.ovpworld.org/KinetisUSBHS	freescale.ovpworld.org/KinetisVREF	freescale.ovpworld.org/KinetisWDOG
freescale.ovpworld.org/Uart	freescale.ovpworld.org/VybridADC	freescale.ovpworld.org/VybridANADIG
freescale.ovpworld.org/VybridCCM	freescale.ovpworld.org/VybridDMA	

7.0 General Information on Peripheral Models

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers etc. and configuration options and general information for peripheral modeling with Imperas OVP.

7.1 Background

Imperas OVP simulation technology enables very high performance simulation, debug and analysis of platforms containing multiple processors and peripheral models. The technology is designed to be extensible: you can create new models of processors, peripherals and other platform components using interfaces and libraries defined by OVP.

The peripheral models created using the OVP APIs run on the Peripheral Simulation Engine (PSE).

The model is typically written in C and compiled into an executable for the PSE processor architecture. The model is compiled for speed of execution and to protect IP. It is dynamically loaded by the simulator at run time.

8.0 Building peripherals easily with Imperas iGen

To aid with model creation, Imperas products include iGen, a model generation tool. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process. iGen creates the needed C files. iGen also creates the C++ SystemC TLM2 interface files needed to run peripheral models in SystemC simulations.

iGen takes as input a simple script specification that includes device internals such as registers and memories, port information, component descriptors, and other elements. iGen then builds the C code model files and user editable templates. These include model frameworks with registers, function calls, memory map, and other items. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.

More information on iGen can be found: imperas.com/products.

Please contact Imperas to get access to the Imperas documents: Imperas_Model_Generator_Guide.pdf and Imperas_Peripheral_Generator_Guide.pdf.

9.0 Peripheral model internals

Each instance of a peripheral model runs on its own virtual machine with an address space large enough for the model. This processor (the PSE) and its memory are separate from any processors, memories and buses

in the platform being simulated; they exist only to execute the code of the peripheral model.

Interception of functions defined in the peripheral model allows the use of features of the host system in the implementation of the behavior of a peripheral. As an example, a real platform might contain a video display device. When simulating this system, it is generally more convenient not to simulate the complete video display device but to use a video package available on the host machine, such as SDL, and to use this to render to the host display. Also models of uarts, ethernet devices and USB components can make use of the host PC resources during simulation, to allow, for example, a simulation to browse the real internet, or the simulation to connect to a real USB device.

10.0 Parts of peripheral models

10.1 Configuring the Peripheral Instance with Parameters

A peripheral can include the behaviour of several configurations. These are controlled when the peripheral is instanced in the platform by setting parameters defined on the peripheral.

10.2 Net Ports

Peripherals may be connected to other peripherals or processors with signal wires (nets). These can be used to act as interrupt signals or used to control behavior between peripherals.
The wires are created in the platform as nets and this net is connected into the peripheral using a net port.

10.3 Bus master ports

A bus master port initiates (and controls the address of) a bus cycle. Bus cycles are generated by behavioral code within the peripheral model.

10.4 Bus slave ports

A peripheral can be defined as having several bus slave ports. The bus slave ports can be split into several address blocks. Each address block be either local memory or memory mapped registers. Both of these can have associated callback functions. A memory mapped register can also be defined as specific read/write access, whether it is volatile, and also whether it is associated with a reset pin and mask. A memory mapped register can also have specific bit fields defined.

10.5 Packetnets

A peripheral can be defined as being connected to packetnet ports. A packetnet is used to model packet based communication such as Ethernet, CAN bus or GSM. A packetnet is created in a platform, then connected to packetnet ports on model instances. A packetnet can have many connections, each able to send or receive packets. A packetnet is used as an efficient method of communication within OVP models.

For more information on modeling with packetnets, please see the peripheral modeling documentation: OVP_Peripheral_Modeling_Guide.pdf, OVPsim_and_CpuManager_User_Guide.pdf and the example: $IMPERAS_HOME/Examples/Models/Peripherals/packetnet.

11.0 More information (documentation) on peripheral models and modeling

More information on modeling and APIs can be found at: OVPworld.org/technology_apis.

Specifics on modeling peripherals can be found: OVP_Peripheral_Modeling_Guide.pdf.

A full list of the currently available OVP documentation is available: OVPworld.org/documentation.
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