



## Imperas Peripheral Model Guide

### Model Specific Information for smsc.ovpworld.org / LAN9118

#### Imperas Software Limited

Imperas Buildings, North Weston  
Thame, Oxfordshire, OX9 2HA, U.K.  
docs@imperas.com.



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## Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit [OVPworld.org](http://OVPworld.org).

## Table Of Contents

<b>1.0 Model Specific Information</b>	4
1.1 Description	4
1.2 Licensing	4
1.3 Limitations	4
1.4 Reference	4
1.5 Location	4
<b>2.0 Peripheral Instance Parameters</b>	4
<b>3.0 Net Ports</b>	4
<b>4.0 Bus Slave Ports</b>	5
4.1 Bus Slave Port: bport1	5
<b>5.0 Platforms that use this peripheral component</b>	6
<b>6.0 Peripheral components in the library</b>	7
<b>7.0 General Information on Peripheral Models</b>	9
7.1 Background	9
<b>8.0 Building peripherals easily with Imperas iGen</b>	9
<b>9.0 Peripheral model internals</b>	9
<b>10.0 Parts of peripheral models</b>	10
10.1 Configuring the Peripheral Instance with Parameters	10
10.2 Net Ports	10
10.3 Bus master ports	10
10.4 Bus slave ports	10
10.5 Packetnets	10
<b>11.0 More information (documentation) on peripheral models and modeling</b>	10

## 1.0 Model Specific Information

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers, other component parts, and configuration options and general information for peripheral modeling with Imperas OVP.

### 1.1 Description

Fully functional Model of SMSC LAN9118 for Arm Versatile Express platforms. For full details please consult README-EMAC.txt

### 1.2 Licensing

Open Source Apache 2.0

### 1.3 Limitations

See README-EMAC.txt

### 1.4 Reference

SMSC LAN9118 High Performance single-chip 10/100 Non-PCI Ethernet Controller Datasheet Revision 1.5 (07-11-08)

### 1.5 Location

The LAN9118 peripheral model is located in an Imperas/OVP installation at the VLNV: [smsc.ovpworld.org / peripheral / LAN9118 / 1.0](http://smsc.ovpworld.org/peripheral/LAN9118/1.0).

## 2.0 Peripheral Instance Parameters

This model accepts the following parameters:

Table 1. Peripheral Parameters

Name	Type	Description
pollDelay	uns32	Read pollDelay
outfile	string	Wireshark capture file
record	string	Record external events into this file
replay	string	Replay external events from this file
tapDevice	string	The name of the TAP device
redir	string	Redirection instruction
tftpPrefix	string	Path to the root of the tftp directory

## 3.0 Net Ports

This model has the following net ports:

Table 2. Net Ports

Name	Type	Must Be Connected	Description
irq	output	F (False)	IRQ Pin

## 4.0 Bus Slave Ports

This model has the following bus slave ports:

### 4.1 Bus Slave Port: *bport1*

Table 3. Bus Slave Port: bport1

Name	Size (bytes)	Must Be Connected	Description
bport1	0x1000	F (False)	

Table 4. Bus Slave Port: bport1 Registers:

Name	Offset	Width (bits)	Description	R/W	is Volatile
ab_RX_DATA_FIFO	0x0	32			
ab_RX_DATA_FIFO_1	0x4	32			
ab_RX_DATA_FIFO_2	0x8	32			
ab_RX_DATA_FIFO_3	0xc	32			
ab_RX_DATA_FIFO_4	0x10	32			
ab_RX_DATA_FIFO_5	0x14	32			
ab_RX_DATA_FIFO_6	0x18	32			
ab_RX_DATA_FIFO_7	0x1c	32			
ab_TX_DATA_FIFO	0x20	32			
ab_TX_DATA_FIFO_1	0x24	32			
ab_TX_DATA_FIFO_2	0x28	32			
ab_TX_DATA_FIFO_3	0x2c	32			
ab_TX_DATA_FIFO_4	0x30	32			
ab_TX_DATA_FIFO_5	0x34	32			
ab_TX_DATA_FIFO_6	0x38	32			
ab_TX_DATA_FIFO_7	0x3c	32			
ab_RX_STATUS_FIFO	0x40	32			
ab_RX_STATUS_FIFO_PEEK	0x44	32			
ab_TX_STATUS_FIFO	0x48	32			
ab_TX_STATUS_FIFO_PEEK	0x4c	32			
ab_ID_REV	0x50	32			
ab_IRQ_CFG	0x54	32			
ab_INT_STS	0x58	32			
ab_INT_EN	0x5c	32			
ab_BYTE_TEST	0x64	32			
ab_FIFO_INT	0x68	32			
ab_RX_CFG	0x6c	32			
ab_TX_CFG	0x70	32			
ab_HW_CFG	0x74	32			
ab_RX_DP_CTRL	0x78	32			
ab_RX_FIFO_INF	0x7c	32			
ab_TX_FIFO_INF	0x80	32			

ab_PMT_CTRL	0x84	32			
ab_GPIO_CFG	0x88	32			
ab_GPT_CFG	0x8c	32			
ab_GPT_CNT	0x90	32			
ab_WORD_SWAP	0x98	32			
ab_FREE_RUN	0x9c	32			
ab_RX_DROP	0xa0	32			
ab_MAC_CSR_CMD	0xa4	32			
ab_MAC_CSR_DATA	0xa8	32			
ab_AFC_CFG	0xac	32			
ab_E2P_CMD	0xb0	32			
ab_E2P_DATA	0xb4	32			

## 5.0 Platforms that use this peripheral component

Peripheral components can be used in many different platforms, including those developed by Imperas or by other users of OVP. You can use this peripheral in your own platforms.

Table 5. Publicly available platforms using peripheral 'LAN9118'

Platform Name	Vendor
ArmIntegratorCP	arm.ovpworld.org
ArmVersatileExpress	arm.ovpworld.org
ArmVersatileExpress-CA15	arm.ovpworld.org
ArmVersatileExpress-CA9	arm.ovpworld.org
QuadArmVersatileExpress	imperas.ovpworld.org
ArmIntegratorCP_TLM2.0	arm.ovpworld.org
ArmVersatileExpress_CA9_TLM2	arm.ovpworld.org

## 6.0 Peripheral components in the library

Table 6. Publicly available Imperas/OVP peripheral models (158 models)

Peripheral	Peripheral	Peripheral
smmc.ovpworld.org/LAN91C111	ti.ovpworld.org/UartInterface	xilinx.ovpworld.org/mdm
xilinx.ovpworld.org/mpmc	xilinx.ovpworld.org/xps-gpio	xilinx.ovpworld.org/xps-iic
xilinx.ovpworld.org/xps-intc	xilinx.ovpworld.org/xps-ll-temac	xilinx.ovpworld.org/xps-mch-emc
xilinx.ovpworld.org/xps-sysace	xilinx.ovpworld.org/xps-timer	xilinx.ovpworld.org/xps-uartlite
altera.ovpworld.org/dw-apb-timer	altera.ovpworld.org/dw-apb-uart	altera.ovpworld.org/IntervalTimer32Core
altera.ovpworld.org/IntervalTimer64Core	altera.ovpworld.org/JtagUart	altera.ovpworld.org/PerformanceCounterCore
altera.ovpworld.org/RSTMGR	altera.ovpworld.org/SystemIDCore	altera.ovpworld.org/Uart
amd.ovpworld.org/79C970	arm.ovpworld.org/AaciPL041	arm.ovpworld.org/CompactFlashRegs
arm.ovpworld.org/CoreModule9x6	arm.ovpworld.org/DebugLedAndDipSwitch	arm.ovpworld.org/DMemCtrlPL341
arm.ovpworld.org/IcpControl	arm.ovpworld.org/IcpCounterTimer	arm.ovpworld.org/IntICP
arm.ovpworld.org/IntICP	arm.ovpworld.org/KbPL050	arm.ovpworld.org/L2CachePL310
arm.ovpworld.org/LcdPL110	arm.ovpworld.org/MmcPL181	arm.ovpworld.org/RtcPL031
arm.ovpworld.org/SerBusDviRegs	arm.ovpworld.org/SmartLoaderArm64Linux	arm.ovpworld.org/SmartLoaderArmLinux
arm.ovpworld.org/SMemCtrlPL354	arm.ovpworld.org/SysCtrlSP810	arm.ovpworld.org/TimerSP804
arm.ovpworld.org/TzpcBP147	arm.ovpworld.org/UartPL011	arm.ovpworld.org/VexpressSysRegs
arm.ovpworld.org/WdtSP805	atmel.ovpworld.org/AdvancedInterruptController	atmel.ovpworld.org/ParallelIOController
atmel.ovpworld.org/PowerSaving	atmel.ovpworld.org/SpecialFunction	atmel.ovpworld.org/TimerCounter
atmel.ovpworld.org/UsartInterface	atmel.ovpworld.org/WatchdogTimer	cirrus.ovpworld.org/GD5446
freescale.ovpworld.org/KinetisADC	freescale.ovpworld.org/KinetisAIPS	freescale.ovpworld.org/KinetisAXBS
freescale.ovpworld.org/KinetisCAN	freescale.ovpworld.org/KinetisCMP	freescale.ovpworld.org/KinetisCMT
freescale.ovpworld.org/KinetisCRC	freescale.ovpworld.org/KinetisDAC	freescale.ovpworld.org/KinetisDDR
freescale.ovpworld.org/KinetisDMA	freescale.ovpworld.org/KinetisDMAC	freescale.ovpworld.org/KinetisDMAMUX
freescale.ovpworld.org/KinetisENET	freescale.ovpworld.org/KinetisEWM	freescale.ovpworld.org/KinetisFB
freescale.ovpworld.org/KinetisFMC	freescale.ovpworld.org/KinetisFTFE	freescale.ovpworld.org/KinetisFTM
freescale.ovpworld.org/KinetisGPIO	freescale.ovpworld.org/KinetisI2C	freescale.ovpworld.org/KinetisI2S
freescale.ovpworld.org/KinetisLLWU	freescale.ovpworld.org/KinetisLPTMR	freescale.ovpworld.org/KinetisMCG
freescale.ovpworld.org/KinetisMPU	freescale.ovpworld.org/KinetisNFC	freescale.ovpworld.org/KinetisOSC
freescale.ovpworld.org/KinetisPDB	freescale.ovpworld.org/KinetisPIT	freescale.ovpworld.org/KinetisPMC
freescale.ovpworld.org/KinetisPORT	freescale.ovpworld.org/KinetisRCM	freescale.ovpworld.org/KinetisRFSYS
freescale.ovpworld.org/KinetisRFVBAT	freescale.ovpworld.org/KinetisRNG	freescale.ovpworld.org/KinetisRTC
freescale.ovpworld.org/KinetisSDHC	freescale.ovpworld.org/KinetisSIM	freescale.ovpworld.org/KinetisSMC
freescale.ovpworld.org/KinetisSPI	freescale.ovpworld.org/KinetisTSI	freescale.ovpworld.org/KinetisUART
freescale.ovpworld.org/KinetisUSB	freescale.ovpworld.org/KinetisUSBDCD	freescale.ovpworld.org/KinetisUSBHS
freescale.ovpworld.org/KinetisVREF	freescale.ovpworld.org/KinetisWDOG	freescale.ovpworld.org/Uart
freescale.ovpworld.org/VybridADC	freescale.ovpworld.org/VybridANADIG	freescale.ovpworld.org/VybridCCM
freescale.ovpworld.org/VybridDMA	freescale.ovpworld.org/VybridGPIO	freescale.ovpworld.org/VybridI2C
freescale.ovpworld.org/VybridLCD	freescale.ovpworld.org/VybridQUADSPI	freescale.ovpworld.org/VybridSDHC
freescale.ovpworld.org/VybridSPI	freescale.ovpworld.org/VybridUART	freescale.ovpworld.org/VybridUSB
intel.ovpworld.org/82077AA	intel.ovpworld.org/82371EB	intel.ovpworld.org/8253
intel.ovpworld.org/8259A	intel.ovpworld.org/NorFlash48F4400	intel.ovpworld.org/PciIDE
intel.ovpworld.org/PciPM	intel.ovpworld.org/PciUSB	intel.ovpworld.org/Ps2Control
marvell.ovpworld.org/GT6412x	mips.ovpworld.org/16450C	mips.ovpworld.org/MaltaFPGA
mips.ovpworld.org/SmartLoaderLinux	motorola.ovpworld.org/MC146818	national.ovpworld.org/16450

<a href="http://national.ovpworld.org/16550">national.ovpworld.org/16550</a>	<a href="http://ovpworld.org/Alpha2x16Display">ovpworld.org/Alpha2x16Display</a>	<a href="http://ovpworld.org/dummyPort">ovpworld.org/dummyPort</a>
<a href="http://ovpworld.org/DynamicBridge">ovpworld.org/DynamicBridge</a>	<a href="http://ovpworld.org/FlashDevice">ovpworld.org/FlashDevice</a>	<a href="http://ovpworld.org/ledRegister">ovpworld.org/ledRegister</a>
<a href="http://ovpworld.org/SerInt">ovpworld.org/SerInt</a>	<a href="http://ovpworld.org/SimpleDma">ovpworld.org/SimpleDma</a>	<a href="http://ovpworld.org/VirtioBlkMMIO">ovpworld.org/VirtioBlkMMIO</a>
<a href="http://philips.ovpworld.org/ISP1761">philips.ovpworld.org/ISP1761</a>	<a href="http://renesas.ovpworld.org/adc">renesas.ovpworld.org/adc</a>	<a href="http://renesas.ovpworld.org/bcu">renesas.ovpworld.org/bcu</a>
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<a href="http://renesas.ovpworld.org/memc">renesas.ovpworld.org/memc</a>	<a href="http://renesas.ovpworld.org/rng">renesas.ovpworld.org/rng</a>	<a href="http://renesas.ovpworld.org/taa">renesas.ovpworld.org/taa</a>
<a href="http://renesas.ovpworld.org/tms">renesas.ovpworld.org/tms</a>	<a href="http://renesas.ovpworld.org/tmt">renesas.ovpworld.org/tmt</a>	<a href="http://renesas.ovpworld.org/uartc">renesas.ovpworld.org/uartc</a>
<a href="http://renesas.ovpworld.org/UPD70F3441Logic">renesas.ovpworld.org/UPD70F3441Logic</a>	<a href="http://smc.ovpworld.org/LAN9118">smc.ovpworld.org/LAN9118</a>	



## 7.0 General Information on Peripheral Models

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers etc. and configuration options and general information for peripheral modeling with Imperas OVP.

### 7.1 Background

Imperas OVP simulation technology enables very high performance simulation, debug and analysis of platforms containing multiple processors and peripheral models. The technology is designed to be extensible: you can create new models of processors, peripherals and other platform components using interfaces and libraries defined by OVP.

The peripheral models created using the OVP APIs run on the Peripheral Simulation Engine (PSE).

The model is typically written in C and compiled into an executable for the PSE processor architecture. The model is compiled for speed of execution and to protect IP. It is dynamically loaded by the simulator at run time.

## 8.0 Building peripherals easily with Imperas iGen

To aid with model creation, Imperas products include iGen, a model generation tool. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process. iGen creates the needed C files. iGen also creates the C++ SystemC TLM2 interface files needed to run peripheral models in SystemC simulations.

iGen takes as input a simple script specification that includes device internals such as registers and memories, port information, component descriptors, and other elements. iGen then builds the C code model files and user editable templates. These include model frameworks with registers, function calls, memory map, and other items. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.

More information on iGen can be found: [imperas.com/products](http://imperas.com/products).

Please contact Imperas to get access to the Imperas documents: `Imperas_Model_Generator_Guide.pdf` and `Imperas_Peripheral_Generator_Guide.pdf`.

## 9.0 Peripheral model internals

Each instance of a peripheral model runs on its own virtual machine with an address space large enough for the model. This processor (the PSE) and its memory are separate from any processors, memories and buses

in the platform being simulated; they exist only to execute the code of the peripheral model.

Interception of functions defined in the peripheral model allows the use of features of the host system in the implementation of the behavior of a peripheral. As an example, a real platform might contain a video display device. When simulating this system, it is generally more convenient not to simulate the complete video display device but to use a video package available on the host machine, such as SDL, and to use this to render to the host display. Also models of uarts, ethernet devices and USB components can make use of the host PC resources during simulation, to allow, for example, a simulation to browse the real internet, or the simulation to connect to a real USB device.

## **10.0 Parts of peripheral models**

### ***10.1 Configuring the Peripheral Instance with Parameters***

A peripheral can include the behaviour of several configurations. These are controlled when the peripheral is instanced in the platform by setting parameters defined on the peripheral.

### ***10.2 Net Ports***

Peripherals may be connected to other peripherals or processors with signal wires (nets). These can be used to act as interrupt signals or used to control behavior between peripherals.

The wires are created in the platform as nets and this net is connected into the peripheral using a net port.

### ***10.3 Bus master ports***

A bus master port initiates (and controls the address of) a bus cycle. Bus cycles are generated by behavioral code within the peripheral model.

### ***10.4 Bus slave ports***

A peripheral can be defined as having several bus slave ports. The bus slave ports can be split into several address blocks. Each address block be either local memory or memory mapped registers. Both of these can have associated callback functions. A memory mapped register can also be defined as specific read/write access, whether it is volatile, and also whether it is associated with a reset pin and mask. A memory mapped register can also have specific bit fields defined.

### ***10.5 Packetnets***

A peripheral can be defined as being connected to packetnet ports. A packetnet is used to model packet based communication such as Ethernet, CAN bus or GSM. A packetnet is created in a platform, then connected to packetnet ports on model instances. A packetnet can have many connections, each able to send or receive packets. A packetnet is used as an efficient method of communication within OVP models.

For more information on modeling with packetnets, please see the peripheral modeling documentation: [OVP\\_Peripheral\\_Modeling\\_Guide.pdf](#), [OVPsim\\_and\\_CpuManager\\_User\\_Guide.pdf](#) and the example: [\\$IMPERAS\\_HOME/Examples/Models/Peripherals/packetnet](#).

## **11.0 More information (documentation) on peripheral models and modeling**

More information on modeling and APIs can be found at: [OVPworld.org/technology\\_apis](http://OVPworld.org/technology_apis).

Specifics on modeling peripherals can be found: [OVP\\_Peripheral\\_Modeling\\_Guide.pdf](#).

A full list of the currently available OVP documentation is available: [OVPworld.org/documentation](http://OVPworld.org/documentation).

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