



## Imperas Peripheral Model Guide

### Model Specific Information for freescale.ovpworld.org / KinetisNFC

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## Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit [OVPworld.org](http://OVPworld.org).

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## 1.0 Model Specific Information

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers, other component parts, and configuration options and general information for peripheral modeling with Imperas OVP.

### 1.1 Licensing

Open Source Apache 2.0

### 1.2 Location

The KinetisNFC peripheral model is located in an Imperas/OVP installation at the VLNV: [freescale.ovpworld.org / peripheral / KinetisNFC / 1.0](http://freescale.ovpworld.org/peripheral/KinetisNFC/1.0).

## 2.0 Net Ports

This model has the following net ports:

Table 1. Net Ports

Name	Type	Must Be Connected	Description
Reset	input	F (False)	

## 3.0 Bus Slave Ports

This model has the following bus slave ports:

### 3.1 Bus Slave Port: *bport1*

Table 2. Bus Slave Port: *bport1*

Name	Size (bytes)	Must Be Connected	Description
bport1	0x4000	F (False)	

Table 3. Bus Slave Port: *bport1* Registers:

Name	Offset	Width (bits)	Description	R/W	is Volatile
ab_CMD1	0x3f00	32	Flash command 1, offset: 0x3F00		
ab_CMD2	0x3f04	32	Flash command 2, offset: 0x3F04		
ab_CAR	0x3f08	32	Column address, offset: 0x3F08		
ab_RAR	0x3f0c	32	Row address, offset: 0x3F0C		
ab_RPT	0x3f10	32	Flash command repeat, offset: 0x3F10		
ab_RAI	0x3f14	32	Row address increment, offset: 0x3F14		
ab_SR1	0x3f18	32	Flash status 1, offset: 0x3F18		

ab_SR2	0x3f1c	32	Flash status 2, offset: 0x3F1C		
ab_DMA1	0x3f20	32	DMA channel 1 address, offset: 0x3F20		
ab_DMACFG	0x3f24	32	DMA configuration, offset: 0x3F24		
ab_SWAP	0x3f28	32	Cach swap, offset: 0x3F28		
ab_SECSZ	0x3f2c	32	Sector size, offset: 0x3F2C		
ab_CFG	0x3f30	32	Flash configuration, offset: 0x3F30		
ab_DMA2	0x3f34	32	DMA channel 2 address, offset: 0x3F34		
ab_ISR	0x3f38	32	Interrupt status, offset: 0x3F38		

## 4.0 Peripheral components in the library

Table 4. Publicly available Imperas/OVP peripheral models (158 models)

Peripheral	Peripheral	Peripheral
<a href="http://freescale.ovpworld.org/KinetisOSC">freescale.ovpworld.org/KinetisOSC</a>	<a href="http://freescale.ovpworld.org/KinetisPDB">freescale.ovpworld.org/KinetisPDB</a>	<a href="http://freescale.ovpworld.org/KinetisPIT">freescale.ovpworld.org/KinetisPIT</a>
<a href="http://freescale.ovpworld.org/KinetisPMC">freescale.ovpworld.org/KinetisPMC</a>	<a href="http://freescale.ovpworld.org/KinetisPORT">freescale.ovpworld.org/KinetisPORT</a>	<a href="http://freescale.ovpworld.org/KinetisRCM">freescale.ovpworld.org/KinetisRCM</a>
<a href="http://freescale.ovpworld.org/KinetisRFSYS">freescale.ovpworld.org/KinetisRFSYS</a>	<a href="http://freescale.ovpworld.org/KinetisRFVBAT">freescale.ovpworld.org/KinetisRFVBAT</a>	<a href="http://freescale.ovpworld.org/KinetisRNG">freescale.ovpworld.org/KinetisRNG</a>
<a href="http://freescale.ovpworld.org/KinetisRTC">freescale.ovpworld.org/KinetisRTC</a>	<a href="http://freescale.ovpworld.org/KinetisSDHC">freescale.ovpworld.org/KinetisSDHC</a>	<a href="http://freescale.ovpworld.org/KinetisSIM">freescale.ovpworld.org/KinetisSIM</a>
<a href="http://freescale.ovpworld.org/KinetisSMC">freescale.ovpworld.org/KinetisSMC</a>	<a href="http://freescale.ovpworld.org/KinetisSPI">freescale.ovpworld.org/KinetisSPI</a>	<a href="http://freescale.ovpworld.org/KinetisTSI">freescale.ovpworld.org/KinetisTSI</a>
<a href="http://freescale.ovpworld.org/KinetisUART">freescale.ovpworld.org/KinetisUART</a>	<a href="http://freescale.ovpworld.org/KinetisUSB">freescale.ovpworld.org/KinetisUSB</a>	<a href="http://freescale.ovpworld.org/KinetisUSBDCD">freescale.ovpworld.org/KinetisUSBDCD</a>
<a href="http://freescale.ovpworld.org/KinetisUSBHS">freescale.ovpworld.org/KinetisUSBHS</a>	<a href="http://freescale.ovpworld.org/KinetisVREF">freescale.ovpworld.org/KinetisVREF</a>	<a href="http://freescale.ovpworld.org/KinetisWDOG">freescale.ovpworld.org/KinetisWDOG</a>
<a href="http://freescale.ovpworld.org/Uart">freescale.ovpworld.org/Uart</a>	<a href="http://freescale.ovpworld.org/VybridADC">freescale.ovpworld.org/VybridADC</a>	<a href="http://freescale.ovpworld.org/VybridANADIG">freescale.ovpworld.org/VybridANADIG</a>
<a href="http://freescale.ovpworld.org/VybridCCM">freescale.ovpworld.org/VybridCCM</a>	<a href="http://freescale.ovpworld.org/VybridDMA">freescale.ovpworld.org/VybridDMA</a>	<a href="http://freescale.ovpworld.org/VybridGPIO">freescale.ovpworld.org/VybridGPIO</a>
<a href="http://freescale.ovpworld.org/VybridI2C">freescale.ovpworld.org/VybridI2C</a>	<a href="http://freescale.ovpworld.org/VybridLCD">freescale.ovpworld.org/VybridLCD</a>	<a href="http://freescale.ovpworld.org/VybridQUADSPI">freescale.ovpworld.org/VybridQUADSPI</a>
<a href="http://freescale.ovpworld.org/VybridSDHC">freescale.ovpworld.org/VybridSDHC</a>	<a href="http://freescale.ovpworld.org/VybridSPI">freescale.ovpworld.org/VybridSPI</a>	<a href="http://freescale.ovpworld.org/VybridUART">freescale.ovpworld.org/VybridUART</a>
<a href="http://freescale.ovpworld.org/VybridUSB">freescale.ovpworld.org/VybridUSB</a>	<a href="http://intel.ovpworld.org/82077AA">intel.ovpworld.org/82077AA</a>	<a href="http://intel.ovpworld.org/82371EB">intel.ovpworld.org/82371EB</a>
<a href="http://intel.ovpworld.org/8253">intel.ovpworld.org/8253</a>	<a href="http://intel.ovpworld.org/8259A">intel.ovpworld.org/8259A</a>	<a href="http://intel.ovpworld.org/NorFlash48F4400">intel.ovpworld.org/NorFlash48F4400</a>
<a href="http://intel.ovpworld.org/PciIDE">intel.ovpworld.org/PciIDE</a>	<a href="http://intel.ovpworld.org/PciPM">intel.ovpworld.org/PciPM</a>	<a href="http://intel.ovpworld.org/PciUSB">intel.ovpworld.org/PciUSB</a>
<a href="http://intel.ovpworld.org/Ps2Control">intel.ovpworld.org/Ps2Control</a>	<a href="http://marvell.ovpworld.org/GT6412x">marvell.ovpworld.org/GT6412x</a>	<a href="http://mips.ovpworld.org/16450C">mips.ovpworld.org/16450C</a>
<a href="http://mips.ovpworld.org/MaltaFPGA">mips.ovpworld.org/MaltaFPGA</a>	<a href="http://mips.ovpworld.org/SmartLoaderLinux">mips.ovpworld.org/SmartLoaderLinux</a>	<a href="http://motorola.ovpworld.org/MC146818">motorola.ovpworld.org/MC146818</a>
<a href="http://national.ovpworld.org/16450">national.ovpworld.org/16450</a>	<a href="http://national.ovpworld.org/16550">national.ovpworld.org/16550</a>	<a href="http://ovpworld.org/Alpha2x16Display">ovpworld.org/Alpha2x16Display</a>
<a href="http://ovpworld.org/dummyPort">ovpworld.org/dummyPort</a>	<a href="http://ovpworld.org/DynamicBridge">ovpworld.org/DynamicBridge</a>	<a href="http://ovpworld.org/FlashDevice">ovpworld.org/FlashDevice</a>
<a href="http://ovpworld.org/ledRegister">ovpworld.org/ledRegister</a>	<a href="http://ovpworld.org/SerInt">ovpworld.org/SerInt</a>	<a href="http://ovpworld.org/SimpleDma">ovpworld.org/SimpleDma</a>
<a href="http://ovpworld.org/VirtioBlkMMIO">ovpworld.org/VirtioBlkMMIO</a>	<a href="http://philips.ovpworld.org/ISP1761">philips.ovpworld.org/ISP1761</a>	<a href="http://renesas.ovpworld.org/adc">renesas.ovpworld.org/adc</a>
<a href="http://renesas.ovpworld.org/bcu">renesas.ovpworld.org/bcu</a>	<a href="http://renesas.ovpworld.org/brg">renesas.ovpworld.org/brg</a>	<a href="http://renesas.ovpworld.org/can">renesas.ovpworld.org/can</a>
<a href="http://renesas.ovpworld.org/can">renesas.ovpworld.org/can</a>	<a href="http://renesas.ovpworld.org/clkggen">renesas.ovpworld.org/clkggen</a>	<a href="http://renesas.ovpworld.org/crc">renesas.ovpworld.org/crc</a>
<a href="http://renesas.ovpworld.org/csib">renesas.ovpworld.org/csib</a>	<a href="http://renesas.ovpworld.org/csie">renesas.ovpworld.org/csie</a>	<a href="http://renesas.ovpworld.org/dma">renesas.ovpworld.org/dma</a>
<a href="http://renesas.ovpworld.org/intc">renesas.ovpworld.org/intc</a>	<a href="http://renesas.ovpworld.org/memc">renesas.ovpworld.org/memc</a>	<a href="http://renesas.ovpworld.org/rng">renesas.ovpworld.org/rng</a>
<a href="http://renesas.ovpworld.org/taa">renesas.ovpworld.org/taa</a>	<a href="http://renesas.ovpworld.org/tms">renesas.ovpworld.org/tms</a>	<a href="http://renesas.ovpworld.org/tmt">renesas.ovpworld.org/tmt</a>
<a href="http://renesas.ovpworld.org/uartc">renesas.ovpworld.org/uartc</a>	<a href="http://renesas.ovpworld.org/UPD70F3441Logic">renesas.ovpworld.org/UPD70F3441Logic</a>	<a href="http://smc.ovpworld.org/LAN9118">smc.ovpworld.org/LAN9118</a>
<a href="http://smc.ovpworld.org/LAN91C111">smc.ovpworld.org/LAN91C111</a>	<a href="http://ti.ovpworld.org/UartInterface">ti.ovpworld.org/UartInterface</a>	<a href="http://xilinx.ovpworld.org/mdm">xilinx.ovpworld.org/mdm</a>
<a href="http://xilinx.ovpworld.org/mpmc">xilinx.ovpworld.org/mpmc</a>	<a href="http://xilinx.ovpworld.org/xps-gpio">xilinx.ovpworld.org/xps-gpio</a>	<a href="http://xilinx.ovpworld.org/xps-iic">xilinx.ovpworld.org/xps-iic</a>
<a href="http://xilinx.ovpworld.org/xps-intc">xilinx.ovpworld.org/xps-intc</a>	<a href="http://xilinx.ovpworld.org/xps-ll-temac">xilinx.ovpworld.org/xps-ll-temac</a>	<a href="http://xilinx.ovpworld.org/xps-mch-emc">xilinx.ovpworld.org/xps-mch-emc</a>
<a href="http://xilinx.ovpworld.org/xps-sysace">xilinx.ovpworld.org/xps-sysace</a>	<a href="http://xilinx.ovpworld.org/xps-timer">xilinx.ovpworld.org/xps-timer</a>	<a href="http://xilinx.ovpworld.org/xps-uartlite">xilinx.ovpworld.org/xps-uartlite</a>
<a href="http://altera.ovpworld.org/dw-apb-timer">altera.ovpworld.org/dw-apb-timer</a>	<a href="http://altera.ovpworld.org/dw-apb-uart">altera.ovpworld.org/dw-apb-uart</a>	<a href="http://altera.ovpworld.org/IntervalTimer32Core">altera.ovpworld.org/IntervalTimer32Core</a>
<a href="http://altera.ovpworld.org/IntervalTimer64Core">altera.ovpworld.org/IntervalTimer64Core</a>	<a href="http://altera.ovpworld.org/JtagUart">altera.ovpworld.org/JtagUart</a>	<a href="http://altera.ovpworld.org/PerformanceCounterCore">altera.ovpworld.org/PerformanceCounterCore</a>
<a href="http://altera.ovpworld.org/RSTMGR">altera.ovpworld.org/RSTMGR</a>	<a href="http://altera.ovpworld.org/SystemIDCore">altera.ovpworld.org/SystemIDCore</a>	<a href="http://altera.ovpworld.org/Uart">altera.ovpworld.org/Uart</a>
<a href="http://amd.ovpworld.org/79C970">amd.ovpworld.org/79C970</a>	<a href="http://arm.ovpworld.org/AaciPL041">arm.ovpworld.org/AaciPL041</a>	<a href="http://arm.ovpworld.org/CompactFlashRegs">arm.ovpworld.org/CompactFlashRegs</a>
<a href="http://arm.ovpworld.org/CoreModule9x6">arm.ovpworld.org/CoreModule9x6</a>	<a href="http://arm.ovpworld.org/DebugLedAndDipSwitch">arm.ovpworld.org/DebugLedAndDipSwitch</a>	<a href="http://arm.ovpworld.org/DMemCtrlPL341">arm.ovpworld.org/DMemCtrlPL341</a>
<a href="http://arm.ovpworld.org/IcpControl">arm.ovpworld.org/IcpControl</a>	<a href="http://arm.ovpworld.org/IcpCounterTimer">arm.ovpworld.org/IcpCounterTimer</a>	<a href="http://arm.ovpworld.org/IntICP">arm.ovpworld.org/IntICP</a>
<a href="http://arm.ovpworld.org/IntICP">arm.ovpworld.org/IntICP</a>	<a href="http://arm.ovpworld.org/KbPL050">arm.ovpworld.org/KbPL050</a>	<a href="http://arm.ovpworld.org/L2CachePL310">arm.ovpworld.org/L2CachePL310</a>
<a href="http://arm.ovpworld.org/LcdPL110">arm.ovpworld.org/LcdPL110</a>	<a href="http://arm.ovpworld.org/MmcPL181">arm.ovpworld.org/MmcPL181</a>	<a href="http://arm.ovpworld.org/RtcPL031">arm.ovpworld.org/RtcPL031</a>
<a href="http://arm.ovpworld.org/SerBusDviRegs">arm.ovpworld.org/SerBusDviRegs</a>	<a href="http://arm.ovpworld.org/SmartLoaderArm64Linux">arm.ovpworld.org/SmartLoaderArm64Linux</a>	<a href="http://arm.ovpworld.org/SmartLoaderArmLinux">arm.ovpworld.org/SmartLoaderArmLinux</a>
<a href="http://arm.ovpworld.org/SMemCtrlPL354">arm.ovpworld.org/SMemCtrlPL354</a>	<a href="http://arm.ovpworld.org/SysCtrlSP810">arm.ovpworld.org/SysCtrlSP810</a>	<a href="http://arm.ovpworld.org/TimerSP804">arm.ovpworld.org/TimerSP804</a>
<a href="http://arm.ovpworld.org/TzpcBP147">arm.ovpworld.org/TzpcBP147</a>	<a href="http://arm.ovpworld.org/UartPL011">arm.ovpworld.org/UartPL011</a>	<a href="http://arm.ovpworld.org/VexpressSysRegs">arm.ovpworld.org/VexpressSysRegs</a>
<a href="http://arm.ovpworld.org/WdtSP805">arm.ovpworld.org/WdtSP805</a>	<a href="http://atmel.ovpworld.org/AdvancedInterruptController">atmel.ovpworld.org/AdvancedInterruptController</a>	<a href="http://atmel.ovpworld.org/ParallelIOController">atmel.ovpworld.org/ParallelIOController</a>
<a href="http://atmel.ovpworld.org/PowerSaving">atmel.ovpworld.org/PowerSaving</a>	<a href="http://atmel.ovpworld.org/SpecialFunction">atmel.ovpworld.org/SpecialFunction</a>	<a href="http://atmel.ovpworld.org/TimerCounter">atmel.ovpworld.org/TimerCounter</a>

atmel.ovpworld.org/UsartInterface	atmel.ovpworld.org/WatchdogTimer	cirrus.ovpworld.org/GD5446
freescale.ovpworld.org/KinetisADC	freescale.ovpworld.org/KinetisAIPS	freescale.ovpworld.org/KinetisAXBS
freescale.ovpworld.org/KinetisCAN	freescale.ovpworld.org/KinetisCMP	freescale.ovpworld.org/KinetisCMT
freescale.ovpworld.org/KinetisCRC	freescale.ovpworld.org/KinetisDAC	freescale.ovpworld.org/KinetisDDR
freescale.ovpworld.org/KinetisDMA	freescale.ovpworld.org/KinetisDMAC	freescale.ovpworld.org/KinetisDMAMUX
freescale.ovpworld.org/KinetisENET	freescale.ovpworld.org/KinetisEWM	freescale.ovpworld.org/KinetisFB
freescale.ovpworld.org/KinetisFMC	freescale.ovpworld.org/KinetisFTFE	freescale.ovpworld.org/KinetisFTM
freescale.ovpworld.org/KinetisGPIO	freescale.ovpworld.org/KinetisI2C	freescale.ovpworld.org/KinetisI2S
freescale.ovpworld.org/KinetisLLWU	freescale.ovpworld.org/KinetisLPTMR	freescale.ovpworld.org/KinetisMCG
freescale.ovpworld.org/KinetisMPU	freescale.ovpworld.org/KinetisNFC	

## 5.0 General Information on Peripheral Models

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers etc. and configuration options and general information for peripheral modeling with Imperas OVP.

### 5.1 Background

Imperas OVP simulation technology enables very high performance simulation, debug and analysis of platforms containing multiple processors and peripheral models. The technology is designed to be extensible: you can create new models of processors, peripherals and other platform components using interfaces and libraries defined by OVP.

The peripheral models created using the OVP APIs run on the Peripheral Simulation Engine (PSE).

The model is typically written in C and compiled into an executable for the PSE processor architecture. The model is compiled for speed of execution and to protect IP. It is dynamically loaded by the simulator at run time.

## 6.0 Building peripherals easily with Imperas iGen

To aid with model creation, Imperas products include iGen, a model generation tool. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process. iGen creates the needed C files. iGen also creates the C++ SystemC TLM2 interface files needed to run peripheral models in SystemC simulations.

iGen takes as input a simple script specification that includes device internals such as registers and memories, port information, component descriptors, and other elements. iGen then builds the C code model files and user editable templates. These include model frameworks with registers, function calls, memory map, and other items. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.

More information on iGen can be found: [imperas.com/products](http://imperas.com/products).

Please contact Imperas to get access to the Imperas documents: `Imperas_Model_Generator_Guide.pdf` and `Imperas_Peripheral_Generator_Guide.pdf`.

## 7.0 Peripheral model internals

Each instance of a peripheral model runs on its own virtual machine with an address space large enough for the model. This processor (the PSE) and its memory are separate from any processors, memories and buses



in the platform being simulated; they exist only to execute the code of the peripheral model.

Interception of functions defined in the peripheral model allows the use of features of the host system in the implementation of the behavior of a peripheral. As an example, a real platform might contain a video display device. When simulating this system, it is generally more convenient not to simulate the complete video display device but to use a video package available on the host machine, such as SDL, and to use this to render to the host display. Also models of uarts, ethernet devices and USB components can make use of the host PC resources during simulation, to allow, for example, a simulation to browse the real internet, or the simulation to connect to a real USB device.

## **8.0 Parts of peripheral models**

### ***8.1 Configuring the Peripheral Instance with Parameters***

A peripheral can include the behaviour of several configurations. These are controlled when the peripheral is instanced in the platform by setting parameters defined on the peripheral.

### ***8.2 Net Ports***

Peripherals may be connected to other peripherals or processors with signal wires (nets). These can be used to act as interrupt signals or used to control behavior between peripherals.

The wires are created in the platform as nets and this net is connected into the peripheral using a net port.

### ***8.3 Bus master ports***

A bus master port initiates (and controls the address of) a bus cycle. Bus cycles are generated by behavioral code within the peripheral model.

### ***8.4 Bus slave ports***

A peripheral can be defined as having several bus slave ports. The bus slave ports can be split into several address blocks. Each address block be either local memory or memory mapped registers. Both of these can have associated callback functions. A memory mapped register can also be defined as specific read/write access, whether it is volatile, and also whether it is associated with a reset pin and mask. A memory mapped register can also have specific bit fields defined.

### ***8.5 Packetnets***

A peripheral can be defined as being connected to packetnet ports. A packetnet is used to model packet based communication such as Ethernet, CAN bus or GSM. A packetnet is created in a platform, then connected to packetnet ports on model instances. A packetnet can have many connections, each able to send or receive packets. A packetnet is used as an efficient method of communication within OVP models.

For more information on modeling with packetnets, please see the peripheral modeling documentation: [OVP\\_Peripheral\\_Modeling\\_Guide.pdf](#), [OVPsim\\_and\\_CpuManager\\_User\\_Guide.pdf](#) and the example: [\\$IMPERAS\\_HOME/Examples/Models/Peripherals/packetnet](#).

## **9.0 More information (documentation) on peripheral models and modeling**

More information on modeling and APIs can be found at: [OVPworld.org/technology\\_apis](http://OVPworld.org/technology_apis).

Specifics on modeling peripherals can be found: [OVP\\_Peripheral\\_Modeling\\_Guide.pdf](#).

A full list of the currently available OVP documentation is available: [OVPworld.org/documentation](http://OVPworld.org/documentation).

#