Imperas Peripheral Model Guide

Model Specific Information for freescale.ovpworld.org / KinetisFMC

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

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1.0 Model Specific Information

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers, other component parts, and configuration options and general information for peripheral modeling with Imperas OVP.

1.1 Licensing

Open Source Apache 2.0

1.2 Location

The KinetisFMC peripheral model is located in an Imperas/OVP installation at the VLNV: freescale.ovpworld.org / peripheral / KinetisFMC / 1.0.

2.0 Net Ports

This model has the following net ports:

Table 1. Net Ports

Name	Type	Must Be Connected	Description
Reset	input	F (False)	

3.0 Bus Slave Ports

This model has the following bus slave ports:

3.1 Bus Slave Port: bport1

Table 2. Bus Slave Port: bport1

Name	Size (bytes)	Must Be Connected	Description
bport1	0x1000	F (False)	

Table 3. Bus Slave Port: bport1 Registers:

Name	Offset	Width (bits)	Description	R/W	is Volatile
ab_PFAPR	0x0	32	Flash Access Protection Register, offset: 0x0		
ab_PFB01CR	0x4	32	Flash Bank 0-1 Control Register, offset: 0x4		
ab_PFB23CR	0x8	32	Flash Bank 2-3 Control Register, offset: 0x8		
ab_TAGVDW0S0	0x100	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_TAGVDW0S1	0x104	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_TAGVDW0S2	0x108	32	Cache Tag Storage, array offset: 0x100, array step:		

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			index*0x10, index2*0x4		
ab_TAGVDW0S3	0x10c	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_TAGVDW1S0	0x110	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_TAGVDW1S1	0x114	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_TAGVDW1S2	0x118	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_TAGVDW1S3	0x11c	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_TAGVDW2S0	0x120	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_TAGVDW2S1	0x124	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_TAGVDW2S2	0x128	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_TAGVDW2S3	0x12c	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_TAGVDW3S0	0x130	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_TAGVDW3S1	0x134	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_TAGVDW3S2	0x138	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_TAGVDW3S3	0x13c	32	Cache Tag Storage, array offset: 0x100, array step: index*0x10, index2*0x4		
ab_DATAW0S0UM	0x200	32	Cache Data Storage (uppermost word), array offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW0S0MU	0x204	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW0S0ML	0x208	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW0S0LM	0x20c	32	Cache Data Storage (lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW0S1UM	0x210	32	Cache Data Storage (uppermost word), array		

			offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW0S1MU	0x214	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW0S1ML	0x218	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW0S1LM	0x21c	32	Cache Data Storage (lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW0S2UM	0x220	32	Cache Data Storage (uppermost word), array offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW0S2MU	0x224	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW0S2ML	0x228	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW0S2LM	0x22c	32	Cache Data Storage (lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW0S3UM	0x230	32	Cache Data Storage (uppermost word), array offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW0S3MU	0x234	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW0S3ML	0x238	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW0S3LM	0x23c	32	Cache Data Storage (lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW1S0UM	0x240	32	Cache Data Storage (uppermost word), array offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW1S0MU	0x244	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW1S0ML	0x248	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW1S0LM	0x24c	32	Cache Data Storage		

			(lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW1S1UM	0x250	32	Cache Data Storage (uppermost word), array offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW1S1MU	0x254	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW1S1ML	0x258	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW1S1LM	0x25c	32	Cache Data Storage (lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW1S2UM	0x260	32	Cache Data Storage (uppermost word), array offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW1S2MU	0x264	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW1S2ML	0x268	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW1S2LM	0x26c	32	Cache Data Storage (lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW1S3UM	0x270	32	Cache Data Storage (uppermost word), array offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW1S3MU	0x274	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW1S3ML	0x278	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW1S3LM	0x27c	32	Cache Data Storage (lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW2S0UM	0x280	32	Cache Data Storage (uppermost word), array offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW2S0MU	0x284	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		

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ab_DATAW2S0ML	0x288	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW2S0LM	0x28c	32	Cache Data Storage (lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW2S1UM	0x290	32	Cache Data Storage (uppermost word), array offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW2S1MU	0x294	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW2S1ML	0x298	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW2S1LM	0x29c	32	Cache Data Storage (lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW2S2UM	0x2a0	32	Cache Data Storage (uppermost word), array offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW2S2MU	0x2a4	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW2S2ML	0x2a8	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW2S2LM	0x2ac	32	Cache Data Storage (lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW2S3UM	0x2b0	32	Cache Data Storage (uppermost word), array offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW2S3MU	0x2b4	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW2S3ML	0x2b8	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW2S3LM	0x2bc	32	Cache Data Storage (lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW3S0UM	0x2c0	32	Cache Data Storage (uppermost word), array offset: 0x200, array step:		

			index*0x40, index2*0x10		
ab_DATAW3S0MU	0x2c4	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW3S0ML	0x2c8	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW3S0LM	0x2cc	32	Cache Data Storage (lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW3S1UM	0x2d0	32	Cache Data Storage (uppermost word), array offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW3S1MU	0x2d4	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW3S1ML	0x2d8	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW3S1LM	0x2dc	32	Cache Data Storage (lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW3S2UM	0x2e0	32	Cache Data Storage (uppermost word), array offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW3S2MU	0x2e4	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW3S2ML	0x2e8	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW3S2LM	0x2ec	32	Cache Data Storage (lowermost word), array offset: 0x20C, array step: index*0x40, index2*0x10		
ab_DATAW3S3UM	0x2f0	32	Cache Data Storage (uppermost word), array offset: 0x200, array step: index*0x40, index2*0x10		
ab_DATAW3S3MU	0x2f4	32	Cache Data Storage (mid-upper word), array offset: 0x204, array step: index*0x40, index2*0x10		
ab_DATAW3S3ML	0x2f8	32	Cache Data Storage (mid-lower word), array offset: 0x208, array step: index*0x40, index2*0x10		
ab_DATAW3S3LM	0x2fc	32	Cache Data Storage (lowermost word), array		

			offset: 0x20C, array step: index*0x40, index2*0x10		

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4.0 Peripheral components in the library

Table 4. Publicly available Imperas/OVP peripheral models (158 models)

Peripheral	Peripheral	Peripheral
freescale.ovpworld.org/KinetisFTFE	freescale.ovpworld.org/KinetisFTM	freescale.ovpworld.org/KinetisGPIO
freescale.ovpworld.org/KinetisI2C	freescale.ovpworld.org/KinetisI2S	freescale.ovpworld.org/KinetisLLWU
freescale.ovpworld.org/KinetisLPTMR	freescale.ovpworld.org/KinetisMCG	freescale.ovpworld.org/KinetisMPU
freescale.ovpworld.org/KinetisNFC	freescale.ovpworld.org/KinetisOSC	freescale.ovpworld.org/KinetisPDB
freescale.ovpworld.org/KinetisPIT	freescale.ovpworld.org/KinetisPMC	freescale.ovpworld.org/KinetisPORT
freescale.ovpworld.org/KinetisRCM	freescale.ovpworld.org/KinetisRFSYS	freescale.ovpworld.org/KinetisRFVBAT
freescale.ovpworld.org/KinetisRNG	freescale.ovpworld.org/KinetisRTC	freescale.ovpworld.org/KinetisSDHC
freescale.ovpworld.org/KinetisSIM	freescale.ovpworld.org/KinetisSMC	freescale.ovpworld.org/KinetisSPI
freescale.ovpworld.org/KinetisTSI	freescale.ovpworld.org/KinetisUART	freescale.ovpworld.org/KinetisUSB
freescale.ovpworld.org/KinetisUSBDCD	freescale.ovpworld.org/KinetisUSBHS	freescale.ovpworld.org/KinetisVREF
freescale.ovpworld.org/KinetisWDOG	freescale.ovpworld.org/Uart	freescale.ovpworld.org/VybridADC
freescale.ovpworld.org/VybridANADIG	freescale.ovpworld.org/VybridCCM	freescale.ovpworld.org/VybridDMA
freescale.ovpworld.org/VybridGPIO	freescale.ovpworld.org/VybridI2C	freescale.ovpworld.org/VybridLCD
freescale.ovpworld.org/VybridQUADSPI	freescale.ovpworld.org/VybridSDHC	freescale.ovpworld.org/VybridSPI
freescale.ovpworld.org/VybridUART	freescale.ovpworld.org/VybridUSB	intel.ovpworld.org/82077AA
intel.ovpworld.org/82371EB	intel.ovpworld.org/8253	intel.ovpworld.org/8259A
intel.ovpworld.org/NorFlash48F4400	intel.ovpworld.org/PciIDE	intel.ovpworld.org/PciPM
intel.ovpworld.org/PciUSB	intel.ovpworld.org/Ps2Control	marvell.ovpworld.org/GT6412x
mips.ovpworld.org/16450C	mips.ovpworld.org/MaltaFPGA	mips.ovpworld.org/SmartLoaderLinux
motorola.ovpworld.org/MC146818	national.ovpworld.org/16450	national.ovpworld.org/16550
ovpworld.org/Alpha2x16Display	ovpworld.org/dummyPort	ovpworld.org/DynamicBridge
ovpworld.org/FlashDevice	ovpworld.org/ledRegister	ovpworld.org/SerInt
ovpworld.org/SimpleDma	ovpworld.org/VirtioBlkMMIO	philips.ovpworld.org/ISP1761
renesas.ovpworld.org/adc	renesas.ovpworld.org/bcu	renesas.ovpworld.org/brg
renesas.ovpworld.org/can	renesas.ovpworld.org/can	renesas.ovpworld.org/clkgen
renesas.ovpworld.org/crc	renesas.ovpworld.org/csib	renesas.ovpworld.org/csie
renesas.ovpworld.org/dma	renesas.ovpworld.org/intc	renesas.ovpworld.org/memc
renesas.ovpworld.org/rng	renesas.ovpworld.org/taa	renesas.ovpworld.org/tms
renesas.ovpworld.org/tmt	renesas.ovpworld.org/uartc	renesas.ovpworld.org/UPD70F3441Logic
smsc.ovpworld.org/LAN9118	smsc.ovpworld.org/LAN91C111	ti.ovpworld.org/UartInterface
xilinx.ovpworld.org/mdm	xilinx.ovpworld.org/mpmc	xilinx.ovpworld.org/xps-gpio
xilinx.ovpworld.org/xps-iic	xilinx.ovpworld.org/xps-intc	xilinx.ovpworld.org/xps-ll-temac
xilinx.ovpworld.org/xps-mch-emc	xilinx.ovpworld.org/xps-sysace	xilinx.ovpworld.org/xps-timer
xilinx.ovpworld.org/xps-uartlite	altera.ovpworld.org/dw-apb-timer	altera.ovpworld.org/dw-apb-uart
altera.ovpworld.org/IntervalTimer32Core	altera.ovpworld.org/IntervalTimer64Core	altera.ovpworld.org/JtagUart
altera.ovpworld.org/PerformanceCounterCore	altera.ovpworld.org/RSTMGR	altera.ovpworld.org/SystemIDCore
altera.ovpworld.org/Uart	amd.ovpworld.org/79C970	arm.ovpworld.org/AaciPL041
arm.ovpworld.org/CompactFlashRegs	arm.ovpworld.org/CoreModule9x6	arm.ovpworld.org/DebugLedAndDipSwitch
arm.ovpworld.org/DMemCtrlPL341	arm.ovpworld.org/IcpControl	arm.ovpworld.org/IcpCounterTimer
arm.ovpworld.org/IntICP	arm.ovpworld.org/IntICP	arm.ovpworld.org/KbPL050
arm.ovpworld.org/L2CachePL310	arm.ovpworld.org/LcdPL110	arm.ovpworld.org/MmciPL181
arm.ovpworld.org/RtcPL031	arm.ovpworld.org/SerBusDviRegs	arm.ovpworld.org/SmartLoaderArm64Linux
arm.ovpworld.org/SmartLoaderArmLinux	arm.ovpworld.org/SMemCtrlPL354	arm.ovpworld.org/SysCtrlSP810

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arm.ovpworld.org/TimerSP804	arm.ovpworld.org/TzpcBP147	arm.ovpworld.org/UartPL011
arm.ovpworld.org/VexpressSysRegs	arm.ovpworld.org/WdtSP805	atmel.ovpworld.org/AdvancedInterruptController
atmel.ovpworld.org/ParallelIOController	atmel.ovpworld.org/PowerSaving	atmel.ovpworld.org/SpecialFunction
atmel.ovpworld.org/TimerCounter	atmel.ovpworld.org/UsartInterface	atmel.ovpworld.org/WatchdogTimer
cirrus.ovpworld.org/GD5446	freescale.ovpworld.org/KinetisADC	freescale.ovpworld.org/KinetisAIPS
freescale.ovpworld.org/KinetisAXBS	freescale.ovpworld.org/KinetisCAN	freescale.ovpworld.org/KinetisCMP
freescale.ovpworld.org/KinetisCMT	freescale.ovpworld.org/KinetisCRC	freescale.ovpworld.org/KinetisDAC
freescale.ovpworld.org/KinetisDDR	freescale.ovpworld.org/KinetisDMA	freescale.ovpworld.org/KinetisDMAC
freescale.ovpworld.org/KinetisDMAMUX	freescale.ovpworld.org/KinetisENET	freescale.ovpworld.org/KinetisEWM
freescale.ovpworld.org/KinetisFB	freescale.ovpworld.org/KinetisFMC	

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5.0 General Information on Peripheral Models

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers etc. and configuration options and general information for peripheral modeling with Imperas OVP.

5.1 Background

Imperas OVP simulation technology enables very high performance simulation, debug and analysis of platforms containing multiple processors and peripheral models. The technology is designed to be extensible: you can create new models of processors, peripherals and other platform components using interfaces and libraries defined by OVP.

The peripheral models created using the OVP APIs run on the Peripheral Simulation Engine (PSE).

The model is typically written in C and compiled into an executable for the PSE processor architecture. The model is compiled for speed of execution and to protect IP. It is dynamically loaded by the simulator at run time.

6.0 Building peripherals easily with Imperas iGen

To aid with model creation, Imperas products include iGen, a model generation tool. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process. iGen creates the needed C files. iGen also creates the C++ SystemC TLM2 interface files needed to run peripheral models in SystemC simulations.

iGen takes as input a simple script specification that includes device internals such as registers and memories, port information, component descriptors, and other elements. iGen then builds the C code model files and user editable templates. These include model frameworks with registers, function calls, memory map, and other items. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.

More information on iGen can be found: imperas.com/products.

Please contact Imperas to get access to the Imperas documents: Imperas_Model_Generator_Guide.pdf and Imperas_Peripheral_Generator_Guide.pdf.

7.0 Peripheral model internals

Each instance of a peripheral model runs on its own virtual machine with an address space large enough for the model. This processor (the PSE) and its memory are separate from any processors, memories and buses

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in the platform being simulated; they exist only to execute the code of the peripheral model.

Interception of functions defined in the peripheral model allows the use of features of the host system in the implementation of the behavior of a peripheral. As an example, a real platform might contain a video display device. When simulating this system, it is generally more convenient not to simulate the complete video display device but to use a video package available on the host machine, such as SDL, and to use this to render to the host display. Also models of uarts, ethernet devices and USB components can make use of the host PC resources during simulation, to allow, for example, a simulation to browse the real internet, or the simulation to connect to a real USB device.

8.0 Parts of peripheral models

8.1 Configuring the Peripheral Instance with Parameters
A peripheral can include the behaviour of several configurations. These are controlled when the peripheral is instanced in the platform by setting parameters defined on the peripheral.

8.2 Net Ports
Peripherals may be connected to other peripherals or processors with signal wires (nets). These can be used to act as interrupt signals or used to control behavior between peripherals.
The wires are created in the platform as nets and this net is connected into the peripheral using a net port.

8.3 Bus master ports
A bus master port initiates (and controls the address of) a bus cycle. Bus cycles are generated by behavioral code within the peripheral model.

8.4 Bus slave ports
A peripheral can be defined as having several bus slave ports. The bus slave ports can be split into several address blocks. Each address block be either local memory or memory mapped registers. Both of these can have associated callback functions. A memory mapped register can also be defined as specific read/write access, whether it is volatile, and also whether it is associated with a reset pin and mask. A memory mapped register can also have specific bit fields defined.

8.5 Packetnets
A peripheral can be defined as being connected to packetnet ports. A packetnet is used to model packet based communication such as Ethernet, CAN bus or GSM. A packetnet is created in a platform, then connected to packetnet ports on model instances. A packetnet can have many connections, each able to send or receive packets. A packetnet is used as an efficient method of communication within OVP models.

For more information on modeling with packetnets, please see the peripheral modeling documentation:
OVP_Peripheral_Modeling_Guide.pdf, OVPsim_and_CpuManager_User_Guide.pdf and the example:
$IMPERAS_HOME/Examples/Models/Peripherals/packetnet.

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9.0 More information (documentation) on peripheral models and modeling

More information on modeling and APIs can be found at: OVPworld.org/technology_apis.

Specifics on modeling peripherals can be found: OVP_Peripheral_Modeling_Guide.pdf.

A full list of the currently available OVP documentation is available: OVPworld.org/documentation.
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