OVP Guide to Using Processor Models

Model Specific Information for variant renesas_v850_V850E2

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1.0 Overview

This document provides the details of an OVP Fast Processor Model variant.
OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.
The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance.
Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.
The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners.
There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

V850 Family Processor Model.

1.2 Licensing

Open Source Apache 2.0

1.3 Limitations

This variant is currently under development.

1.4 Verification

Models have been extensively tested by Imperas, In addition Verification suites have been supplied by Renesas for CORE validation

1.5 Features

2.0 Configuration

2.1 Location

The model source and object file is found in the VLNV tree at:
renesas.ovpworld.org/processor/v850/1.0

2.2 GDB Path

The default GDB for this model is found at:
$IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/v850-elf-gdb

2.3 Semi-Host Library

The default semi-host library file is found in the VLNV tree at :
renesas.ovpworld.org/semihosting/v850Newlib/1.0

2.4 Processor Endian-ness

This is a LITTLE endian model.

2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

2.6 Processor ELF Code

ELF codes supported by this model are: , 0x57, 0x24, 0x70f1, 0x70ff and 0x747b.

3.0 Other Variants in this Model

Table 1.

Variant
V850
V850E1
V850E1F
V850ES
V850E2
V850E2M
V850E2R

4.0 Bus Ports

Table 2.

Type	Name	Bits
master (initiator)	INSTRUCTION	32
master (initiator)	DATA	32

5.0 Net Ports

Table 3.

Name	Type	Description
intp	input	Interrupt Port
nmi0	input	Non-Maskable Interrupt Port
nmi1	input	Non-Maskable Interrupt Port
nmi2	input	Non-Maskable Interrupt Port
reset	input	Reset Port
mireti	output	Return from Interrupt Port
intack	output	Interrupt Acknowledge Port

6.0 FIFO Ports

No FIFO Ports in this model.

7.0 Parameters

Table 4.

Name	Type	Description
verbose	Boolean	Specify verbose output messages
GDBSIMMODE	Boolean	GDB Simulator Compatibility Mode

8.0 Execution Modes

No execution modes.

9.0 Exceptions

Table 5.

Name	Code	Description
reset	0	Reset Signal Exception
nmi0	16	Non Maskable Interrupt(0) Exception
nmi1	32	Non Maskable Interrupt(1) Exception
nmi2	48	Non Maskable Interrupt(2) Exception
intp	65535	Maskable Interrupt Exception - Vector value = (0x0000ffff AND intp)
trap0	64	TRAP0 Exception
trap1	80	TRAP1 Exception
ilgop	96	Illegal OPCODE Exception

10.0 Hierarchy of the model

A CPU core may allow the user to configure it to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.
OVP processor models can be written to include SMP blocks and to have many levels of hierarchy.

Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

10.1 Level 1:

This level in the model hierarchy has 2 commands.

This level in the model hierarchy has 2 register groups:

Table 6.

Group name	Registers
User	32
System	117

This level in the model hierarchy has no children.

11.0 Model Commands

11.1 Level 1:

Table 7.

Name	Arguments
isync	specify instruction address range for synchronous execution
itrace	enable or disable instruction tracing

12.0 Registers

12.1 Level 1:

12.1.1 User

Table 8.

Name	Bits	Initial value (Hex)		Description
R0	32	0	r-	Zero Register
R1	32	0	rw	Assembler-reserved register
R2	32	0	rw	Address/data variable register (when the real-time OS to be used is not using r2)
R3	32	0	rw	Stack pointer (SP)
R4	32	0	rw	Global pointer (GP)
R5	32	0	rw	Test pointer (TP)
R6	32	0	rw	Address/data variable registers
R7	32	0	rw	Address/data variable registers
R8	32	0	rw	Address/data variable registers
R9	32	0	rw	Address/data variable registers
R10	32	0	rw	Address/data variable registers
R11	32	0	rw	Address/data variable registers
R12	32	0	rw	Address/data variable registers
R13	32	0	rw	Address/data variable registers
R14	32	0	rw	Address/data variable registers
R15	32	0	rw	Address/data variable registers
R16	32	0	rw	Address/data variable registers
R17	32	0	rw	Address/data variable registers
R18	32	0	rw	Address/data variable registers
R19	32	0	rw	Address/data variable registers
R20	32	0	rw	Address/data variable registers
R21	32	0	rw	Address/data variable registers
R22	32	0	rw	Address/data variable registers
R23	32	0	rw	Address/data variable registers
R24	32	0	rw	Address/data variable registers
R25	32	0	rw	Address/data variable registers
R26	32	0	rw	Address/data variable registers

R27	32	0	rw	Address/data variable registers
R28	32	0	rw	Address/data variable registers
R29	32	0	rw	Address/data variable registers
R30	32	0	rw	Element pointer (EP)
R31	32	0	rw	Link pointer (LP)

12.1.2 System

Table 9.

Name	Bits	Initial value (Hex)		Description
EIPC	32	0	r-	Interrupt status-saving register PC
EIPSW	32	0	r-	Interrupt status-saving register PSW
FEPC	32	0	r-	NMI status-saving register PC
FEPSW	32	0	r-	NMI status-saving register PSW
ECR	32	0	r-	Exception cause register
PSW	32	20	r-	Program status word
PID	32	0	r-	_UNIMPLEMENTED_
CFG	32	0	r-	_UNIMPLEMENTED_
SR8	32	0	r-	_UNIMPLEMENTED_
SR9	32	0	r-	_UNIMPLEMENTED_
SR10	32	0	r-	_UNIMPLEMENTED_
SCCFG	32	0	r-	_UNIMPLEMENTED_
SCBP	32	0	r-	_UNIMPLEMENTED_
EIIC	32	0	r-	EI Cause Register
FEIC	32	0	r-	FE Cause Register
DBIC	32	0	r-	DB Cause Register
CTPC	32	0	r-	CALLT status-saving register PC
CTPSW	32	0	r-	CALLT status-saving register PSW
DBPC	32	0	r-	Exception/Debug trap status-saving register PC
DBPSW	32	0	r-	Exception/Debug trap status-saving register PSW
CTBP	32	0	r-	CALLT base pointer
DIR	32	0	r-	Debug Interface register
SR22	32	0	r-	_UNIMPLEMENTED_
SR23	32	0	r-	_UNIMPLEMENTED_
SR24	32	0	r-	_UNIMPLEMENTED_
SR25	32	0	r-	_UNIMPLEMENTED_
SR26	32	0	r-	_UNIMPLEMENTED_
SR27	32	0	r-	_UNIMPLEMENTED_
EIWR	32	0	r-	EIWR
FEWR	32	0	r-	FEWR
DBWR	32	0	r-	DBWR
BSEL	32	0	r-	Bank Select Register

PC	32	0	rw	Program Counter
FPVIP	32	0	r-	
SR33	32	0	r-	
SR34	32	0	r-	
SR35	32	0	r-	
VMECR	32	0	r-	
VMTID	32	0	r-	
VMADR	32	0	r-	
SR39	32	0	r-	
VPECR	32	0	r-	
VPTID	32	0	r-	
VPADR	32	0	r-	
SR43	32	0	r-	
VDECR	32	0	r-	
VDTID	32	0	r-	
SR46	32	0	r-	
SR47	32	0	r-	
SR48	32	0	r-	
SR49	32	0	r-	
SR50	32	0	r-	
SR51	32	0	r-	
SR52	32	0	r-	
SR53	32	0	r-	
SR54	32	0	r-	
SR55	32	0	r-	
SR56	32	0	r-	
SR57	32	0	r-	
SR58	32	0	r-	
SR59	32	0	r-	
MPM	32	0	r-	
MPC	32	0	r-	
TID	32	0	r-	
PPA	32	0	r-	
PPM	32	0	r-	
PPC	32	0	r-	
DCC	32	0	r-	
DCV0	32	0	r-	
DCV1	32	0	r-	
SR69	32	0	r-	
SPAL	32	0	r-	
SPAU	32	0	r-	
IPA0L	32	0	r-	

IPA0U	32	0	r-	
IPA1L	32	0	r-	
IPA1U	32	0	r-	
IPA2L	32	0	r-	
IPA2U	32	0	r-	
IPA3L	32	0	r-	
IPA3U	32	0	r-	
DPA0L	32	0	r-	
DPA0U	32	0	r-	
DPA1L	32	0	r-	
DPA1U	32	0	r-	
DPA2L	32	0	r-	
DPA2U	32	0	r-	
DPA3L	32	0	r-	
DPA3U	32	0	r-	
SR88	32	0	r-	
SR89	32	0	r-	
SR80	32	0	r-	
SR91	32	0	r-	
SR92	32	0	r-	
SR93	32	0	r-	
FPSR	32	20000	r-	
FPEPC	32	0	r-	
FPST	32	0	r-	
FPCC	32	0	r-	
FPCFG	32	0	r-	
SR99	32	0	r-	
SR100	32	0	r-	
SR101	32	0	r-	
SR102	32	0	r-	
SR103	32	0	r-	
SR104	32	0	r-	
SR105	32	0	r-	
SR106	32	0	r-	
SR107	32	0	r-	
SR108	32	0	r-	
SR109	32	0	r-	
SR100	32	0	r-	
SR101	32	0	r-	
SR102	32	0	r-	
SR103	32	0	r-	
SR104	32	0	r-	

SR105	32	0	r-	

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