



## Imperas Peripheral Model Guide

### Model Specific Information for [freescale.ovpworld.org](http://freescale.ovpworld.org) / VybridUSB

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## Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit [OVPworld.org](http://OVPworld.org).

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## 1.0 Model Specific Information

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers, other component parts, and configuration options and general information for peripheral modeling with Imperas OVP.

### 1.1 Licensing

Open Source Apache 2.0

### 1.2 Location

The VybridUSB peripheral model is located in an Imperas/OVP installation at the VLNV: [freescale.ovpworld.org / peripheral / VybridUSB / 1.0](http://freescale.ovpworld.org/peripheral/VybridUSB/1.0).

## 2.0 Net Ports

This model has the following net ports:

Table 1. Net Ports

Name	Type	Must Be Connected	Description
Reset	input	F (False)	

## 3.0 Bus Slave Ports

This model has the following bus slave ports:

### 3.1 Bus Slave Port: *bport1*

Table 2. Bus Slave Port: bport1

Name	Size (bytes)	Must Be Connected	Description
bport1	0x1000	F (False)	

Table 3. Bus Slave Port: bport1 Registers:

Name	Offset	Width (bits)	Description	R/W	is Volatile
ab_ID	0x0	32	Identification register, offset: 0x0		
ab_HWGENERAL	0x4	32	Hardware General, offset: 0x4		
ab_HWHOST	0x8	32	Host Hardware Parameters, offset: 0x8		
ab_HWDEVICE	0xc	32	Device Hardware Parameters, offset: 0xC		
ab_HWTXBUF	0x10	32	TX Buffer Hardware Parameters, offset: 0x10		
ab_HWRXBUF	0x14	32	RX Buffer Hardware Parameters, offset: 0x14		
ab_GPTIMEROLD	0x80	32	General Purpose Timer #0 Load, offset: 0x80		

ab_GPTIMER0CTRL	0x84	32	General Purpose Timer #0 Controller, offset: 0x84		
ab_GPTIMER1LD	0x88	32	General Purpose Timer #1 Load, offset: 0x88		
ab_GPTIMER1CTRL	0x8c	32	General Purpose Timer #1 Controller, offset: 0x8C		
ab_SBUSCFG	0x90	32	System Bus Config, offset: 0x90		
ab_CAPVERSION	0x100	32	Capability Register Length, offset: 0x100		
ab_HCSPARAMS	0x104	32	Host Controller Structural Parameters, offset: 0x104		
ab_HCCPARAMS	0x108	32	Host Controller Capability Parameters, offset: 0x108		
ab_DCIVERSION	0x120	32	Device Controller Interface Version, offset: 0x120		
ab_DCCPARAMS	0x124	32	Device Controller Capability Parameters, offset: 0x124		
ab_USBCMD	0x140	32	USB Command Register, offset: 0x140		
ab_USBSTS	0x144	32	USB Status Register, offset: 0x144		
ab_USBINTR	0x148	32	Interrupt Enable Register, offset: 0x148		
ab_FRINDEX	0x14c	32	USB Frame Index, offset: 0x14C		
ab_DEVICEADDR	0x154	32	Device_FrameList Base Address, offset: 0x154		
ab_ASYNCLISTADDR	0x158	32	Next Asynch_Enpoint List Address, offset: 0x158		
ab_BURSTSIZE	0x160	32	Programmable Burst Size, offset: 0x160		
ab_TXFILLTUNING	0x164	32	TX FIFO Fill Tuning, offset: 0x164		
ab_ENDPTNAK	0x178	32	Endpoint NAK, offset: 0x178		
ab_ENDPTNAKEN	0x17c	32	Endpoint NAK Enable, offset: 0x17C		
ab_PORTSC1	0x184	32	Port Status & Control, offset: 0x184		
ab_OTGSC	0x1a4	32	On-The-Go Status & control, offset: 0x1A4		
ab_USBMODE	0x1a8	32	USB Device Mode, offset: 0x1A8		
ab_ENDPTSETUPSTAT	0x1ac	32	Endpoint Setup Status, offset: 0x1AC		
ab_ENDPTPRIME	0x1b0	32	Endpoint Initialization, offset: 0x1B0		
ab_ENDPTFLUSH	0x1b4	32	Endpoint De-Initialize, offset: 0x1B4		

ab_ENDPTSTAT	0x1b8	32	Endpoint Status, offset: 0x1B8		
ab_ENDPTCOMPLETE	0x1bc	32	Endpoint Complete, offset: 0x1BC		
ab_ENDPTCTRL0	0x1c0	32	Endpoint Control0, offset: 0x1C0		
ab_ENDPTCTRL1	0x1c4	32	Endpoint Control1, offset: 0x1C4		
ab_ENDPTCTRL2	0x1c8	32	Endpoint Control2, offset: 0x1C8		
ab_ENDPTCTRL3	0x1cc	32	Endpoint Control3, offset: 0x1Cc		
ab_ENDPTCTRL4	0x1d0	32	Endpoint Control4, offset: 0x1d0		
ab_ENDPTCTRL5	0x1d4	32	Endpoint Control5, offset: 0x1d4		
ab_CTRL	0x800	32	Non-Core Register: USB Control Register		
ab_PHY	0x818	32	Non-Core Register: USB PHY Control Register		

## 4.0 Peripheral components in the library

Table 4. Publicly available Imperas/OVP peripheral models (158 models)

Peripheral	Peripheral	Peripheral
<a href="http://intel.ovpworld.org/82077AA">intel.ovpworld.org/82077AA</a>	<a href="http://intel.ovpworld.org/82371EB">intel.ovpworld.org/82371EB</a>	<a href="http://intel.ovpworld.org/8253">intel.ovpworld.org/8253</a>
<a href="http://intel.ovpworld.org/8259A">intel.ovpworld.org/8259A</a>	<a href="http://intel.ovpworld.org/NorFlash48F4400">intel.ovpworld.org/NorFlash48F4400</a>	<a href="http://intel.ovpworld.org/PciIDE">intel.ovpworld.org/PciIDE</a>
<a href="http://intel.ovpworld.org/PciPM">intel.ovpworld.org/PciPM</a>	<a href="http://intel.ovpworld.org/PciUSB">intel.ovpworld.org/PciUSB</a>	<a href="http://intel.ovpworld.org/Ps2Control">intel.ovpworld.org/Ps2Control</a>
<a href="http://marvell.ovpworld.org/GT6412x">marvell.ovpworld.org/GT6412x</a>	<a href="http://mips.ovpworld.org/16450C">mips.ovpworld.org/16450C</a>	<a href="http://mips.ovpworld.org/MaltaFPGA">mips.ovpworld.org/MaltaFPGA</a>
<a href="http://mips.ovpworld.org/SmartLoaderLinux">mips.ovpworld.org/SmartLoaderLinux</a>	<a href="http://motorola.ovpworld.org/MC146818">motorola.ovpworld.org/MC146818</a>	<a href="http://national.ovpworld.org/16450">national.ovpworld.org/16450</a>
<a href="http://national.ovpworld.org/16550">national.ovpworld.org/16550</a>	<a href="http://ovpworld.org/Alpha2x16Display">ovpworld.org/Alpha2x16Display</a>	<a href="http://ovpworld.org/dummyPort">ovpworld.org/dummyPort</a>
<a href="http://ovpworld.org/DynamicBridge">ovpworld.org/DynamicBridge</a>	<a href="http://ovpworld.org/FlashDevice">ovpworld.org/FlashDevice</a>	<a href="http://ovpworld.org/ledRegister">ovpworld.org/ledRegister</a>
<a href="http://ovpworld.org/SerInt">ovpworld.org/SerInt</a>	<a href="http://ovpworld.org/SimpleDma">ovpworld.org/SimpleDma</a>	<a href="http://ovpworld.org/VirtioBlkMMIO">ovpworld.org/VirtioBlkMMIO</a>
<a href="http://philips.ovpworld.org/ISP1761">philips.ovpworld.org/ISP1761</a>	<a href="http://renesas.ovpworld.org/adc">renesas.ovpworld.org/adc</a>	<a href="http://renesas.ovpworld.org/bcu">renesas.ovpworld.org/bcu</a>
<a href="http://renesas.ovpworld.org/brg">renesas.ovpworld.org/brg</a>	<a href="http://renesas.ovpworld.org/can">renesas.ovpworld.org/can</a>	<a href="http://renesas.ovpworld.org/can">renesas.ovpworld.org/can</a>
<a href="http://renesas.ovpworld.org/clkgen">renesas.ovpworld.org/clkgen</a>	<a href="http://renesas.ovpworld.org/crc">renesas.ovpworld.org/crc</a>	<a href="http://renesas.ovpworld.org/csib">renesas.ovpworld.org/csib</a>
<a href="http://renesas.ovpworld.org/csie">renesas.ovpworld.org/csie</a>	<a href="http://renesas.ovpworld.org/dma">renesas.ovpworld.org/dma</a>	<a href="http://renesas.ovpworld.org/intc">renesas.ovpworld.org/intc</a>
<a href="http://renesas.ovpworld.org/memc">renesas.ovpworld.org/memc</a>	<a href="http://renesas.ovpworld.org/rng">renesas.ovpworld.org/rng</a>	<a href="http://renesas.ovpworld.org/taa">renesas.ovpworld.org/taa</a>
<a href="http://renesas.ovpworld.org/tms">renesas.ovpworld.org/tms</a>	<a href="http://renesas.ovpworld.org/tmt">renesas.ovpworld.org/tmt</a>	<a href="http://renesas.ovpworld.org/uartc">renesas.ovpworld.org/uartc</a>
<a href="http://renesas.ovpworld.org/UPD70F3441Logic">renesas.ovpworld.org/UPD70F3441Logic</a>	<a href="http://smc.ovpworld.org/LAN9118">smc.ovpworld.org/LAN9118</a>	<a href="http://smc.ovpworld.org/LAN91C111">smc.ovpworld.org/LAN91C111</a>
<a href="http://ti.ovpworld.org/UartInterface">ti.ovpworld.org/UartInterface</a>	<a href="http://xilinx.ovpworld.org/mdm">xilinx.ovpworld.org/mdm</a>	<a href="http://xilinx.ovpworld.org/mpmc">xilinx.ovpworld.org/mpmc</a>
<a href="http://xilinx.ovpworld.org/xps-gpio">xilinx.ovpworld.org/xps-gpio</a>	<a href="http://xilinx.ovpworld.org/xps-iic">xilinx.ovpworld.org/xps-iic</a>	<a href="http://xilinx.ovpworld.org/xps-intc">xilinx.ovpworld.org/xps-intc</a>
<a href="http://xilinx.ovpworld.org/xps-ll-temac">xilinx.ovpworld.org/xps-ll-temac</a>	<a href="http://xilinx.ovpworld.org/xps-mch-emc">xilinx.ovpworld.org/xps-mch-emc</a>	<a href="http://xilinx.ovpworld.org/xps-sysace">xilinx.ovpworld.org/xps-sysace</a>
<a href="http://xilinx.ovpworld.org/xps-timer">xilinx.ovpworld.org/xps-timer</a>	<a href="http://xilinx.ovpworld.org/xps-uartlite">xilinx.ovpworld.org/xps-uartlite</a>	<a href="http://altera.ovpworld.org/dw-apb-timer">altera.ovpworld.org/dw-apb-timer</a>
<a href="http://altera.ovpworld.org/dw-apb-uart">altera.ovpworld.org/dw-apb-uart</a>	<a href="http://altera.ovpworld.org/IntervalTimer32Core">altera.ovpworld.org/IntervalTimer32Core</a>	<a href="http://altera.ovpworld.org/IntervalTimer64Core">altera.ovpworld.org/IntervalTimer64Core</a>
<a href="http://altera.ovpworld.org/JtagUart">altera.ovpworld.org/JtagUart</a>	<a href="http://altera.ovpworld.org/PerformanceCounterCore">altera.ovpworld.org/PerformanceCounterCore</a>	<a href="http://altera.ovpworld.org/RSTMGR">altera.ovpworld.org/RSTMGR</a>
<a href="http://altera.ovpworld.org/SystemIDCore">altera.ovpworld.org/SystemIDCore</a>	<a href="http://altera.ovpworld.org/Uart">altera.ovpworld.org/Uart</a>	<a href="http://amd.ovpworld.org/79C970">amd.ovpworld.org/79C970</a>
<a href="http://arm.ovpworld.org/AaciPL041">arm.ovpworld.org/AaciPL041</a>	<a href="http://arm.ovpworld.org/CompactFlashRegs">arm.ovpworld.org/CompactFlashRegs</a>	<a href="http://arm.ovpworld.org/CoreModule9x6">arm.ovpworld.org/CoreModule9x6</a>
<a href="http://arm.ovpworld.org/DebugLedAndDipSwitch">arm.ovpworld.org/DebugLedAndDipSwitch</a>	<a href="http://arm.ovpworld.org/DMemCtrlPL341">arm.ovpworld.org/DMemCtrlPL341</a>	<a href="http://arm.ovpworld.org/IcpControl">arm.ovpworld.org/IcpControl</a>
<a href="http://arm.ovpworld.org/IcpCounterTimer">arm.ovpworld.org/IcpCounterTimer</a>	<a href="http://arm.ovpworld.org/IntICP">arm.ovpworld.org/IntICP</a>	<a href="http://arm.ovpworld.org/IntICP">arm.ovpworld.org/IntICP</a>
<a href="http://arm.ovpworld.org/KbPL050">arm.ovpworld.org/KbPL050</a>	<a href="http://arm.ovpworld.org/L2CachePL310">arm.ovpworld.org/L2CachePL310</a>	<a href="http://arm.ovpworld.org/LcdPL110">arm.ovpworld.org/LcdPL110</a>
<a href="http://arm.ovpworld.org/MmciPL181">arm.ovpworld.org/MmciPL181</a>	<a href="http://arm.ovpworld.org/RtcPL031">arm.ovpworld.org/RtcPL031</a>	<a href="http://arm.ovpworld.org/SerBusDviRegs">arm.ovpworld.org/SerBusDviRegs</a>
<a href="http://arm.ovpworld.org/SmartLoaderArm64Linux">arm.ovpworld.org/SmartLoaderArm64Linux</a>	<a href="http://arm.ovpworld.org/SmartLoaderArmLinux">arm.ovpworld.org/SmartLoaderArmLinux</a>	<a href="http://arm.ovpworld.org/SMemCtrlPL354">arm.ovpworld.org/SMemCtrlPL354</a>
<a href="http://arm.ovpworld.org/SysCtrlSP810">arm.ovpworld.org/SysCtrlSP810</a>	<a href="http://arm.ovpworld.org/TimerSP804">arm.ovpworld.org/TimerSP804</a>	<a href="http://arm.ovpworld.org/TzpcBP147">arm.ovpworld.org/TzpcBP147</a>
<a href="http://arm.ovpworld.org/UartPL011">arm.ovpworld.org/UartPL011</a>	<a href="http://arm.ovpworld.org/VexpressSysRegs">arm.ovpworld.org/VexpressSysRegs</a>	<a href="http://arm.ovpworld.org/WdtSP805">arm.ovpworld.org/WdtSP805</a>
<a href="http://atmel.ovpworld.org/AdvancedInterruptController">atmel.ovpworld.org/AdvancedInterruptController</a>	<a href="http://atmel.ovpworld.org/ParallelIOController">atmel.ovpworld.org/ParallelIOController</a>	<a href="http://atmel.ovpworld.org/PowerSaving">atmel.ovpworld.org/PowerSaving</a>
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<a href="http://freescale.ovpworld.org/KinetisFTFE">freescale.ovpworld.org/KinetisFTFE</a>	<a href="http://freescale.ovpworld.org/KinetisFTM">freescale.ovpworld.org/KinetisFTM</a>	<a href="http://freescale.ovpworld.org/KinetisGPIO">freescale.ovpworld.org/KinetisGPIO</a>
<a href="http://freescale.ovpworld.org/KinetisI2C">freescale.ovpworld.org/KinetisI2C</a>	<a href="http://freescale.ovpworld.org/KinetisI2S">freescale.ovpworld.org/KinetisI2S</a>	<a href="http://freescale.ovpworld.org/KinetisLLWU">freescale.ovpworld.org/KinetisLLWU</a>
<a href="http://freescale.ovpworld.org/KinetisLPTMR">freescale.ovpworld.org/KinetisLPTMR</a>	<a href="http://freescale.ovpworld.org/KinetisMCG">freescale.ovpworld.org/KinetisMCG</a>	<a href="http://freescale.ovpworld.org/KinetisMPU">freescale.ovpworld.org/KinetisMPU</a>
<a href="http://freescale.ovpworld.org/KinetisNFC">freescale.ovpworld.org/KinetisNFC</a>	<a href="http://freescale.ovpworld.org/KinetisOSC">freescale.ovpworld.org/KinetisOSC</a>	<a href="http://freescale.ovpworld.org/KinetisPDB">freescale.ovpworld.org/KinetisPDB</a>
<a href="http://freescale.ovpworld.org/KinetisPIT">freescale.ovpworld.org/KinetisPIT</a>	<a href="http://freescale.ovpworld.org/KinetisPMC">freescale.ovpworld.org/KinetisPMC</a>	<a href="http://freescale.ovpworld.org/KinetisPORT">freescale.ovpworld.org/KinetisPORT</a>

freescale.ovpworld.org/KinetisRCM	freescale.ovpworld.org/KinetisRFSYS	freescale.ovpworld.org/KinetisRFVBAT
freescale.ovpworld.org/KinetisRNG	freescale.ovpworld.org/KinetisRTC	freescale.ovpworld.org/KinetisSDHC
freescale.ovpworld.org/KinetisSIM	freescale.ovpworld.org/KinetisSMC	freescale.ovpworld.org/KinetisSPI
freescale.ovpworld.org/KinetisTSI	freescale.ovpworld.org/KinetisUART	freescale.ovpworld.org/KinetisUSB
freescale.ovpworld.org/KinetisUSBDCD	freescale.ovpworld.org/KinetisUSBHS	freescale.ovpworld.org/KinetisVREF
freescale.ovpworld.org/KinetisWDOG	freescale.ovpworld.org/Uart	freescale.ovpworld.org/VybridADC
freescale.ovpworld.org/VybridANADIG	freescale.ovpworld.org/VybridCCM	freescale.ovpworld.org/VybridDMA
freescale.ovpworld.org/VybridGPIO	freescale.ovpworld.org/VybridI2C	freescale.ovpworld.org/VybridLCD
freescale.ovpworld.org/VybridQUADSPI	freescale.ovpworld.org/VybridSDHC	freescale.ovpworld.org/VybridSPI
freescale.ovpworld.org/VybridUART	freescale.ovpworld.org/VybridUSB	



## 5.0 General Information on Peripheral Models

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers etc. and configuration options and general information for peripheral modeling with Imperas OVP.

### 5.1 Background

Imperas OVP simulation technology enables very high performance simulation, debug and analysis of platforms containing multiple processors and peripheral models. The technology is designed to be extensible: you can create new models of processors, peripherals and other platform components using interfaces and libraries defined by OVP.

The peripheral models created using the OVP APIs run on the Peripheral Simulation Engine (PSE).

The model is typically written in C and compiled into an executable for the PSE processor architecture. The model is compiled for speed of execution and to protect IP. It is dynamically loaded by the simulator at run time.

## 6.0 Building peripherals easily with Imperas iGen

To aid with model creation, Imperas products include iGen, a model generation tool. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process. iGen creates the needed C files. iGen also creates the C++ SystemC TLM2 interface files needed to run peripheral models in SystemC simulations.

iGen takes as input a simple script specification that includes device internals such as registers and memories, port information, component descriptors, and other elements. iGen then builds the C code model files and user editable templates. These include model frameworks with registers, function calls, memory map, and other items. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.

More information on iGen can be found: [imperas.com/products](http://imperas.com/products).

Please contact Imperas to get access to the Imperas documents: `Imperas_Model_Generator_Guide.pdf` and `Imperas_Peripheral_Generator_Guide.pdf`.

## 7.0 Peripheral model internals

Each instance of a peripheral model runs on its own virtual machine with an address space large enough for the model. This processor (the PSE) and its memory are separate from any processors, memories and buses

in the platform being simulated; they exist only to execute the code of the peripheral model.

Interception of functions defined in the peripheral model allows the use of features of the host system in the implementation of the behavior of a peripheral. As an example, a real platform might contain a video display device. When simulating this system, it is generally more convenient not to simulate the complete video display device but to use a video package available on the host machine, such as SDL, and to use this to render to the host display. Also models of uarts, ethernet devices and USB components can make use of the host PC resources during simulation, to allow, for example, a simulation to browse the real internet, or the simulation to connect to a real USB device.

## **8.0 Parts of peripheral models**

### ***8.1 Configuring the Peripheral Instance with Parameters***

A peripheral can include the behaviour of several configurations. These are controlled when the peripheral is instanced in the platform by setting parameters defined on the peripheral.

### ***8.2 Net Ports***

Peripherals may be connected to other peripherals or processors with signal wires (nets). These can be used to act as interrupt signals or used to control behavior between peripherals.

The wires are created in the platform as nets and this net is connected into the peripheral using a net port.

### ***8.3 Bus master ports***

A bus master port initiates (and controls the address of) a bus cycle. Bus cycles are generated by behavioral code within the peripheral model.

### ***8.4 Bus slave ports***

A peripheral can be defined as having several bus slave ports. The bus slave ports can be split into several address blocks. Each address block be either local memory or memory mapped registers. Both of these can have associated callback functions. A memory mapped register can also be defined as specific read/write access, whether it is volatile, and also whether it is associated with a reset pin and mask. A memory mapped register can also have specific bit fields defined.

### ***8.5 Packetnets***

A peripheral can be defined as being connected to packetnet ports. A packetnet is used to model packet based communication such as Ethernet, CAN bus or GSM. A packetnet is created in a platform, then connected to packetnet ports on model instances. A packetnet can have many connections, each able to send or receive packets. A packetnet is used as an efficient method of communication within OVP models.

For more information on modeling with packetnets, please see the peripheral modeling documentation: [OVP\\_Peripheral\\_Modeling\\_Guide.pdf](#), [OVPsim\\_and\\_CpuManager\\_User\\_Guide.pdf](#) and the example: [\\$IMPERAS\\_HOME/Examples/Models/Peripherals/packetnet](#).

## **9.0 More information (documentation) on peripheral models and modeling**

More information on modeling and APIs can be found at: [OVPworld.org/technology\\_apis](http://OVPworld.org/technology_apis).

Specifics on modeling peripherals can be found: [OVP\\_Peripheral\\_Modeling\\_Guide.pdf](#).

A full list of the currently available OVP documentation is available: [OVPworld.org/documentation](http://OVPworld.org/documentation).

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