I3C 总线协议详细解析（第一章）

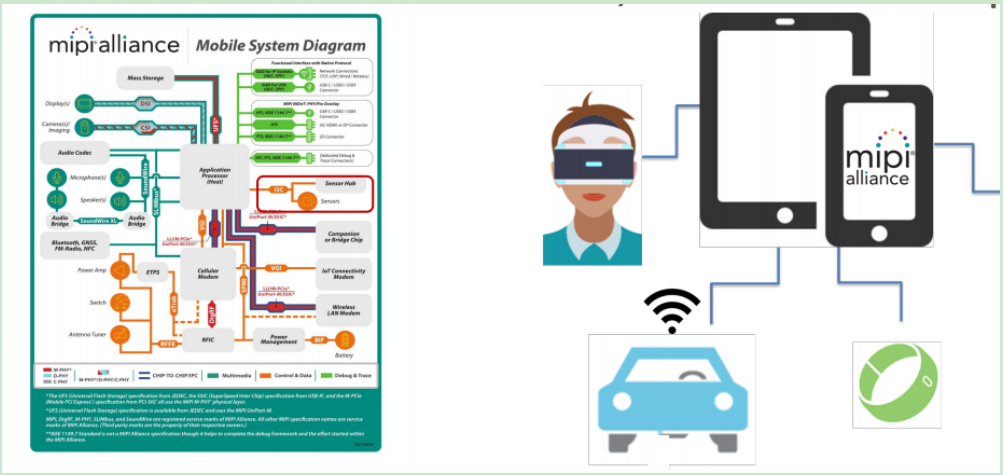
目前随着手机等移动设备包含的sensor越来越多，传统应用在sensor上的I2C/SPI接口的局限性也越来越明显，典型的缺陷如下：

1、sensor等设备的增加，对控制总线的速度和功耗提出了更加严苛的要求；

2、虽然I2C是一种2线接口，但是往往此类device需要额外增加一条中断INT信号线；

处于解决上述问题的原因，推出了I3C的接口总线和协议，下面一起来看下I3C总线的特性。

一、I3C的应用场景



从上图中我们可以看到：

1、I3C总线可以应用在各种sensor中；

2、可以使用在任何传统的I2C/SPI/UART等接口的设备中。

二、什么是I3C

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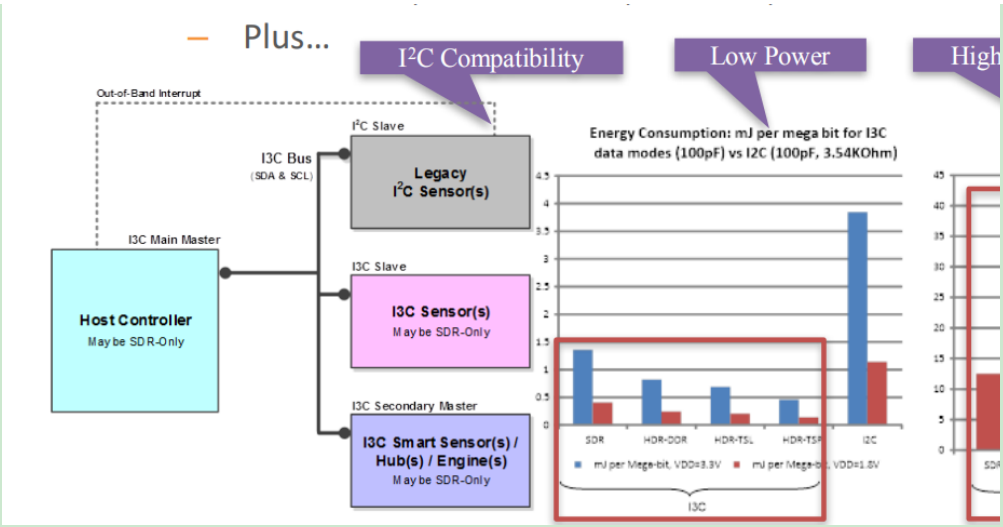


I3C吸纳了I2C和SPI的关键特性，并将其统一起来，同时在I2C的基础上，保留了2线的串行接口结构，这样工程师就可以在单个设备中连接大量的传感器。

从上图中我们可以将特性具体一下：

1、I3C总线可以支持multi-master即多主设备

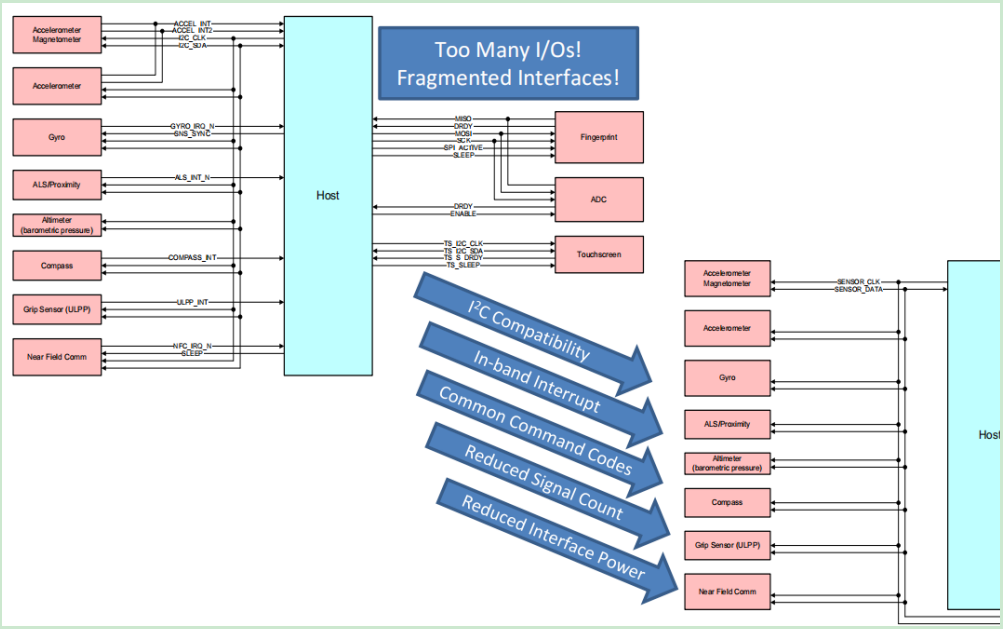
2、I3C总线与传统的I2C设备仍然是兼容的

3、可以支持软中断

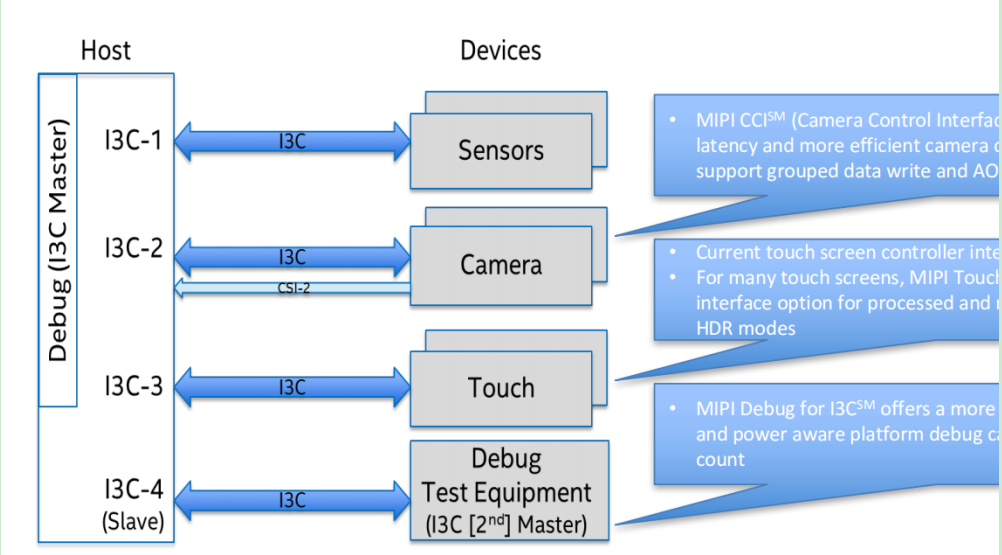
4、相比较于I2C总线的功耗更低

5、速度更快，可以支持到12.5MHZ

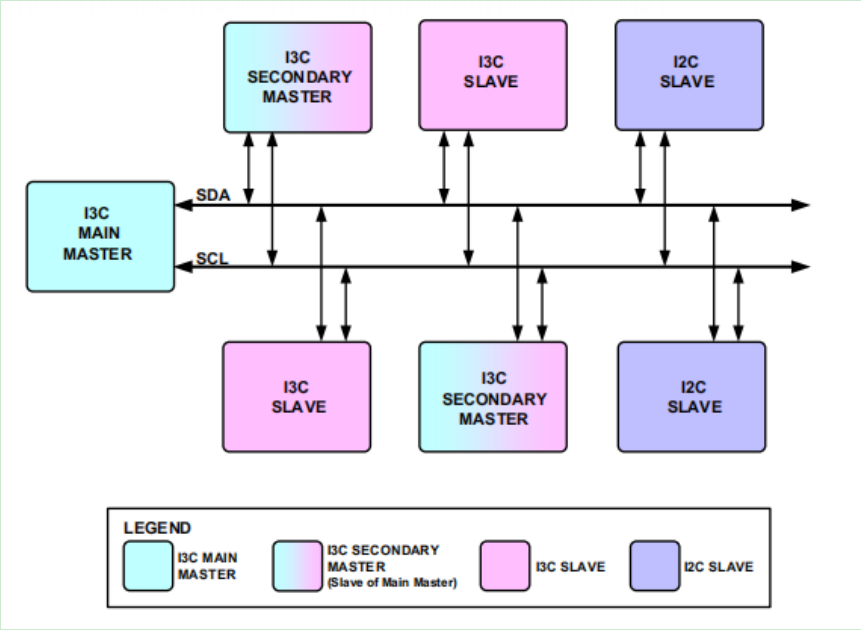
从下图中可以看到在传统的I2C接口设备中包含了太多的I/0口了(碎片式的接口），将之（I2C/SPI)替换成I3C之后可以节省很大部分的信号线（省去了中断信号的一根线EINT，若取代SPI，可以省的更多）的开销，在布局布线时也更方便.



按照目前MIPI联盟的规划，I3C总线在将来除了应用sensor之外，还有如下的应用领域：camera、TP等



三、I3C接口协议



从上图就可以很清楚的看到I3C总线的应用了，I3C总线中支持多主设备，同时兼容I2C。

其中支持设备的具体类型有：

1、I3C主设备

-----SDR-only master

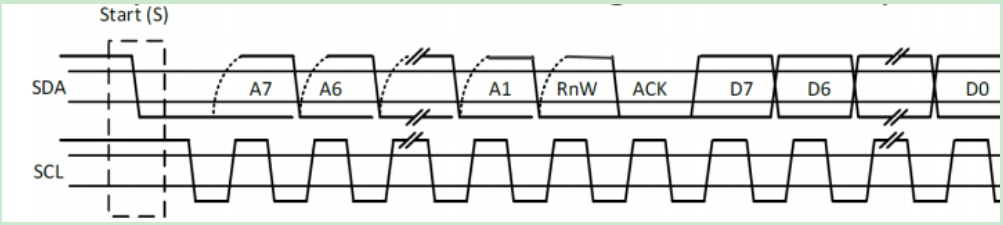
2、I3C secondary MASTER

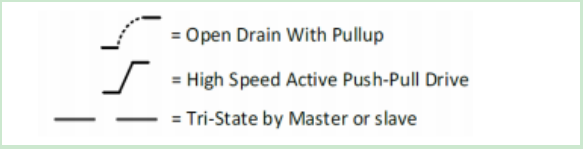
-----SDR-only secondary master（注意是slave of main master,即相比较主设备而言仍然时从设备）

3、I3C 从设备

-----SDR only slave

4、I2C slave





上图为I3C的串行clk和data传输的波形，注意下方的标注：SDA的接口为开漏结构，而SCL的接口为推挽结构！

四、I3C特性详细介绍

1、SDR动态地址分配

---I3C可以为所有的I3C从设备动态的分配7-bit address（注：在I3C从设备中会有两个standardized characteristics register和内部的48-bit的临时ID去协助此过程，具体咋协助俺还不知道）

---仍然支持I2C的静态地址

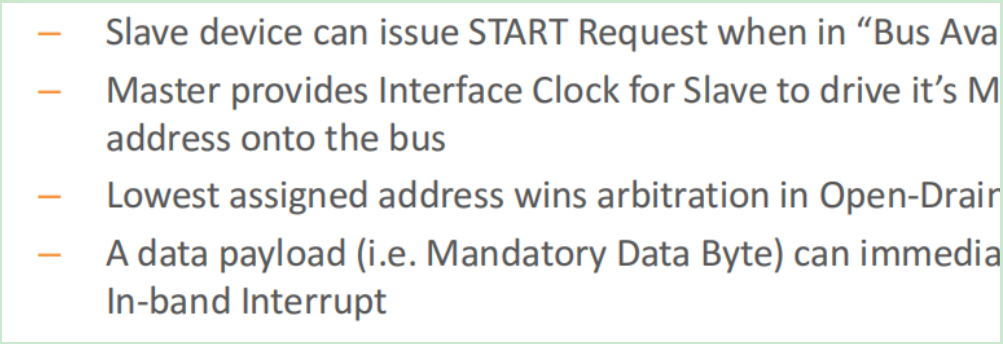
2、SDR的带内中断

---在“bus available(总线空闲）”的状态下，从设备可以发出“START"请求信号；

---当主设备接收到请求信号后，主设备发出时钟信号并将分配的地址驱动到总线上，然后从设备响应地址（为防止理解问题，英文描述如下）

---如果此时有多个从设备响应中断，那么分配的地址中最低的一个设备将会赢得仲裁

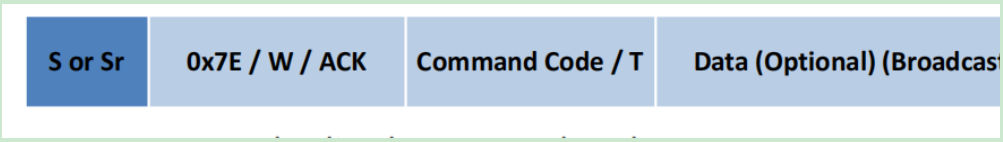
---数据载荷（即强制数据位）可以和带内中断一起使用（？？？未明白，后面填坑）



3、error detection and recovery methodology（错误检测和恢复方法）

---主要针对master 和slave产生的错误（9种错误类型：奇偶性、循环冗余校验CRC5）

4、common command codes(公共命令码）



- Standardized Command Codes
  - Event Enable/Disable
  - Activity States
  - Payload Mgmt
  - I3C Feature Mgmt (Dynamic Address Assignment, M
    Timing Control)
  - Test Modes
  - Extensible Space (MIPI and Vendor)

5、对I2C总线的支持

---支持I2C的fast mode/fast mode+（note:fast speed 1Mbit/s,high speed 3.4Mbit/s)

---对于the velocity of i3c clk 12.5MHZ需要50ns的spike filters(tsp)尖峰滤波器

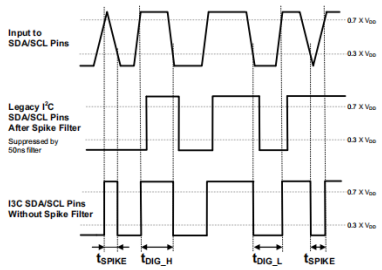
---I3C不支持clock stretching（时钟拉伸，不了解的童鞋可以查查I2C的协议）

---不使用open-drai驱动器

---不支持10-bit的I2C扩展地址

Guidelines - Legacy I²C Device Suppo

- Fm and Fm+ Speeds Supported
- 50ns Spike Filter (t_{SP}) Needed for 12.5MHz I3C^{SM}



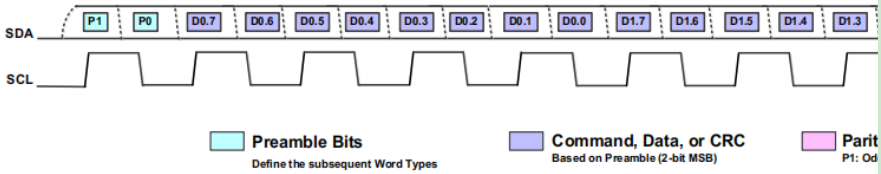
t_{SP}: pulse width of spikes that must be suppressed by the input filter

*UM10204: I2C

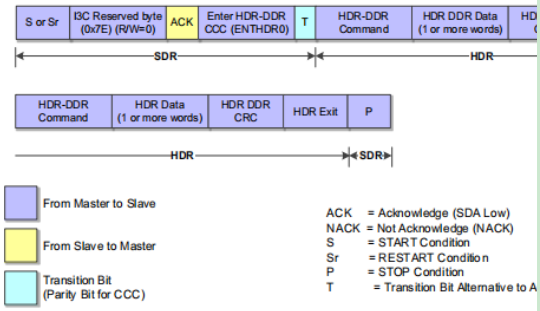
- Clock Stretching is Not Allowed – I3C SCL is Push/
- 20mA Open Drain Drivers (I_{OL}) are Not Used
- I²C Extended Addresses (10 bit) are Not Used

6、I3C的HDR-DDR 模式

- **HDR-DDR: Double Data Rate**
  - Uses SCL as a clock, however Data and Commands change SD
    contrast, SDR Mode changes SDA only when SCL is Low
  - HDR-DDR moves data by Words, which generally contains 2 p
    bytes and 2 parity bits. 4 Word Types defined: Command, Dat



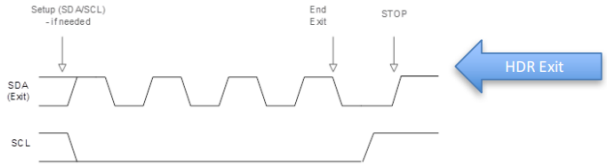
  - Simple protocol:



- Enter HDR Commands Supported

I3C			Msg1			Msg2	
START	Brdcst CCC	EnterHDRx	HDR Cmd	HDR Data	HDR Restart Pattern	HDR Cmd	HDR Data

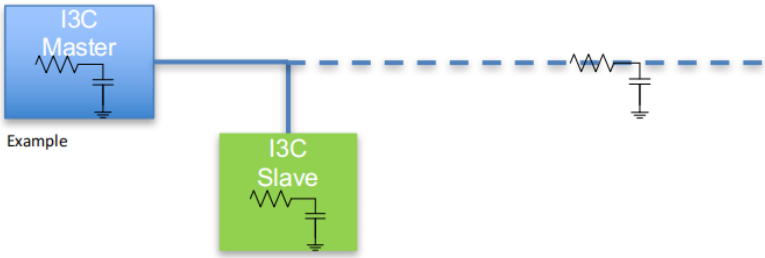
- HDR Exit Pattern detected by all I3C Devices



- Non-HDR Devices shall ignore I3C HDR bus traffic Pattern is detected

7、I3C的拓扑

Guidelines - Varied Topologies



- Impacts on signal transition/transit times (max
  - SDA/SCL drive strength: “weaker” for lower power and interf over larger topologies/loads
  - Trace length and material: short vs long and pcb vs cable
  - SCL/SDA pad capacitance
  - Clock to Data Turnaround Time (t_{SCO})
- Legacy I^2C Devices impact maximum bus frequ
  - Must run I3C at speeds/pulses beyond Spike Filter or slow Bu
- Impacts on signal integrity/reliability
  - Device Location: close and far Devices can cause interferenc

Summarized Good Design Practices

- Thoroughly understand capability of coexistent
  - 50ns Spike Filter
  - Disabled Clock Stretch
- Understand bus topology and performance trac and Legacy I^2C Devices) vs Pure Bus (I3C Device
  - Trace length and material
  - SDA/SCL pad capacitance
  - Clock to Data Turnaround Time (t_{SCO})
  - Device location

附：相关知识点

1、clk stretching(时钟拉伸，翻译怪怪的）

照例附上I2C协议中关于I2C stretching的介绍，其主要的作用就是在I2C总线进行通信是，其速度是由主设备决定的，与RS232不同，I2C总线会根据预先设定好的波特率在主设备和从设备之间提供一个严格精确的时钟信号，然而在某些时候，I2C的从设备并没有准备好进行通信（翻译很简略，详细见下文），需要慢一点儿，那么实现这一功能的机制就是clock stretching，当slave需要进行clock stetcing的时候，就需要将clk信号拉低以减小总线的速度，同时，作为master而言，需要等待clk被拉高才能继续传输(主设备需要不断的回读）；

In an I2C communication, the master device determines the clock speed. U
bus provides an explicit clock signal which relieves master and slave from
exactly to a predefined baud rate.

However, there are situations where an I2C slave is not able to co-operate
given by the master and needs to slow down a little. This is done by a mech
clock stretching.

An I2C slave is allowed to hold down the clock if it needs to reduce the bus
on the other hand, is required to read back the clock signal after releasing i
and wait until the line has actually gone high.

Bandwith

Clock stretching sounds a bit odd but is common practice. However, the tota
shared bus might be significantly decreased. So, especially for I2C buses sha
devices, it is important to estimate the impacts of clock stretching. So do not
I2C device dominate your bus performance.

Clock Stretching in High Speed Mode

Clock stretching in High-Speed-Mode is only allowed after the ACK bit (and b
the next byte). Stretching between bits 2-9 is illegal because the edges of the
boosted with an additional current source. See I2C specification Rev. 03 chap
further details.

分类: 嵌入式系统架构

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