程式碼:

library ieee;

use ieee.std\_logic\_1164.all;

entity lab5 is

PORT (w,reset,clock :in std\_logic;

s: out std\_logic\_vector(2 downto 0));

end lab5;

ARCHITECTURE Behavior OF lab5 IS

TYPE State\_type IS (Start, S1, S2a,S2b,S3,S4) ;

SIGNAL y\_present, y\_next : State\_type ;

SIGNAL temp :std\_logic\_vector(2 downto 0);

BEGIN

PROCESS

BEGIN

wait until clock'event and clock='1';

CASE y\_present IS

WHEN Start=>

IF w = '0' THEN

y\_present <= Start;

temp<="000";

ELSE

y\_present <= S1 ;

temp<="001";

END IF;

IF reset = '1' THEN

y\_present <= Start;

temp<="000";

END IF ;

WHEN S1 =>

IF w = '0' THEN

y\_present <= S2a;

temp<="010";

ELSE

y\_present <= S2b ;

temp<="011";

END IF ;

WHEN S2a=>

IF w = '0' THEN

y\_present <= S3;

temp<="100";

ELSE

y\_present <= S3 ;

temp<="100";

END IF ;

WHEN S2b =>

IF w = '0' THEN

y\_present <= S3;

temp<="100";

ELSE

y\_present <= S3 ;

temp<="100";

END IF ;

WHEN S3=>

IF w = '0' THEN

y\_present <= S1;

temp<="001";

ELSE

y\_present <= S4 ;

temp<="101";

END IF ;

WHEN S4=>

IF w = '0' THEN

y\_present <= S4;

temp<="101";

ELSE

y\_present <= S4 ;

temp<="101";

END IF ;

END CASE ;

end process;

s<=temp;

end Behavior;

心得:

經過這次的實驗，讓我更加了解怎麼運用Type以及Case還有狀態機以及vhdl語法，在寫程式的過程中我們卡了很久，原本以為是process跟Case的問題，但最後發現是因為沒有把下一個狀態給現在的狀態，導致我們只有輸出S1，但reset不知道為甚麼一直沒辦法動，修正後，發現clock要按兩次才會有反應，後來發現可能是wait until clock'event and clock='1';擺錯位置或是原本加入的if clock=’1’的問題，再刪除if clock=’1’的敘述以及移動wait until clock'event and clock='1'後就順利的解決了