

# VE527 Computer-Aided Design of Integrated Circuits

## Written Assignment One

Out: Sep. 20, 2019; Due: Oct. 9, 2019; 6 Questions

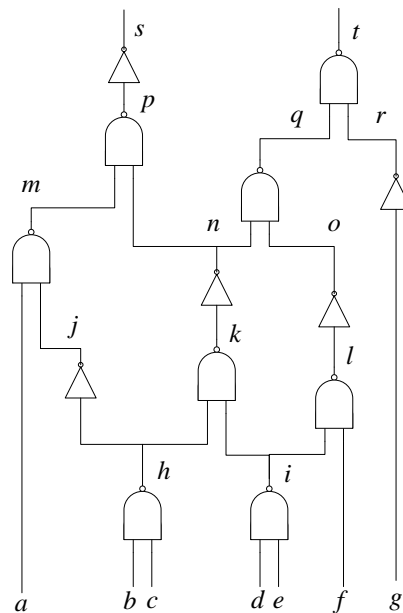
### 1. (6%) Technology Mapping: Basics

Which of the following statements are correct about technology mapping?

- a) An asymmetric target gate will have more than one possible way for matching.
- b) After technology mapping, the netlist is expressed in a set of pre-designed gates from a technology library, and it is technology dependent.
- c) The tree-covering algorithm can be modified to minimize the total number of gates used from the technology library.
- d) Any basic logic gate can be represented as a tree of NAND2 and NOT gates.

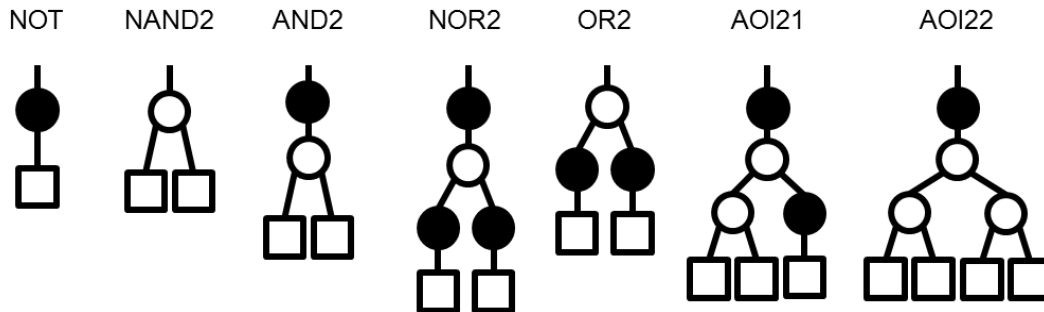
### 2. (20%) Treeifying the Network

Consider the following network of NAND2 and NOT gates, which is an uncommitted logic we need to map. As we explained in the lecture, our mapping algorithm requires us to start with trees, not DAGs. Please draw the set of trees you obtain by applying the treeifying method we discussed in lecture.



### 3. (36%) Technology Mapping

Consider the technology library shown below, which consists of 7 gates. We use the same notation as was used in lecture when drawing these gates: black circle represents a NOT gate, white circle represents a NAND gate, and square represents an input.

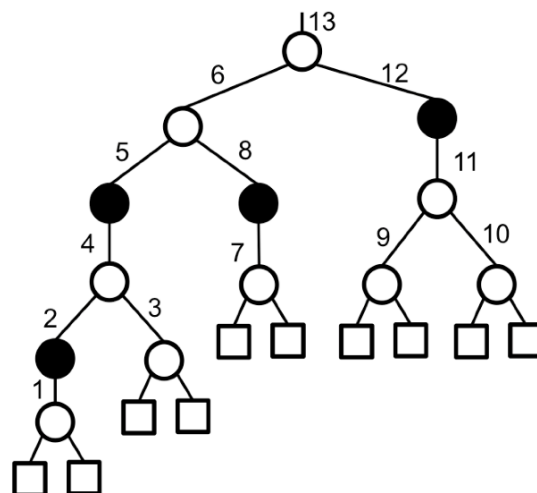


Suppose that the costs of the gates are:

$\text{cost}(\text{NOT}) = 2$ ;  $\text{cost}(\text{NAND2}) = 3$ ;  $\text{cost}(\text{AND2}) = 4$ ;  $\text{cost}(\text{NOR2}) = 6$ ;  $\text{cost}(\text{OR2}) = 5$ ;  
 $\text{cost}(\text{AOI21}) = 7$ ;  $\text{cost}(\text{AOI22}) = 7$ .

Run the tree covering algorithm discussed in lecture by hand to find the mincost cover for the tree below. We label the internal wires with numbers, so you can refer to the node by the number on the wire above it. Note that you should show the final mincost cover, not just the minimum cost value.

**Hint:** in the tree covering algorithm, you should first find what library patterns match each node. Then, you should apply the recursive mincost tree covering algorithm to find the mincost cover. As you may notice, the mincost tree covering algorithm is a nice dynamic programming algorithm. Thus, if you like, you can run it in a bottom-up way.



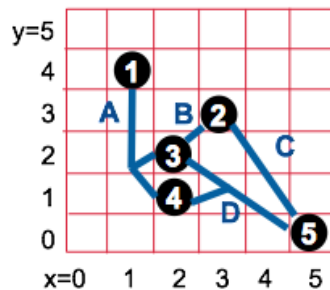
#### 4. (6%) Placement: Basics

Which of the following statements are correct about placement?

- a) The goal of ASIC placement is to arrange the standard cells in an input netlist to minimize the estimated wirelength, to ensure the next tool in the layout flow — the router — can complete all the wire connections.
- b) Placement methods use detailed routing methods in their inner loops, to precisely determine the path of each needed wire for each proposed placement.
- c) The goal of ASIC placement is to arrange the standard cells in an input netlist to maximize the estimated wirelength.
- d) Standard cells in an ASIC technology library are placed in rows.

#### 5. (20%) Half-Perimeter Wirelength (HPWL) Calculation

Consider the following simple placement of 5 gates in a small 6x6 grid.



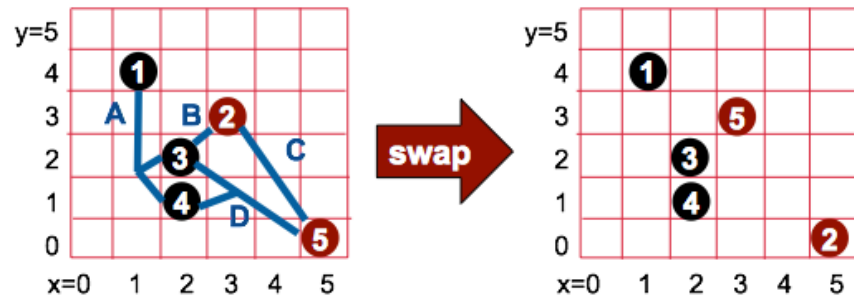
Each gate is drawn as a circle with number (1–5). Assume the gate is located at the center of the grid cell, and its (X, Y) coordinates are taken from the column (X) and row (Y) coordinates in the figure. There are 4 nets, labeled A, B, C and D, connected as follows:

- Net A: gates 1, 3, 4
- Net B: gates 2, 3
- Net C: gates 2, 5
- Net D: gates 3, 4, 5

(a) (8%) What is the total half-perimeter wirelength (HPWL) for this placement, calculated across these 4 nets?

(b) (8%) Suppose we now swap the locations of gates 2 and 5, as shown below. Which nets could have their HPWLs changed? What is  $\Delta L = (\text{new HPWL after swap}) - (\text{old HPWL before swap})$ ?

(c) (4%) Suppose the current temperature is 10. Then, what is the probability of accepting the above swap?



## 6. (12%) Placement by Simulated Annealing

Consider the following detailed pseudo-code description of an annealing-based placer, like the method we described in class. The lines are numbered for clarity in the questions. Assume that there are  $G$  total gates and  $N$  total nets.  $L$  is the evolving total HPWL wirelength.

```
0. for(L=0, i=0; i<N; i++)
1.   L = L + HPWL( net[i] );
2. T = 1000.0;
3. TCount = 0;
4. OldHpwl = 0;
5. frozen = false;
6. while ( ! frozen ) {
7.   for (s=1; s<=500*G; s++) {
8.     Swap 2 random gates G[i] and G[j]
9.      $\Delta L$  = [total HPWL after swap] - [total HPWL before swap]
10.    if (  $\Delta L < 0$  ) {
11.      accept this swap
12.      L = L +  $\Delta L$ ;
13.    }
14.    else if( uniform_random() < exp( - $\Delta L/T$  ) ) {
15.      accept this swap
16.      L = L +  $\Delta L$ ;
17.    }
18.    else undo this swap
19.  } // for
20.  TCount = TCount + 1;
21.  if ( TCount >= 20 ) {
22.    LChange = 100* abs( OldHpwl - L)/L ;
23.    if ( LChange < 0.1 )
24.      frozen = true;
25.  }
26.  OldHpwl = L;
27.  T = 0.85 * T // cool the temperature; do more gate swaps
28. } // while
29. return (final placement as best solution)
```

Which of the following statements are correct?

- a) The annealer will attempt 500 swaps at each temperature.
- b) Lines 10-13 implement the Metropolis criterion for probabilistic acceptance.

- c) The second temperature in the annealing run will be 850.
- d) The annealer terminates the placement when (i) at least 20 temperatures have been tried, and (ii) the total HPWL length  $L$  has not changed by more than 0.1% between the last temperature and the current temperature.
- e) Line 12 updates the total HPWL after an accepted downhill swap.