SYNOPSYS®

DesignWare Interface and Standards IP

Quick Reference Guide

AMBA, Cores, PHYs, and ARC Processors

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Preface

Related Documentation

Synopsys Tools

- coreConsultant User Guide, Synopsys, Inc. (included with the coreConsultant tool)
  https://www.synopsys.com/dw/doc.php/doc/coretools/latest/coreconsultant_user.pdf

Web Resources

- DesignWare IP product information: http://www.designware.com
- Your custom DesignWare IP page: http://www.mydesignware.com
- Documentation through SolvNet: https://solvnet.synopsys.com (Synopsys password required)
- Synopsys Common Licensing (SCL): http://www.synopsys.com/keys

1 Digital IP Overview

Synopsys DesignWare IP, the world's most widely-used, silicon-proven IP provides designers with a broad portfolio of synthesizable implementation IP, hardened PHYs for ASIC, SoC and FPGA designs. The DesignWare family includes the following products:

- "DesignWare Library" on page 7 - contains the principal ingredients for design and synthesis including high speed datapath components, AMBA On-Chip Bus, memory portfolio, foundry libraries, and popular Star IP cores.
- "DesignWare Cores (Digital and Mixed-Signal)" on page 12 - silicon-proven, digital and mixed-signal standards-based connectivity IP such as PCI Express, PCI-X, PCI, USB 2.0 On-the-Go (OTG), USB 2.0 PHY, USB 1.1 and Ethernet.
- "Microcontrollers" on page 14 - Microprocessor and microcontrollers.
- "ARC Processor Family" on page 14 - high-performance processors for imbedded processing applications.

1.1 DesignWare Library

The DesignWare Library provides designers with a comprehensive collection of synthesizable IP and foundry libraries. The library contains the following principal ingredients for ASIC, SoC, and FPGA design:

- Building Block IP (Datapath, Data Integrity, DSP, Test, and more)
- DesignWare minPower Component (components and datapath optimization for low power)
- AMBA Bus Fabric and Peripherals
- Memory portfolio (memory controller, memory BIST, memory models and more)
- Microcontrollers (8051 and 6811)

A single license gives you access to all the IP in the library. For more information on the DesignWare Library, refer to the following:

http://www.synopsys.com/IP

For a detailed search of the available IP, refer to the following:

http://www.designware.com

1.1.1 Building Block IP

The DesignWare Building Block IP is a collection of over 200 technology-independent, high-quality, high-performance IP. Most of these IP elements include multiple implementations to provide a variety of performance and area trade-off options.

Component groups for the Building Block IP are identified in the following table. For more detail, refer to the *DesignWare Building Blocks Quick Reference Guide*.

Component Group	Description	Component Type
Datapath	Arithmetic, floating point, trigonometric, and sequential math IP	Synthesizable RTL
Data Integrity	Data integrity IP such as CRC, ECC, 8b10b...	Synthesizable RTL
Digital Signal Processing (DSP)	FIR and IIR filters	Synthesizable RTL
Application Specific	Debugger IP	Synthesizable RTL
Logic	Combinational, sequential, and control IP	Synthesizable RTL
Interface	Clock Domain Crossing (CDC)	Synthesizable RTL
Memory	Registers, FIFO, synchronous and asynchronous RAM, and stack IP	Synthesizable RTL
Test	JTAG IP such as boundary scan, TAP controller	Synthesizable RTL
GTECH	Technology-independent IP library to aid users in developing technology-independent parts	Synthesizable RTL

For information on low power versions of these components, and low power synthesis of datapath intensive designs, see "DesignWare minPower Components" on page 9.

1.1.2 DesignWare minPower Components

The DesignWare minPower Components offer power-optimized datapath architectures that enable DC Ultra™ to automatically generate circuits that suppress switching activity and glitches, reducing both dynamic and leakage power for mobile devices and high-performance applications. Based on the actual switching activities, transition probabilities, available standard cells and analysis of possible configurations, the DesignWare minPower Components architectures are automatically configured by DC Ultra to implement the optimal structure with the lowest power consumption. In addition to the automatically inferable components, DesignWare minPower Components also include more than 40 instantiable blocks that incorporate low power design techniques such as enhanced clock gating, built-in datapath gating and patented data-tracking pipeline management technology to reduce power consumption.

- Innovative low power datapath architectures with lower switching and glitches
- Configured automatically by DC Ultra for most fitted implementation based on power costing and switch activities or transition probabilities
- Smart architecture generation for lower leakage cell mapping
- Integrated datapath gating within datapath blocks eliminates the timing overhead resulted from inserted isolation gates
- Instantiated IP with enhanced clock gating and built-in isolation logic for better dynamic power
- New data tracking IP reduce dynamic power consumption for pipelined architectures
- Extend battery life for mobile applications by lowering the power consumption for circuits with extensive active times
- Reduce power consumption for high-performance computing circuits

Component groups for DesignWare minPower Components are identified in the following table.

Component Group	Description	Component Type
Low Power	New components, and enhanced DWBB components that incorporate power-saving features, such as clock gating, pipelining, and operand isolation. NOTE: A special implementation and license (“lpwr” / DesignWare-LP) is required to enable these new low power components and DWBB low power enhancements.	Synthesizable RTL
Datapath	Arithmetic, floating point, trigonometric, and sequential math IP	Synthesizable RTL
Data Integrity	Data integrity IP such as CRC, ECC, 8b10b...	Synthesizable RTL
Interface	Clock Domain Crossing (CDC)	Synthesizable RTL

To enable the use of DesignWare minPower Components and enhanced low power optimizations during synthesis within DC-Ultra, a minPower (DesignWare-LP) license is required.

The latest documentation is available on the Synopsys website at the following location:

http://www.synopsys.com/dw/ipdir.php?ds=dw_minpower

1.1.3 DesignWare AMBA Family of Components

AMBA is a standard bus architecture system developed by ARM for rapid development of processor-driven systems. The AMBA standard also allows a number of bus peripherals and resources to be connected in a consistent way. The following is a complete listing of the Synopsys DesignWare IP for the AMBA protocol.

Component Name	DesignWare AMBA Synthesizable IP
DW_ahb	AHB bus, arbitration, decode, and control logic (page 18)
DW_ahb_dmac	AHB Central Direct Memory Access (DMA) Controller (page 20)
DW_ahb_h2h	AHB to AHB Bridge (page 23)
DW_ahb_eh2h	Enhanced AHB to AHB Bridge (page 21)
DW_ahb_icm	AHB Multi-layer Interconnection Matrix (page 25)
DW_ahb_ictl	AHB Interrupt Controller (page 26)
DW_apb	APB bus, decode, and bridge (page 27)
DW_apb_gpio	APB General Purpose I/O (GPIO) (page 28)
DW_apb_i2c	APB I^2C Interface (page 29)
DW_apb_i2s	APB I^2S Interface (page 30)
DW_apb_ictl	APB Interrupt Controller (page 31)
DW_apb_rap	APB Remap & Pause (page 32)
DW_apb_rtc	APB Real Time Clock (page 33)
DW_apb_ssi	APB Synchronous Serial Interface (page 34)
DW_apb_timers	APB Timer (page 36)
DW_apb_uart	APB UART (page 37)
DW_apb_wdt	APB Watch Dog Timer (page 39)
DW_axi	Multiple Address, Multiple Data AXI Interconnect (page 40)
DW_axi_dmac	Transfer Data from Source to Destination over AMBA AXI Bus (page 42)
DW_axi_gm	Generic Interface (GIF) to AMBA AXI Module (page 44)
DW_axi_gs	AMBA AXI Slave to Generic Interface (page 45)
DW_axi_hmx	Connects AMBA AXI Slave to AHB Master (page 46)
DW_axi_rs	AMBA AXI Register Slice (page 47)
DW_axi_x2h	AXI to AHB Bridge (page 48)
DW_axi_x2p	AXI to APB Bridge (page 49)
DW_axi_x2x	AXI to AXI Bridge (page 51)

Component Name	DesignWare AMBA Synthesizable IP
DW_axi_a2x	AXI Master to AXI Slave Bridge (page 53)

1.1.4 Memory IP

Component Name	Component Description	Component Type
Memory IP	DesignWare contains thousands of pre-verified memory models, with over 10,000 devices from more than 25 vendors. (page 181)	Verification Models
DW_memctl	DesignWare Memory Controller (page 182)	Synthesizable RTL
DW Memory Building Block IP	DesignWare Building Block IP contains many memory-related IP. For details, see the *DesignWare Building Blocks Quick Reference Guide*	Synthesizable RTL
DDR/DDR2/DDR3 Cores		
dwc_ddr2_3l_mddr_phy	"DDR2/3-Lite/mDDR PHY" on page 80	Hard IP
dwc_ddr2_ddr_phy	"DDR2/DDR PHY" on page 82	Hard IP
dwc_ddr3_ddr2_phy	"DDR3/2 PHY" on page 84	Hard IP
ddr_multi_phy	"DDR multiPHY" on page 86	Hard IP
dwc_ddr_upctl, dwc_ddr_umctl, and dwc_ddr_umctl2	"Universal DDR Protocol and Memory Controllers" on page 88	Synthesizable RTL
Mobile Storage Core		
dwc_mobile_storage	Secure Digital (SD), Multimedia Card (MMC) and CE-ATA (page 78)	Synthesizable RTL

To view the complete DesignWare memory portfolio, refer to the following:

http://www.synopsys.com/IP/InterfaceIP/DDRn

1.1.5 Verification

For information on verifying digital cores and IP, visit the Verification web page at:

http://www.synopsys.com/Tools/Verification

1.2 DesignWare Cores (Digital and Mixed-Signal)

The DesignWare Cores shown in the following table provide system designers with silicon-proven, digital and analog connectivity IP. DesignWare Cores are licensed individually, on a fee-per-project business model.

Component Name	Component Description	Component Type
Ethernet Cores		
dwc_ether_mac10_100_universal	Ethernet MAC 10/100 Universal (page 58)	Synthesizable RTL
dwc_ether_mac10_100_1000_universal	Ethernet MAC 10/100/1G Universal (page 60)	Synthesizable RTL
dwc_ether_xgmac	XGMAC 10G Ethernet MAC Core (page 62)	Synthesizable RTL
dwc_ether_pcs	Ethernet PCS core (page 67)	Synthesizable RTL
dwc_ether_qos	Ethernet Quality-of-Service Core (page 73)	Synthesizable RTL
DDR/DDR2/DDR3 Cores		
dwc_ddr2_3l_mddr_phy	"DDR2/3-Lite/mDDR PHY" on page 80	Hard IP
dwc_ddr2_ddr_phy	"DDR2/DDR PHY" on page 82	Hard IP
dwc_ddr3_ddr2_phy	"DDR3/2 PHY" on page 84	Hard IP
ddr_multi_phy	"DDR multiPHY" on page 86	Hard IP
dwc_ddr_upctl, dwc_ddr_umctl, and dwc_ddr_umctl2	"dwc_ddr_upctl, dwc_ddr_umctl, and dwc_ddr_umctl2" on page 88	Synthesizable RTL
Mobile Storage Core		
dwc_mobile_storage	Secure Digital (SD), Multimedia Card (MMC) and CE-ATA (page 78)	Synthesizable RTL
IEEE 1394 Cores		
dwc_1394_av_link	IEEE 1394 AVLink (page 92)	Synthesizable RTL
dwc_1394_cphy-native	IEEE 1394 Cable PHY (page 94)	Synthesizable RTL
PCI Cores		
dwc_pci	32/64 bit, 33/66-MHz PCI Core (page 95)	Synthesizable RTL
dwc_pci-x	32/64 bit, 133-MHz PCI-X Core (page 96)	Synthesizable RTL
PCI Express Cores		
dwc_pci_express_ep	PCI Express Endpoint Core (page 100)	Synthesizable RTL
dwc_pci_express_rc	PCI Express Root Port Core (page 101)	Synthesizable RTL
dwc_pci_express_sw	PCI Express Switch Port Core (page 102)	Synthesizable RTL
dwc_pci_express_dm	PCI Express Dual Mode Core (page 103)	Synthesizable RTL

dwcore_pcie_phy	PCI Express PHY Core (page 104)	Hard IP
SATA Cores		
DWC_ahsata	SATA Host (page 105)	Synthesizable RTL
DWC_dsata	SATA Host (page 106)	Synthesizable RTL
dwc_sata_phy	SATA PHY (page 108)	Hard IP
USB Cores		
dwc_usb_1_1_device	USB 1.1. Device Controller (page 109)	Synthesizable RTL
dwc_usb_1_1_ohci_host	USB 1.1 OHCI Host Controller (page 110)	Synthesizable RTL
dwc_usb_1_1_hub-native	USB 1.1. Hub Controller (page 111)	Synthesizable RTL
dwc_usb_2_0_host_subsystem-pci-ahb	USB 2.0 Host Controller - UHOST2 (page 113)	Synthesizable RTL
dwc_usb_2_0_hs_otg_subsystem-ahb	USB 2.0 Hi-Speed On-the-Go Controller Subsystem (page 115)	Synthesizable RTL
dwc_usb_2_0_device	USB 2.0 Device Controller (page 118)	Synthesizable RTL
dwc_usb2_phy	USB 2.0 PHY (page 120)	Hard IP
dwc_usb2_hsotg_phy	USB 2.0 Hi-Speed On-the-Go PHY (page 122)	Hard IP
dwc_wiusb_device_controller	Wireless USB Device Controller (page 120)	Synthesizable RTL
dwc_usb2_nanophy	USB 2.0 nanoPHY (page 128)	Hard IP
dwc_usb_3_0_device	SuperSpeed USB 3.0 Device Controller (page 122)	Synthesizable RTL
dwc_usb_3_0_host	SuperSpeed USB 3.0 Host Controller (page 131)	Synthesizable RTL
dwc_usb_3_0_drd	SuperSpeed USB 3.0 Dual Role Device Controller (page 122)	Synthesizable RTL
dwc_usb_3_0_hub	SuperSpeed USB 3.0 Hub Controller (page 137)	Synthesizable RTL
dwc_usb3.0_femtophy	USB 3.0 femtoPHY IP (page 139)	Hard IP
JPEG Core		
dwc_jpeg	JPEG CODEC (page 140)	Synthesizable RTL
HDMI		
DWC_hdmi_rx	“HDMI Receiver Controllers” (page 142)	Synthesizable RTL
DWC_hdmi_tx	“HDMI Transmitter Controller” (page 144)	Synthesizable RTL
MIPI		
dwc_mipi_dsi_host	“MIPI DSI Host Controller” (page 157)	Synthesizable RTL
dwc_mipi_dphy_bd2	“MIPI DPHY Bidirectional 2 Lanes” (page 161)	Synthesizable RTL

dwc_mipi_dphy_bd4	"MIPI DPHY Bidirectional 4 Lanes" (page 163)	Synthesizable RTL
dwc_mipi_dphy_rx2	"MIPI DPHY RX 2 Data Lanes" (page 165)	Synthesizable RTL
dwc_mipi_dphy_rx4	"MIPI DPHY RX 4 Data Lanes" (page 166)	Synthesizable RTL
dwc_mphy_type1_1tx_1rx	"MIPI MPHY TYPE1 1Tx1RX" (page 167)	Synthesizable RTL
dwc_mipi_mphy_type1_2tx_2rx	"MIPI MPHY TYPE1 2Tx2RX" (page 169)	Synthesizable RTL
dwc_mipi_digrf	"MIPI DigRF 2.5G-3G Physical Layer" (page 171)	Synthesizable RTL
dwc_mipi_csi2_host	MIPI CSI-2 Host Controller (page 173)	Synthesizable RTL
dwc_3g_digrf_slave_controller	MIPI 3G DigRF Slave Controller (page 175)	Synthesizable RTL
dwc_3g_digrf_master_controller	"MIPI DigRF 3G Master Controller" (page 177)	Synthesizable RTL
dwc_ufshc	"DesignWare UFS Host Controller" (page 159)	Synthesizable RTL
dwc_mipi_unipro	"MIPI UniPro" (page 179)	Synthesizable RTL
XAUI		
dwc_xaui_phy	XAUI PHY (page 75)	Hard IP

Also visit the DesignWare Cores web page at:

http://www.synopsys.com/IP/InterfaceIP

1.3 Microcontrollers

Component Name	Component Description	Component Type
DW_6811	8-Bit Microcontroller (page 188)	Synthesizable RTL
DW8051	8-Bit Microcontroller (page 190)	Synthesizable RTL

For more information on microcontroller IP, refer to the following:

http://www.synopsys.com/dw/ipdir.php?ds=dw_microcontrollers

1.4 ARC Processor Family

Processor Group	Description
ARC HS Family	"ARC HS Family" on page 195
ARC EM Family	"ARC EM Family" on page 196
ARC AS200 Audio Family	"ARC AS200 Audio Family" on page 197
ARC 600 Family	"ARC 600 Family" on page 198
ARC 700 Family	"ARC 700 Family" on page 199

For more information on microcontroller IP, refer to the following:

http://www.synopsys.com/dw/ipdir.php?ds=dw_microcontrollers

2 AMBA Bus Fabric and Peripheral IP

AMBA is a standard bus architecture developed by ARM for rapid development of processor-driven systems. AMBA allows a number of bus peripherals and resources to be connected in a consistent way. The following Synopsys DesignWare AMBA 2.0 and 3.0-compliant components are described in this section:

Component Name	DesignWare AMBA Synthesizable IP
DW_ahb	AHB bus, arbitration, decode, and control logic (page 18)
DW_ahb_dmac	AHB Central Direct Memory Access (DMA) Controller (page 20)
DW_ahb_eh2h	Enhanced AHB to AHB Bridge (page 21)
DW_ahb_h2h	AHB to AHB Bridge (page 23)
DW_ahb_icm	AHB Multi-layer Interconnection Matrix (page 25)
DW_ahb_ictl	AHB Interrupt Controller (page 26)
DW_apb	APB bus, decode, and bridge (page 27)
DW_apb_gpio	APB General Purpose I/O (GPIO) (page 28)
DW_apb_i2c	APB I^2C Interface (page 29)
DW_apb_i2s	APB I^2S Interface (page 30)
DW_apb_ictl	APB Interrupt Controller (page 31)
DW_apb_rap	APB Remap & Pause (page 32)
DW_apb_rtc	APB Real Time Clock (page 33)
DW_apb_ssi	APB Synchronous Serial Interface (page 34)
DW_apb_timers	APB Timer (page 36)
DW_apb_uart	APB UART (page 37)
DW_apb_wdt	APB Watch Dog Timer (page 39)
DW_axi	Multiple Address, Multiple Data AXI Interconnect (page 40)
DW_axi_dmac	Transfer Data from Source to Destination over AMBA AXI Bus (page 42)
DW_axi_gm	Generic Interface (GIF) to AMBA AXI Module (page 44)
DW_axi_gs	AMBA AXI Slave to Generic Interface (page 45)
DW_axi_hmx	AMBA AXI Slave to AHB Master Interface (page 46)
DW_axi_rs	AMBA AXI Register Slice (page 47)
DW_axi_x2h	AXI to AHB Bridge (page 48)
DW_axi_x2p	AXI to APB Bridge (page 49)
DW_axi_x2x	AXI Master to AXI Slave Bridge (page 51)

Component Name	DesignWare AMBA Synthesizable IP
DW_axi_a2x	AXI Master to AXI Slave Bridge (page 53)

A brief introduction to DesignWare AMBA components is available at the following location:

http://www.synopsys.com/IP/DesignWare/AMBA

2.1 Source Licenses Available

You can configure any of the DesignWare AMBA synthesizable components and write out encrypted RTL using only a DesignWare license. If you want to write unencrypted RTL source code, you must purchase a special source license. For more information about licenses, please refer to the *DesignWare AMBA Synthesizable Components Installation Guide*:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/dw_amba_install.pdf

2.2 AMBA Components

The following pages provide general descriptions of the AMBA components.

AMBA Compliant

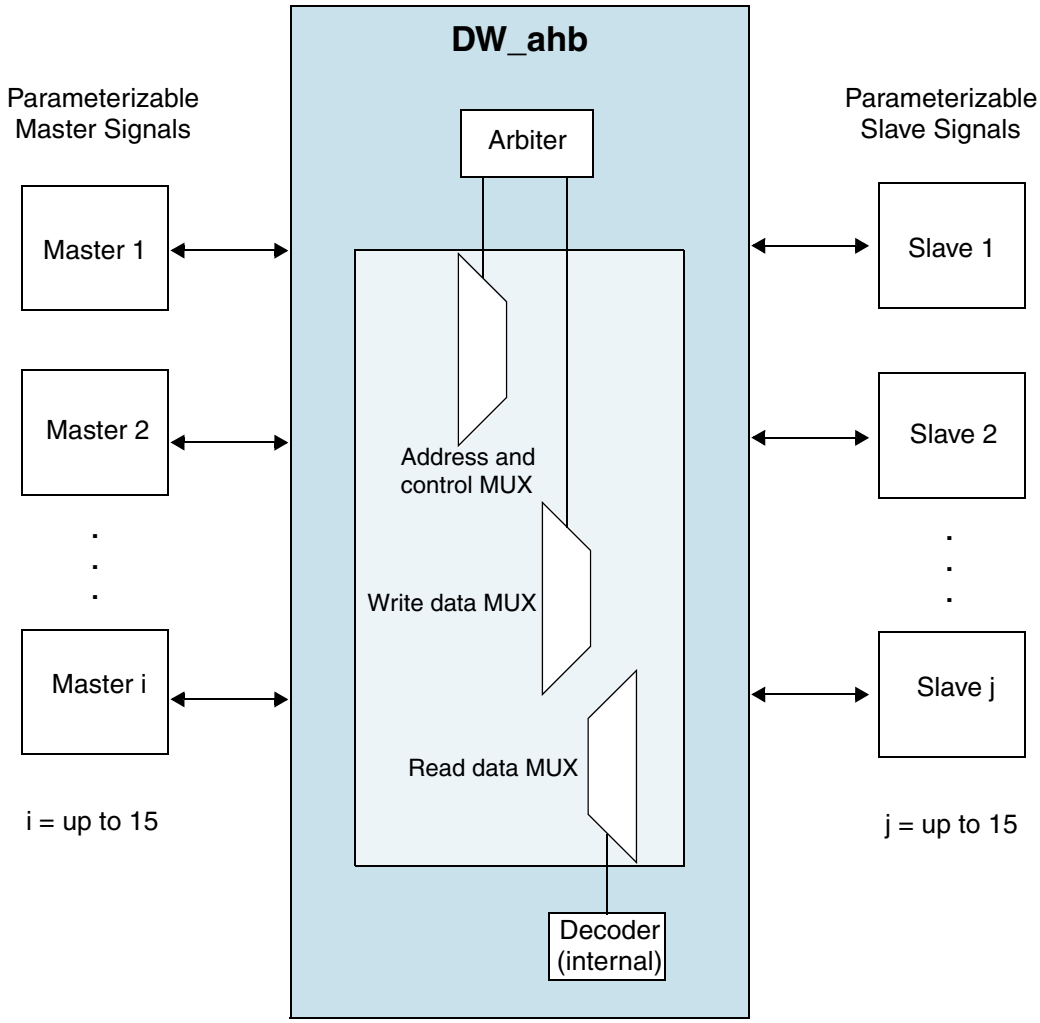
DW_ahb
Advanced High-Performance Bus

- Configuration of AMBA Lite system
- Configuration of up to 15 masters in a non-AMBA Lite system
- Configuration of up to 15 slaves
- Configuration of data bus width of up to 256 bits
- System address width of 32 or 64 bits
- Configuration of system endianness — big or little endian; can be controlled by external input or set during configuration of component
- Optional arbiter slave interface
- Optional internal decoder
- Programmable arbitration scheme:
- Weighted token
- Programmable or fixed priority
- Fair-Among-Equals
- Arbitration for up to 15 masters
- Individual grant signals for each master
- Support for split, burst, and locked transfers
- Optional support for early burst termination
- Configurable support for termination of undefined length bursts by masters of equal or higher priority
- Configurable or programmable priority assignments to masters
- Disabling of masters and protection against self disable
- Optional support for AMBA memory remap feature
- Optional support for pausing of the system, immediately or when bus is IDLE
- Contiguous and non-contiguous memory allocation options for slaves
- External debug mode signals, giving visibility

Also, see the block diagram on the following page.

This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler



The *DesignWare DW_ahb Databook* is available at:

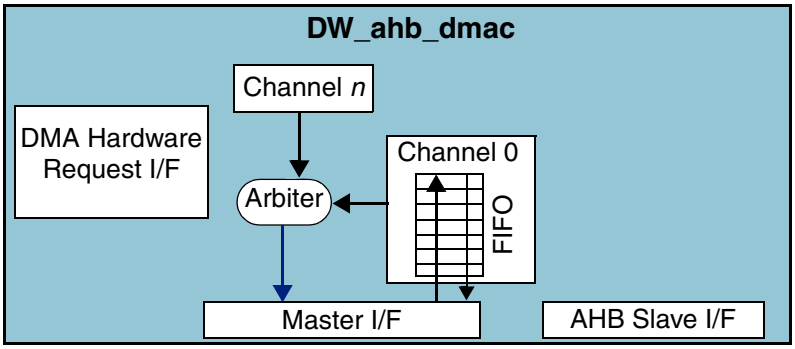
http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_ahb_dmac

AHB Central Direct Memory Access (DMA) Controller

- AHB slave interface – used to program the DW_ahb_dmac
- AHB master interface(s)
  - Up to four independent AHB master interfaces that allows:
    - Up to four simultaneous DMA transfers
    - Masters that can be on different AMBA layers (multi-layer support)
    - Source and destination that can be on different AMBA layers (pseudo flyby performance)
  - Configurable data bus width (up to 256 bits) for each AHB master interface
  - Configurable endianness for master interfaces
- Configurable identification register
- Encoded parameters
- Channels
  - Up to eight channels, one per source and destination pair
  - Unidirectional channels – data transfers in one direction only
  - Programmable channel priority
- Transfers
  - Support for memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral DMA transfers
  - DW_ahb_dmac to or from APB peripherals through the APB bridge
- Component parameters for configurable software driver support
- coreAssembler ready



The *DesignWare DW_ahb_dmac Databook* is available at:

http://www.synopsys.com/products/designware/docs

DW_ahb_eh2h

Enhanced AHB to AHB Bridge

Clocks

- Asynchronous or synchronous clocks, any clock ratio
- Fully registered outputs
- Optional pipeline stages to reduce logic levels on bus inputs

AHB Slave interface

- Data width: 32,64,128, or 256 bits
- Address width: 32 or 64 bits
- Big or little endian
- Zero or two wait states OKAY response
- ERROR response
- No RETRY response
- SPLIT response
- HSPLIT generation
- Handling of multiple, outstanding split transactions
- Multiple HSELs
- HREADY low (alternative to SPLIT response) operation mode

Software interface

- Interrupt signal on write errors
- Interrupt status/clear registers

Sideband signals

- Input sstall pin to qualify an address phase for HREADY low operation mode
- Output sflush pin to monitor the flushing operation on the read buffer

AHB Master interface

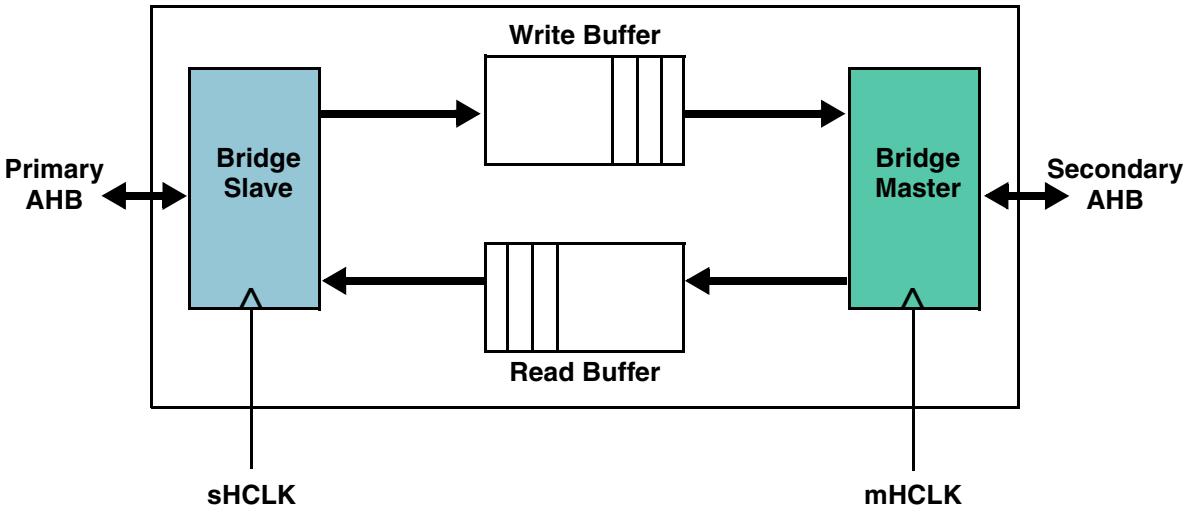
- Data width: 32,64,128, or 256 bits
- Address width: 32 or 64 bits
- Big or little endian
- Lock and bus request generation
- SINGLE, INCR burst type generation for writes
- Any burst type generation for reads
- Downsizing of wider transfers

Write operations

- Configurable depth write buffer
- Buffered writes (always, HPROT is don't care)
- SPLIT response on write buffer full
- Maximum of two wait states on non-sequential access
- Zero wait states (full bandwidth) on sequential access
- Zero BUSY cycles (full bandwidth), secondary burst generation

Read operations

- Configurable depth read buffer
- Pre-fetched reads
- Non-prefetched reads
- SPLIT response on non-sequential (non yet prefetched) access
- Zero wait states (full bandwidth) on prefetched read data



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

The *DesignWare DW_ahb_eh2h Databook* is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

AMBA Compliant

DW_ahb_h2h
AHB to AHB Bridge

System Level

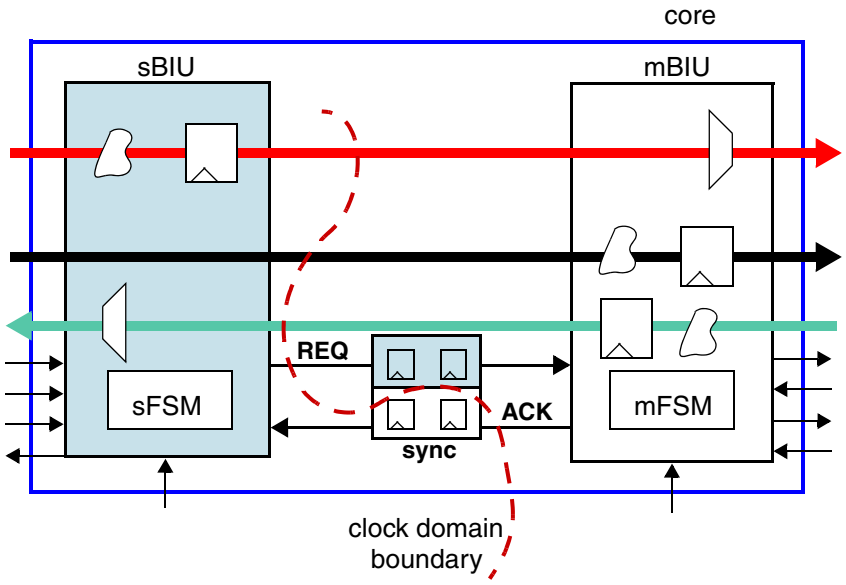
- Configurable asynchronous or synchronous clocks – any clock ratio
- Four clocking modes for synchronous clock configurations – two with and two without clock enables
- Low-gate count implementation (minimum configuration below 2K gates)
- Sub-optimal throughput performance (non-buffered architecture)
- High clock-speed operations (fully registered outputs, operating frequency more than 300 MHz)

AHB Master Interface

- Configurable AHB address width (32 or 64 bits)
- Configurable AHB data width (32, 64, 128, or 256 bits)
- Configurable endianness
- HLOCK generation
- HBUSREQ generation
- HTRANS: generation of IDLE or NSEQ bus cycles
- Non-pipelined transfers: address phase always followed by IDLE cycles until data phase completes
- HBURST: fixed to SINGLE
- All other AHB control signals forwarded unchanged
- AHB Lite configuration to remove redundant logic
- Deadlock detection

AHB Slave Interface

- Deadlock protection: SPLIT response generation after deadlock detection at the master interface
- Bus held off (HREADY low) until the secondary transfer data phase completes and is acknowledged back from the master interface
- SPLIT response (from secondary) forwarded back to primary as RETRY
- Component ID code retrievable from read data bus
- Support for locked transfers (any HTRANS) through HMASTLOCK
- IDLE and BUSY non-locked cycles ignored



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

The *DesignWare DW_ahb_h2h Databook* is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

DW_ahb_icm

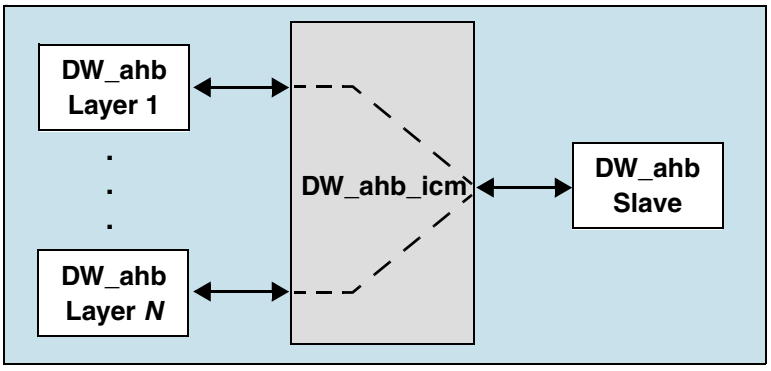
AHB Multi-layer Interconnection Matrix

Features

- Layer arbitration and master multiplexing
- Input stage address and control holding registers for each layer
- Mapping of slave response onto correct layer
- Returning of splits onto the correct layer
- Common clock and reset shared amongst all layers
- coreAssembler ready.

User-defined parameters

- AMBA Lite
- AHB address bus width, (same width on all layers)
- AHB data bus width, (same width on each layer)
- AHB master layers, (up to 4)
- Split or non-split capable slave
- Slave with/without multiple select lines
- Slave with/without protection control
- Slave with/without burst control
- Slave with/without lock control
- Layer release scheme
- Baseline arbitration scheme
- External arbitration priority control



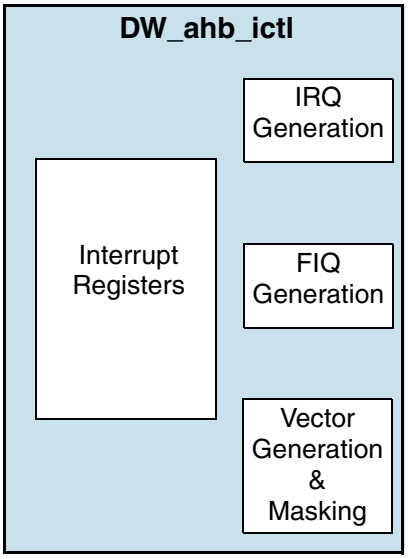
The *DesignWare DW_ahb_icm Databook* is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

AMBA Compliant

DW_ahb_ictl
AHB Interrupt Controller

- 2 to 64 IRQ normal interrupt sources
- 1 to 8 FIQ fast interrupt sources (optional)
- Vectored interrupts (optional)
- Software interrupts
- Configuration ID registers
- Priority filtering (optional)
- Masking
- Scan mode (optional)
- Programmable interrupt priorities (after configuration)
- Encoded parameters
- Note: Does not support split transfers



This component is coreAssembler ready. For more information about coreAssembler:

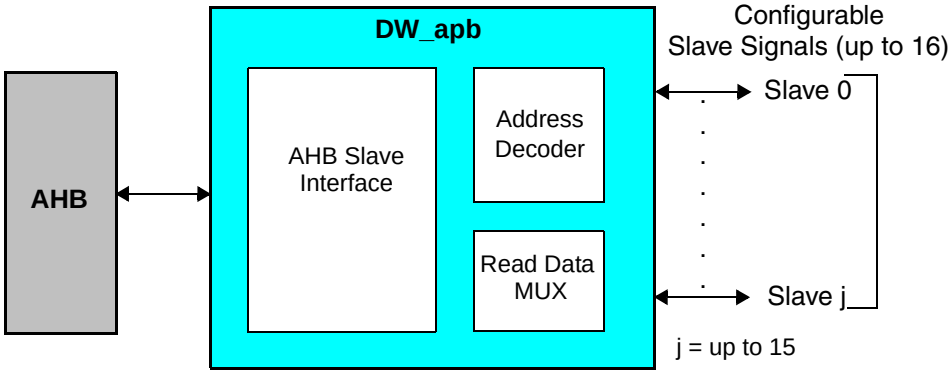
http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

The *DesignWare DW_ahb_ictl Databook* is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

DW_apb
Advanced Peripheral Bus

- APB Bridge and APB bus functionality incorporated
- AHB slave
- Supports up to 16 APB slaves
- Supports big- and little-endian AHB systems
- Supports little-endian APB slaves
- Supports 32, 64, 128, 256 AHB data buses
- Supports 8, 16, and 32-bit APB data buses
- Supports single and burst AHB transfers
- Supports synchronous hclk/pclk; hclk is an integer multiple of pclk
- The AHB slave side does not support SPLIT, RETRY or ERROR responses



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

The *DesignWare DW_apb Databook* is available at:

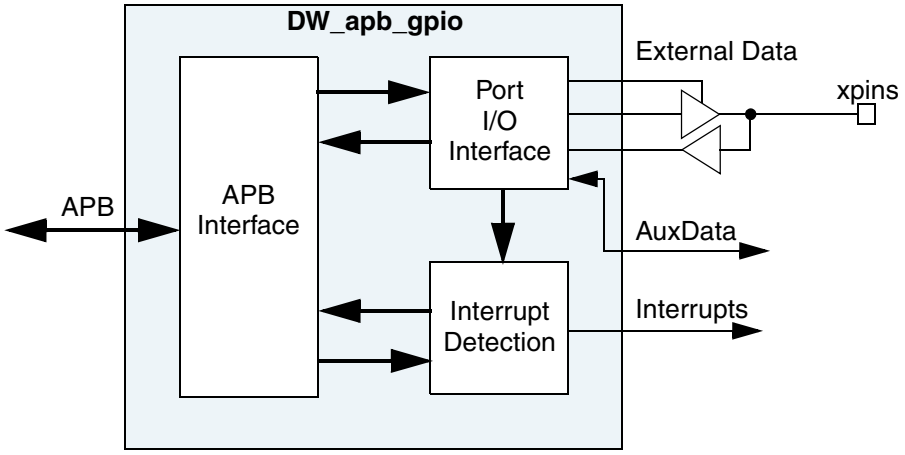
https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

AMBA Compliant

DW_apb_gpio

APB General Purpose Programmable I/O

- Up to 128 independently configurable pins (If more than 128 pins are required, another DW_apb_gpio should be instantiated.)
- Up to four ports, A to D, which are separately configurable
- Separate data registers and data direction registers for each port
- Configurable hardware and software control for each port, or for each bit of each port.
- Separate auxiliary data input, data output, and data control for each I/O in Hardware Control mode
- Independently controllable port bits
- Configurable interrupt mode for Port A
- Configurable debounce logic with an external slow clock to debounce interrupts
- Option to generate single or multiple interrupts
- GPIO Component Type register
- GPIO Component Version register
- Configurable reset values on output ports



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

The *DesignWare DW_apb_gpio Databook* is available at:

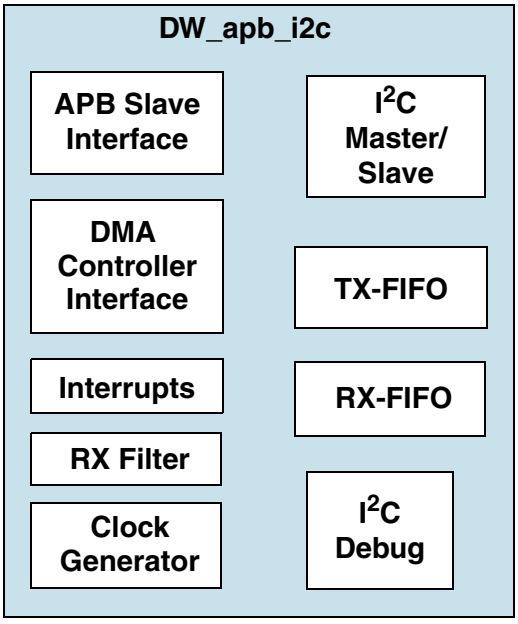
https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

AMBA Compliant

DW_apb_i2c

APB I2C Interface

- Two-wire I2C serial interface
- Three speeds:
  - Standard mode (100 Kbps)
  - Fast mode (400 Kbps)
  - High-speed mode (3.4 Mbps)
- Supports clock synchronization
- Master or slave I2C operation
- Supports multi-Master operation (bus arbitration)
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- Slave bulk transfer mode
- Component parameters for configurable software driver support
- Ignores CBUS addresses (an older ancestor of I2C that used to share the I2C bus)
- Transmit and receive buffers
- Interrupt or polled mode operation
- Handles Bit and Byte waiting at all bus speeds
- Simple software interface consistent with DesignWare APB peripherals
- Digital filter for the received SDA and SCL lines
- Support for APB data bus widths of 8, 16, and 32 bits
- DMA handshaking interface compatible with the DW_ahb_dmac handshaking interface



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

The *DesignWare DW_apb_i2c Databook* is available at:

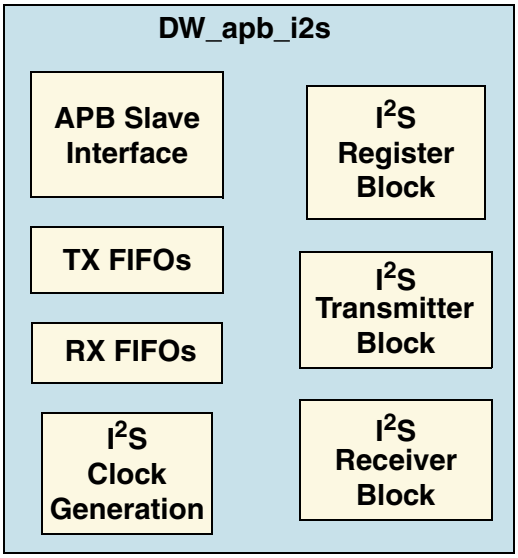
https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

AMBA Compliant

DW_apb_i2s

APB I2S Bus

- APB data bus widths of 8, 16, and 32 bits
- I2S transmitter and/or receiver based on the Philips I2S serial protocol
- Configurable number of stereo channels (up to 4) for both transmitter and receiver
- Full duplex communication due to the independence of transmitter and receiver
- Asynchronous clocking of APB bus and I2S sclk
- Master or slave mode of operation
- Audio data resolutions of 12, 16, 20, 24, and 32 bits
- External sclk gating and enable signals
- Configurable FIFO depth of 2, 4, 8, 16 bits
- Configurable support for programmable DMA registers
- Programmable FIFO thresholds
- Component parameters for configurable software driver support



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

The *DesignWare DW_apb_i2s Databook* is available at:

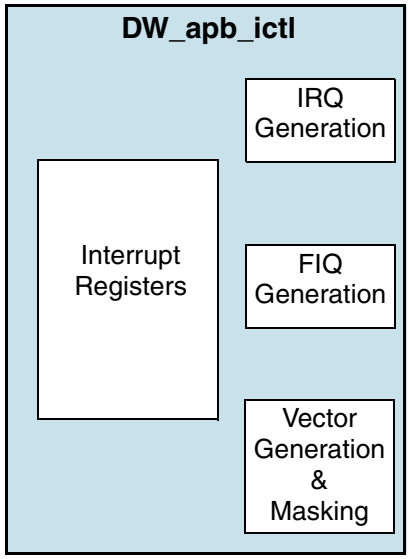
https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

DW_apb_ictl

APB Interrupt Controller

- 2 to 64 IRQ normal interrupt sources
- 1 to 8 FIQ fast interrupt sources (optional)
- Vectored interrupts (optional)
- Software interrupts
- Priority filtering (optional)
- Masking
- Scan mode (optional)
- Programmable interrupt priorities (after configuration)

NOTE: DW_apb_ictl is an exact replacement for the original component DW_amba_ictl (name change only).



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

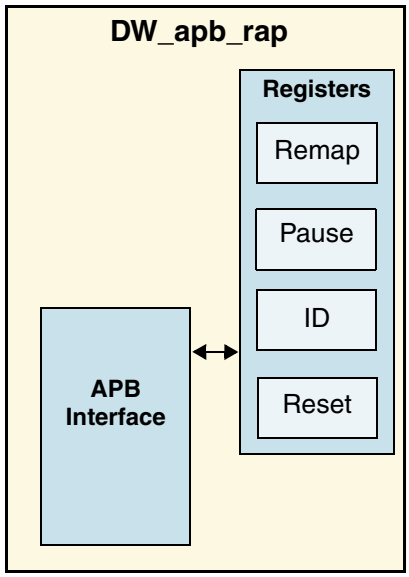
The *DesignWare DW_apb_ictl Databook* is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

AMBA Compliant

DW_apb_rap
APB Remap and Pause

- Configuration of APB data bus width 8, 16, or 32
- Remap Control: Used to switch the DW_ahb address decoder from boot mode to normal mode operation.
- Pause Mode: Used to put the DW_ahb's arbiter into low-power (pause) mode.
- In pause mode the dummy master is granted the AHB bus until an interrupt occurs.
- Reset Status Register: Keeps track of status from up to eight separate system reset signals.
- Identification Code Register: Implements a configurable, read-only ID register



This component is coreAssembler ready. For more information about coreAssembler:

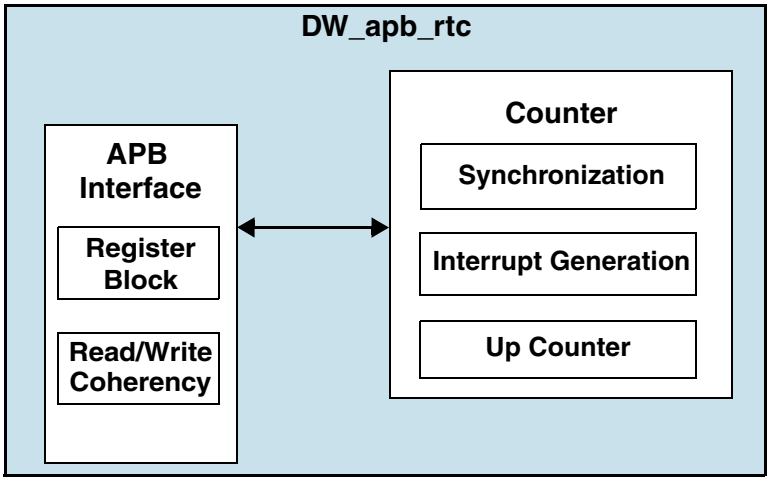
http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

The *DesignWare DW_apb_rap Databook* is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

DW_apb_rtc
APB Real Time Clock

- APB slave interface with read/write coherency for registers
- Incrementing counter and comparator for interrupt generation
- Free-running pclk
- User-defined parameters:
  - APB data bus width
  - Counter width
  - Clock relationship between bus clock and counter clock
  - Interrupt polarity level
  - Interrupt clock domain location
  - Counter enable mode
- Counter wrap mode
- Some uses of the DW_apb_rtc are:
  - Real-time clock – used with software for keeping track of time
  - Long-term, exact chronometer – When clocked with a 1 Hz clock, it can keep track of time from now up to 136 years in the future
  - Alarm function – generates an interrupt after a programmed number of cycles
  - Long-time, base counter – clocked with a very slow clock signal



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

The *DesignWare DW_apb_rtc Databook* is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

AMBA Compliant

DW_apb_ssi

APB Synchronous Serial Interface

Features

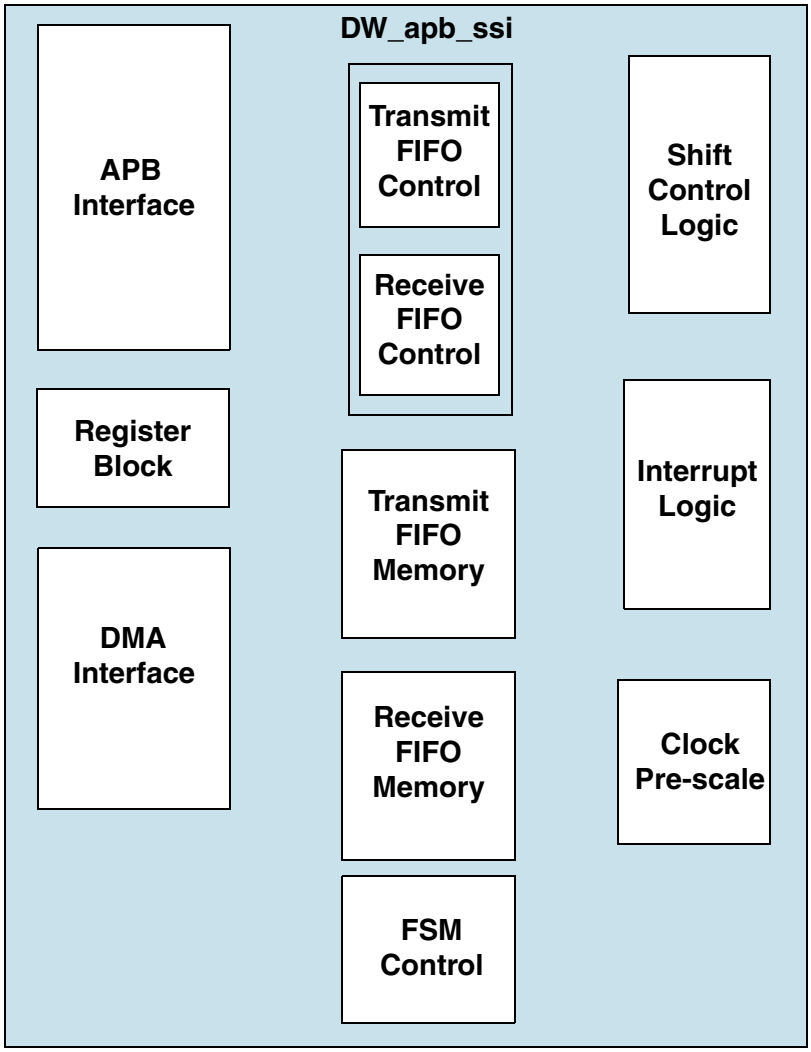
- AMBA APB interface – Allows for easy integration into an AMBA System on Chip (SoC) implementation.
- Scalable APB data bus width – Supports APB data bus widths of 8, 16, and 32 bits.
- Serial-master or serial-slave operation – Enables serial communication with serial-master or serial-slave peripheral devices.
- DMA Controller Interface – Enables the DW_apb_ssi to interface to a DMA controller over the AMBA bus using a handshaking interface for transfer requests.
- Independent masking of interrupts – Master collision, transmit FIFO overflow, transmit FIFO empty, receive FIFO full, receive FIFO underflow, and receive FIFO overflow interrupts can all be masked independently.
- Multi-master contention detection – Informs the processor of multiple serial-master accesses on the serial bus.
- Bypass of meta-stability flip-flops for synchronous clocks – When the APB clock (pclk) and the DW_apb_ssi serial clock (ssi_clk) are synchronous, meta-stable flip-flops are not used when transferring control signals across these clock domains.

Programmable features

- Serial interface operation – Choice of Motorola SPI, Texas Instruments Synchronous Serial Protocol or National Semiconductor Microwire.
- Clock bit-rate – Dynamic control of serial bit rate of data transfer; used in only serial-master mode.
- Data Item size (4 to 16 bits) – Item size of each data transfer under control of programmer.

Configurable features

- FIFO depth – Configurable depth of transmit and receive FIFO buffers from 2 to 256 words deep; FIFO width fixed at 16 bits.
- Number of slave select outputs – When operating as serial master, 1 to 16 serial slave-select output signals can be generated.
- Hardware/software slave-select – Dedicated hardware slave-select lines or software control for targeting serial-slave device.
- Combined or individual interrupt lines
- Interrupt polarity – Selects serial-clock phase of SPI format directly after reset.



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

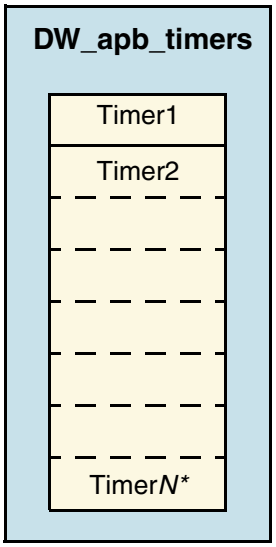
The *DesignWare DW_apb_ssi Databook* is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

AMBA Compliant

DW_apb_timers
APB Programmable Timers

- Up to eight programmable timers
- Configurable timer width: 8 to 32 bits
- Support for two operation modes: free-running and user-defined count
- Support for independent clocking of timers
- Configurable polarity for each individual interrupt
- Configurable option for a single or combined interrupt output flag
- Configurable option to have read/write coherency registers for each timer
- Configurable option to include timer toggle output, which toggles each time counter reloads



* *N* <= 8

This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

The *DesignWare DW_apb_timers Databook* is available at:

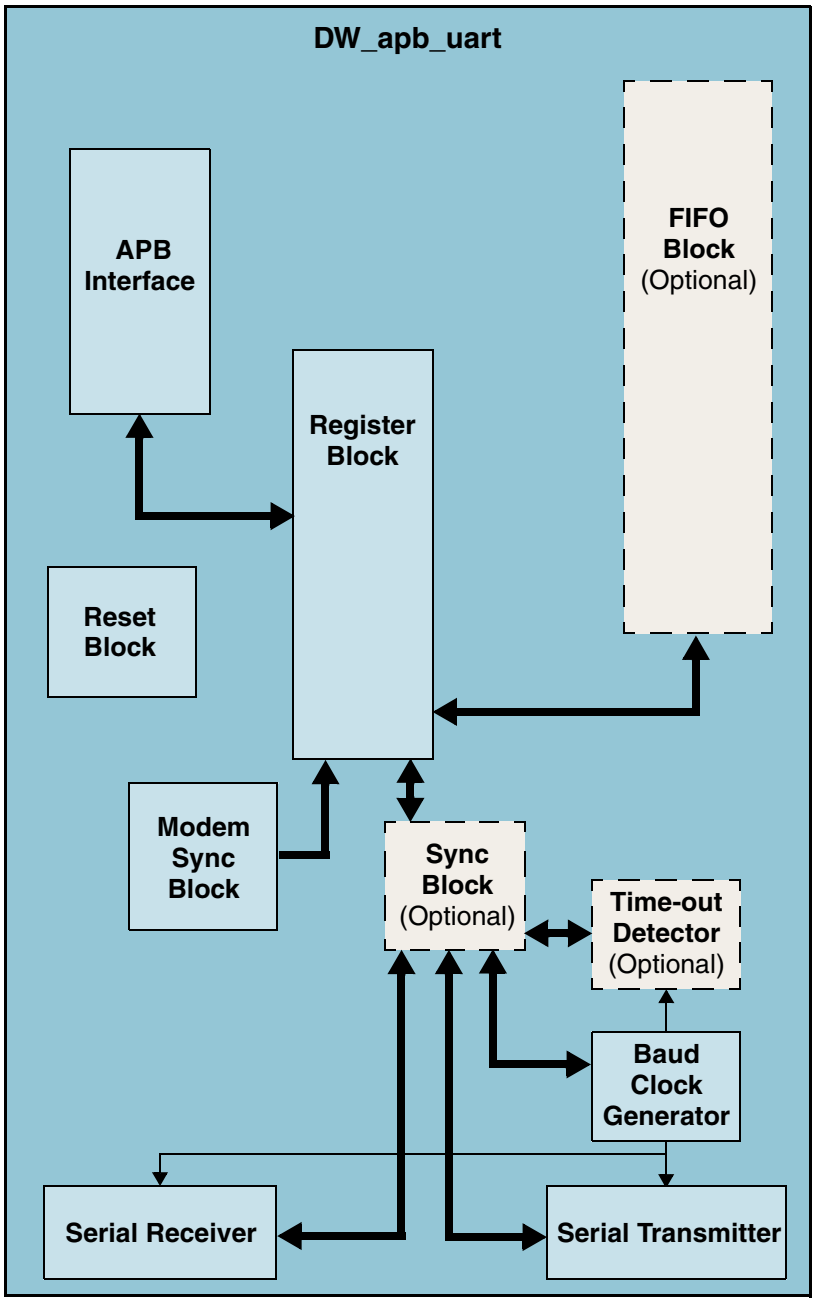
https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

DW_apb_uart

APB Universal Asynchronous Receiver/Transmitter

- AMBA APB interface allows easy integration into AMBA SoC implementations
- Configurable APB data bus widths of 8, 16 and 32
- Functionality based on the 16550 industry standard, that is as follows:
  - Programmable character properties, such as number of data bits per character (5-8), optional parity bit (with odd or even select) and number of stop bits (1, 1.5 or 2)
  - Line break generation and detection
  - DMA signaling with two programmable modes
  - Prioritized interrupt identification
- Configurable selection of additional DMA interface signals for compatibility with DesignWare DMA interface
- Configurable selection of DMA interface signal polarity
- Configurable transmit and receive FIFO depths of none, 16, 32, 64,…,2048
- Configurable internal or external FIFO (RAM) selection
- Programmable FIFO enable/disable External read enable signal for RAM wake-up when using external RAMs
- Configurable selection of the use two clocks (pclk and sclk) instead of one (pclk)
- Programmable Auto Flow Control mode as specified in the 16750 standard
- Programmable Transmitter Holding Register Empty (THRE) interrupt mode
- Configurable IrDA 1.0 SIR mode support with up to 115.2 Kbaud data rate and a pulse duration (width) as follows: width = 3/16 × *bit period* as specified in the IrDA physical layer specification
- Programmable serial data baud rate
- Configurable baud clock reference output signal
- Modem and status lines are independently controlled
- Programmable Loopback mode that enables greater testing of Modem Control and Auto Flow Control features (Loopback support in IrDA SIR mode is available)
- Selectable clock gate enable output(s) used to indicate that the TX and RX pipeline is clear (no data) and no activity has occurred for more than one character time, so clocks may be gated
- Separate system resets for each clock domain to prevent metastability
- Selectable FIFO access mode (for FIFO testing) so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master

Also see the block diagram on the following page.



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

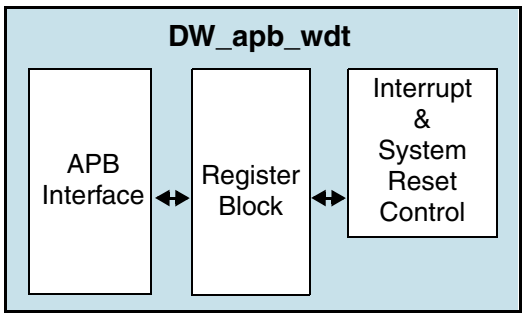
The *DesignWare DW_apb_uart Databook* is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

DW_apb_wdt

APB Watchdog Timer

- AMBA APB interface used to allow easy integration into AMBA System-on-Chip (SoC) implementations.
- Configurable APB data bus widths of 8, 16, and 32 bits.
- Configurable watchdog counter width of 16 to 32 bits.
- Counter counts down from a pre-set value to zero to indicate the occurrence of a time-out.
- Optional external clock enable signal to control the rate at which the counter counts.
- If a time-out occurs the DW_apb_wdt can perform one of the following operations:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second time-out occurs then generate a system reset
- Programmable time-out range (period). The option of hard coding this value during configuration is available to reduce the register requirements.
- Optional dual programmable time-out period, used when the duration waited for the first kick is different than that required for subsequent kicks. The option of hard coding these values is available.
- Programmable and hard coded reset pulse length.
- Prevention of accidental restart of the DW_apb_wdt counter.
- Prevention of accidental disabling of the DW_apb_wdt.
- Optional support for Pause mode with the use of external pause enable signal.
- Test mode signal to decrease the time required during functional test.
- coreAssembler ready.



The *DesignWare DW_apb_i2c Databook* is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

AMBA Compliant

DW_axi

Multiple Address, Multiple Data AXI Interconnect

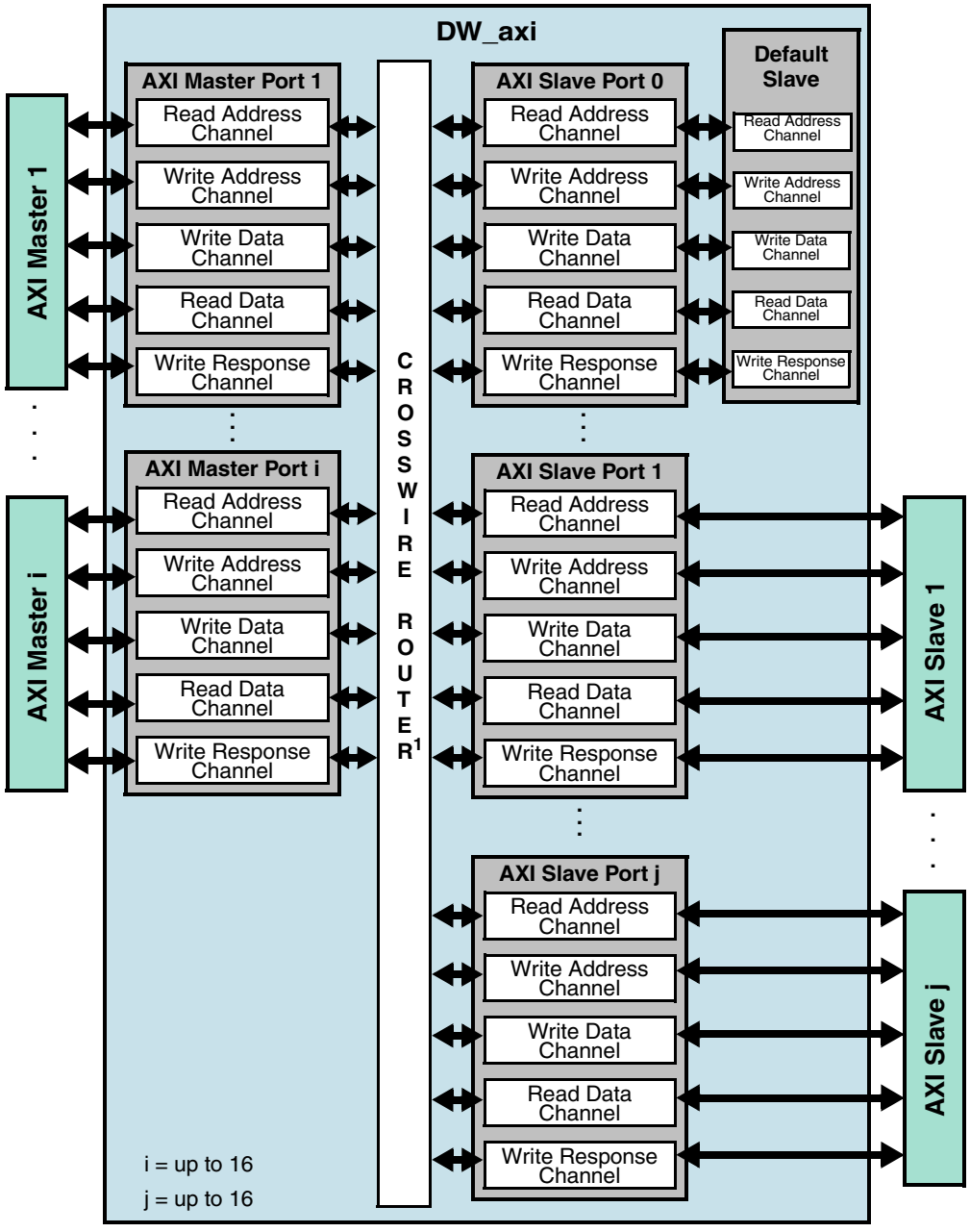
- High performance multiple address bus, multiple data (MAMD) bus AXI interconnect architecture
- Configurable number of master and slave ports (up to 16 each)
- Configurable system decoder (optional)
- Configurable master and slave priorities used for arbitration (configured statically or driven dynamically through input ports)
- Default slave included
- Configurable slave visibility per master
- Built-in out-of-order deadlock avoidance
- Address width of 32 or 64 bits
- coreAssembler ready
- Data widths of 8, 16, 32, 64, 128, 256, and 512 bits
- Equal data widths of master and slave ports
- Support for data bursts up to 256 beats
- Single clock frequency for all master and slave ports
- Equal data widths of master and slave ports
- No buffering of AXI channel payload in interconnect
- Locked transfer support
- Automatically optimized in single AXI master subsystems
- Optional user sideband signals for each AXI channel, allowing additional control/status per channel (for example, data parity)

The following page contains a block diagram of the DW_axi.

Documentation for this product is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

Figure 2-1 DW_axi Block Diagram



AMBA Compliant

DW_axi_dmac

AXI Central Direct Memory Access (DMA) Controller

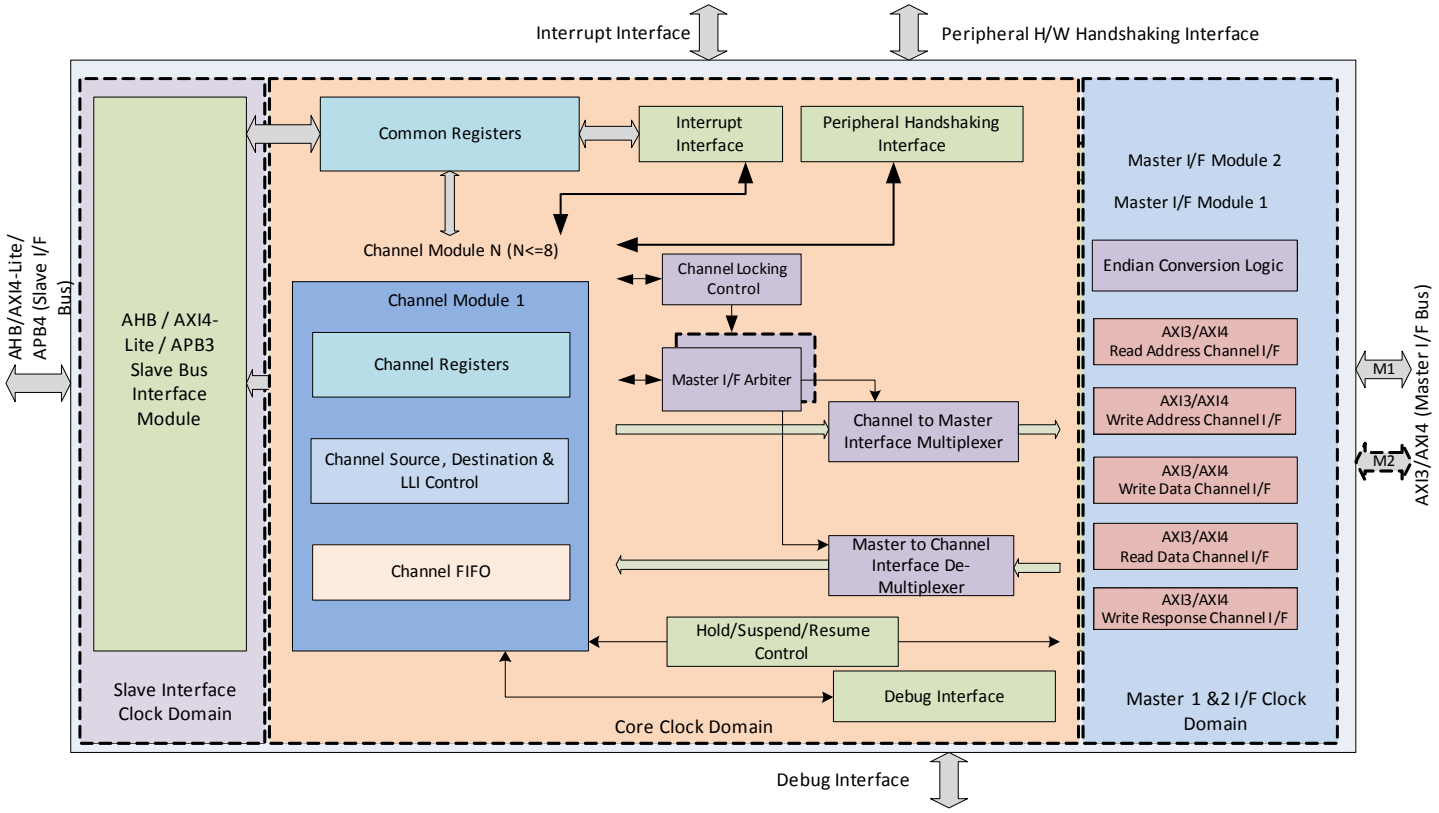
- Independent core, slave interface and master interface clocks
- Shutting down the slave interface clock
  - Master can shut down the slave interface clock when the slvif_busy output is de-asserted.
  - Master must restart the clock before trying to access the slave interface again.
- Individually shutting down the master interface clocks when no peripheral is active
- Up to eight channels, one per source and destination pair, configurable in coreConsultant
- Data transfers in one direction only (each channel is unidirectional)
- Up to two AXI master interfaces, configurable in coreConsultant
  - Two master interfaces for multilayer support
  - Multiple AXI masters increase bus performance by allowing direct connection of peripherals on different AXI interconnects
  - Support for different ACLK on different AMBA layers
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral DMA transfers
- AMBA 3 AXI/AMBA 4 AXI-compliant master interface
- AHB/AXI4-Lite/APB3 slave interface for programming the DMA controller
  - Only AHB supported in this version
  - AHB slave interface supports only SINGLE transfers (hburst = 3'b000).
- AXI master data bus width up to 512 bits (for both AXI master interfaces), configurable in coreConsultant
- Endianness support
  - Endian mode can be selected statically or dynamically for AXI master interfaces, configurable in coreConsultant
  - Input pin to dynamically select endian scheme
  - Independent control for endian scheme of linked list access on master interfaces, configurable in coreConsultant
- Optional identification register, configurable in coreConsultant
- Locking support
  - Channel locking support
  - Supports locking of the internal channel arbitration for the master bus interface at different transfer hierarchy
- DMAC status indication outputs
  - Idle/busy indication

The following page contains a block diagram of the DW_axi_dmac.

Documentation for this product is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

Figure 2-2 DW_axi_dmac Block Diagram

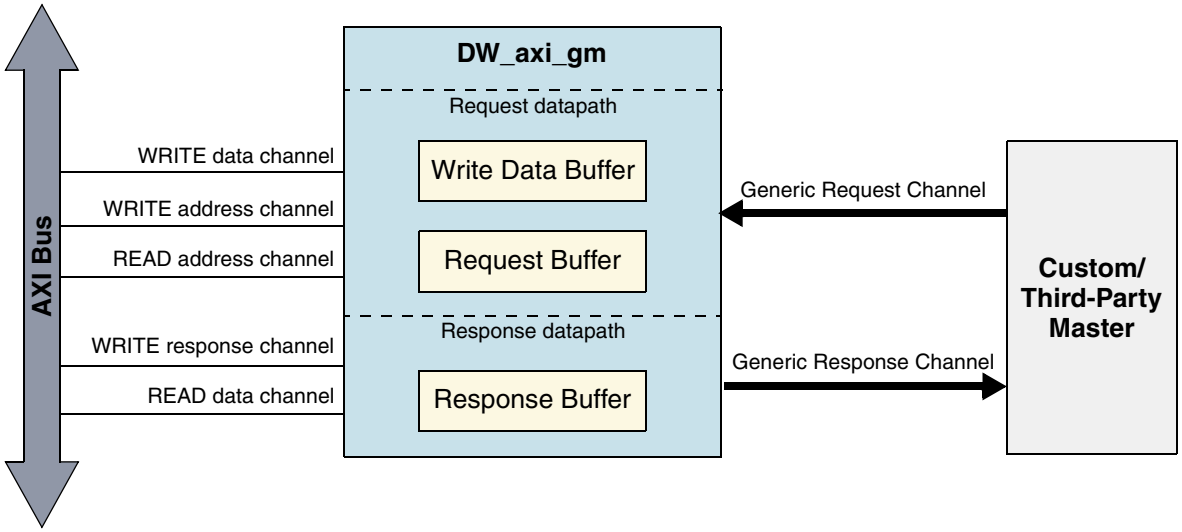


AMBA Compliant

DW_axi_gm

Generic Interface (GIF) to AMBA AXI Module

- Full support of the AXI protocol, except for exclusive accesses
- Full support of AXI low-power interface
- Two-way flow control
- Synchronous point-to-point communication on generic interface (GIF)
- Independent request and response GIF channels
- Unlimited outstanding transactions
- Synchronous clock support; including slower GIF clock
- Configurable micro-architecture
- Transaction block control



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

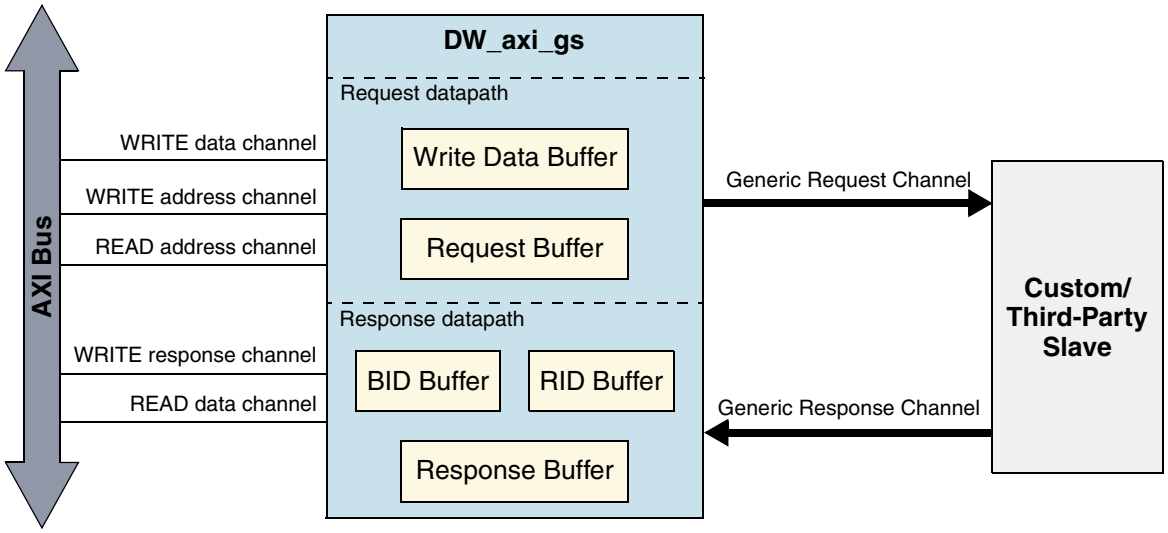
Documentation for this product is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

DW_axi_gs

AMBA AXI Slave to Generic Interface (GIF)

- Full support of the AXI protocol
- Configurable number of exclusive access monitors
- Full support of AXI low-power interface
- Two-way flow control
- Synchronous point-to-point communication on GIF
- Independent request and response GIF channels
- Configurable number of outstanding transactions
- Synchronous clock support; including slower GIF clock
- Configurable microarchitecture
- Configurable I/O signals to support simple peripherals



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

Documentation for this product is available at:

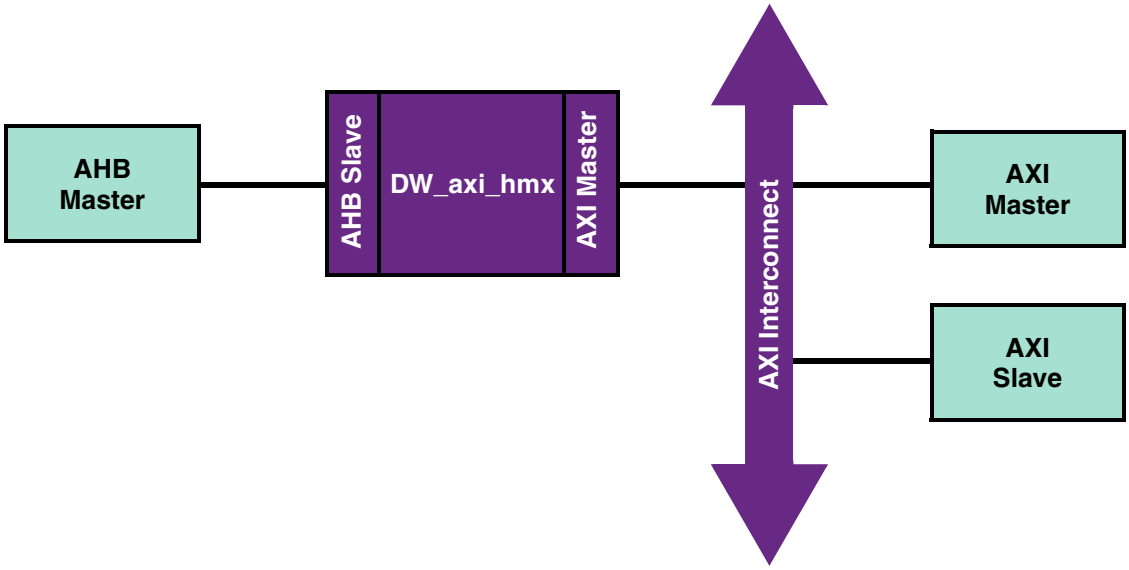
https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

AMBA Compliant

DW_axi_hmx

Connects AMBA AXI Slave to AHB Master

- Connects a single AHB master to a single AXI slave without use of AHB bus fabric
- Single clock design with quasi-synchronous hclk
- Buffered write transactions
- Write error indication by hardware interface
- Low-power interface
- Big endian AHB-to-AXI conversion
- Locked transactions
- Support for all AHB burst types
- Timing mode options to ease timing closure
- Option to block writes
- Static setting of AWPORT/ARPORT secure bit



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

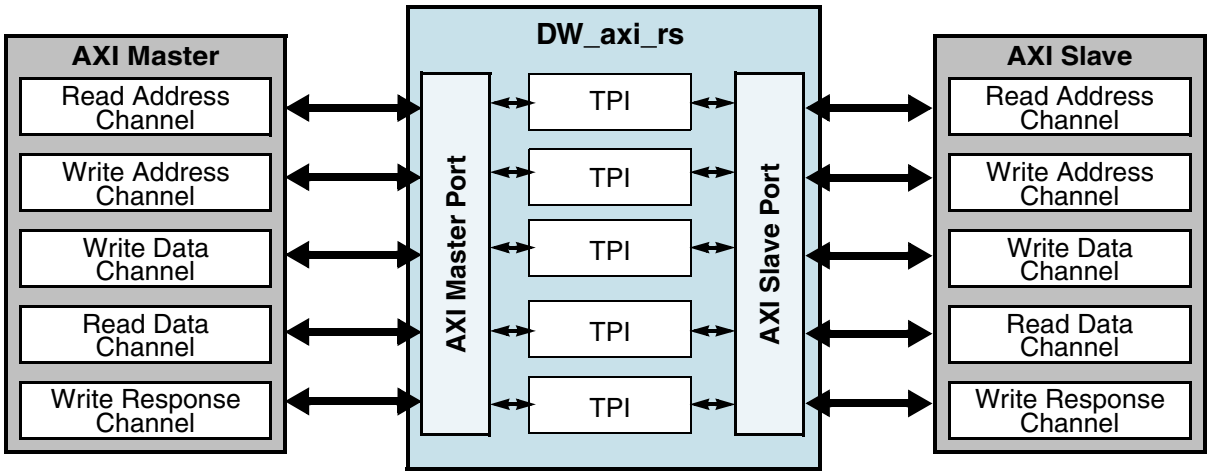
Documentation for this product is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

DW_axi_rs

AMBA AXI Register Slice

- Full support of the AXI protocol
- Supports the following timing modes:
  - Pass Through
  - Forward Registered
  - Fully Registered
  - Backward Registered
- Configurable timing mode option on a per channel basis. The timing mode option selected for a channel is independent of the option selected for the other AXI channels.
- No throughput penalty for any of the timing mode options
- Sideband signaling support
- Master and slave have same address width, data width, ID width, and burst width
- Same clock domain for attached master and slave
- Adds one cycle of latency on registered paths



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

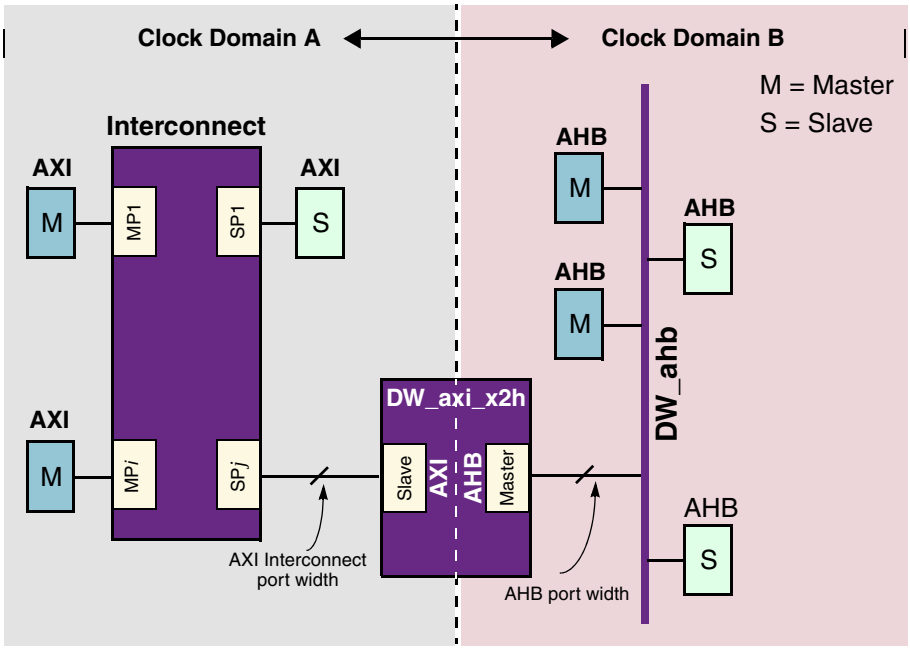
Documentation for this product is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

AMBA Compliant

DW_axi_x2h
AXI to AHB Bridge

- Bridge from AXI to AHB bus, allowing for easy integration of legacy AHB designs with newer AXI designs
- Configurable AXI Slave interface
- Configurable AHB Master interface; includes AHB Lite support
- AMBA AXI and AMBA 2.0 (AHB) compliant
- Configurable depths on command, data, and response queues
- All transactions passed through industry-standard DesignWare FIFOs
- Supports transfer downsizing; AHB data width can be the same as AXI or narrower
- Configurable synchronous or asynchronous AXI/AHB clock operations with any clock ratio



This component is coreAssembler ready. For more information about coreAssembler, refer here:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

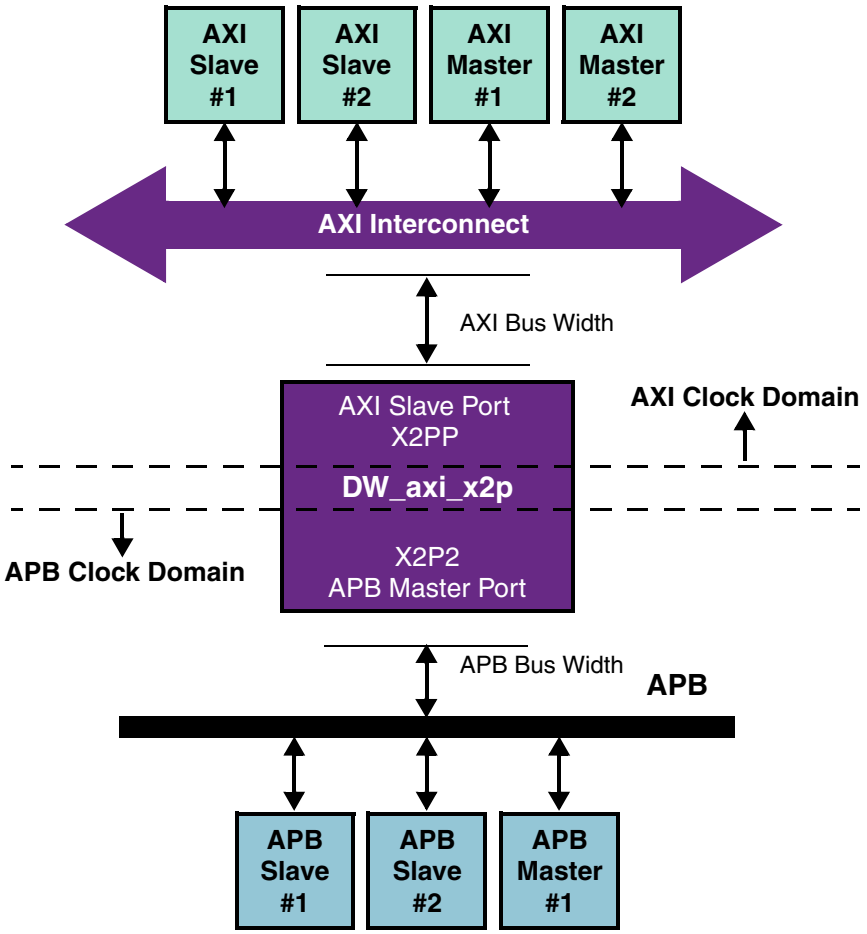
The *DesignWare DW_axi_x2h Databook* is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

DW_axi_x2p

Connects AMBA AXI Slave to AHP Master

- Translates AXI transactions into APB transfers
  - Compliance with *AMBA 3 APB Protocol Specification*, Rev. 1.0 and AMBA AXI Protocol Rev. 1.0 from ARM
  - Configuration option for AMBA 2 (APB) compatibility
  - Accepts simultaneous read/write AXI transactions
  - APB attempts to honor AXI data transfer intent on each APB transfer.
- Support for different clock domains
  - Single clock or two clocks of any clock integer ratio
  - Support for quasi-synchronous clocking – single clock with the use of a pclk_enable allows APB side of bridge to issue at a slower rate than the system.
- Flexible address and data port configurations
  - AXI data ports: 8, 16, 32, 64, 128, 256, or 512 bits wide
  - APB data ports: 8, 16, or 32 bits wide
  - AXI address ports: 32 or 64 bits
  - APB address ports: 32 bits
  - AXI little or big endian byte ordering (byte invariant). APB is always little endian.
- Buffers AXI transactions
  - Buffers activity on all of the AXI channels, minimizing waits on AXI control, data, and response
  - Supports a wide range of user-selectable depths for the command queues, response buffer, read data, and write data buffers



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

Documentation for this product is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

DW_axi_x2x

Connects AMBA AXI Master to AXI Slave

General Features

- Translates AXI transactions into APB transfers
- Compliance with AMBA AXI Protocol Rev. 1.0 from ARM
- Transparent Operation—transaction attributes altered when necessary to fit on secondary bus
- Accepts simultaneous AXI transfers on all 5 channels; passes to primary/secondary AXI bus
- Configurable buffer depths for all 5 channels to allow off-loading of payload source bus to sink bus
- Support for asynchronous clocks on Slave Port and Master Port sides
- Optimizations for quasi-synchronous clocking of any integer ratio

Address Channel Features

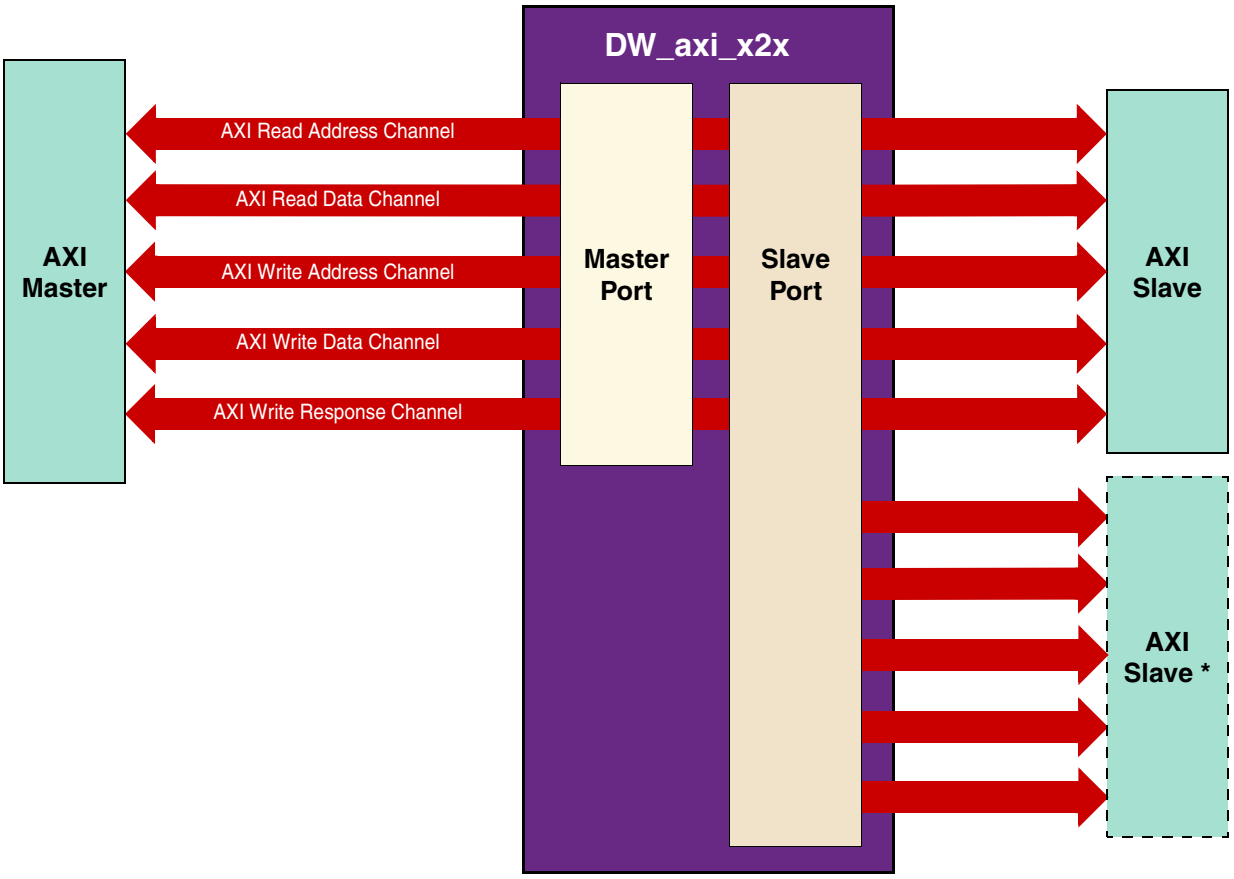
- Address width configurable to any value in range 32-64 on both Slave and Master Ports
- Changes attributes for transactions that cannot fit on the secondary bus
- For upsizing, increases SIZE of transaction and decreases length to generate transaction of SIZE equal to maximum on secondary bus
- Configures which channels exist—write-only, read and write; allows for use in purely write interleaving fanout mode
- Supports burst lengths of up to 256

Data Channel Features

- Data Ports: 8, 16, 32, 64, 128, 256, 512 bits wide
- Master Port and Slave Port data widths can be configured to different widths
- Transfer unpacking done to translate larger Master Port data width to smaller Slave Port data width; on return from Slave Port to Master Port, transfers packed to match size of original transaction from primary bus
- Can upsize transactions; that is, pack data from primary into shorter transaction of larger SIZE on secondary
- AXI little- and big-endian Byte Ordering (byte invariant) is individually configurable for each interface
- Configurable read interleaving depth; allows external slave to reorder and/or interleave read data up to this depth
- Configurable write interleaving depth

DW_axi_x2x
Connects AMBA AXI Master to AXI Slave

AMBA Compliant



* Optional AXI Slave only with write interleaving fan-out

This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/dw/ipdir.php?ds=core_assembler

Documentation for this product is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

DW_axi_a2x

Connects AMBA AHB or AXI Bus to AXI Bus

General Features

- Connects AHB bus fabric, or AXI bus fabric to AXI bus fabric
- Supports asynchronous, synchronous, and quasi-synchronous clocking
- Provides asynchronous timing mode options to ease clock domain crossing
- Configurable buffer depth for address and data channels
- Configurable Store and Forward or Cut-Through mode
- Configurable address port widths of any range from 32 to 64
- Configurable data bus widths of 8, 16, 32 64, 128, 256, 512 bits
- Support for transaction down-sizing (larger AHB/AXI bus to smaller AXI bus)
- Dynamic controllable support for transaction up-sizing (smaller AHB/AXI bus to larger AXI bus)
- Provides support for read data interleaving

AHB Features

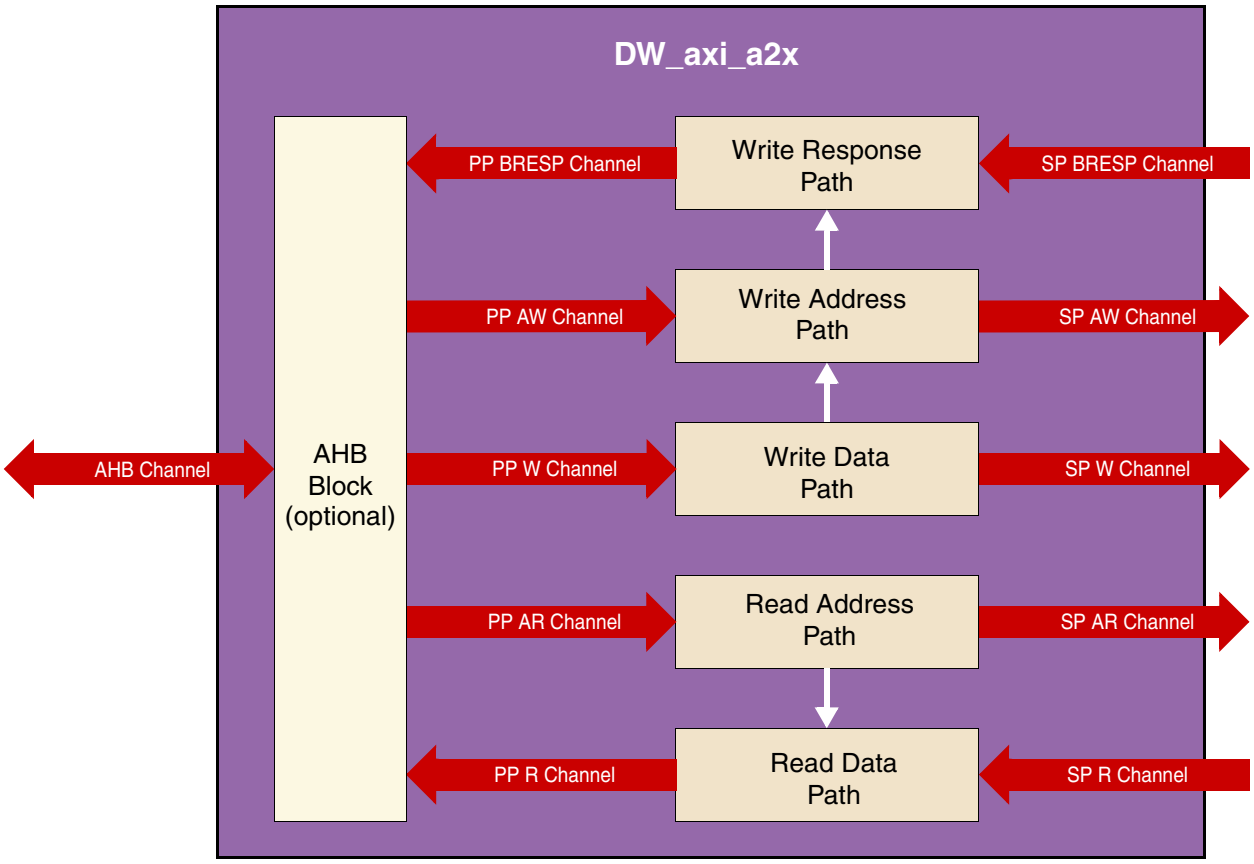
- AHB SPLIT response used to control AHB bus for efficiency and coherency with bus arbiter
- AHB master ID to AXI ID translation
- Support for all AHB burst types
- Conversion of undefined length AHB read INCR transactions to defined-length AXI burst
- Conversion of undefined length AHB write INCR transactions to defined-length AXI burst
- Supports AHB locked to AXI locked translation
- Ability to control transaction ordering from a single AHB master in non-bufferable or dynamic configurations
- Provides AHB-Lite mode
  - SPLIT response not supported
  - hready driven low

The following page contains a block diagram of the DW_axi_a2x.

Documentation for this product is available at:

https://www.synopsys.com/dw/doc.php/doc/amba/latest/intro.pdf

Figure 2-3 DW_axi_a2x Block Diagram



3 DesignWare Cores (Digital/Mixed-Signal IP)

DesignWare Cores provide system designers with silicon-proven, digital and analog connectivity IP. Provided as heavily-annotated, synthesizable RTL source code, or in GDS format, these cores enable you to design innovative, cost-effective systems-on-chip and embedded systems. DesignWare Cores are licensed individually on a fee-per-project business model.

For more information, visit the DesignWare Cores web page at:

http://www.synopsys.com/IP/InterfaceIP

The following table identifies the available DesignWare Cores:

Component Name	Component Description	Component Type
Ethernet Cores		
dwc_ether_mac10_100_universal	Ethernet MAC 10/100 Universal (page 58)	Synthesizable RTL
dwc_ether_mac10_100_1000_universal	Ethernet MAC 10/100/1G Universal (page 60)	Synthesizable RTL
dwc_ether_xgmac	10 Gigabit Ethernet Mac (page 62)	Synthesizable RTL
dwc_ether_xlgmac	10 Gigabit Ethernet Mac (page 65)	Synthesizable RTL
dwc_ether_pcs	PCS Layer of 10 Gigabit Extended sub-layer (page 67)	Synthesizable RTL
dwc_xlgpcs	PCS Layer of 10 Gigabit Extended sub-layer (page 70)	Synthesizable RTL
dwc_ether_qos	Ethernet Quality-of-Service Core (page 73)	Synthesizable RTL
dwc_xaui_phy	XAUI PHY (page 75)	Hard IP
dwc_12g_phy	Enterprise 12G PHY (page 76)	Hard IP
Mobile Storage Core		
dwc_mobile_storage	Secure Digital (SD), Multimedia Card (MMC) and CE-ATA (page 78)	Synthesizable RTL
DDR/DDR2/DDR3 Cores		
dwc_ddr2_3l_mddr_phy	“DDR2/3-Lite/mDDR PHY” on page 80	Hard IP
dwc_ddr2_ddr_phy	“DDR2/DDR PHY” on page 82	Hard IP
dwc_ddr3_ddr2_phy	“DDR3/2 PHY” on page 84	Hard IP
ddr_multi_phy	“DDR multiPHY” on page 86	Hard IP
dwc_ddr_upctl, dwc_ddr_umctl, and dwc_ddr_umctl2	“dwc_ddr_upctl, dwc_ddr_umctl, and dwc_ddr_umctl2” on page 88	Synthesizable RTL
IEEE 1394 Cores		
dwc_1394_av_link	IEEE 1394 AVLink (page 92)	Synthesizable RTL

dwc_1394_cphy-native	IEEE 1394 Cable PHY (page 94)	Synthesizable RTL
PCI Cores		
dwc_pci	32/64 bit, 33/66-MHz PCI Core (page 95)	Synthesizable RTL
dwc_pci-x	32/64 bit, 133-MHz PCI-X Core (page 96)	Synthesizable RTL
PCI Express Cores		
dwc_pci_express_ep	PCI Express Endpoint Core (page 100)	Synthesizable RTL
dwc_pci_express_rc	PCI Express Root Port Core (page 101)	Synthesizable RTL
dwc_pci_express_sw	PCI Express Switch Port Core (page 102)	Synthesizable RTL
dwc_pci_express_dm	PCI Express Dual Mode Core (page 103)	Synthesizable RTL
dwcore_pcie_phy	PCI Express PHY Core (page 104)	Hard IP
SATA Cores		
DWC_ahsata	SATA AHCI (page 105)	Synthesizable RTL
DWC_dsata	SATA Device (page 106)	Synthesizable RTL
dwc_sata_phy	SATA PHY (page 108)	Hard IP
USB Cores		
dwc_usb_1_1_device	USB 1.1. Device Controller (page 109)	Synthesizable RTL
dwc_usb_1_1_ohci_host	USB 1.1 OHCI Host Controller (page 110)	Synthesizable RTL
dwc_usb_1_1_hub-native	USB 1.1. Hub Controller (page 111)	Synthesizable RTL
dwc_usb_2_0_host_subsystem-pci-ahb	USB 2.0 Host Controller - UHOST2 (page 113)	Synthesizable RTL
dwc_usb_2_0_hs_otg_subsystem-ahb	USB 2.0 Hi-Speed On-the-Go Controller Subsystem (page 115)	Synthesizable RTL
dwc_usb_2_0_device	USB 2.0 Device Controller (page 118)	Synthesizable RTL
dwc_usb2_phy	USB 2.0 PHY (page 120)	Hard IP
dwc_usb2_hsotg_phy	USB 2.0 Hi-Speed On-the-Go PHY (page 122)	Hard IP
dwc_wiusb_device_controller	Wireless USB Device Controller (page 120)	Synthesizable RTL
dwc_usb2_nanophy	USB 2.0 nanoPHY (page 122)	Hard IP
dwc_usb2_picophy	USB 2.0 picoPHY (page 124)	Hard IP
dwc_usb2_femtophy	USB 2.0 femptoPHY (page 126)	Hard IP
dwc_usb_3_0_device	SuperSpeed USB 3.0 Device Controller (page 128)	Hard IP
dwc_usb_3_0_host	SuperSpeed USB 3.0 Host Controller (page 131)	Hard IP
dwc_usb_3_0_drd	USB 3.0 Dual Role Device Controller (page 134)	Synthesizable RTL
dwc_usb_3_0_hub	SuperSpeed USB 3.0 Hub Controller (page 137)	Hard IP

JPEG Core		
dwc_jpeg	JPEG CODEC (page 140)	Synthesizable RTL
HDMI Cores		
DWC_hdmi_rx	HDMI 1.3 and 1.4 Receiver Controllers (page 142)	Synthesizable RTL
DWC_hdmi_tx	HDMI Transmitter Controller (page 144)	Synthesizable RTL
dwc_hdmi20_rx_phy	HDMI 2.0 RX PHY IP (page 148)	Synthesizable RTL
dwc_hdmi20_mhl_rx_phy	HDMI-MHL RX PHY (page 149)	Synthesizable RTL
dwc_hdmi20_tx_phy	HDMI 2.0 TX PHY IP (page 151)	Synthesizable RTL
dwc_hdmi20_mhl_tx_phy	HDMI-MHL TX PHY (page 153)	Synthesizable RTL
MIPI Cores		
dwc_mipi_dsi_host	MIPI DSI Host Controller (page 157)	Synthesizable RTL
dwc_ufshc	DesignWare UFS Host Controller (page 159)	Synthesizable RTL
dwc_mipi_dphy_bd2	MIPI DPHY Bidirectional 2 Lanes (page 161)	Synthesizable RTL
dwc_mipi_dphy_bd4	MIPI DPHY Bidirectional 4 Lanes (page 163)	Synthesizable RTL
dwc_mipi_dphy_rx2	MIPI DPHY RX 2 Data Lanes (page 165)	Synthesizable RTL
dwc_mipi_dphy_rx4	MIPI DPHY RX 4 Data Lanes (page 166)	Synthesizable RTL
dwc_mphy_type1_1tx_1rx	MIPI MPHY TYPE1 1Tx1RX (page 167)	Synthesizable RTL
dwc_mipi_mphy_type1_2tx_2rx	MIPI MPHY TYPE1 2Tx2RX (page 169)	Synthesizable RTL
dwc_mipi_digrf	MIPI DigRF 2.5G-3G Physical Layer (page 171)	Synthesizable RTL
dwc_mipi_csi2_host	MIPI CSI-2 Host Controller (page 173)	Synthesizable RTL
dwc_mipi_unipro	MIPI UniPro (page 179)	Synthesizable RTL

dwc_ether_mac10_100_universal

Ethernet MAC 10/100 Universal Core

The DesignWare Ethernet MAC 10/100 Universal Core enables the host to communicate data using the Ethernet protocol (IEEE 802.3). This silicon-proven core is configurable and scalable to meet multiple Ethernet application requirements and system architectures. Its high-performance architecture is optimized for low latency and low gate count.

The Synopsys Ethernet MAC 10/100 Universal Core enables Ethernet functionality for switch, NIC, and system-on-chip applications. The DesignWare Ethernet MAC implements more functionality than standard Ethernet MACs, including MAC station management, address check, IP checksum offload engine, time stamping and Control/Status Register (CSR) blocks. These additional features provide higher-level system functionality usually implemented in firmware or using separate products. With these additional capabilities, the Ethernet MAC simplifies system implementation.

General Features

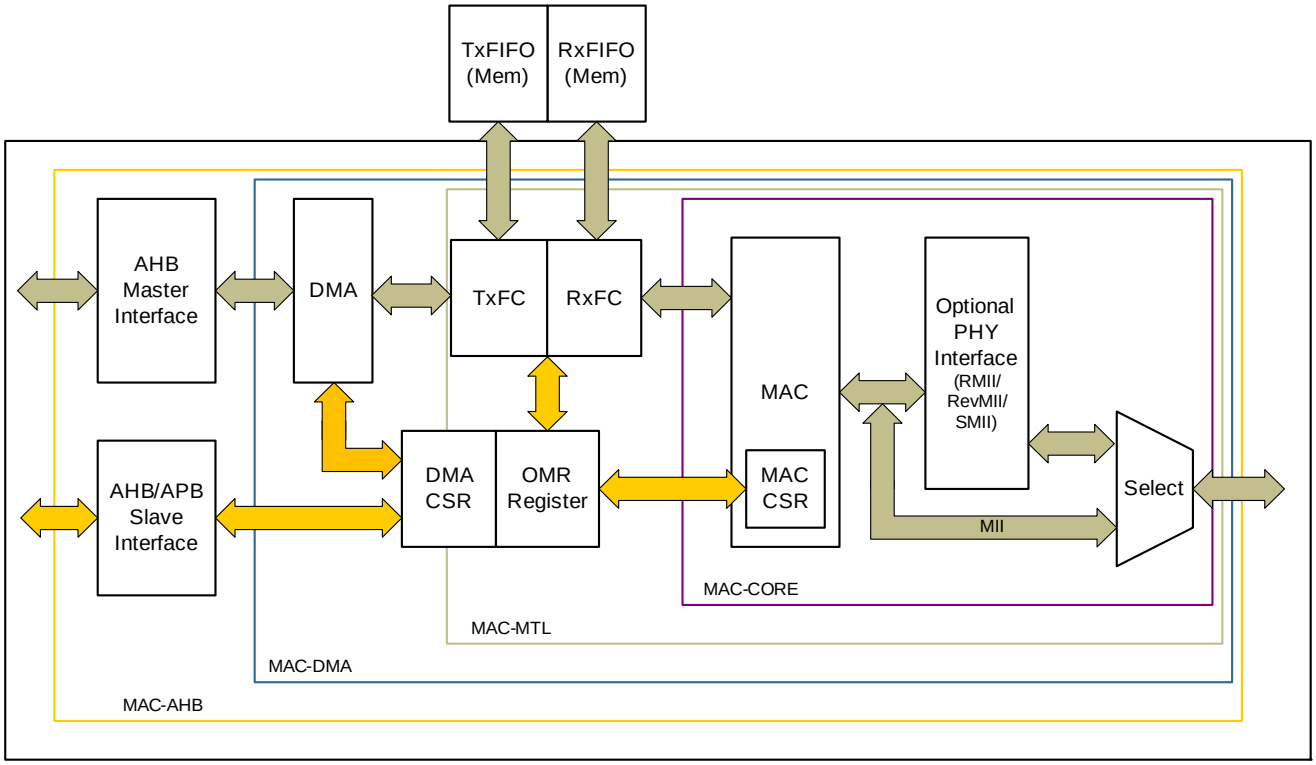
- Complies with IEEE 802.3-2008 specification
- Supports IEEE 802.1Q VLAN tag detection for reception frames
- Supports CSMA/CD protocol for half-duplex operation
- Supports Full-Duplex-Only configuration
- Supports IEEE 802.3x flow control for full-duplex operation
- Supports IEEE 1588-2002 precision clock synchronization
- Supports complete network statistics (optional) with RMON/MIB counters (RFC2819/RFC2665)
- Provides optional module for Remote Wake-Up frames and AMD Magic Packet frames
- Supports IEEE 1801-2009 (Unified Power Format) standard
- Supports Receive Checksum Offload for IP and TCP/UDP packets

PHY Interface Features

- Supports MII, SMII, RMII, and RevMII interfaces
- Supports MDIO Master Interface (optional) for PHY device configuration and management

Application Interface Features

- Data interface configurable to support FIFO interface, native interface, or AHB interface
- CSR interface configurable to AHB, APB, or APB 3 Slave interface
- Supports 32/64/128-bit data on the AHB master and slave ports
- Supports SPLIT, RETRY, and ERROR AHB responses in AHB master interface
- Supports little-endian or big-endian modes
- Supports all AHB burst types in AHB slave interface
- Software can select the type of AHB burst in an AHB master interface



The dwc_ethernet_mac10_100_universal datasheet is available at:

http://www.synopsys.com/dw/doc.php/ds/c/dwc_ether_mac10_100_universal.pdf

dwc_ether_mac10_100_1000_universal

Ethernet MAC 10/100/1000 Universal Core

The Synopsys DesignWare Ethernet MAC 10/100/1G Universal Core enables the host to communicate using the Gigabit Ethernet protocol (IEEE 802.3). The Ethernet MAC 10/100/1G Universal Core is composed of three main layers: the Gigabit Ethernet Media Access Controller (GMAC), the MAC Transaction Layer (MTL), and the MAC DMA Controller (MDC). Other features include the following:

General Features

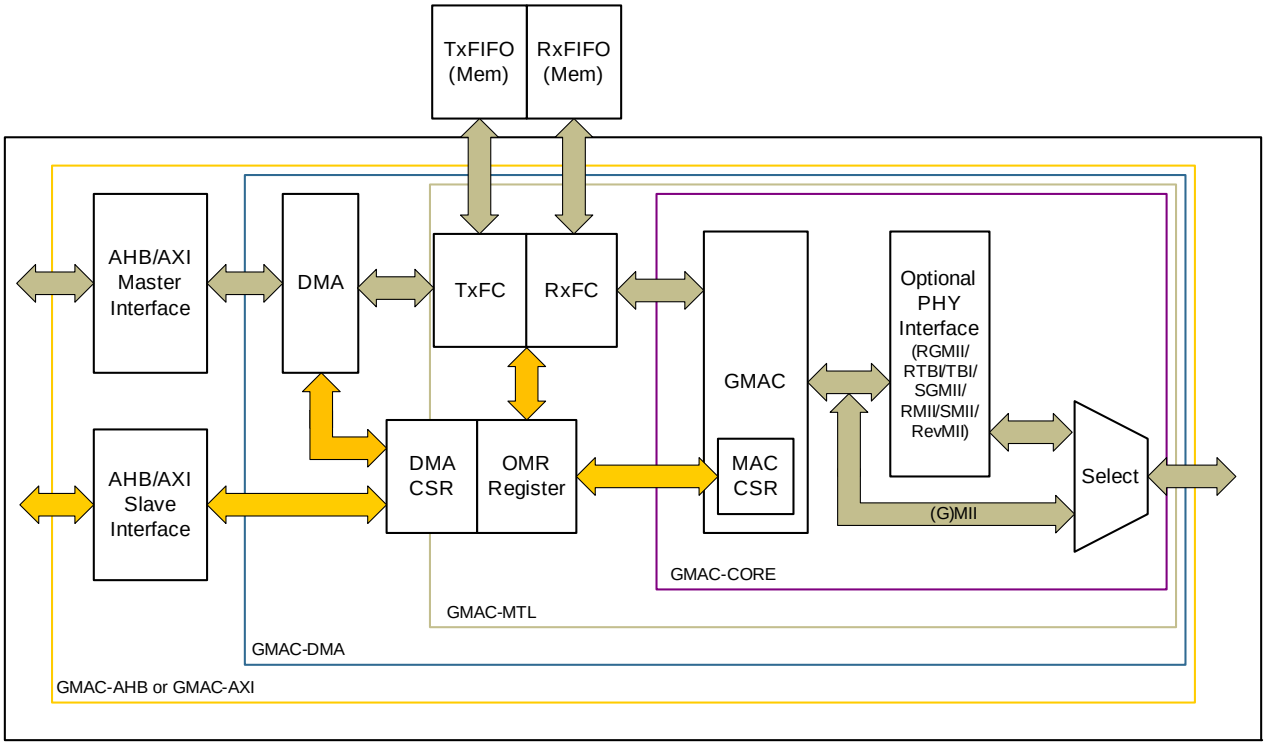
- Compliant with IEEE Std 1588-2002 and IEEE Std 1588-2008 Precision Clock Synchronization
- Compliant with IEEE Std 802.3-2008
- Supports IEEE Std 802.1Q VLAN tag detection for reception frames
- Configurable to support the following data transfer rates:
  - 10 Mbps, 100 Mbps, or 1000 Mbps
  - 10 Mbps or 100 Mbps only
  - 1000 Mbps only
- Supports CSMA/CD protocol for half-duplex operation
- Supports Full-Duplex-Only configuration
- Supports packet bursting and frame extension in 1000-Mbps half-duplex mode
- Supports IEEE 802.3x flow control for full-duplex operation
- Supports a variety of flexible address filtering modes
- Provides complete network statistics (optional) with RMON/MIB counters (RFC2819/RFC2665)
- Provides optional module for Remote Wake-Up frames and AMD Magic Packet frames
- Supports IEEE Std 1801-2009 (Unified Power Format)
- Supports IEEE Std 802.3az - 2010 for Energy Efficient Ethernet.
- Supports Receive and Transmit Checksum Offload for IP and TCP/UDP packets
- Supports Receive Layer 3 and Layer 4 based packet filtering
- Supports Transmit Source Address and VLAN Tag insertion or replacement

PHY Interface Features

- IEEE Std 802.3-compliant GMII and MII interfaces
- IEEE Std 802.3z-compliant TBI and RTBI interfaces with auto-negotiation support
- SGMII, RGMII, RMII, Serial-MII (SMII), and Reverse MII (RevMII) interfaces
- MDIO Master interface (optional) for PHY device configuration and management

Application Interface Features

- The following application interfaces are configurable:
  - GMAC-only with native interface
  - GMAC with MTL native interface
  - DMA with native interface
  - DMA with AHB interface
  - DMA with AXI interface
- Data interface, configurable to support FIFO, native DMA, and AHB or AXI interfaces
- CSR interface configurable to 32-bit AHB, AXI, APB, or APB 3 Slave interface
- Supports 32-bit, 64-bit, or 128-bit data on the AHB or AXI Master and Slave ports



The dwc_ethernet_mac10_100_1G_universal datasheet is available at:

http://www.synopsys.com/dw/doc.php/ds/c/dwc_ether_mac10_100_1000_universal.pdf

dwc_ether_xgmac

XGMAC 10G Ethernet MAC Core

The DesignWare XGMAC core is specifically designed for easy integration with 1G/2.5G/10G-Ethernet host applications. It enables a host to transmit and receive data over Ethernet in compliance with IEEE 802.3-2008 standards. The native application interface of XGMAC-CORE, XGMAC-MTL, and AXI4 interface of XGMAC-AXI enables easy integration with 10-gigabit host applications.

The XGMAC subsystem provides a 10-Gigabit Media-Independent Interface (XGMII, an IEEE 802.3 compliant reconciliation sub-layer) for communication with the 10-Gigabit PHY. The XGMAC IP also provides a Management Data Input/Output (MDIO) interface capable of addressing MDIO devices that comply with Clause 45 of the IEEE 802.3 standard and Clause 22 of the 802.3-2008 standards.

General Features

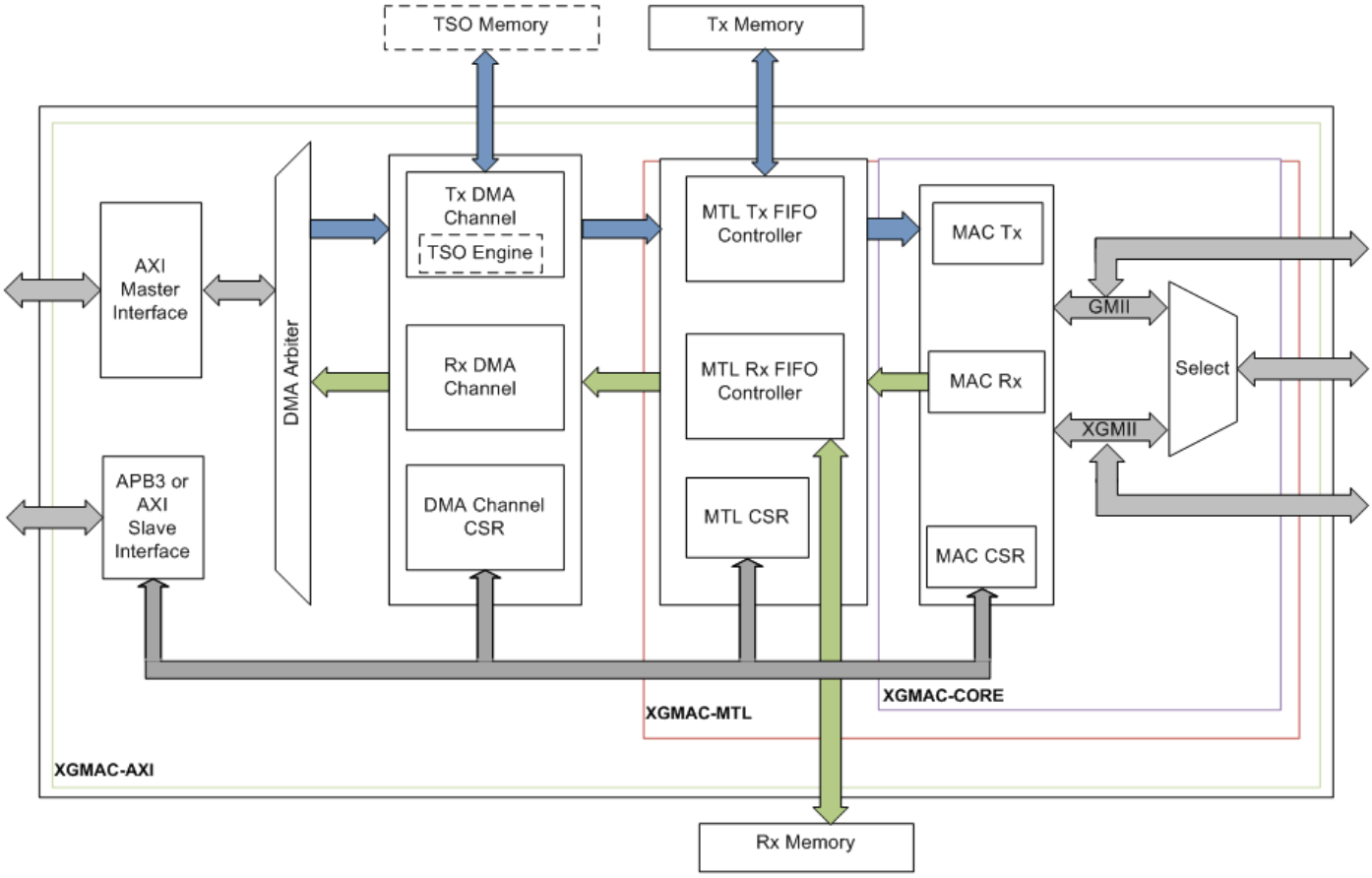
- Complies with the following standards:
  - IEEE 802.3-2008 specification
  - IEEE Std 1588- 2008 Precision Clock Synchronization
- Supports IEEE Std 802.1-Qaz-2011 and IEEE Std 802.1-Qbb-2011 for Data Center Bridging applications
  - Separate and independent channels or queues for data transfer
  - Up to 12 queues for segregating Received traffic and 16 queues on the Transmit path for classifying up to 8 traffic classes
  - Single Tx FIFO and Rx FIFO memory for all selected queues with programmable queue lengths
- IEEE Std 802.1Q-2011 (Virtual Bridged Local Area Networks) support
- IEEE Std 802.3az-2010 standard for Energy Efficient Ethernet (EEE)
- Full duplex-only operation supporting 10G, 2.5G and 1G data rates
- Separate transmission, reception, and control interfaces
- 32-bit CRC generation for transmit frames
- Per-frame CRC checking and stripping on the receive path
- Transmission padding for less than 64 bytes
- Support for Jumbo frames up to 9KB expandable up to 16KB
- Flow control operations based on IEEE 802.3x Pause packets and IEEE 802.3bd Priority Flow Control packets
- Programmable source address inclusion and replacement for Transmit frames
- Supports QinQ VLAN tags for filtering, stripping in Receive path and insertion or replacement in Transmit path
- Optional Network statistics with RMON or MIB counters
- Provides optional module for Remote Wake-Up frames and AMD Magic Packet frames
- Internal loopback on XGMII for system packet debugging
- Flexible and comprehensive packet filtering functions based on Layer 2, Layer 3 or Layer 4 fields of received packets
- Supports Receive Side Scaling and Out-of-Sequence detection function for enabling Large Receive Offload
- Optional ARP Offload engine and PTP packet offload engine
- TCP, UDP, or ICMP checksum offload (IPv4 and IPv6) for transmission and reception
- Configurable big-endian or little-endian support for transmission and reception data paths
- Control frame filtering other than PAUSE/PFC
- Optional module to support Ethernet packet timestamping as described in IEEE 1588-2008
- TCP/IP Segmentation Offload in Transmit
- Optional support for VxLAN/NvGRE tunnelling functions

PHY Interface Features

- IEEE Std 802.3-2008 (Clause 46) XGMII
- IEEE Std 802.3-2008 (Clause 35) GMII Interface

Application Interface Features

- The following application interfaces are configurable:
  - XG MAC only (XGMAC-CORE) with native interface
  - XG MAC with transaction layer (XGMAC-MTL)
  - XG MAc with AXI-DMA (XGMAC-AXI)
- CSR interface configurable to AXI, APB3, or native Slave interface
- Supports 64-bit, or 128-bit data on the AXI Master or native interfaces



The dwc_ether_xgmac datasheet is available at:

http://www.synopsys.com/dw/doc.php/ds/c/dwc_ether_xgmac.pdf

dwc_ether_xlgmac

XLGMAC 40G Ethernet MAC Core

The DesignWare XLGMAC core is specifically designed for easy integration with 1G/2.5G/10G/40G - Ethernet host applications. It enables a host to transmit and receive data over Ethernet in compliance with IEEE 802.3 standards. The native application interface of XLGMAC-CORE enables easy integration with 40-gigabit host applications.

The XLGMAC subsystem provides a 40-Gigabit Media-Independent Interface (XLGMII, an IEEE 802.3ba-2010 compliant reconciliation sub-layer) for communication with the 40-Gigabit PHY and a GMII interface for integration with the 1-Gigabit PHY. The XGMAC IP also provides an optional Management Data Input/Output (MDIO) interface capable of addressing MDIO devices that comply with Clauses 22 or 45 of 802.3-2008 standards.

General Features

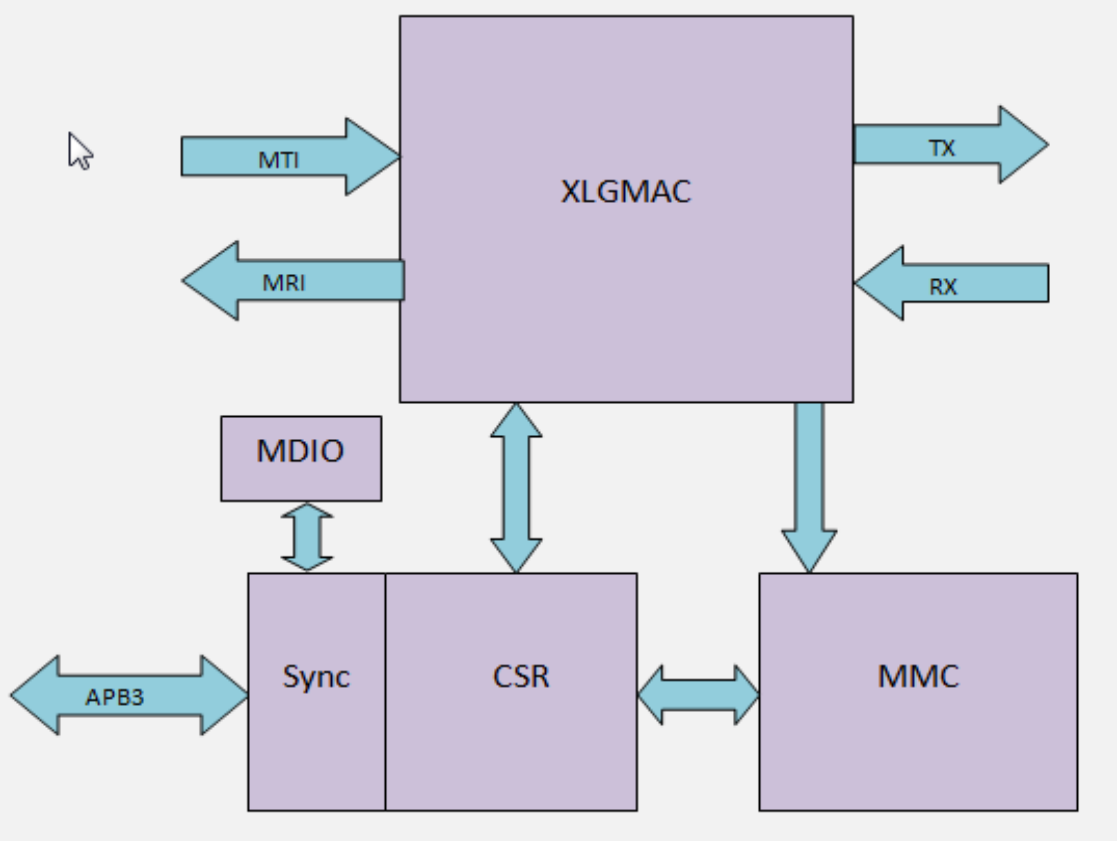
- IEEE Std 802.3ba-2010 support
- Clause 78 of IEEE Std 802.3az-2010 (Energy Efficient Ethernet) support
- AMBA 3.0 for APB3 slave ports
- IEEE Std 802.1Q-2010 (Virtual Bridged Local Area Networks) support
- QinQ Double VLAN tag inclusion, replacement, and detection on the transmit path and stripping in the receive path
- Separate transmission, reception, and control interfaces
- 32-bit CRC generation for transmit frames
- Per-frame CRC checking and stripping on the receive path
- Transmission padding for less than 64 bytes
- Support for Jumbo frames up to 9KB expandable up to 16KB
- Flow Control based on PAUSE packets and 802.3bd based PFC packets
- Classification of received traffic based on VLAN tag priority
- Flexible filtering schemes based on Ethernet DA, SA and VLAN fields of received packets
- Programmable source address inclusion and replacement for Transmit frames
- Optional Network statistics with RMON or MIB counters
- Detection of LAN Wake-Up frames and AMD Magic Packet frames during power-down mode
- Loopback capability at XLGMII/GMII
- Configurable big-endian or little-endian support for transmission and reception data paths

PHY Interface Features

- IEEE Std 802.3ba-2010 (Clause 81) XLGMII
- IEEE Std 802.3-2008 (Clause 46) XGMII
- IEEE Std 802.3-2008 (Clause 35) GMII Interface

Application Interface Features

- The following application interfaces are configurable:
  - XLGMAC-only with native interface



The dwc_ether_xgmac datasheet is available at:
https://www.synopsys.com/dw/doc.php/ds/c/dwc_ether_40g_mac.pdf

dwc_ether_pcs

Ethernet PCS Core

The DesignWare Ethernet PCS Core implements the Ethernet PCS Layer which is located between the MAC and the PHY. The DesignWare Ethernet PCS Core interfaces with the MAC or XGMAC through GMII or XGMII interface. The DesignWare Ethernet PCS Core interfaces with a PHY to support the following physical links:

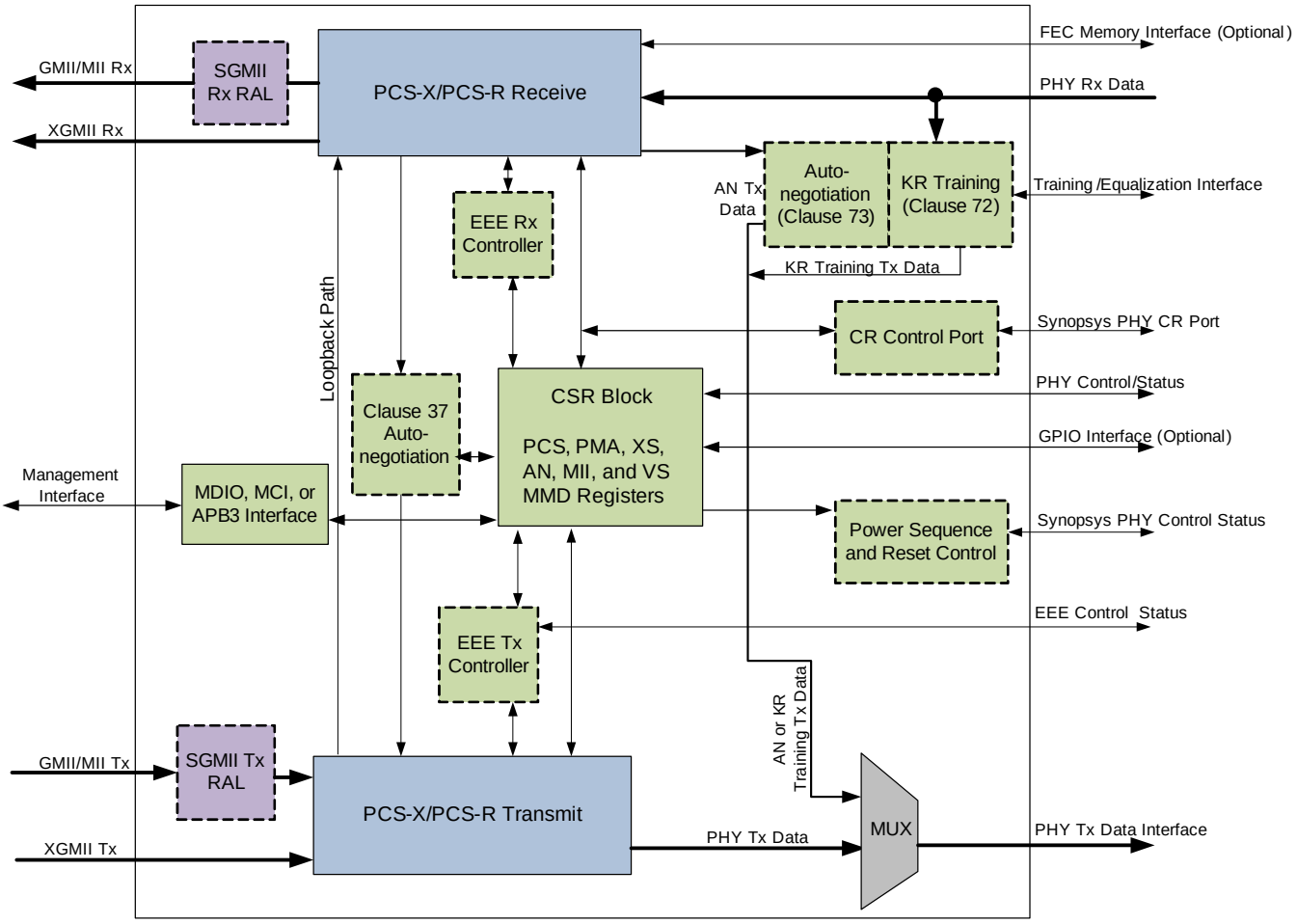
- XAUI or RXAUI
- 1000Base-X or SGMII
- 10GBASE-CX4, 10GBASE-KX4, 10GBASE-KR, 1000BASE-KX
- 10GBASE-R, 10GBASE-LR, 10GBASE-SR, 10GBASE-ER, 10GBASE-LRM

The DesignWare Ethernet PCS Core supports the Clause 37 auto-negotiation for 1000BASE-X or SGMII mode and Clause 73 auto-negotiation for Backplane Ethernet 1000BASE-KX, 10GBASE-KX4, and 10GBASE-KR modes.

dwc_ether_pcs
Ethernet PCS Core

Features

- Compliant with the following IEEE Standards:
  - IEEE Std 802.3-2008 Clause 35, 36, 37, 45, 46, 47, 48, 49, 69, 72, 73, and 74
  - IEEE Std 802.3az-2010
  - RXAUI - Reduced Pin XAUI specification, Dune Networks, January 2008
  - RXAUI Interface and RXAUI Adapter Specifications, Marvell, June 2008
  - Serial-GMII (SGMII) Specification, Revision 1.8, Cisco Systems
  - AMBA 3 APB Protocol, version 1.0, ARM Limited
- Configurable MAC Interface:
  - GMII (1G) or XGMII (10G) interface
  - SDR, DDR, or DDW with XGMII interface
- Configurable Management Interface:
  - MDIO
  - MCI
  - AMBA APB3
- Supported configurations:
  - XGXS PCS
  - 10GBASE-X PCS
  - Backplane Ethernet PCS
  - 1000BASEX-Only PCS
  - 10GBASE-R PCS
- Supported Backplane Ethernet PCS modes:
  - KX4_KX
  - KX4_Only
  - KX_Only
  - KR_KX4_KX
  - KR_KX4
  - KR_KX
  - KR_Only
- Energy Efficient Ethernet support
- Configurable (Synopsys or Non-Synopsys) PHY support (Gen1, Gen2, Gen4, and Gen5 10G PHY)
- Forward Error Correction (FEC) block support in KR mode
- Clause 72 Training support in KR Mode
- Clause 73 Auto-negotiation support
- Optional support for Clause 37 auto-negotiation in KX mode
  - Standard PCS MMD
  - Standard PMA/PMD MMD
  - Standard AN MMD
  - Vendor-Specific MII MMD
  - Vendor Specific Control MMD
- Supports 16,20,32,33 and 66-bit Gear Box Interface in 10GBASE-R and 10GBASE-KR modes.
- Encoding or decoding of GMII or XGMII data:
  - 64/66 in 10GBASE-R and 10GBASE-KR modes
  - 8b/10b in other modes
- Code-group boundary detection on the Receive path
- Synchronization, Block Lock, and Bit Error Rate (BER) monitoring on the Receive path
- Skew removal on incoming data from multiple lanes
- Support for Clock Rate Compensation to enable MAC or XGMAC to work in single clock domain
- Test pattern generation, test pattern checking, and error monitoring support for debugging
- Receive to Transmit loopback support for debugging
- Clock gating support to save power when the MAC initiates Energy Efficient Ethernet (EEE) mode
- Rapid FEC Block Lock support to enable fast synchronization in the Receive path during EEE mode



The Ethernet PCS datasheet is available at:

http://www.synopsys.com/dw/doc.php/ds/c/dwc_ether_xgxs_pcs.pdf

dwc_xlgpcs

Enterprise Ethernet PCS Core

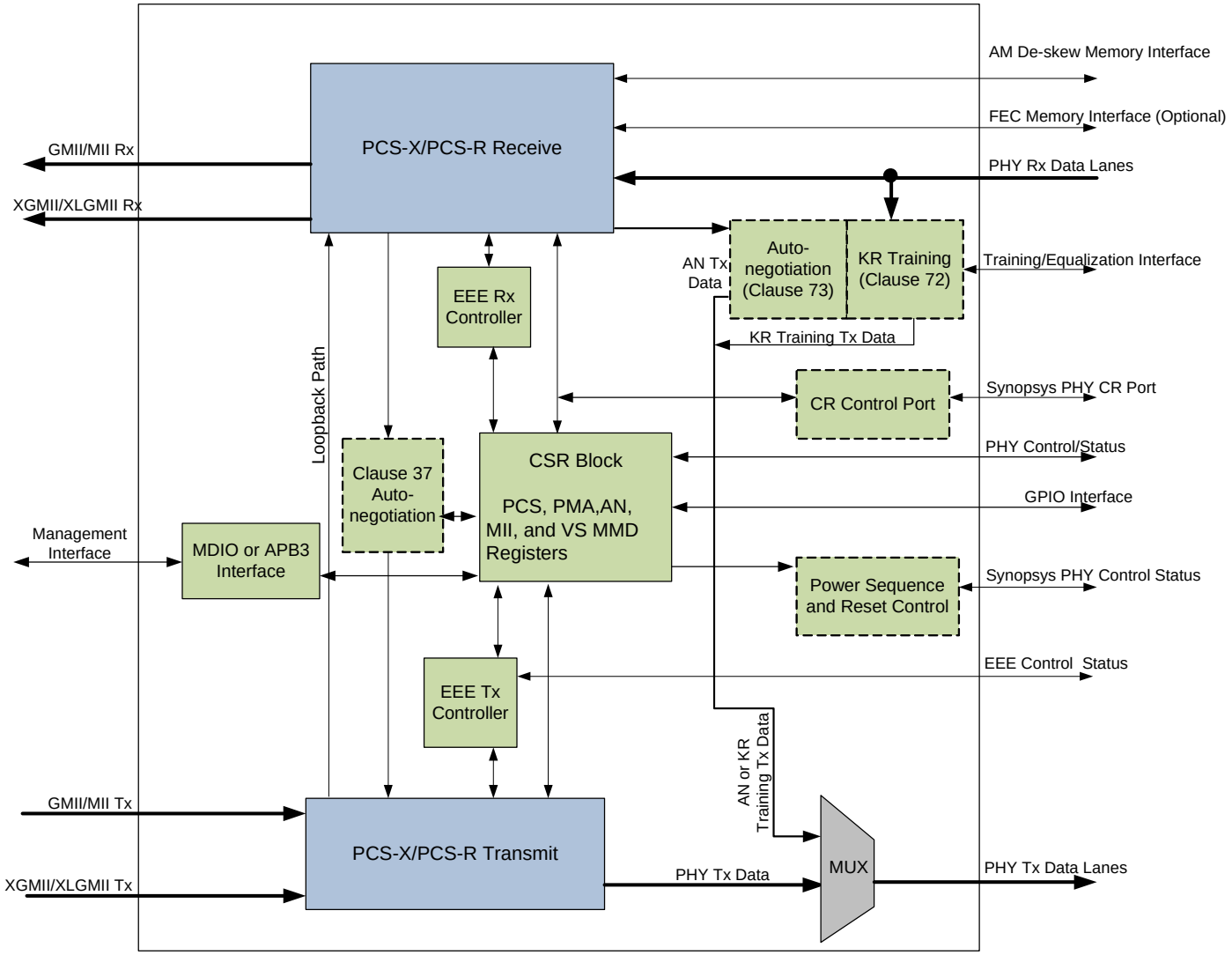
The DesignWare Cores Enterprise Ethernet PCS core (DWC_xlgpcs) provides a solution to implement the Ethernet PCS layer targeted to work at 40G link speeds. DWC_xlgpcs implements the Enterprise Ethernet PCS layer, which is located between the 40GMACand the PHY layer. The DesignWare Cores Enterprise Ethernet PCS core interfaces with a PHY to support the following physical links:

- 40GBASE-R/ 40GBASE-KR4
- 20GBASE-KR2
- 10GBASE-KR
- 10GBASE-KX4
- 1000BASE-KX
- XAUI or RXAUI
- SGMII

The DesignWare Enterprise Ethernet PCS Core supports the Clause 37 auto-negotiation for 1000BASE-X and SGMII mode and Clause 73 auto-negotiation for Backplane Ethernet 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, and 40GBASE-KR4 modes.

Features

- Compliant with the following IEEE Standards:
  - IEEE Std 802.3-2008 Clause 35, 36, 37, 45, 46, 47, 48, 49, 69, 72, 73, and 74
  - IEEE Std 802.3az-2010
  - IEEE Std 802.3ba-2010
  - RXAUI - Reduced Pin XAUI specification, Dune Networks, January 2008
  - RXAUI Interface and RXAUI Adapter Specifications, Marvell, June 2008
  - Serial-GMII (SGMII) Specification, Revision 1.8, Cisco Systems
  - AMBA 3 APB Protocol, version 1.0, ARM Limited
- Supported MAC Interface:
  - For 40G (40GBASE-R, KR4) - XLGMII Interface (128-bit interface)
  - For 10G (KX4, KR) - XGMII Interface (32-bit interface)
  - For 1G - GMII Interface
- Configurable Management Interface:
  - MDIO
  - AMBA APB3
- Support for Vendor-Specific 20GBASE-KR2 mode to allow interface with 2-lane PMA, with each lane operating at a speed of 10Gbps
- Energy Efficient Ethernet support as per 802.3az-2010 for 1G and 10G speed modes
- Vendor-specific EEE approach to save power in KR4 Mode
- Configurable (Synopsys or Non-Synopsys) PHY support (Gen5 10G PHY)
- Forward Error Correction (FEC) block support in KR/KR4 mode
- Clause 72 Training support in KR/KR4 Mode
- Supports Alignment Marker Insertion in 40G and 20G Modes at programmable intervals
- Clause 73 Auto-negotiation support
- Optional support for Clause 37 auto-negotiation in KX mode
- Supports multiple MMDs:
  - Standard PCS MMD
  - Standard PMA/PMD MMD
  - Standard AN MMD
  - Vendor-Specific MII MMD
  - Vendor Specific Control MMD
- Supports 16,20,32,33 and 66-bit Gear Box Interface in 10GBASE-KR and 40GBASE-KR4 modes.
- Encoding or decoding of GMII, XGMII, or XLGMII data:
  - 64/66 in BASE-KR and BASE-KR4 modes
  - 8b/10b in other modes
- Code-group boundary detection on the Receive path
- Synchronization, Block Lock, and Bit Error Rate (BER) monitoring on the Receive path
- Skew removal on incoming data from multiple lanes
- Support for Clock Rate Compensation to enable MAC, XGMAC, or XLGMAC to work in single clock domain
- Test pattern generation, test pattern checking, and error monitoring support for debugging
- Receive to Transmit loopback support for debugging
- Clock gating support to save power when the MAC initiates Energy Efficient Ethernet (EEE) mode
- Rapid FEC Block Lock support to enable fast synchronization in the Receive path during EEE mode



The Enterprise Ethernet PCS datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_ether_40g_pcs.pdf

dwc_ether_qos

Ethernet Quality-of-Service Core

The DesignWare Ethernet Quality-of-Service (QoS) core implements the link layer of an OSI Ethernet system. The Ethernet QoS core enables transmission of time-synchronized and low-latency Audio-Video data over Ethernet networks. The Ethernet QoS core is composed of three main layers: the Gigabit Ethernet Media Access Controller (GMAC), the MAC Transaction Layer (MTL), and the MAC DMA Controller (MDC). Other features include the following:

General Features

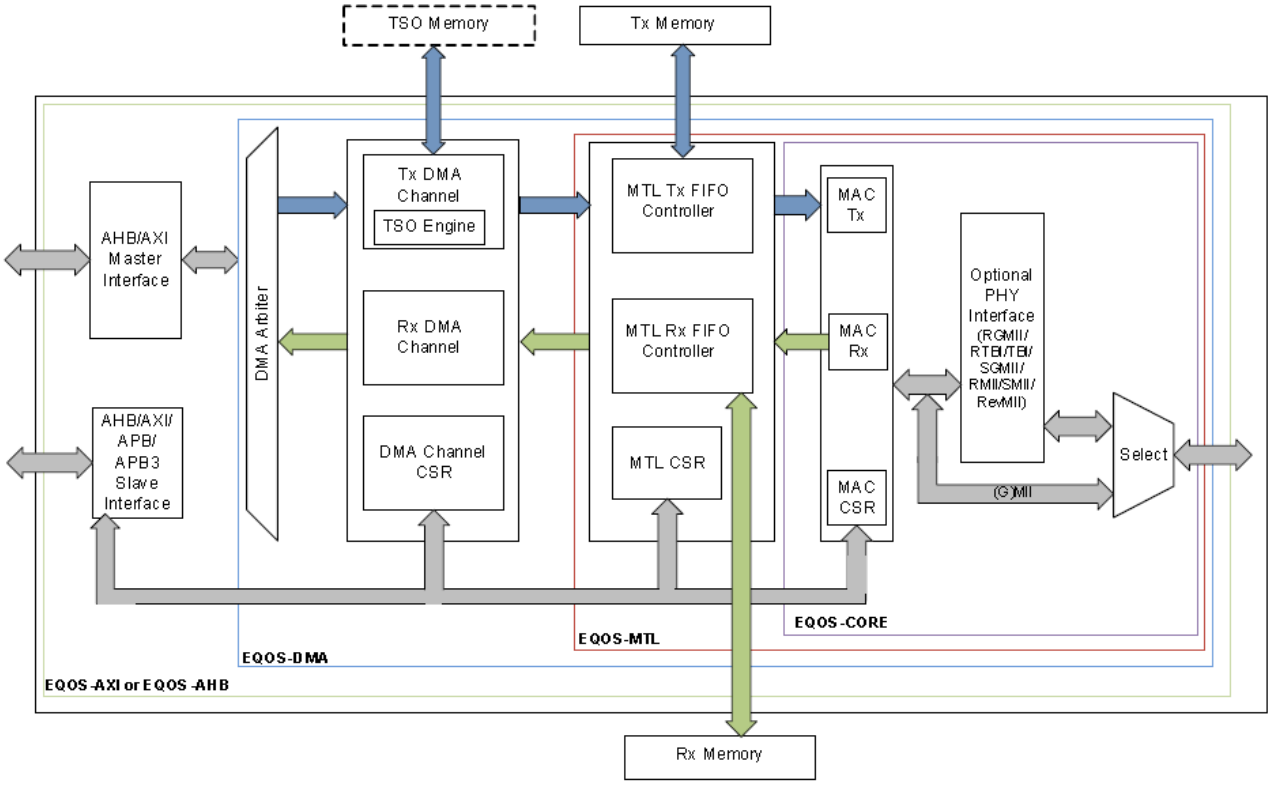
- Complies with the following standards:
  - IEEE Std 1588-2008 Precision Clock Synchronization
  - IEEE 802.3-2008 specification
- Supports IEEE Std 802.1-AS-2011 and IEEE Std 802.1-Qav-2009 for Audio Video (AV) traffic
  - Separate channels or queues for AV data transfer in the 100 Mbps and 1000 Mbps modes.
  - Up to eight queues on the Receive paths for AV traffic and seven queues on the Transmit path for AV traffic
  - IEEE 802.1-Qav specified credit-based shaper (CBS) algorithm for the additional transmit channels.
  - Single Tx FIFO and Rx FIFO memory for all selected queues (system-side interface [AHB, AXI, or native] remains the same)
- IEEE Std 1801-2009 (Unified Power Format)
- IEEE Std 802.3az-2010 standard for Energy Efficient Ethernet (EEE)
- CSMA/CD protocol for half-duplex operation
- Full-duplex flow control operations (IEEE 802.3x Pause packets, and IEEE 802.1Qbb-2011 and IEEE 802.3bd-2011 for Priority flow control)
- Packet bursting and packet extension in 1000-Mbps half-duplex mode
- Variety of flexible address filtering modes based on Layer 2, Layer 3, or Layer 4 packet fields.
- Complete network statistics (optional) with RMON/MIB counters (RFC2819/RFC2665)
- Optional module for Remote Wake-Up frames and AMD Magic Packet frames
- Receive and Transmit Checksum Offload for IP and TCP/UDP packets
- TCP/IP Segmentation Offload function in Transmit
- Receive Layer 3 and Layer 4 based packet filtering
- Optional ARP Offload engine and PTP packet offload engine
- Supports QinQ VLAN tags for filtering, stripping in Receive path and insertion or replacement in Transmit path
- Supports Source Address insertion of replacement in Transmit
- Transmit Source Address and VLAN Tag insertion or replacement

PHY Interface Features

- IEEE Std 802.3-compliant GMII and MII interfaces
- IEEE Std 802.3z-compliant TBI and RTBI interfaces with auto-negotiation support
- SGMII, RGMII, RMII, Serial-MII (SMII), and Reverse MII (RevMII) interfaces
- MDIO Master interface (optional) for PHY device configuration and management

Application Interface Features

- The following application interfaces are configurable:
  - GMAC-only with native interface
  - GMAC with MTL native interface
  - DMA with native interface
  - DMA with AHB interface
  - DMA with AXI interface
- Data interface, configurable to support FIFO, native DMA, and AXI or AHB interfaces
- CSR interface configurable to AHB, AXI, APB, or APB 3 Slave interface



The dwc_ethernet_qos datasheet is available at:

http://www.synopsys.com/dw/doc.php/ds/c/dwc_ether_qos.pdf

dwc_xaui_phy
XAUI PHY IP

The DesignWare XAUI PHY IP is designed for use in any networking or high-end, computing SoC solutions. Designed for the latest high-speed backplanes, the DesignWare XAUI PHY supports the 10-gigabit Ethernet standards that are commonly used in high-speed communications applications. Based on Synopsys's silicon-proven and award-winning high-speed SERDES technology, the XAUI PHY provides a cost-effective and extremely low-power solution designed to meet the needs of today's XAUI designs.

Designed for advanced manufacturing processes, the XAUI PHY is targeted to popular low-power and high-performance CMOS digital logic processes. The XAUI PHY integrates high-speed mixed-signal custom CMOS circuitry compliant with the XAUI IEEE base specification 802.3ae. While extremely low in power consumption and area requirements, the DesignWare XAUI PHY substantially exceeds the electrical specifications in key performance areas such as jitter and receiver sensitivity.

To handle increasing communication system speeds, the XAUI standard was designed to take a 10-Gbps serial stream and divide it into four 2.5-Gbps serial streams that run over copper traces and chip-to-chip connections using 8b10b coding at 3.125 Gbaud. By taking advantage of copper links, higher performance communications applications can be cost effectively deployed.

Features

- Supports 10GBASE-CX4
- Transmits 3.125 Gbps differential NRZ serial stream
- Receives 3.125 Gbps differential NRZ serial stream
- Supports asynchronous operation
- Supports both 10-bit and 20-bit parallel ASIC interfaces
- Supports popular data rates: 3.125 Gbps, 3.0 Gbps, 2.5 Gbps, 1.5 Gbps, and 1.25 Gbps
- Provides on-die scope and diagnostics for fast system verification
- Small, cost-effective die size
- Supports popular 130-nm, 90-nm, and 65-nm common platform processes
- Supports 4x and 8x lane widths
- Supports many reference clock frequencies: 25 MHz–156.25 MHz, including popular 125-MHz and 156.25-MHz clocks
- Interoperable with the Synopsys DesignWare XGXS-PCS IP
- Provides flexible Tx pre-emphasis and Rx equalization settings to support a variety of lossy channels

Performance

- Low-jitter PLL technology with excellent supply isolation
- Low-offset, high-sensitivity receiver with high resolution CDR
- Robust PHY architecture, tolerates wide PVT variations
- Short training sequences and fast transitions between power states enable highly efficient operation
- ± 10% supply variation
- Excellent performance margin and receive sensitivity
- Very low power design — down to half the power compared to conventional PHYs

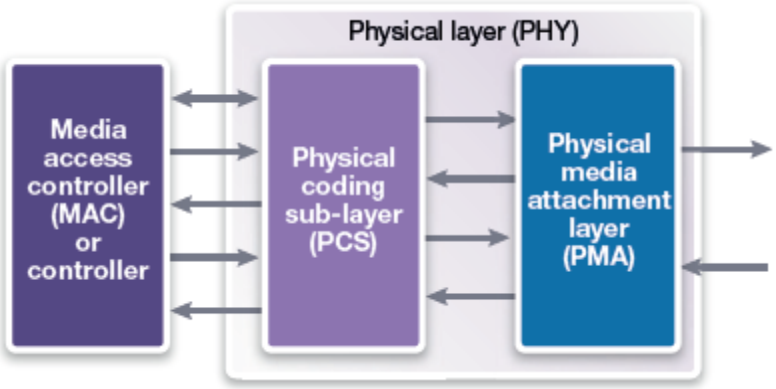
The DesignWare dwc_xaui_phy datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_xaui_phy.pdf

dwc_12g_phy
Enterprise 12G PHY

The multi-channel, multi-protocol DesignWare Enterprise 12G PHY IP is part of Synopsys' high-performance multi-rate transceiver portfolio, meeting the growing needs for high bandwidth in enterprise applications. Using leading-edge design, analysis, simulation, and measurement techniques, the Enterprise 12G PHY delivers exceptional signal integrity and jitter performance that exceeds the standards' electrical specifications. The PHY is small in area and provides a low-power, cost-effective solution that supports multiple industry standards to meet the needs of applications with high-speed port side, chip-to-chip, board-to-board, and backplane interfaces.

The transmitter and receiver equalizers enable customers to control and optimize signal integrity and at-speed performance. The high-performance analog front-end incorporates power saving features in both active and standby modes of operation. The hybrid transmit drivers support low power voltage mode and high swing current mode, with optional I/O supply under drive. The embedded BER tester and internal eye monitor provide on-chip testability and visibility into channel performance. The PHY integrates seamlessly with the DesignWare Physical Sublayer cores and the digital controllers/media access controllers (MACs) to reduce design time and to help designers achieve first-pass silicon success. These features reduce both product development cycles and the need for costly field support.

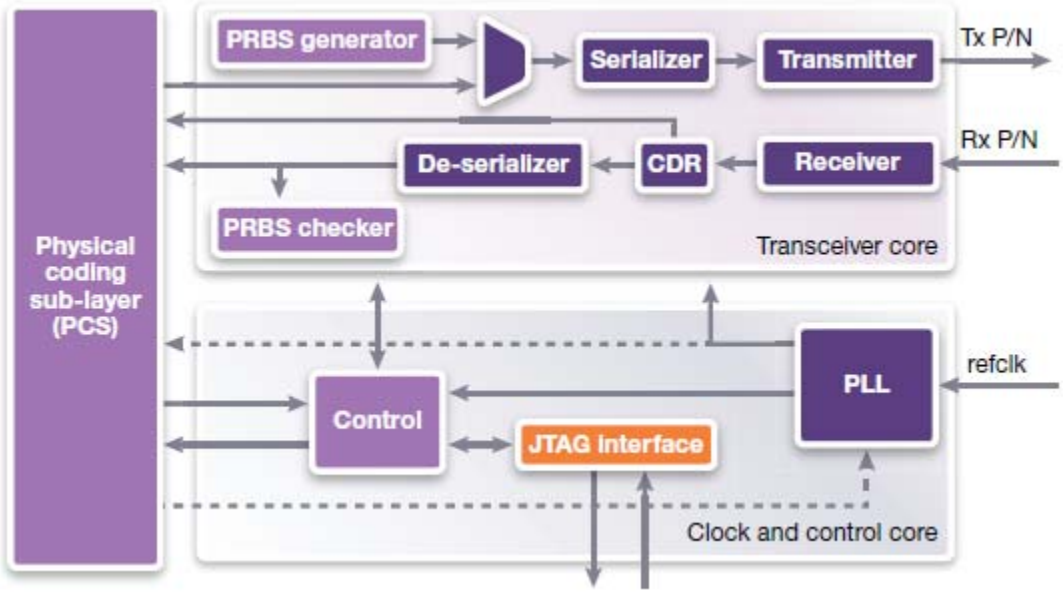


The multiprotocol DesignWare Enterprise 12G PHY is architected to address designers' growing performance/power trade-off challenges. It includes one, two or four full-duplex transceivers (transmit and receive functions) as well as the relevant physical coding sublayer (PCS) block that is needed for the PCIe 3.0, SATA and 10GBASE-R encoding, backchannel initialization, aggregation, bifurcation, and power management.

The multi-channel PHY shares a single clock and support core. The core provides the high-speed serial and low-speed parallel clocks to both the transceiver and the PCS. Both the internal and external reference clock connections to the PHY are supported.

The combination of the multi-featured transmitter and receiver equalization are beneficial to both port side and to legacy backplane applications. This improves Rx jitter tolerance, supports a wider range of board layout designs, improves immunity to interference (cross talk), and reduces design constraints on board signal paths. In addition, Synopsys' PHY IP equalization design reduces power consumption.

The following illustrates a simplified single-channel PHY block diagram.



The product datasheet can be downloaded from the following site:

http://www.synopsys.com/designware

Highlights

- Single, dual and quad channels
- IEEE 802.3 10G and 40G backplane (XAUI, KR & KR4), port side 40G, 100G (CR4 & CR10), and 10G (XFI, SFF-8431/SFI)
- IEEE 802.3az Electrical Energy Efficient
- SGMII, and QSGMII
- PCI-SIG PCI Express (PCIe) 3.0/2.1/1.1
- SATA 6G/3G/1.5G (Rev 3.2)
- OIF CEI-6G and CEI-11G
- CPRI, OBSAI, JESD204B
- Aggregation (x2 to x16) & bifurcation
- Auto-negotiation (AN) and optional forward error correction (FEC)
- L1 substate power management and SRIS
- Multi-tap adaptive and configurable continuous time linear equalizer (CTLE) and decision feedback equalization (DFE)
- Embedded bit error rate (BER) tester and internal eye monitor
- Built-in self test (BIST) including 7-, 9-, 11-, 15-, 23-, and 31-bit pseudo random bit stream (PRBS) generation and checker
- IEEE 1149.6 AC Boundary Scan

dwc_mobile_storage
Mobile Storage Host Controller

DWC_mobile_storage Features

- Supports:
  - Secure Digital memory protocol commands
  - Secure Digital I/O protocol commands
  - Multimedia Card protocol commands
  - CE-ATA digital protocol commands
  - Command Completion signal and interrupt to host processor
  - Command Completion Signal disable feature
- The following features of eMMC 5.0 are supported:
  - DDR Data sampling method
  - Support for card clock frequency (cclk_in) up to 200 MHz
  - Only 8-bit bus width is supported in HS400 mode
  - Register programming for signaling levels of 1.8V and 1.2V IO voltage
  - Support for Block length of 512 Bytes

Internal DMA Block Features

- Supports 16/32/64-bit data transfers
- Single-channel; single engine used for Transmit and Receive
- Fully synchronous design operating on a single system clock
- Dual-buffer and chained descriptor linked list
- Descriptor architecture allows large blocks of data transfer with minimum CPU intervention
- Comprehensive status reporting for normal operation and transfers with errors
- Programmable burst size for optimal host bus utilization
- Programmable interrupt options for different operational conditions

AHB Master Interface Features

- Supports 16/32/64-bit data
- Supports split, retry, and error AHB responses
- Configurable Little-Endian or Big-Endian mode
- Selection of AHB burst type through software

Bus Interface Features

- Supports either AMBA AHB or APB interface
- Supports data widths of 16, 32, or 64 bits
- Supports optional external DMA controllers for data transfers
- Provides these types of DMA interfaces:
  - Interface to DW_ahb_dmac DMA controller
  - Generic DMA interface with dedicated bus
  - Interface to non-DesignWare DMA controller
- Supports pin-based Little-endian or Big-endian modes of AHB operation
- Supports separate clocks for bus interface and card interface for ease of integration
- Supports combined single FIFO for both transmit and receive operations
- Supports configurable FIFO depths of 8 to 4096
- FIFO controller shipped with a register-based single clock, dual-port synchronous read, and synchronous write RAM
- Supports FIFO overrun and under-run prevention by stopping card clock

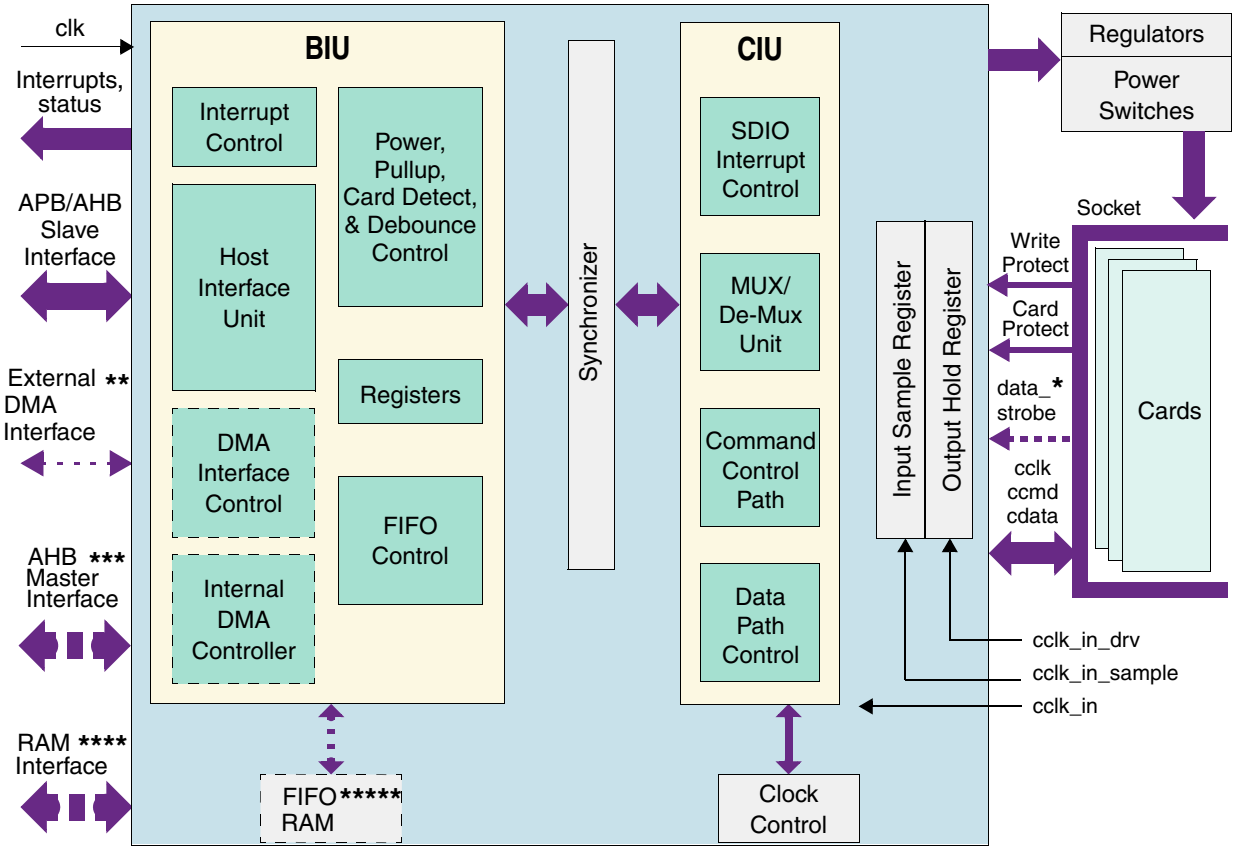
Card Interface Features

- Can be configured as MMC-Ver3.3-only controller or SD_MMC controller
- Supports 1 to 30 cards in MMC-Ver3.3-only mode, and 1 to 16 SD or MMC (3.3 or 4.0) or eMMC (4.41 onwards) or CE-ATA devices in SD_MMC_CE-ATA mode
- Supports Command Completion Signal and interrupts to host
- Supports Command Completion Signal disable
- Supports CRC generation and error detection
- Supports programmable baud rate
- Supports up to 4 clock dividers to support simultaneous operation of multiple cards with different clock speed requirements
- Provides individual clock control to selectively turn ON or OFF clock to a card

- Supports host pull-up control
- Supports card detection and initialization
- Supports write protection
- Supports SDIO interrupts in 1-bit and 4-bit modes
- Supports HS400 mode, as defined by eMMC 5.0

Verification Environment Features

- AMBA, SD memory, SDIO, and MMC verification IP (VIP) and AHB verification IP (VIP)
- SDMMC VIP supports only Vera and Verilog; support for System Verilog, VHDL and C are not provided
- Configurable and self-checking testbench and test suites in sample Verilog testbench



* Available only when SUPPORT_HS400=1
** Optional External DMA Interface; present only if internal DMAC is *not* present
*** Optional AHB/APB Master Interface; present only if internal DMAC is present
**** Optional RAM Interface
***** FIFO RAM can be chosen as either internal or external RAM

- optional

Note: The card_detect and write-protect signals are from the SD/MMC card socket and not from the SD/MMC card.

The DesignWare DWC_mobile_storage datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_mobile_storage.pdf

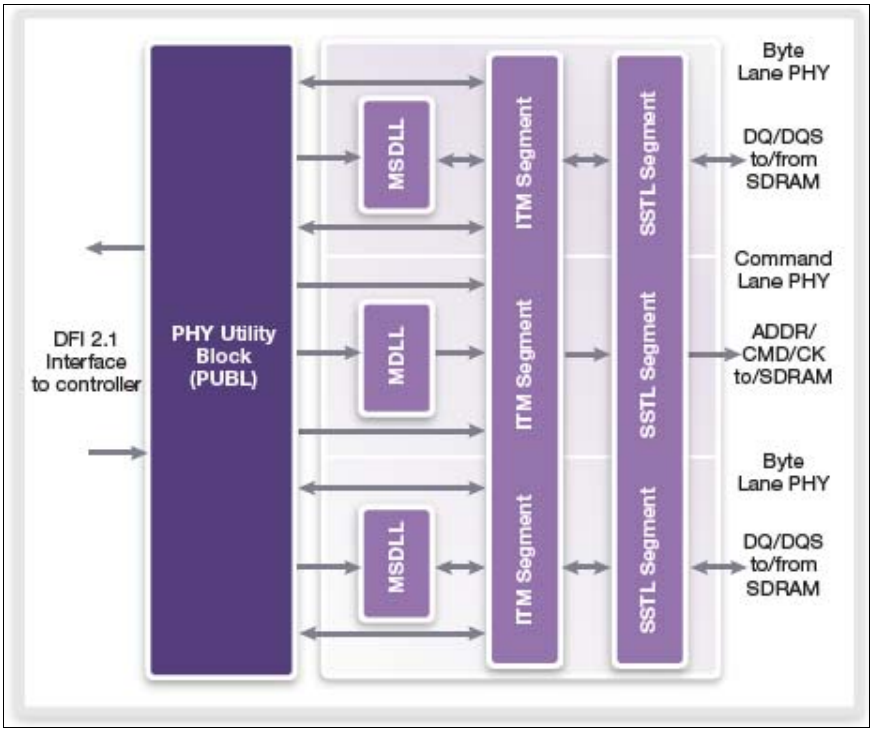
dwc_ddr2_3l_mddr_phy

DDR2/3-Lite/mDDR PHY

The DesignWare DDR2/3-Lite/mDDR PHY is a complete, silicon-proven, physical (PHY) layer IP interface solution for ASICs, ASSPs, System-on-Chip (SoC) and System-in-Package applications requiring high-performance LPDDR/Mobile DDR (mDDR)/DDR2/DDR3/DDR3L* SDRAM interfaces operating at up to 1066Mbps. The DesignWare DDR2/3-Lite/mDDR IP is ideal for systems that do not require the higher performance capability of DDR3. It is targeted at designs that are initially going to market using DDR2 IP with the ability to transition to DDR3 IP, should the equivalent DDR3 products become more cost effective. In addition, with full support of mDDR SDRAMs from 0 to 400Mbps, the DDR2/3-Lite/mDDR IP offers mDDR only interface capability or the ability to combine mDDR along with DDR2 and/or DDR3 for chips targeting multiple applications.

Optimized for low area and power, the DesignWare DDR2/3-Lite/mDDR SDRAM PHY is provided as a "hard" DDR PHY that is primarily delivered as GDSII and includes the application specific I/Os supporting mDDR, DDR2, DDR3 and DDR3L* (1.35V DDR3) SDRAMs. The advantage of the hard PHY approach is that difficult timing closure often encountered with "soft" RTL-based DDR PHYs is avoided. The high quality, silicon-proven DDR2/3-Lite/mDDR PHY enables designers to focus on product differentiation and not on the memory subsystem design issues that are present as data rates exceed 667Mbps, thus significantly reducing design integration risk and accelerating overall development time.

Supporting the GDSII based PHY is the RTL-based PHY Utility Block ("PUBL") that features Process, Voltage and Temperature (PVT) compensation logic, calibration logic, test logic and a DFI 2.1 interface to the memory controller.



The product datasheet can be downloaded from the following site:

http://www.synopsys.com/designware

Highlights

- Supports JEDEC standard DDR2,DDR3, DDR3L* (1.35V DDR3) and LPDDR/Mobile DDR SDRAMs
- Supports data rates from 0 to1066Mbps
- GDSII-based “hard” PHY avoids timing closure problems common with “soft” RTL-based DDR PHYs
- Designed for rapid integration with Synopsys Protocol or Memory controller for a complete DDR interface solution
- Includes application specific DDR I/Os including programmable drive strength and ODT
- DFI 2.1 compliant controller interface

Features

- Operating range of 100MHz (200Mbps) to 533MHz (1066Mbps) in DDR2, DDR3 and DDR3L* modes
- Operating range of DC to 200MHz in Mobile DDR mode
- PHY includes PVT compensated I/Os that are compatible with wire bond, CUP and flip chip (ESD included)
- Small PHY area – e.g., 0.87mm2 for a 16-bit PHY in 40nm (including I/Os)
- Low power – e.g., below 300mW for a 16-bit PHY with DDR3 SDRAMs, below 60mW for a 16-bit PHY with mDDR SDRAMs
- Configurable external memory channel widths in 8-bit increments from 8 to 72-bits
- Permits operating with a narrower memory channel than the implemented memory channel width (for example, an SoC supporting a 32-bit memory channel can optionally operate with a 16-bit channel)
- Programmable I/O output drive strength and On Die Termination (ODT) impedance with dynamic PVT compensation
- Embedded Dynamic Drift Detection in the PHY to facilitate Dynamic Drift Compensation for gating the data strobe input buffer during read operations
  - Squelches noise on the data strobes
- Utilizes low-jitter analog Master and Slave DLLs for precise timing management
  - Accurate data strobe placement in data eyes that is immune to voltage and temperature variation
- Library-based hard PHY to permit maximum flexibility while ensuring high data rates
- Flexible I/O ring design permitting exact match to the end system requirements (e.g., straight PHY or can go around a corner, flexible power to signal ratio, number of core power supply pins, number of ranks supported, channel width, number of address pins, etc.)
- PHY deliverables include GDSII database, IBIS models for I/Os, HSPICE netlists for I/O cells, timing models (.lib files), LEF files, LVS netlist, databook, physical implementation guide, application notes, example placement scripts, Verilog netlists and an FPGA emulation PHY example design (available upon request)
- PUBL deliverables include Verilog RTL, databook, synthesis and STA constraints and scripts, verification environment and sample test cases

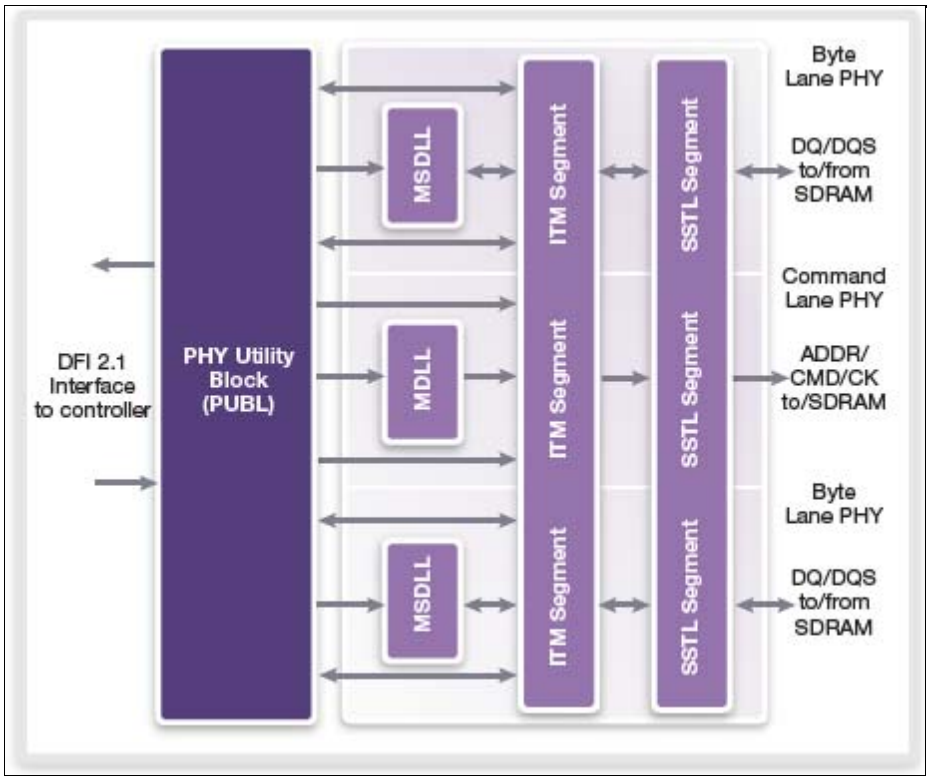
dwc_ddr2_ddr_phy
DDR2/DDR PHY

The DesignWare DDR2/DDR PHY is a complete, silicon-proven, physical (PHY)

layer IP interface solution for ASICs, ASSPs, System-on-Chip (SoC) and System-in-Package applications requiring high-performance DDR2/DDR SDRAM interfaces operating at up to 1066Mbps. The DesignWare DDR2/DDR IP is ideal for systems that do not require the higher performance capability or higher capacity DRAMs offered with DDR3 SDRAMs.

Optimized for low area and power, the DesignWare DDR2/DDR SDRAM PHY is provided as a "hard" DDR PHY that is primarily delivered as GDSII and includes the application specific I/Os supporting DDR2 and DDR SDRAMs. The advantage of the hard PHY approach is that difficult timing closure often encountered with "soft" RTL-based DDR PHYs is avoided. The high quality, silicon-proven DDR2/DDR PHY enables designers to focus on product differentiation and not on the memory subsystem design issues that are present as data rates exceed 667Mbps, thus significantly reducing design integration risk and accelerating overall development time.

Supporting the GDSII based PHY is the RTL-based PHY Utility Block ("PUBL") that features calibration logic, test logic and a DFI2.1 interface to the memory controller.



The product datasheet can be downloaded from the following site:

http://www.synopsys.com/designware

Highlights

- Supports JEDEC standard DDR2 and DDR SDRAMs
- Supports data rates from 250 to 1066Mbps
- GDSII-based “hard” PHY avoids timing closure problems common with “soft” RTL-based DDR PHYs
- Designed for rapid integration with Synopsys Protocol or Memory controller for a complete DDR interface solution
- Includes application specific DDR I/Os including programmable drive strength and ODT
- DFI 2.1 compliant controller interface

Features

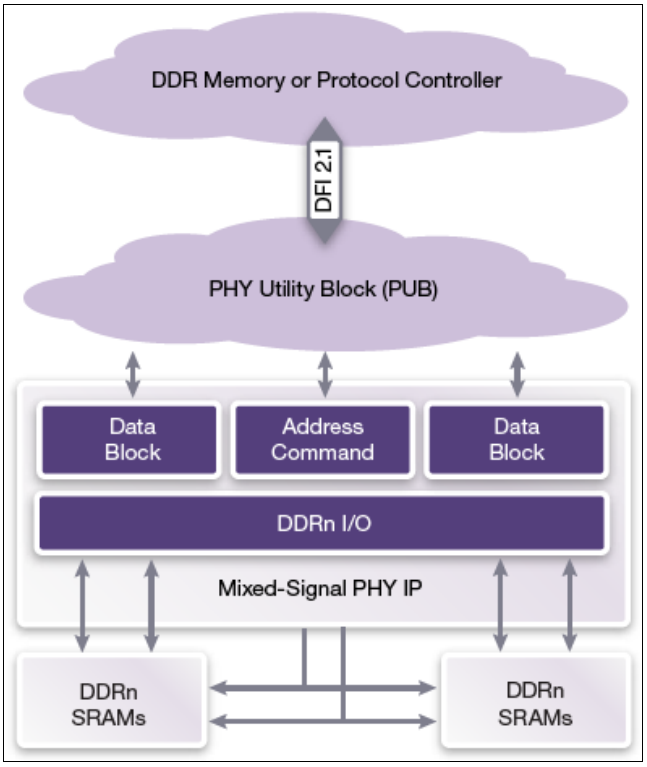
- Operating range of 125MHz (250Mbps) to 533MHz (1066Mbps) in DDR2 modes
- Operating range of 125MHz (250Mbps) to 200MHz (400Mbps) in DDR mode
- PHY includes I/Os that are compatible with wire bond, CUP and flip chip (ESD included)
- Small PHY area – e.g., 1.00mm2 for a 16-bit PHY in 65nm (including I/Os)
- Low power – e.g., below 450mW for a 16-bit PHY with DDR2 SDRAMs
- Configurable external memory channel widths in 8-bit increments from 8 to 72-bits
- Permits operating with a narrower memory channel than the implemented memory channel width (for example, an SoC supporting a 32-bit memory channel can optionally operate with a 16-bit channel)
- Programmable I/O output drive strength and On Die Termination (ODT) impedance
- Embedded Dynamic Drift Detection in the PHY to facilitate Dynamic Drift Compensation for gating the data strobe input buffer during read operations
  - Squelches noise on the data strobes
- Utilizes low-jitter analog Master and Slave DLLs for precise timing management
  - Accurate data strobe placement in data eyes that is immune to voltage and temperature variation
- Library-based hard PHY to permit maximum flexibility while ensuring high data rates
- Flexible I/O ring design permitting exact match to the end system requirements (e.g., straight PHY or can go around a corner, flexible power to signal ratio, number of core power supply pins, number of ranks supported, channel width, number of address pins, etc.)
- PHY deliverables include GDSII database, IBIS models for I/Os, HSPICE netlists for I/O cells, timing models (.lib files), LEF files, LVS netlist, databook, physical implementation guide, application notes, example placement scripts, Verilog netlists and an FPGA emulation PHY example design (available upon request)
- PUBL deliverables include Verilog RTL, databook, synthesis and STA constraints and scripts, verification environment and sample test cases

dwc_ddr3_ddr2_phy
DDR3/2 PHY

The DesignWare DDR3/2 PHY is a complete, silicon-proven, physical (PHY) layer IP interface solution for ASICs, ASSPs, System-on-Chip (SoC) and System-in-Package applications requiring high-performance DDR2/DDR3/DDR3L SDRAM interfaces operating at up to 2133Mbps. It includes full support of DDR2 SDRAMs from 667 to 1066Mbps for backwards compatibility and the ability to use either DDR2 and/or DDR3 SDRAMs for chips targeting multiple applications with varying performance requirements.

Optimized for high performance, low area, low power and ease of integration, the DesignWare DDR3/2 SDRAM PHY is provided as a "hard" DDR PHY that is primarily delivered as GDSII and includes the application specific I/Os supporting DDR2, DDR3 and DDR3L (1.35V DDR3) SDRAMs. The hard PHY approach avoids difficult timing closure often encountered with "soft" RTL-based DDR PHYs.

Supporting the GDSII based PHY is the RTL-based PHY Utility Block ("PUB") that includes PHY control features such as write leveling, data eye training, per-bit data deskew control, PVT compensation, and provides support for production testing of the DWC DDR3/2 PHY.



The product datasheet can be downloaded from the following site:

http://www.synopsys.com/designware

Highlights

- Supports JEDEC standard DDR3, DDR3L (1.35V DDR3) and DDR2 SDRAMs
- High performance DDR PHY supporting data rates from 667 to 2133Mbps
- GDSII based “hard” PHY avoids timing closure problems common with “soft” RTL-based DDR PHYs
- Designed for rapid integration with Synopsys Protocol or Memory controller for a complete DDR interface solution
- Includes application specific DDR I/Os including programmable drive strength and ODT
- DFI 2.1 compliant controller interface

Features

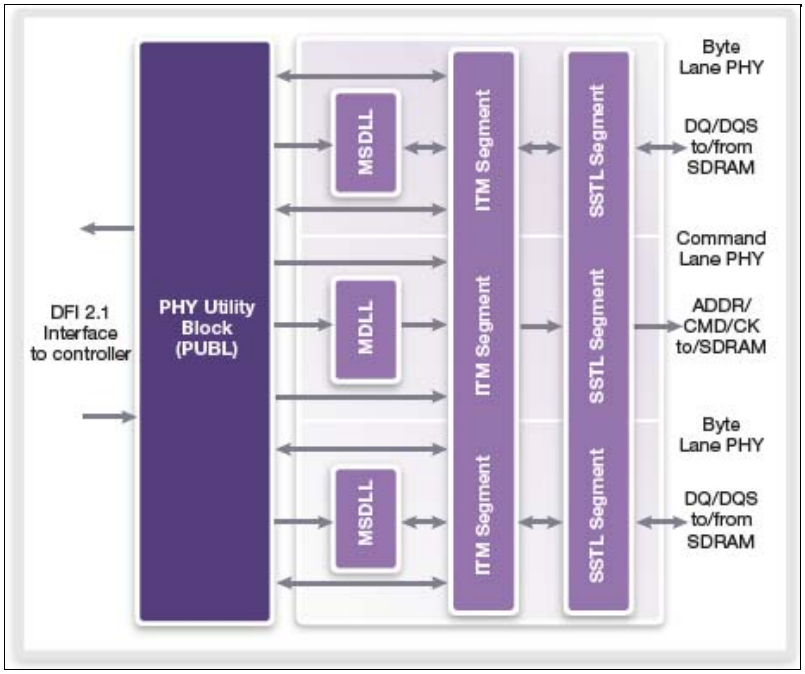
- Compatible with JEDEC standard DDR2/DDR3/DDR3L SDRAMs
- Operates from 667 to 1066Mbsp in DDR2 mode
- Operates from 667 to 2133Mbsp in DDR3 mode
  - Maximum data rate is process dependent
- DFI 2.1 compliant interface to the memory controller
- Small PHY area – e.g., <1.3mm2 for a 16-bit DDR3 PHY in 40nm (including I/Os)
- Low power – e.g., <350mW for a 16-bit PHY with DDR3 SDRAMs
- Configurable external memory channel widths in 8-bit increments from 8 to 72-bits
- Can operate with a narrower memory channel than the implemented width (for example, an SoC supporting a 32-bit memory channel can optionally operate with a 16-bit channel)
- Programmable I/O output drive strength and ODT impedance with dynamic PVT compensation
- Delivery of product as hardened IP components allows precise control of timing critical delay and skew paths
- Includes embedded timing circuits necessary to generate the clocks and strobes for the DRAM interface and meet the narrow timing specifications of DDR3 SDRAMs
- Multiple memory-rank support, up to four ranks
- Flexible I/O ring design permitting exact match to the end system requirements (e.g., straight PHY or can go around a corner, flexible power to signal ratio, number of core power supply pins, number of ranks supported, channel width, number of address pins, etc.)
- Supports DDR3 write leveling
- Write and read timing circuits compensate per-bit delay skew of up to 600ps
- Locally calibrated master and slave timing circuits minimize OCV and ACLV effects, and accommodate timing drift induced by voltage and temperature changes
- At-speed loopback testing on both the address and data channels
- PHY deliverables include GDSII database, IBIS models for I/Os, HSPICE netlists for I/O cells, timing models (.lib files), LEF files, LVS netlist, databook, physical implementation guide, application notes, example placement scripts, Verilog netlists and an FPGA emulation PHY example design (available upon request)
- PUB deliverables include Verilog RTL, databook, synthesis and STA constraints and scripts, verification environment and sample test cases

ddr_multi_phy
DDR multiPHY

Supporting data rates up to 1066 Mbps, the DesignWare DDR multiPHY supports a broad range of DDR SDRAM types such as LPDDR2 (“S2”, “S4” and non-volatile RAM), LPDDR/Mobile DDR (mDDR), DDR3, DDR3L (1.35V), and DDR2 in a single PHY. This allows the host SoC/ASIC to easily be configured for the specific DDR SDRAM variant used in the system via simple software control allowing one chip to target multiple applications using different DDR types. For low power applications, the DesignWare DDR multiPHY enables over twice the memory performance of LPDDR with full support for Low Power Double Data Rate 2 (LPDDR2) SDRAMs. LPDDR2 is the second generation low power DDR SDRAM standard targeting an extensive range of power-sensitive applications such as smart phones, PDAs, GPS units, personal media players and mobile internet devices.

The DesignWare DDR multiPHY features Delay Lock Loop (DLL) bypass modes for operation below 200 MHz as well as an I/O retention mode that allows the chip’s power supplies to be shut down completely while a small number of I/Os remain powered on to keep the external SDRAMs in self refresh mode. The DesignWare DDR multiPHY is also designed to support the anticipated DDR3U standard operating at 1.2 or 1.25V.

The DesignWare DDR multiPHY is primarily delivered as GDSII and includes the application specific, multi-protocol DDR I/Os supporting LPDDR2, mDDR, DDR2, DDR3, DDR3L and DDR3U SDRAMs. The advantage of the hard DDR multiPHY is that the critical physical chip layout of the PHY, including the application specific DDR I/Os and DLL circuits, is optimized for the lowest chip area and lowest power while offering full flexibility of the I/O ring design. In addition, the hard DDR multiPHY embeds the high-speed clock tree and flight time matched data buses to minimize timing skew, alleviating the complexities associated with these high speed paths. Supporting the DDR multiPHY is the RTL-based PHY Utility Block (“PUBL”) that features Process, Voltage and Temperature (PVT) compensation logic, calibration logic, test logic and a DFI 2.1 interface to the memory controller.



Highlights

- Supports JEDEC SDRAM standards including LPDDR2, LPDDR/Mobile DDR, DDR2, DDR3, DDR3L(1.35V) and DDR3U (1.2xV)
- Supports data rates from 0 to1066Mbps
- GDSII-based “hard” PHY avoid stiming closure problems common with “soft” RTL-based DDR PHYs
- Designed for rapid integration with Synopsys Universal DDR memory controller for a complete DDR interface solution
- Includes application specific, multi-protocol DDR I/Os including programmable drive strength and ODT
- DFI 2.1 compliant controller interface

Features

- Operating range of DC to 533MHz in LPDDR2 mode
- Operating range of DC to 200MHz in Mobile DDR mode
- Operating range of 100MHz (200Mbps) to 533MHz (1066Mbps) in DDR2 and DDR3 modes
- PHY includes PVT compensated I/Os that are compatible with wire bond, CUP and flip chip (ESD included)
- Small PHY area – e.g., <0.8mm2 for a 16-bit PHY in 40nm (including all I/Os)
- Low power – e.g., <60mW for a 16-bit LPDDR2 SDRAM PHY (including all I/Os) operating at 533Mbps
- Configurable external memory channel widths in 8-bit increments from 8 to 72-bits
- Permits operating with a narrower memory channel than the implemented memory channel width (for example, an SoC supporting a 32-bit memory channel can optionally operate with a 16-bit channel)
- Programmable I/O output drive strength and On Die Termination (ODT) impedance with dynamic PVT compensation
  - ODT is not required for Mobile DDR or LPDDR2 mode
- Embedded Dynamic Drift Detection in the PHY to facilitate Dynamic Drift Compensation for gating the DQS input buffer during read operations
  - Squelches noise on the data strobes
- Utilizes low-jitter analog Master and Slave DLLs for precise timing management
  - Accurate data strobe placement in data eyes that is immune to voltage and temperature variation
- Library-based hard PHY to permit maximum flexibility while ensuring high data rates and minimal die area
- Flexible I/O ring design permitting exact match to the end system requirements (e.g., straight PHY or can go around a corner, flexible power to signal ratio, number of core power supply pins, number of ranks supported, channel width, number of address pins, etc.)
- PHY deliverables include GDSII database, IBIS models for I/Os, HSPICE netlists for I/O cells, timing models (.lib files), LEF files, LVS netlist, databook, physical implementation guide, application notes, example placement scripts, Verilog netlists and an FPGA emulation PHY example design (available upon request)
- PUBL deliverables include Verilog RTL, databook, synthesis and STA constraints and scripts, verification environment and sample test cases

dwc_ddr_upctl, dwc_ddr_umctl, and dwc_ddr_umctl2

Universal DDR Protocol and Memory Controllers

The DesignWare Universal DDR controller family consists of high performance components: the Universal DDR Protocol Controller (uPCTL), Universal DDR Memory Controller (uMCTL), and Enhanced Universal DDR Memory Controller (uMCTL2). All are capable of controlling JEDEC standard DDR2, DDR3, Mobile DDR and LPDDR2 SDRAMs. The uMCTL2 supports the DDR4 JEDEC standard as well.

The uPCTL delivers efficient bandwidth with minimum latency and provides the designers with transparent access and complete control of the memory subsystem. The uPCTL serves the memory control needs of applications with simple transactions that do not require an internal scheduler, and can also be deployed with custom-designed memory management units. The uPCTL SoC application bus interface supports a lowest-latency "native application interface" (NIF).

The uMCTL is a multi-port memory controller which accepts memory access requests from up to 32 application-side host ports. Application-side interfaces can be connected to the uMCTL either through the standard AMBA 3 AXI/AHB bus interfaces or via Synopsys custom-defined Extended NIF interface (ENIF). The uPCTL is instantiated within the uMCTL. The functionality of the uMCTL is a superset of the uPCTL.

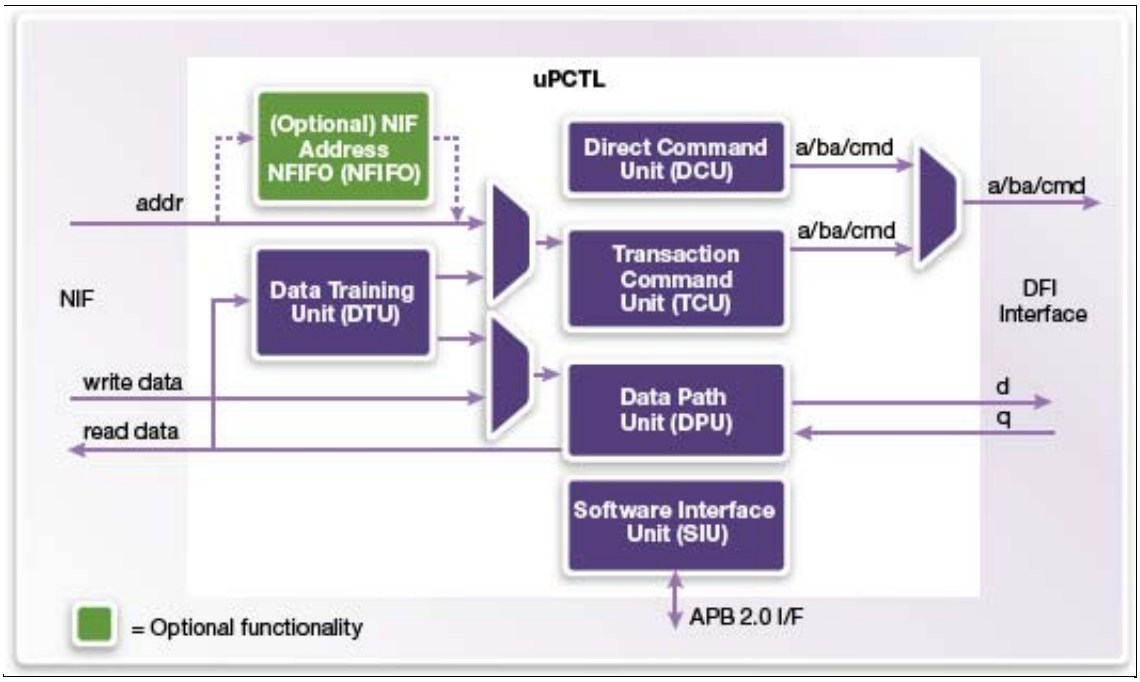
The uPCTL and uMCTL connect to DDR PHY through a DFI 2.1 interface to create a complete memory interface and control solution. Both controllers include software configuration registers, which are accessed through an AMBA 2.0 APB interface.

The Enhanced Universal DDR Memory Controller (uMCTL2) combined with a DWC DDR PHY or other DFI-compatible PHY is a complete memory interface solution for DDR memory subsystems. The uMCTL2 is delivered as configurable Verilog source and is compatible with all popular EDA environments. The uMCTL2 is a flexible and advanced solution for ASIC and SoC designers who need very low power while achieving industry leading high-efficiency, low-latency and high-performance from their memory interface. Supported SDRAM types include DDR2, DDR3, DDR4, MobileDDR/LPDDR, LPDDR2, and LPDDR3. On the host side, there is a choice of either AMBA 4 AXI4, AMBA 3 AXI, AMBA 2 AHB or custom Host Interface (HIF). The AMBA interfaces support single or multi port configurations, while the HIF supports a single port only.

The uMCTL2 can accept memory access requests from up to 16 application-side host ports. Each slave application port can be connected to the uMCTL2 through the standard AMBA 3 AXI/AHB bus interfaces. Mixed configurations of AMBA 4 AXI4, AMBA 3 AXI or AMBA 2 AHB are allowed. The interface between the uMCTL2 and PHY follows the DFI 3.1 Interface Specification.

uPCTL Key Features

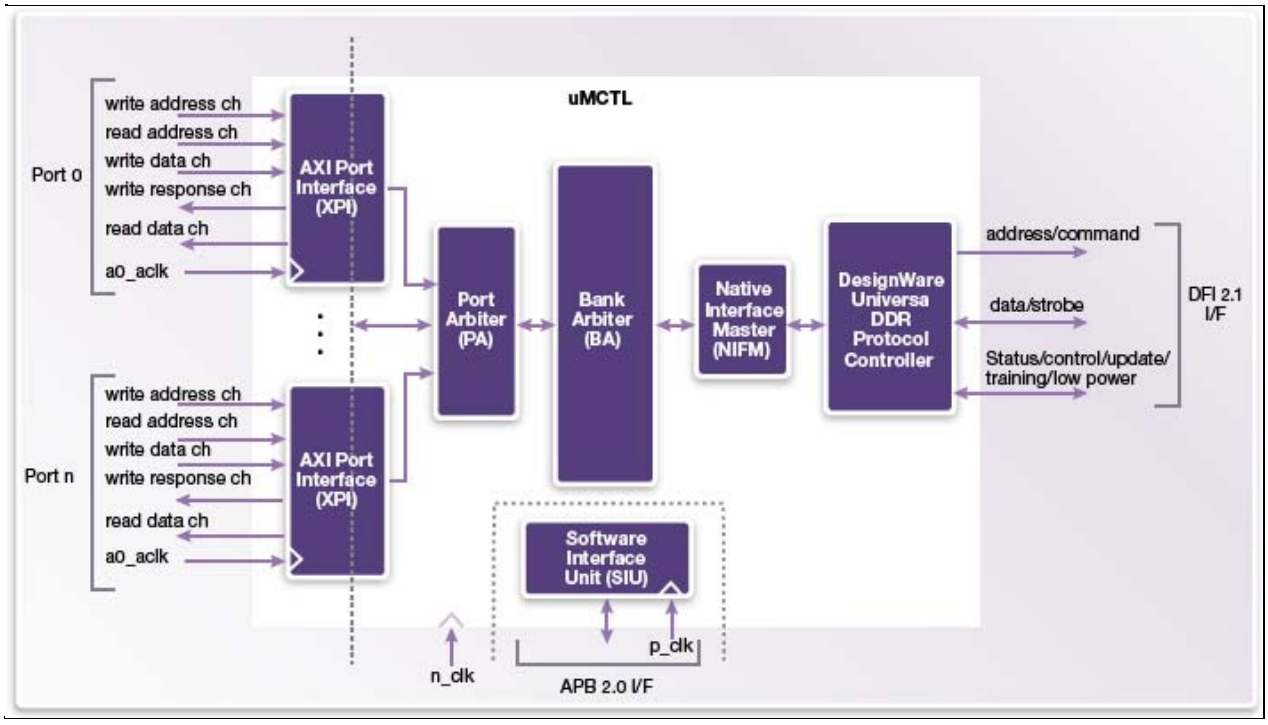
- Complete, integrated, single-vendor DDR solution when combined with Synopsys DWC DDR PHY
- DDR PHY Interface (DFI) support for easy integration with industry standard DFI 2.1-compliant PHYs
- Support for x8, x16, and x32 memories, for a total memory data path width of up to 72 bits
- Support for up to four memory ranks
- Programmable bank management policies: open-page, close-page
- Low area, low power architecture with no buffering on the data, avoiding duplication of storage resources within the system
- NIF slave for easy integration with an external scheduler or standard on-chip buses
- Efficient DDR protocol implementation with in-order column (Read and Write) commands and out-of-order Activate and Precharge commands
- Three clock cycles best case command latency
- 1T or 2T memory command timing
- Automatic power-down entry and exit
- Software driven self-refresh entry and exit
- Programmable memory initialization
- ECC generation and checking for 32-bit and 64-bit memory bus widths
- Optional in-line ECC bits, allowing for external processing of ECC bits
- Support for partial population of memories, where not all DDR byte lanes are populated with memory chips
- APB interface for uPCTL software accessible registers
- Programmable data training interface
  - Assists in training of the data eye of the memory channel
  - Provides a method for testing large sections of memory
- Support for industry standard UDIMMs (Unbuffered DIMMs) and RDIMMs (Registered DIMMs)



uMCTL Key Features

All features of the DesignWare Universal DDR Protocol Controller plus:

- Low latency architecture
- Low area/gate count design
- Up to 32 host ports using AMBA 3 AXI/AHB or Extended Native Interface (ENIF)
- For host ports with the AXI interface:
  - Compatibility with the AMBA 3 AXI protocol
  - Selectable close bank policy (autoprecharge at burst conclusion)
  - Variable burst lengths independent of the programmed DDR SDRAM burst length
  - Support for all AXI burst types: incremental, and wrap
  - AXI clock asynchronous/synchronous to the uMCTL clock
- For host ports with the AHB interface:
  - Compatibility with the AMBA 3 AHB protocol
  - Support for all AHB burst types: single, incr, incr4, incr8, incr16, wrap4, wrap8, wrap16
  - AHB clock asynchronous/synchronous to the uMCTL clock
- Advanced command re-ordering and scheduling to maximize bus utilization
- Two traffic classes, selectable per port:
  - Low latency for high priority traffic
  - Best effort for low priority traffic
- Programmable bandwidth per port
- Configurable and programmable address mapping, including bypass option to support external address mapping
- ECC Read Modify Write Support
- Read/Write command grouping



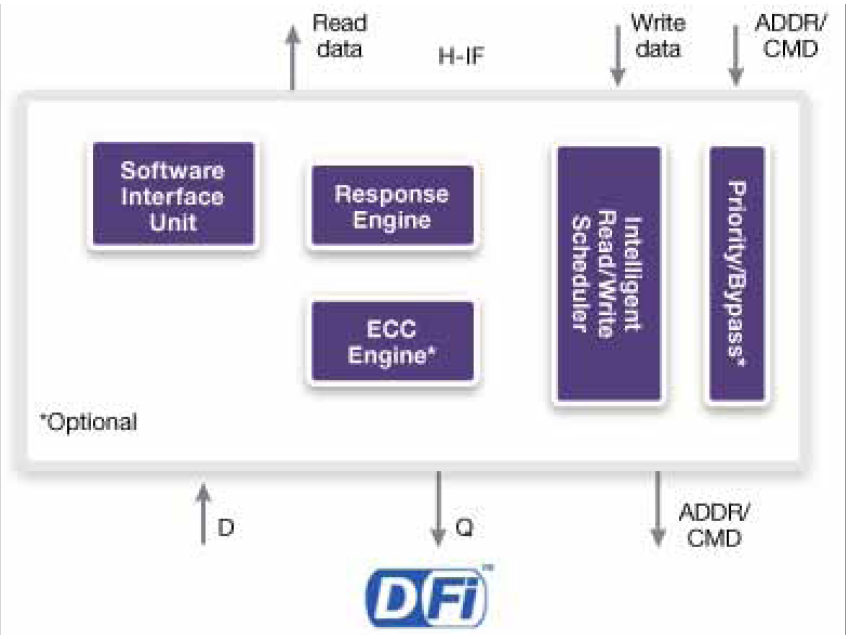
The product datasheet can be downloaded from the following site:

http://www.synopsys.com/designware

uMCTL2 Key Features

All features of the DesignWare uPCTL and uMCTL plus:

- Complete, integrated, single-vendor DDR2, DDR3, DDR4, mDDR, LPDDR2, LPDDR3, LPDDR4 solution when combined with Synopsys DWC DDR PHY
- Supports soldered on DRAM or DIMM DDR subsystems
- Supports up to 4 ranks of DRAM
- Hardware configurable and software programmable Quality of Service (QoS) support
- Programmable memory initialization
- Flexible address mapper logic to allow application specific mapping of row, column, bank, and rank bits
- Single Error Correct (SEC)/and Double Error Detect (DED)
- Read Modify Write Support
- Provides a method for testing large sections of memory
- Supports industry standard JEDEC DRAM and DIMMs
- Supports Dual Data Channel, also called "Shared AC", with a common address and command bus
- Incorporates a unique high-priority bypass option and configurable ‘look-ahead’ feature
- DDR4 protocol up to DDR4-3200 speed grade (MEMC_FREQ_RATIO=2) and DDR4-2133 speed grade (MEMC_FREQ_RATIO=1) are supported by the uMCTL2. The following features are supported:
  - Data Bus Inversion
  - Geardown mode
  - Temperature controlled self-refresh
  - Maximum power saving mode
  - Multi-purpose register reads and writes
  - Per DRAM addressability
  - Fine granularity refresh
  - Cyclic Redundancy Check (CRC) with retry
  - CA parity error with retry
  - Command/address latency
  - Programmable Preamble



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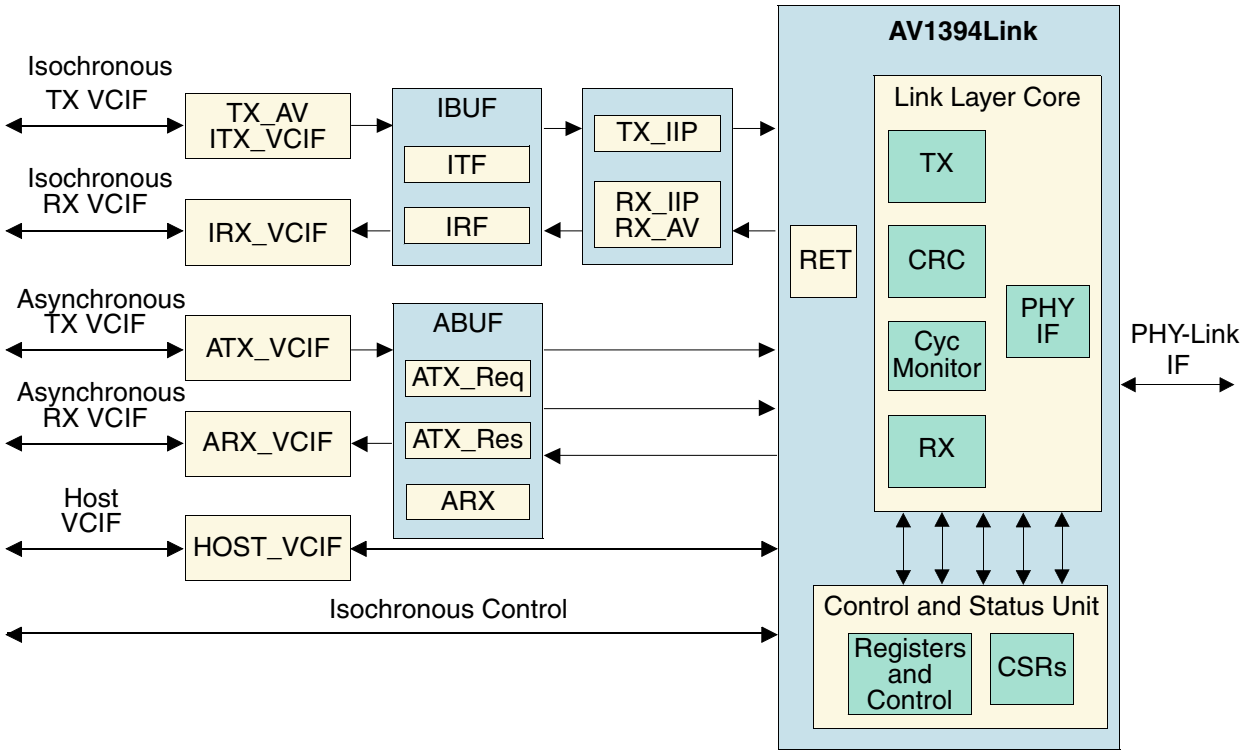
dwc_1394_av_link

Synthesizable IEEE 1394 AVLink DTCP

The Synopsys DesignWare IEEE 1394 AVLink DTCP intellectual property (IP) is a set of highly configurable blocks that implements complete 1394 interface functions tailored to support audio/visual (AV)-oriented IEC 61883 applications. Configured through our RapidScript utility, this device can also be optimized to act as a generic 1394 device controller. Therefore, AVLink can be effectively used in a wide range of applications, such as digital still cameras, video conferencing cameras, printers, scanners, digital audio devices, electronic musical instruments, digital VCRs/VTRs, and storage devices.

Features

- Silicon-proven IEEE 1394 Link Layer Controller for both audio/visual (A/V) and non-A/V applications
- Support for common isochronous packet (CIP) headers, time-stamping, and padded zeros for A/V data transactions
- IEEE 1394-1995 and 1394a-2000 specification compliance
- IEC 61883 requirement for A/V data streaming compliance
- Supports 100/200/400- Mbps data rates
- Full link layer implementation
- Asynchronous, isochronous, and PHY packet transmit and receive operations
- Cycle master and node controller capability
- Automatic isochronous resource manager detection
- Automatic acknowledge packet generation for received asynchronous packets
- Automatic 32-bit CRC generation and error detection interface
- Flexible, 32-bit Virtual Component Interface (VCI) for host
- Asynchronous and isochronous FIFO interface with burst and non-burst access modes
- Multi-speed, concatenated isochronous packet support
- Configurable number of isochronous transmit/receive channels
- Status reporting by extensive maskable interrupt register set
- Supports inbound and outbound single phase retry protocol
- RapidScript custom IP configuration
- Verilog source code
- Optional 1394 verification environment



The dwcore_1394_avlink datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_1394_av_link-dtcp.pdf

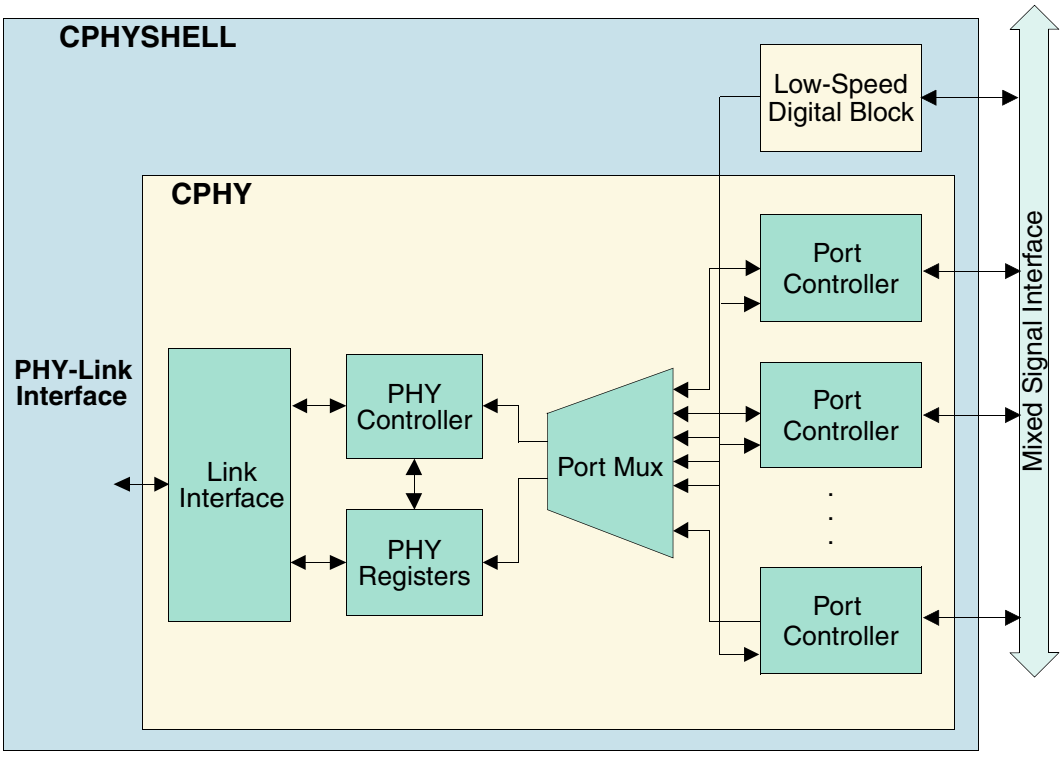
dwc_1394_cphy-native

Synthesizable IEEE 1394 Cable PHY

The Synopsys industry-proven DesignWare 1394 Cable Physical Layer (CPHY) enables devices to interface with the 1394 serial bus. The 1394 CPHY is a synthesizable RTL design that provides all the necessary features to implement the complete IEEE 1394a specification for the digital portion of the cable PHY. CPHY can be combined with an analog PHY and used in a stand-alone ASIC, or it can be integrated into an ASIC with a Link Layer controller. CPHY is well suited for multimedia and mass storage applications requiring high bandwidth, and is suitable for a wide range of applications, from basic low-cost devices (1 port) to sophisticated, high-performance ASICs (up to 16 ports).

Other Features

- Complete IEEE 1394a support
- Supports 100/200/400-Mbps bus speeds
- Configurable number of ports (1 to 16)
- Simple, silicon-proven interface to mixed signal analog circuitry
- Supports suspend/resume protocol
- Supports Link-On LPS protocol
- RapidScript configuration utility for design customization
- Synthesis scripts
- Verilog source code
- Approximately 14K gates (3 port)
- Proven in ASIC applications



The dwcore_1394_cphy datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_1394_cphy-native.pdf

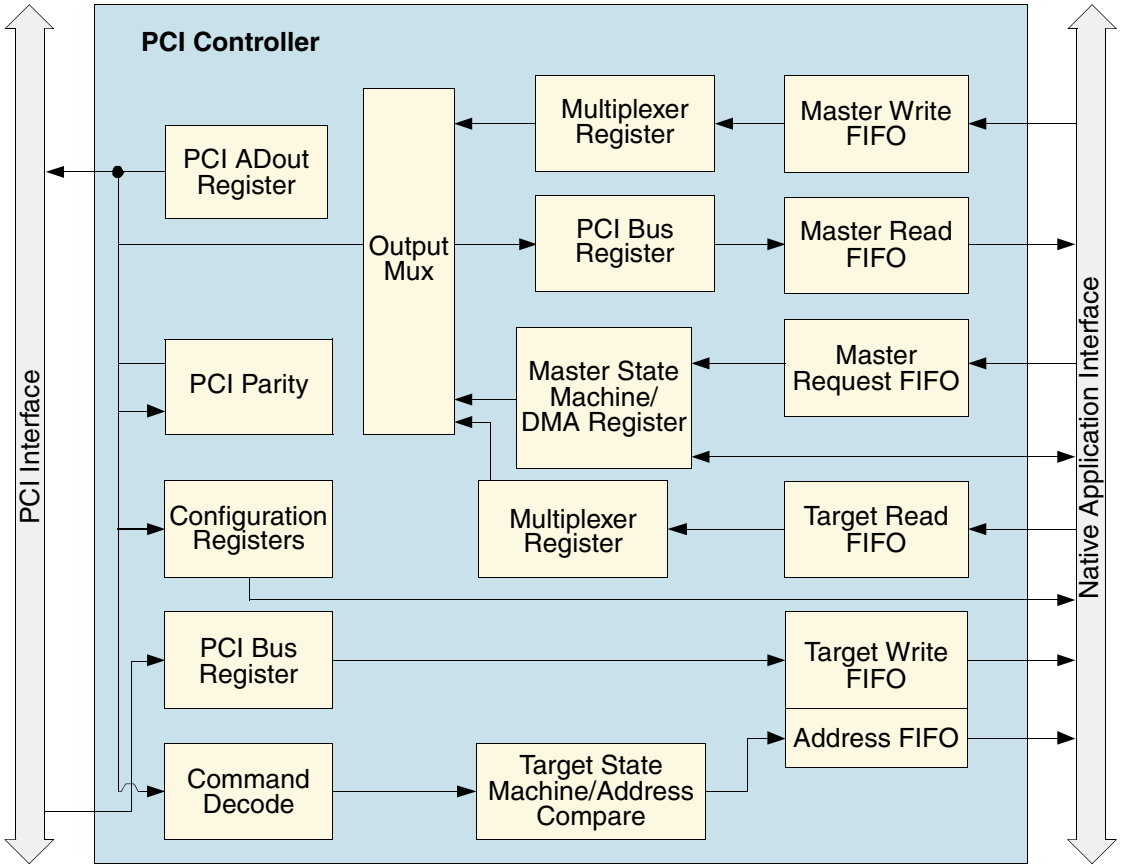
dwc_pci

Universal PCI Controller

The DesignWare IP core for PCI is available as synthesizable RTL source code and provides an interface between the application and the PCI bus. Some of the key features include the following:

Features

- PCI specification 2.3 compliant
- 15 application-optimized PCI IP, available in Verilog
- Silicon-proven 33-MHz and 66-MHz performance
- 32-bit or 64-bit PCI bus path
- 32-bit or 64-bit application data path
- Zero Latency, Fast Back-to-Back transfers
- Zero Wait-State Burst Mode transfers
- Support for Memory Read Line/Multiple and Memory Write and Invalidate commands
- Dual Address cycles
- Loadable configuration space
- Universal configuration optimized for use in both Host Bridge and Add-in Card designs
- Delayed Read support
- PCI power management support
- PCI multifunction support



The dwc_pci datasheet is available at:

http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_solutions

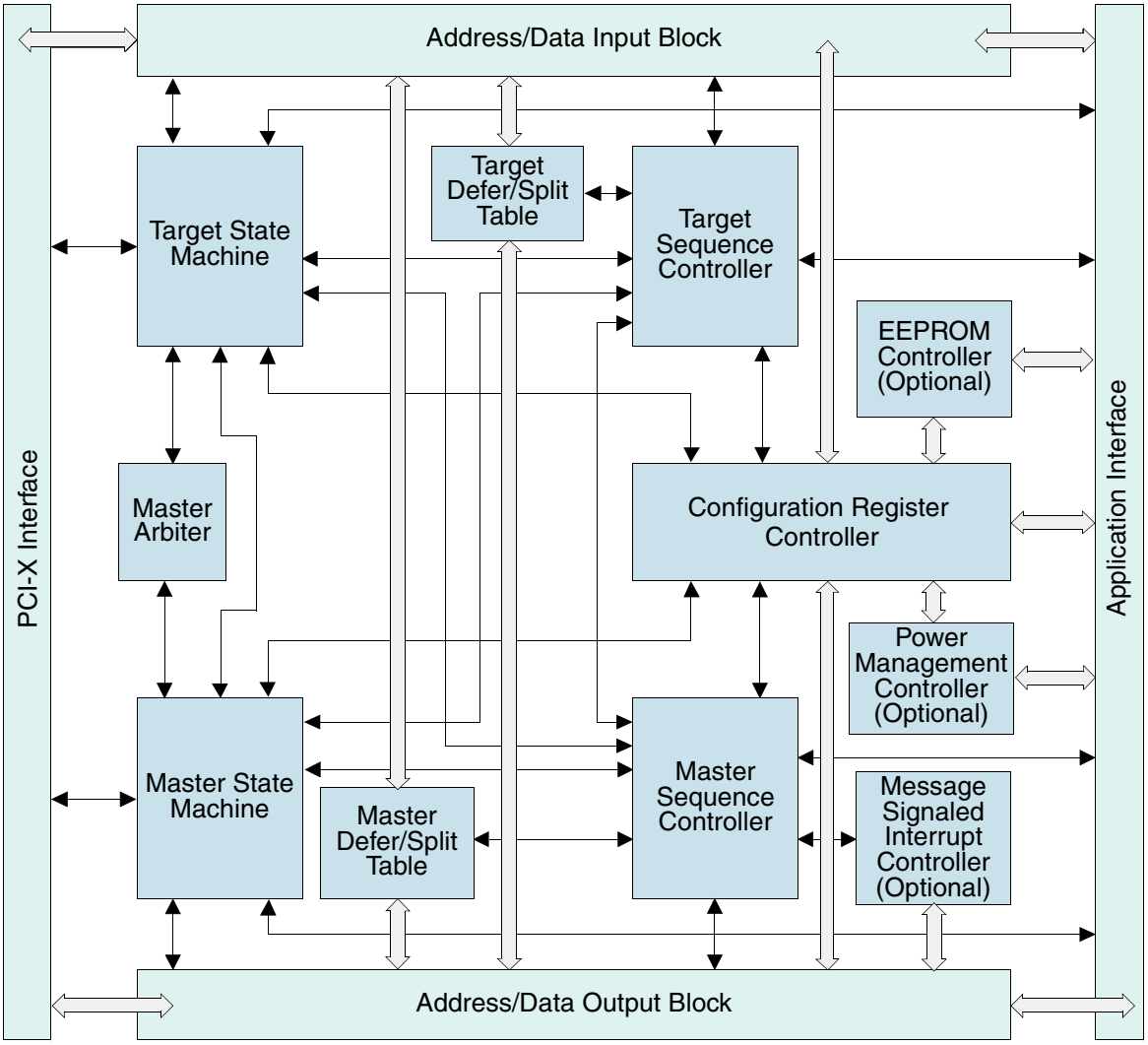
dwc_pci-x

Synthesizable PCI-X Controller and Test Environment

The DesignWare IP core for PCI-X is available as synthesizable RTL source, which enables designers to implement a complete PCI-X interface. PCI-X is highly suitable in a wide range of applications, such as SCSI, Fibre Channel, Gigabit Ethernet, and graphics. Other features include the following:

Other Features

- PCI-X 1.0a compliant
- Host Bridge functionality
- PCI 2.3 compliant
- 32-bit or 64-bit PCI-X bus path
- 64-bit application data path
- Supports 0-133 MHz PCI-X bus
- Supports up to 32 outstanding delayed/split transactions
- Dual Address Cycles (DAC)
- Message Signaled Interrupts (MSI)
- External EEPROM support
- Comprehensive Test Environment — Device Under Test linkable to the test environment
- RapidScript parameterized configuration for fast customization
- Synthesizable Verilog source code



The dwcore_pcix datasheet is available at:

http://www.synopsys.com/dw/ipdir.php?ds=dwc_pci_solutions

PCIe-AHB Bridge

PCI Express to AMBA 2.0 AHB Bridge

The DesignWare PCI Express to AMBA 2.0 AHB Bridge (PCIe-AHB Bridge) enables designers who use the AMBA 2.0 AHB on-chip bus to easily add PCI Express external connectivity to their AMBA 2.0 AHB-bases System-on-Chip (SoC) devices. Other features include the following:

Features

- AHB Master and Slave interfaces for inbound and outbound PCI Express requests
- 32, 64, or 128-bit datapath width
- 32 or 64-bit address width
- Supports full PCI Express configuration, I/O requests, traffic class (EP, TD, etc.) through PCIe-AHB Bridge
- AHB Slave interface for PCI Express core CDM register access through the PCI Express core's DBI interface
- Programmable buffer sizes for AHB Master and Slave requests and response queuing
- Independent programmable clock rates for the PCI Express core and AHB subsystem
- Programmable maximum number of inbound and outbound read requests for AHB
- All burst-sizes supported for both AHB Master and Slave interfaces
- Programmable burst lengths to support 4K read/write burst over AHB Master and Slave interfaces
- Independent maximum read request and transfer sizes between AHB and PCI Express (transfers can be split into multiple transfers)
- Response AHB Slave request gathering from split PCI Express completions
- Response AHB Master request gathering from multiple AHB responses
- Out-of-order transactions for transactions with unique Master IDs
- Interrupt and Message handling
- Response error mapping between PCI Express errors (UR, CA, CRS, poisoned, and ECRC error) and AHB Slave response errors
- Response error mapping between PCI Express errors (UR, CA, CRS, poisoned, and ECRC error) and AHB Master response error
- PCIe-AHB Bridge handles completion time outs

More information is available at:

http://www.synopsys.com/IP/InterfaceIP/PCIExpress

PCIe-AXI Bridge

PCI Express to AMBA 3 AXI Bridge

The DesignWare PCI Express to AMBA 3 AXI Bridge (PCIe-AXI Bridge) enables designers who use the AMBA 3 AXI on-chip bus to easily add PCI Express external connectivity to their AMBA 3 AXI-bases System-on-Chip (SoC) devices. Other features include the following:

Features

- AXI Master and slave interfaces for inbound and outbound PCI Express requests
- 32, 64, 128 or 256-bit datapath width
- 32 or 64-bit address width
- Supports full PCI Express configuration, I/O requests, traffic class (EP, TD, etc.) through PCIe-AXI Bridge
- AXI Slave interface for PCI Express core CDM register access through the PCI Express core's DBI interface
- Independent configuration of bus width for PCI Express core data bus, AXI master bus and AXI slave bus
- Programmable buffer sizes for AXI master and slave requests and response queuing
- Independent programmable clock rates for the PCI Express core, the AXI master bus, the AXI slave bus and the AXI slave DBI bus
- Programmable AXI master and slave address widths, data bus widths, and ID bus widths
- Programmable maximum number of inbound and outbound read requests for AXI
- All burst-sizes supported for both AXI master and slave interfaces
- Programmable burst lengths to support 4K read/write burst over AXI master and slave interfaces
- Supports unaligned AXI transfers using WSTRB and RTSRB for both AXI master and slave interfaces
- Supports independent maximum read request and transfer sizes between AXI and PCI Express (transfers can be split into multiple transfers)
- Supports response AXI slave request gathering from split PCI Express completions
- Supports response AXI master request gathering from multiple AXI responses
- Supports out-of-order transactions for transactions with unique IDs
- Supports Interrupt and Message handling
- Supports response error mapping between PCI Express errors (UR, CA, CRS, poisoned, and ECRC error) and AXI slave response errors (SLVERR and DECERR)
- Supports response error mapping between PCI Express errors (UR, CA, CRS, poisoned, and ECRC error) and AXI master response error (DECERR_W and DECERR_R)
- Support for byte parity check for the address and data buses though the PCIe-AXI Bridge
- PCIe-AXI Bridge handles completion time outs

More information is available at:

http://www.synopsys.com/IP/InterfaceIP/PCIExpress

dwc_pci_express_ep

PCI Express Endpoint Synthesizable Core

The DesignWare Endpoint Core for PCI Express implements the port logic required to build a PCI Express 4.0 Endpoint device. The silicon-proven Endpoint core is configurable and scalable to meet multiple endpoint application requirements ranging from server and desktop systems to mobile devices.

Other features include the following:

- Complies to PCI Express Base Specification, Revision 4.0
- Modular design, including a base core (CXPL) plus additional support modules for Endpoint-specific functionality
- Type 0 configuration space
- 62.5Mhz/125MHz/250MHz/500Mhz/1000MHz operation
- Up to 16 Gen1/Gen2/Gen3/Gen4 2.5/5.0/8.0/16.0-Gbps Lanes (x1, x2, x4, x8 or x16)
- 32, 64, 128 or 256-bit datapath width
- Support for 8/16/32-bit PHYs through the PIPE
- Ultra-low transmit and receive latency
- Configurable retry buffer size
- Configurable number of outstanding Requests
- Configurable Max_Payload_Size size (128 bytes to 4 KB)
- 4-KB maximum Request size
- SR-IOV, ARI and FLR
- Automatic Lane reversal as specified in the PCI Express Base Specification (transmit and receive)
- Polarity inversion on receive
- Multiple Virtual Channels (VCs)
- Multiple Traffic Classes (TCs)
- Multiple Functions (up to 32 with ARI)
- M-PCIe (Low-power over M-PHY) operation
- Supports bypass, cut-through, and store-and-forward queues for received TLPs
- AHB/AXI Bridge Interface (optional)
- ECRC generation and checking
- PCI Express beacon and wake-up mechanism
- PCI power management
- PCI Express Active State Power Management (ASPM)
- Advanced Power and Clock Management
- Power Gating (UPF) Support
- PCI Express Advanced Error Reporting
- MSI and MSI-X
- Internal MSI-X Generation
- All in-band Messages for PCI Express Endpoint
- Configurable Endpoint filtering rules for Posted, Non-Posted, and Completion traffic
- Configurable BAR filtering, I/O filtering, and configuration filtering
- Programmable completion time-out
- Supports up to three independent client interfaces for transmitting TLPs
- Access to configuration space registers and external application registers through local bus controller
- Internal Address Translation Unit
- IDO, TPH, LTR, ATS, OBFF, Resizable BAR, Readiness/Lightweight Notifications, and AtomicOPs ECN support
- Embedded DMA
- Parity checking on transmit buses, memory buses, and internal data buses
- RAS Debug, Error Injection, and Statistics

More information is available at:

http://www.synopsys.com/IP/InterfaceIP/PCIExpress

dwc_pci_express_rc

PCI Express Root Port Synthesizable Core

The DesignWare Root Port core for PCI Express 4.0 is a synthesizable RC port solution that can be configured to address multiple applications, ranging from server and desktop systems to mobile devices.

Features

- Complies to PCI Express Base Specification, Revision 4.0
- M-PCIe (Low-power over M-PHY) operation
- Modular design, including a base core (CXPL) plus additional support modules for Root Port-specific functionality
- Type 1 configuration space
- 62.5MHz/125MHz/250MHz/500MHz/1000MHz operation
- Up to 16 Gen1/Gen2/Gen3/Gen4 2.5/5.0/8.0/16.0-Gbps Lanes (x1, x2, x4, x8 or x16)
- 32, 64, 128 or 256-bit datapath width
- Support for 8/16/32-bit PHYs through the PIPE
- Ultra-low transmit and receive latency
- Configurable retry buffer size
- Configurable number of outstanding Requests
- Configurable Max_Payload_Size size (128 bytes to 4 KB)
- 4-KB maximum Request size
- Automatic Lane reversal as specified in the PCI Express Base Specification (transmit and receive)
- Application-initiated Lane reversal for situations where the core does not detect Lane 0 (for example, an x4 core connected to an x8 device that has its Lanes reversed)
- Polarity inversion on receive
- Multiple Virtual Channels (VCs)
- Multiple Traffic Classes (TCs)
- Supports bypass, cut-through, and store-and-forward queues for received TLPs
- AHB/AXI Bridge Interface (optional)
- Supports ECRC generation and checking
- Supports PCI Express beacon and wake-up mechanism
- Supports PCI power management
- Supports PCI Express Active State Power Management (ASPM)
- Advanced Power and Clock Management
- Power Gating (UPF) Support
- Supports PCI Express Advanced Error Reporting
- Supports all in-band Messages for PCI Express Root Port
- Configurable filtering rules for Posted, Non-Posted, and Completion traffic
- Supports two application transmit clients by default, additional third client optional
- Access to configuration space registers from the application through the DBI
- Internal Address Translation Unit
- IDO, TPH, LTR, ATS, OBFF, Readiness/Lightweight Notifications, and AtomicOPs ECN support
- Supports external priority arbiter (in addition to the internally-implemented transmit arbitration)
- Embedded DMA
- Parity checking on transmit buses, memory buses, and internal data buses
- RAS Debug, Error Injection, and Statistics

More information is available at:

http://www.synopsys.com/IP/InterfaceIP/PCIExpress

dwc_pci_express_sw

PCI Express Switch Port Synthesizable Core

The DesignWare Switch Port core for PCI Express 4.0 is a synthesizable SW port solution that can be configured to address multiple applications, ranging from server and desktop systems to mobile devices. Other features include the following:

Features

- Complies to PCI Express Base Specification, Revision 4.0
- M-PCIe (Low-power over M-PHY) operation
- Modular design including a base core (CXPL) plus additional support modules for Switch-specific functionality
- Type 1 configuration space
- 62.5MHz/125MHz/250MHz/500MHz/1000MHz
- Up to 16 Gen1/Gen2/Gen3/Gen4 2.5/5.0/8.0/16.0-Gbps Lanes (x1, x2, x4, x8 or x16)
- 32, 64, 128 or 256-bit datapath width
- Configurable as upstream Switch Port or downstream Switch Port.
- Support for 8-bit and 16-bit PHYs through the PIPE
- Supports prefetchable memory space
- Transaction filtering and routing look up
- Multiple Virtual Channels (VCs)
- Multiple Traffic Classes (TCs)
- Configurable VC/TC mapping
- Full PCI Express Message passing and processing
- Ultra low transmit and receive latency
- Configurable retry buffer size
- Configurable number of outstanding Requests
- Configurable Max_Payload_Size size (128 bytes to 4 KB)
- 4-KB maximum Request size
- Lane reversal (transmit and receive)
- Polarity inversion (transmit and receive)
- Supports bypass, cut-through, and store-and-forward queues for received TLPs
- Supports ECRC checking and error reporting (optional)
- Supports PCI Express beacon and wake-up mechanism
- Supports PCI power management
- Supports PCI Express Active State Power Management (ASPM)
- Advanced Power and Clock Management
- Power Gating (UPF) Support
- Supports PCI Express Advanced Error Reporting
- Full PCI Express Message passing and processing
- Configurable filtering rules for Posted, Non-Posted, and Completion traffic
- Configurable BAR filtering, I/O filtering, configuration filtering
- Supports two application transmit clients by default, additional third client optional
- Access to configuration space registers and external application registers through local bus controller
- Parity checking on transmit buses, memory buses, and internal data buses
- IDO, LTR, OBFF, Resizable BAR, Readiness/Lightweight Notifications, and AtomicOPs ECN support.
- Internal Address Translation Unit
- RAS Debug, Error Injection, and Statistics

More information is available at:

http://www.synopsys.com/IP/InterfaceIP/PCIExpress

dwc_pci_express_dm

PCI Express RC/EP Dual Mode Synthesizable Core

The DesignWare Dual Mode (Root Port/Endpoint) Core for PCI Express 4.0 is a synthesizable solution that can be configured to address multiple applications, ranging from server and desktop systems to mobile devices. Other features include the following:

- Complies to PCI Express Base Specification, Revision 4.0
- M-PCIe (Low-power over M-PHY) operation
- Modular design, including a base core (CXPL) plus additional support modules for Endpoint-specific functionality
- Operating mode (EP or RC) determined by state of input pin at power-on reset
- Type 0 configuration space in EP mode; type 1 configuration space in RC mode
- 62.5MHz/125MHz/250MHz/500MHz/1000MHz
- Up to 16 Gen1/Gen2/Gen3/Gen4 2.5/5.0/8.0/16.0-Gbps Lanes (x1, x2, x4, x8 or x16)
- 32, 64, 128 or 256-bit datapath width
- Support for 8/16/32-bit PHYs through the PIPE
- Configurable retry buffer size
- Configurable number of outstanding Requests
- Configurable Max_Payload_Size size (128 bytes to 4 KB)
- 4-KB maximum Request size
- Automatic Lane reversal as specified in the PCI Express Base Specification (transmit and receive)
- In RC mode: application-initiated Lane reversal where the core does not detect Lane 0 (for example, an x4 core connected to an x8 device that has its Lanes reversed)
- Polarity inversion on receive
- Multiple Virtual Channels (VCs)
- Multiple Traffic Classes (TCs)
- Multiple Functions (up to 32 with ARI)
- Supports bypass, cut-through, and store-and-forward queues for received TLPs
- AHB/AXI Bridge Interface (optional)
- ECRC generation and checking
- PCI Express beacon and wake-up mechanism
- PCI power management
- PCI Express Active State Power Management (ASPM)
- Advanced Power and Clock Management
- Power Gating (UPF) Support
- PCI Express Advanced Error Reporting
- MSI and MSI-X
- Internal MSI-X Generation Unit
- All in-band Messages supported
- Configurable filtering rules for Posted, Non-Posted, and Completion traffic
- Configurable BAR filtering, I/O filtering, and configuration filtering
- Programmable completion time-out
- Supports up to three independent client interfaces for transmitting TLPs
- Access to configuration space registers and external application registers through local bus controller
- Internal Address Translation Unit
- Automatic generation of Completions for Requests that require Unsupported Request (UR) or Completer Abort (CA) responses
- IDO, TPH, LTR, ATS, OBFF, Resizable BAR, Readiness/Lightweight Notifications, and AtomicOPs ECN support
- Embedded DMA
- Parity checking on transmit buses, memory buses, and internal data buses
- RAS Debug, Error Injection, and Statistics

More information is available at:

http://www.synopsys.com/IP/InterfaceIP/PCIExpress

dwcore_pcie_phy

PCI Express PHY IP

The DesignWare PCI Express PHY IP integrates high-speed mixed-signal custom CMOS circuitry for easy integration into system-on-chip designs. The high-margin, robust PCI Express PHY architecture tolerates manufacturing variations such as process, voltage, and temperature.

While extremely low in power (up to 50% less than conventional PHYs) and area, the DesignWare PCI Express PHY substantially exceeds the electrical specifications defined in the PCI Express base specification in key performance areas such as jitter and receive sensitivity.

The unique, advanced, built-in diagnostics and ATE test vectors available in the DesignWare PCI Express PHY enables designers to implement complete at-speed production testing without the need for expensive test equipment. Furthermore, the PCI Express PHY provides on-chip visibility into the actual link performance and quickly identifies signal integrity issues. This method is superior to the traditional "loopback" mechanism.

PHY Features

- Fully complies with PCI Express 1.1 (2.5 Gbps) and 2.0 (5.0 Gbps) specifications
- Complies with 1.87 PIPE specification
- Supports popular 65-,90-,and 130-nm processes in multiple foundries
- 8- and 16-bit PIPE PHY interfaces
- Supports x1, x4, and x8 lanes
- Supports all power-down modes and spread spectrum clocking
- Supports beaconing, receiver detection, and electrical idle
- Provides excellent performance margin and receive sensitivity
- Consumes very low power (up to half the power compared to conventional PCIe® PHYs)
- Occupies very small die size (up to half the size of conventional PCIe PHYs)
- Provides robust PHY architecture and tolerates wide PVT variations
- Supports flip-chip and low-cost wirebond packages
- Implements low-jitter PLL technology with excellent supply isolation
- Provides low-offset, high-sensitivity receiver with high-resolution CDR
- Supports ± 10% supply variation
- Uses 100-MHz, 125-MHz, and 156.25-MHz reference clocks

Verification Features

- Supports verification at PIPE, 10b, and serial interface
- Supports automatic handling of transaction, data link and physical layer tasks
- Provides full Requester and Completer functions
- Supports up to eight virtual channels
- Supports full LTSSM (Link Training)
- Supports power management
- Supports automatic generation of flow control packets
- Supports single word read and write transfers to memory, I/O, and configuration space
- Supports block read and write transfers to memory space
- Supports message transfers
- Supports orders packets based on PCI Express ordering rules
- Supports transaction reordering and out-of-order completions
- Supports modification and review of internal address spaces with zero cycle commands
- Supports error injection at each layer
- Provides functional coverage of PCI Express packet types

More information is available at:

http://www.synopsys.com/dw/ipdir.php?ds=dwc_pcie2_phy

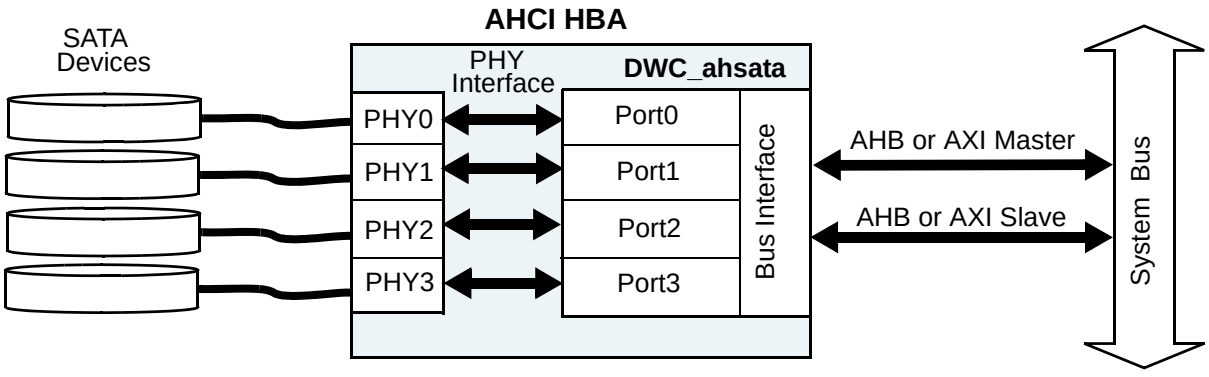
DWC_ahsata

Serial ATA AHCI

The DesignWare SATA AHCI intellectual property (IP) is designed for use in system-on-chip (SoC) solutions. The IP uses the popular AMBA AHB or AXI standard for a host interface and a configurable PHY/link interface to support a number of industry PHYs. Synopsys provides a large set of parameters to enable the IP's integration in systems with different requirements. By leveraging these parameters, the DWC SATA AHCI can optimize gate count and reduce time to market.

Features

- Supports SATA 1.5 Gb/s, SATA 3.0 Gb/s, SATA 6.0 Gb/s speeds (6.0 Gb/s speed requires additional license)
- eSATA (external analog logic also needs to support eSATA)
- Compliant with Serial ATA Specification 3.1 and AHCI Revision 1.31, and AMBA 2.0 and 3.0 AXI specifications
- Highly configurable PHY interface
- User-defined PHY status and control ports
- Configurable features:
  - RX Data Buffer for recovered clock systems
  - Data alignment circuitry when RX data buffer is also included
  - OOB signaling detection and generation
  - 8b/10b encoding/decoding
  - Mechanical presence switch, cold presence detect, and activity LED support
  - Output port to indicate speed that is negotiated after COMRESET for power optimization
  - Device Sleep (DevSleep) Power Mgmt
  - SATA encryption/decryption tools
- When TX OOB signaling is included, the following features are also included:
  - SATA 1.5 Gb/s, SATA 3.0 Gb/s, and SATA 6.0 Gb/s speed negotiation
  - Asynchronous signal recovery, including retry polling
  - Digital support of device hot-plugging
- Power management features including automatic partial-to-slumber transition
- BIST loopback modes
- Up to eight SATA devices (configurable from 1 to 8 ports)
- Configurable AMBA AHB or AXI interface (one master and one slave for each interface)
- Internal DMA engine per port
- Hardware-assisted Native Command Queuing for up to 32 entries
- Port Multiplier with FIS-based switching
- Disabling RX and TX Data clocks during power down modes
- Any sector size



The DesignWare DWC_sata_ahci datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_sata_csds.pdf

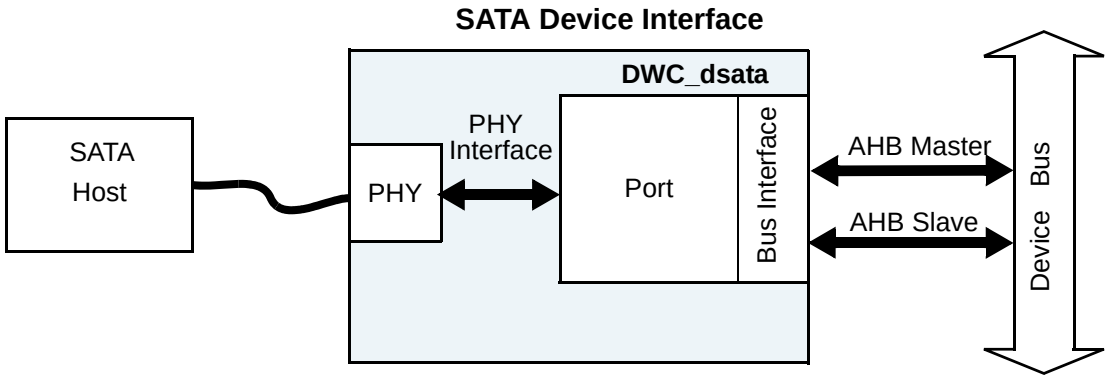
DWC_dsata
Serial ATA Device

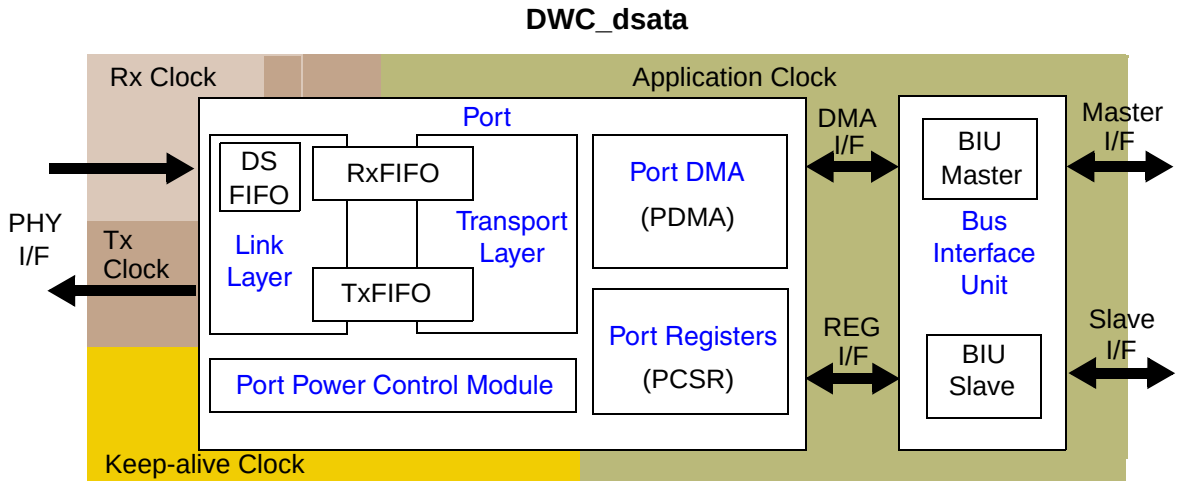
The DesignWare® IP for Serial ATA (SATA) Device Core is compliant to the SATA 2.6 specification for 1.5 and 3 Gbps and the SATA 3.1 specification for 6 Gbps operation ensuring scalability and reuse in your current and future SoC. The digital device core offers a well defined, flexible programming model that minimizes software overhead during data transfers ensuring maximum operational performance. Sample device firmware for various applications is available on request. With its integrated DMA this high speed operation is achieved without additional system overhead.

The core configuration offers one-click integration with the DesignWare IP SATA PHY removing the effort of integrating the digital and mixed signal portions of the SATA interface design. Reduced gate count and very low power consumption is achieved by utilizing the set of highly configurable options which enable the core to optimized based on the exact design requirements. The test environment for the digital device controller IP includes a number of the Verification IP components offering SATA transactions generation, SATA protocol monitoring and AMBA subsystem transaction generation. Verilog-based tests are provided as examples to accelerate system integration.

Features

- Compliant SATA Device for any application, HDD, ODD, SSD….
- SATA 1.5 Gb/s, SATA 3.0 Gb/s, and SATA 6.0 Gb/s speeds (6.0 Gb/s speed requires additional license)
- SATA 3.1 specification compliance
- Command Layer firmware
- Configurable interface:
  - PHY interface
  - AMBA AHB interface (one master and one slave)
- Additional user defined PHY status and control ports
- Configurable settings:
  - RX Data Buffer for recovered clock systems
  - Data alignment circuitry when RX Data Buffer included
  - OOB signalling detection and generation
  - 8b/10b encoding/decoding
  - Device Sleep (DevSleep) Power Management
- SATA 1.5 Gb/s, SATA 3.0 Gb/s, and SATA 6.0 Gb/s speed negotiation when TX OOB signaling is selected
- Power management:
  - Automatic Partial-to-Slumber transition
  - Inactivity Timer feature that allows hardware-initiated power management requests
- SATA BIST loopback modes
- Internal high-performance DMA engine with flexible programming model
- RX and TX data clock disable during power down modes





The DesignWare DWC_dsata datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_sata_csds.pdf

dwc_sata_phy
Serial ATA PHY IP

The DesignWare SATA PHY IP integrates high-speed, mixed-signal, custom CMOS circuitry for easy integration into SoC designs. The high-margin, robust SATA PHY architecture tolerates manufacturing variations such as process, voltage, and temperature. The DesignWare SATA PHY integrates seamlessly with the DesignWare SATA Host core to help reduce design time and achieve first-pass silicon success. While extremely low in power consumption and area, the SATA PHY is compliant with the SATA 2.6 specification and substantially exceeds its electrical specifications in key performance areas such as jitter and receive sensitivity.

The unique, advanced, built-in diagnostics and ATE test vectors available in the DesignWare SATA PHY enables designers to implement complete at-speed production testing without the need for expensive test equipment. Furthermore, the DesignWare SATA PHY provides on-chip visibility into the actual link performance and quickly identifies signal integrity issues. This method is superior to the traditional "loopback" mechanism.

PHY Features

- Provides excellent performance margin and receive sensitivity
- Implements very low power design, up to half the power compared to conventional PHYs
- Provides ATE test vectors for complete at-speed production testing
- Includes on-board scope and diagnostics for fast system verification
- Supports popular 130-nm, 90-nm, and 65-nm processes
- Occupies small, cost-effective die size
- Supports hot-pluggable devices
- Implements low-jitter PLL technology with excellent supply isolation
- Provides low-offset, high-sensitivity receiver with high resolution
- Implements robust architecture that tolerates wide PVT variations

Test Features

- Provides built-in, per-channel BERTs
- Supports flexible, fixed and random pattern generation
- Supports error counting on patterns or disparity
- Supports digital phase or voltage margining (bathtub curves)
- Provides built-in, per-channel scopes for capture of eye diagram or coherent capture of periodic signals
- Supports loopbacks: serial analog (for wafer probe) and digital Tx to Rx
- Supports full analog ATE test on low-cost digital tester using only pass/fail JTAG vectors

The DesignWare dwc_sata_phy datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_sata_phy.pdf

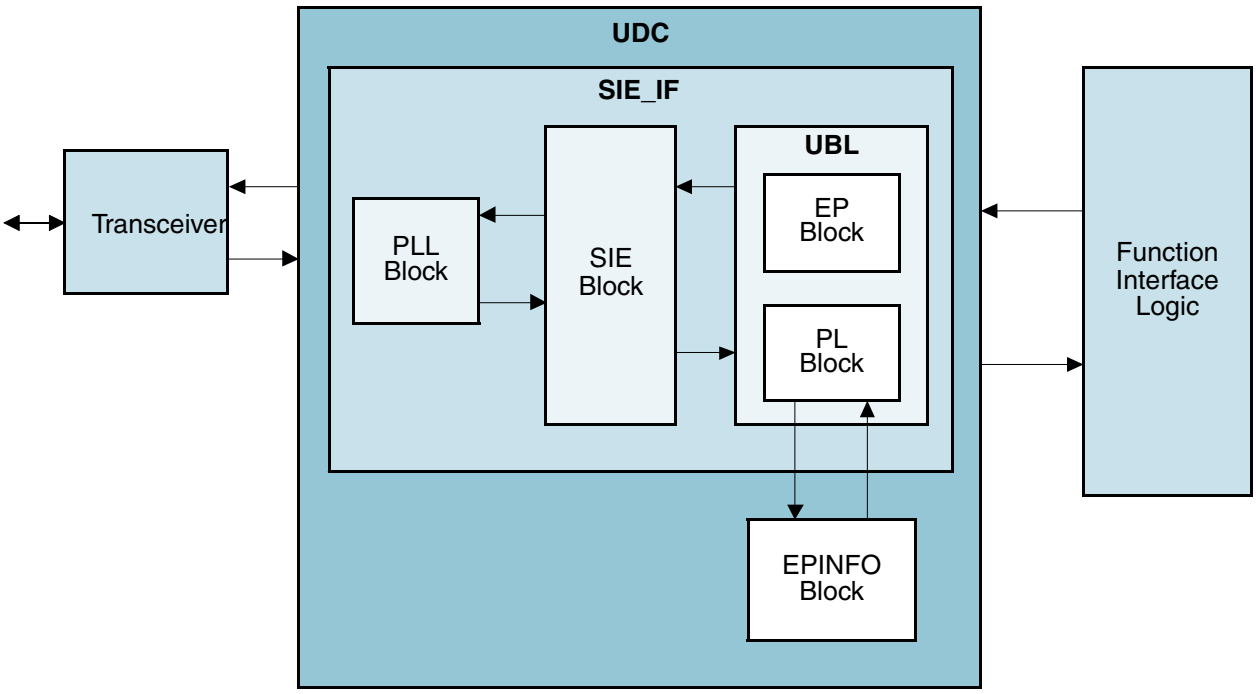
dwc_usb_1_1_device

Synthesizable USB 1.1 Device Controller

The Synopsys DesignWare USB Device Controller (UDC) is a set of synthesizable building blocks for implementing a complete USB device interface.

Features

- 32-bit Virtual Component Interface (VCI)
- Maintains address pointer for endpoint 0 transactions
- Silicon proven
- USB 2.0 Full Speed compatible
- AMBA High-Performance Bus (AHB) interface enables rapid integration into ARM-based designs.
- Option to include internal DMA or interface to external DMA controller.
- Standard register set specification available
- Applications supported include: pointing devices, scanners, cameras, faxes, printers, speakers, monitor
- Verilog source code
- Supports low-speed and full-speed devices
- Programmable number of endpoints
- Easily configurable endpoint organization
- Supports up to 15 configurations, up to 15 interfaces per configuration, and up to 15 alternate settings per interface
- Supports all USB standard commands
- Easy-to-add Vendor/Class commands
- Suspend/resume logic provided
- Approximately 12K gates for 5 physical endpoints



The dwcore_usb1_device datasheet is available at:

http://www.synopsys.com/dw/ipdir.php?ds=dwc_usb_1_1_controllers

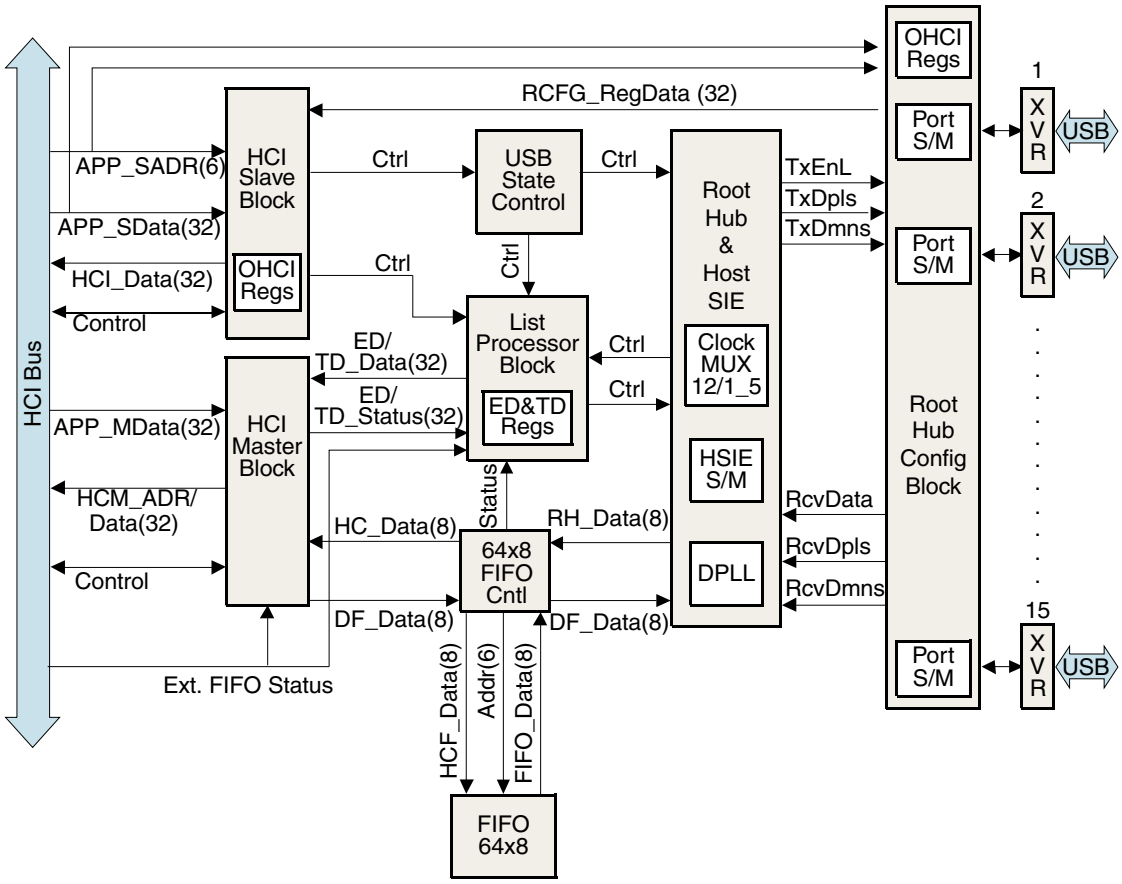
dwc_usb_1_1_ohci_host

Synthesizable USB 1.1 OHCI Host Controller

The Synopsys DesignWare USB 1.1 Host Controller (OHCI) Synthesizable IP is a set of synthesizable building blocks that ASIC/FPGA designers use to implement a complete USB OHCI Host Controller.

Features

- Silicon proven
- USB 1.1 compliant
- AHB interface
- Compatible with Open HCI 1.0 specification
- Verilog source code
- Supports low-speed and full-speed devices
- Configurable root hub supporting up to 15 downstream ports
- Configuration data stored in Port Configurable Block
- Single 48-MHz input clock
- Simple application interface facilitates bridging the host to other system bus such as PCI, and the integration of the controller with chipsets and microcontrollers
- Integrated DPLL
- Support for SMI interrupts
- Approximately 25K gates with 2 ports



The dwcore_usb1_host datasheet is available at:

http://www.synopsys.com/dw/ipdir.php?ds=dwc_usb_1_1_controllers

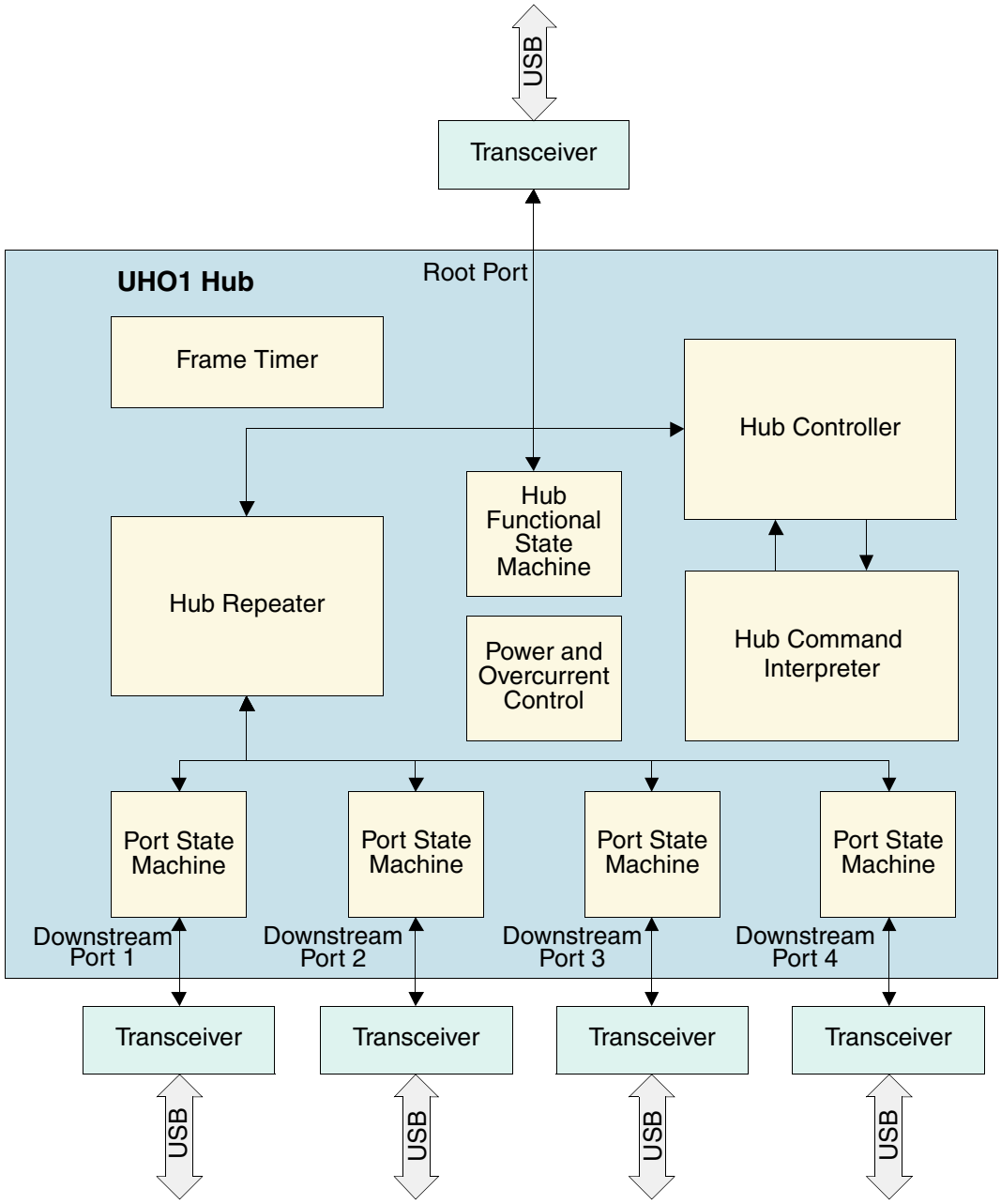
dwc_usb_1_1_hub-native

Synthesizable USB 1.1 Hub Controller

The Synopsys DesignWare USB Hub (UH01) is a set of synthesizable building blocks that ASIC/FPGA designers use to implement a complete USB Hub. The RapidScript utility enables designers to easily configure the device by setting the number of downstream ports. The Synopsys UH01 product consists of the Hub Repeater and the Hub Controller. The Hub Repeater is responsible for connectivity setup and tear-down and supports exception handling such as bus fault detection/recovery and connect/disconnect detection. The Hub Controller provides the mechanism for host to hub communication. Hub-specific status and control commands permit the host to configure a hub and to monitor and control its individual downstream ports. Other features include the following:

Features

- Silicon proven
- USB 1.1 compliant
- Verilog source code
- Supports low-speed and full-speed devices on downstream ports
- Integrated DPLL for clock and data recovery
- Downstream device connect/disconnect detection
- Supports suspend/ resume for power management
- Supports one interrupt endpoint in addition to endpoint 0
- Approximately 12K gates, for four ports



The dwcore_usb1_hub datasheet is available at:

http://www.synopsys.com/dw/ipdir.php?ds=dwc_usb_1_1_controllers

dwc_usb_2_0_host_subsystem-pci-ahb

Synthesizable USB 2.0 Host Controller

The Synopsys DesignWare USB Host Controller (UHOST2) is a set of synthesizable building blocks that ASIC/FPGA designers use to implement a complete USB 2.0 host for 480-Mbps operation. The UHOST2 can be customized and optimized as a stand-alone host chip or as an integrated ASIC for applications such as game consoles, set-top boxes, PCs, PDAs, and telecommunications equipment. In addition, the design can be easily processed in most technologies and can be easily bridged to any industry-standard bus and includes both the PCI and ARM AHB interfaces. The application interface screens USB host controller design complexities, making it easy to integrate the UHOST2 device to customer target applications. Other features include the following:

General

- Design methodology supports full scan for testability
- All clock synchronization is handled within the controller
- coreConsultant utility provided for design configuration
- Descriptor and data prefetching (configuration option)
- No bidirectional or three-state buses
- No level-sensitive latches

Software

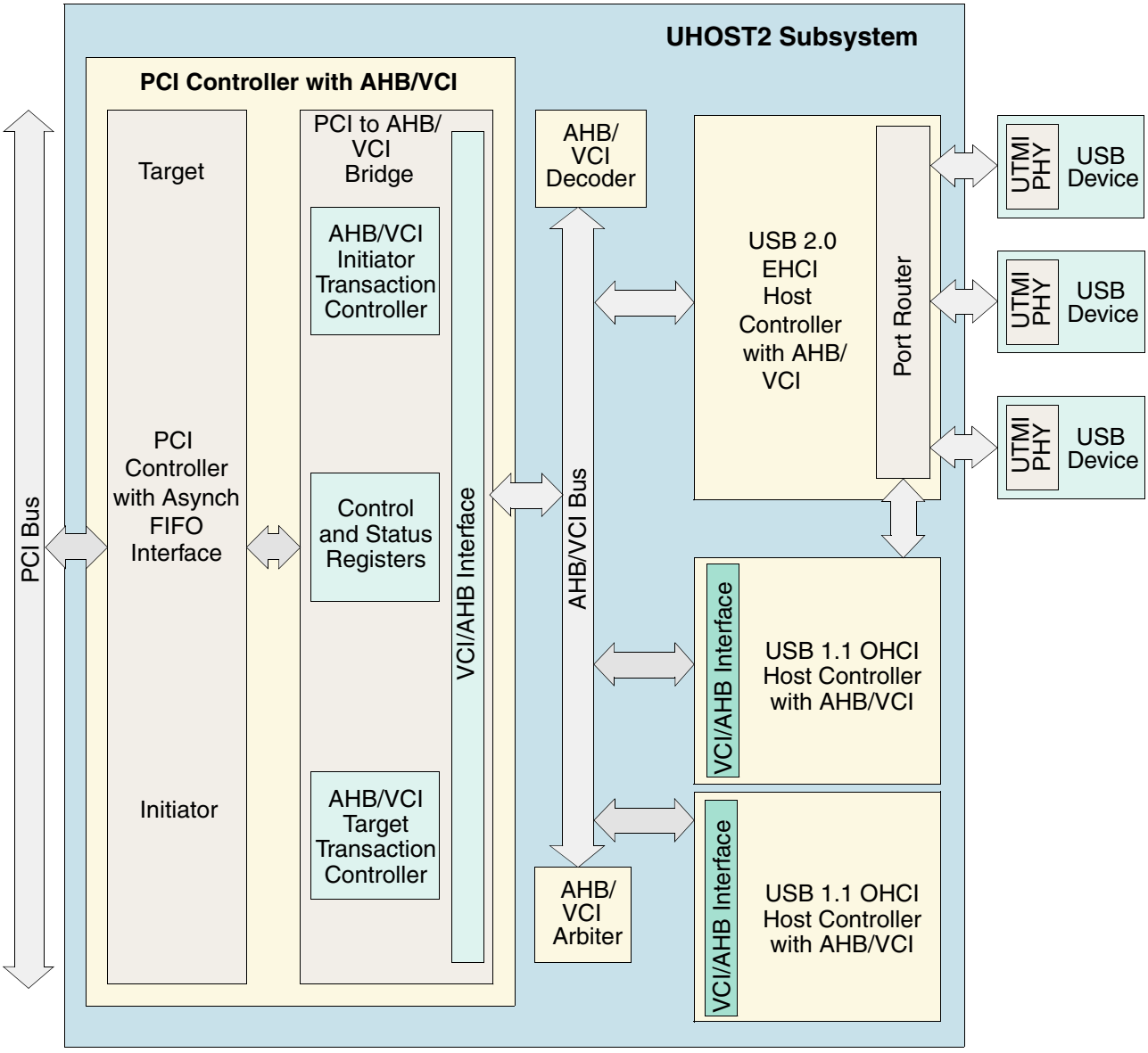
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.

Power Optimization

- ULPI Reduced Power mode with ULPI wrapper operates at 60 MHz, with the remainder of the Root Hub operating at 30 MHz.

Application

- AHB interface to the application
- Complies with the AMBA Specification, Revision 2.0
- Bus Interface Unit (BIU) handles retry, error and split transactions on the AHB
- As an AHB Master supports 8-, or 32- bit data transfers on the AHB
- Supports 32-bit addressing on the AHB
- USB 2.0 Supported Features
- Complies with the USB 2.0 Specification
- Supports ping and split transactions
- UTMI+ or ULPI interface to the PHY
- UTMI PHY interface clock supports 30-MHz operation for a 16-bit interface or 60-MHz operation for an 8-bit interface
- ULPI PHY interface clock supports 60-MHz operation for both 8- and 4-bit interfaces



The dwcore_usb2_host datasheet is available at:

http://www.synopsys.com/dw/ipdir.php?ds=dwc_usb_2_0_digital_controllers

dwc_usb_2_0_hs_otg_subsystem-ahb

Synthesizable Hi-Speed USB On-The-Go (OTG) Controller Subsystem

The DesignWare Hi-Speed USB On-The-Go (HS OTG) Controller Subsystem operates as either a Hi-Speed USB compliant peripheral, host, or OTG Dual-Role Device (DRD). This core has earned Hi-Speed USB OTG certification with the Synopsys USB OTG PHY in three semiconductor processes. Features include the following:

General Features

- Software configurable to OTG1.3 and OTG2.0 modes of operation
  - OTG 2.0 Supports ADP (Attach detection Protocol)
- Support for the following speeds:
  - High-Speed (HS, 480-Mbps),
  - Full-Speed (FS, 12-Mbps) and
  - Low-Speed (LS, 1.5-Mbps) modes
- Multiple options available for low power operations
- Multiple DMA/non DMA mode access support on the application side
- Multiple Interface support on the MAC-Phy
- Supports different clocks for AHB and the PHY interfaces for ease of integration
- Supports up to 16 bidirectional endpoints, including control endpoint 0. 1.
- Low speed is not supported for DWC_otg as a device with a UTMI+ PHY.
- Supports Session Request Protocol (SRP).
- Supports Host Negotiation Protocol (HNP).
- Supports up to 16 host channels. In Host mode, when the number of device endpoints to be supported is more than the number of host channels, software can reprogram the channels to support up to 127 devices, each having 32 endpoints (IN + OUT), for a maximum of 4,064 endpoints.
- Supports the external hub connection in Host Buffer DMA mode, Slave mode, and External DMA mode.

  Note: DWC_otg core in Host Scatter Gather DMA mode of operation does not support split transfers in the hardware. Only Buffer DMA mode of operation supports split transfers in the hardware and hence generic root hub.
- Includes automatic ping capabilities.
- Supports the Keep-Alive in Low-Speed mode and SOFs in High/Full-Speed modes.

Standards Compliance

- Complies with the *On-The-Go Supplement to the USB 2.0 Specification* (Revision 1.3)
- Complies with the *On-The-Go Supplement to the USB 2.0 Specification* (Revision 2.0).
- Supports *Battery Charging Specification* (Revision 1.1)
- Complies with the *USB 2.0 Link Power Management Addendum* applied to *Universal Serial Bus Specification* (Revision 2.0)
- Supports the UTMI+ Level 3 interface (Revision 1.0, February 25th, 2004). 8-, 16-, and 8/16-bit data buses are supported.
- Supports ULPI interface (Revision 1.1rc, September 1st, 2004) - 8-bit SDR, 4-bit DDR, 6-pin Serial, 3- pin Serial and Carkit.

Configurable Features

- Uses the coreConsultant utility to configure the core to user requirements
- Ability to choose multiple power rails for low power modes
- Choice of multiple DMA modes of operation
- Choice of type of Mac-Phy interface required

Application Interface Features

- Interfaces for the application via the AHB:
  - AHB Slave interface for accessing Control and Status Registers (CSRs), the Data FIFO, and queues
    - Optional AHB Master interface for Data FIFO access when Internal DMA is enabled
    - Supports AHB clock frequencies up to 180 MHz with suitable technology (tested with a standard 0.13-micron technology with SDF, and without post-layout delays, clock tree synthesis or gate-level simulations) for certain configurations only.
- Supports only 32-bit data on the AHB.
- Supports Little or Big Endian mode (selectable by pin).
- Supports INCR4, INCR8, INCR16, INCR, and SINGLE transfers on the AHB Slave interface.
- Supports Split, Retry, and Error AHB responses on the AHB Master interface. Split and retry responses are not generated on the AHB Slave interface. Error Response is generated on the AHB slave interface when the transfer size (HSIZE) is not equal to 32 bits.
- Software-selectable AHB burst type on AHB Master interface
- Handles the fixed burst address alignment. For example, INCR16 is used only when lower addresses [5:0] are all 0.
- Generates AHB Busy cycles on the AHB Master interface
- Takes care of the 1KB boundary breakup

MAC-PHY Interface Features

- Support for the following MAC-Phy Interfaces:
  - UTMI 8/16,
  - ULPI,
  - HSIC,
  - IC USB (for Low/Full speed),
  - FS Shared on UTMI
- The UTMI+ L3 and ULPI can both exist and be selected by software, or only the required interface can be specified during coreConsultant configuration.
- HSIC interface can be selected only if UTMI+ is chosen. HSIC interface cannot be selected otherwise.
- I2C interface (for support of *Mini USB Analog Carkit Interface Specification*, CEA-936, Revision 2). Not intended for use with other devices.

System Memory Architecture

- Supports Slave, External DMA Controller Interface, or Internal DMA modes
- Optional Descriptor-Based Scatter/Gather DMA operation when Internal DMA mode is chosen
- Includes optional interface to an external DMA controller; data is transferred through the AHB Slave interface.

Non-DWORD Alignment Support

- Host Mode:
  - Scatter Gather DMA mode, IN and OUT transfers - Non-DWORD alignment of buffer addresses is supported
  - Buffer DMA and Slave mode, IN and OUT transfers - Non-DWORD alignment of buffer addresses is not supported
- Device Mode:
  - Scatter Gather DMA mode, IN and OUT transfers - Non-DWORD alignment of buffer addresses is supported
  - Buffer DMA and Slave mode, IN and OUT transfers - Non-DWORD alignment of buffer addresses is not supported

Note: Non-DWORD alignment support is available only for buffer addresses and not for descriptors.

Internal Memory Features

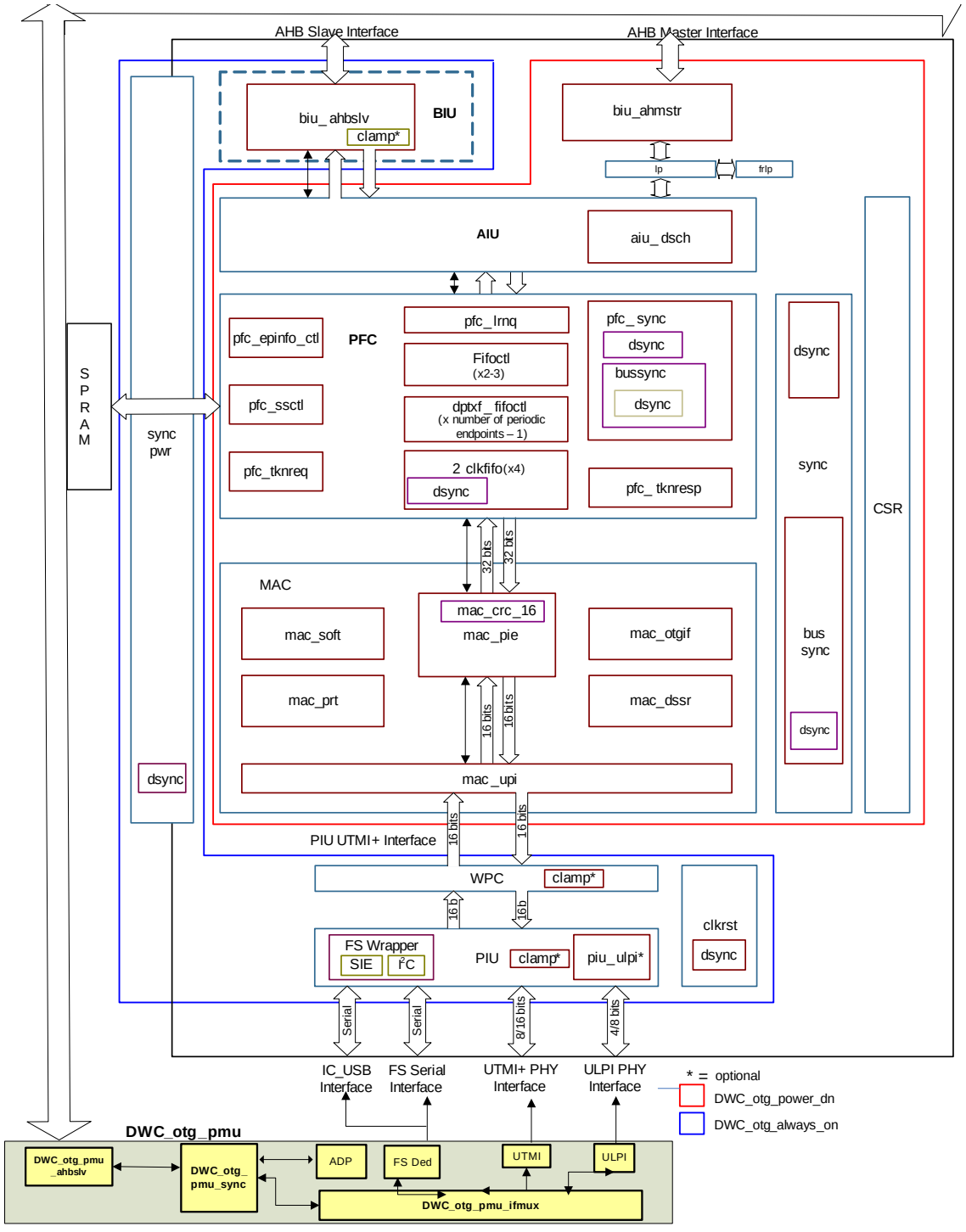
- Optional support for a dedicated transmit FIFO for each of the device IN endpoints in Slave and DMA modes. Each FIFO can hold multiple packets.
- Includes an optional interface for Remote Memory Support used to signal the core of a DMA write complete event on the system.
- Supports packet-based, Dynamic FIFO allocation for endpoints for small FIFOs and flexible, efficient use of RAM.
- Uses single-port RAM instead of dual-port RAM for smaller area and lower power.
- Provides support to change an endpoint's FIFO memory size during transfers.
- Supports endpoint FIFO sizes that are not powers of 2, to allow the use of contiguous memory locations.
- Shares the hardware registers in the Host and Device modes to reduce gate count.
- Optional support for Transmit and Receive thresholding in DMA mode when dedicated Tx FIFO is selected in Device mode. Thresholding and threshold length selectable through global registers. For supporting thresholding, the AHB must be run at 60 MHz or higher.

Software Features

- Software assists hardware for Device mode non-periodic IN sequencing (applicable only in Shared FIFO operation).
- Software handles USB commands (SETUP transactions are detected and their command payloads are forwarded to the application for decoding).
- Software handles USB errors.

Power Optimization Features

- Link Power management Support (Optional- requires additional DWC-HSOTG-LPM license.)
- Several power-saving features including two power rails for advanced power management. The following options are supported:
  - Clock gating,
  - Partial Power Down, and
  - Hibernation - core switched off (optional - requires additional DWC-HSOTG-HIBERNATION license)
  - Extended Hibernation - supported in Device mode only (optional - requires additional DWC-HSOTG-HIBERNATION license)
- PHY clock gating support during USB Suspend, LPM, and Session-Off modes
- AHB clock gating support during USB Suspend and Session-Off modes
- Partial power-off during USB Suspend and Session-Off modes
- Hierarchy to support multiple power rails to enable Hibernation feature during suspend
- Input signals to powered-off blocks driven to safe 0
- Data FIFO RAM chip-select de-asserted when not active
- Data FIFO RAM clock-gating support
- Switching to lower frequency 32-KHz clock support for both Device and Host modes during USB Suspend, LPM, and Session-Off modes



The dwcore_usb2_hsotg datasheet is available at:
http://www.synopsys.com/dw/ipdir.php?ds=dwc_usb_2_0_digital_controllers

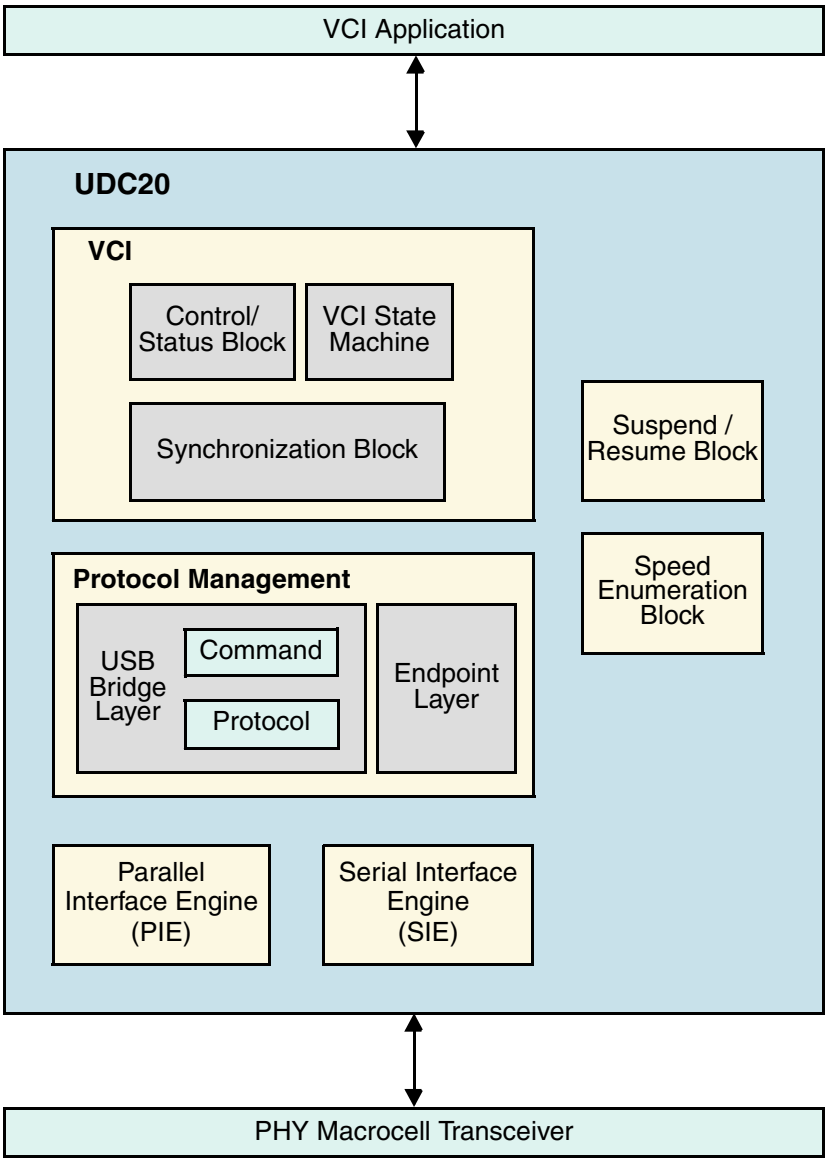
dwc_usb_2_0_device

Synthesizable USB 2.0 Device Controller

The USB 2.0 Device Controller (UDC20) features industry-standard interfaces that easily integrate the USB 2.0 transceiver and application logic. The RapidScript utility builds the core and test environment in source code for the targeted application. Other features include the following:

Features

- Complies with USB 2.0 and USB 1.1 protocols
- Integrates the UDC20/UDCVCI USB device controllers from Synopsys
- Supports high-speed (480 MHz), full-speed (12 MHz) and low-speed (1.5 MHz) operations for UDC20, and supports full-speed and low-speed operations for UDCVCI
- Supports AHB clock (hclk_i) frequencies of 12–133 MHz for UDC-VCI. For UDC20, the range is 16 to 133 MHz.
- Supports up to 16 IN and 16 OUT physical endpoints, which can be tied to different interfaces and configurations to achieve logical endpoints
- Permits user control through memory-mapped control and status registers (CSRs)
- Enables user-configurable endpoint information
- Supports both DMA option and Slave-Only modes
- Supports true scatter-gather DMA implementation
- Supports descriptor-based memory structures in application memory when in DMA mode
- Ideally suited for portable handheld applications requiring optimal memory usage
- Supports adaptive buffering for efficient IN endpoint buffer management
- Completely synchronous design (clock boundary is in the subsystem)
- Supports power management
- In full and high speed operation, UDC-AHB subsystem is compatible with UTMI+ level 3 PHY
- Supports the following UTMI data bus interfaces:
  - Unidirectional 8-bit interface
  - Unidirectional 16-bit interface
  - Bidirectional 8-bit interface
  - Bidirectional 16-bit interface
- ULPI functions defined in the ULPI specification (version 1.0rc) are supported with the following exceptions:
- ULPI in Low Speed mode is not supported
- 60 MHz-only clock speed
- UTMI data width is normally 8 bits input/output
- DDR nibble operation is supported
- OTG, Carkit features are not supported



The dwcore_usb2_device datasheet is available at:

http://www.synopsys.com/dw/ipdir.php?ds=dwc_usb_2_0_digital_controllers

dwc_wiusb_device_controller

Wireless USB Device Controller

Synopsys DesignWare Wireless USB (WiUSB) Device Controller IP, based on the Wireless USB specification from the USB-IF, provides designers with a high-performance WiUSB IP core for SoC integration. The WiUSB Device Controller enables a wide range of portable electronics or PC peripherals the ability to connect without cables and delivers a conservative timing for implementation into a broad range of ASIC and FPGA technologies.

Synopsys designed its DesignWare WiUSB IP core using low-power flows and a low-power architecture, with clock gating and two power rails, to minimize area and power consumption. An extensive verification process, which includes simulation and hardware interoperability testing, enables Synopsys to deliver a high-quality IP core, that lowers overall integration risk and shortens time to results. As a technical contributor to the Certified Wireless USB specification and a member of the WiMedia Alliance standards committee, Synopsys focuses on delivering the highest quality interoperable Wireless USB IP for our customers.

WiMedia Ultra-Wideband (UWB) MAC

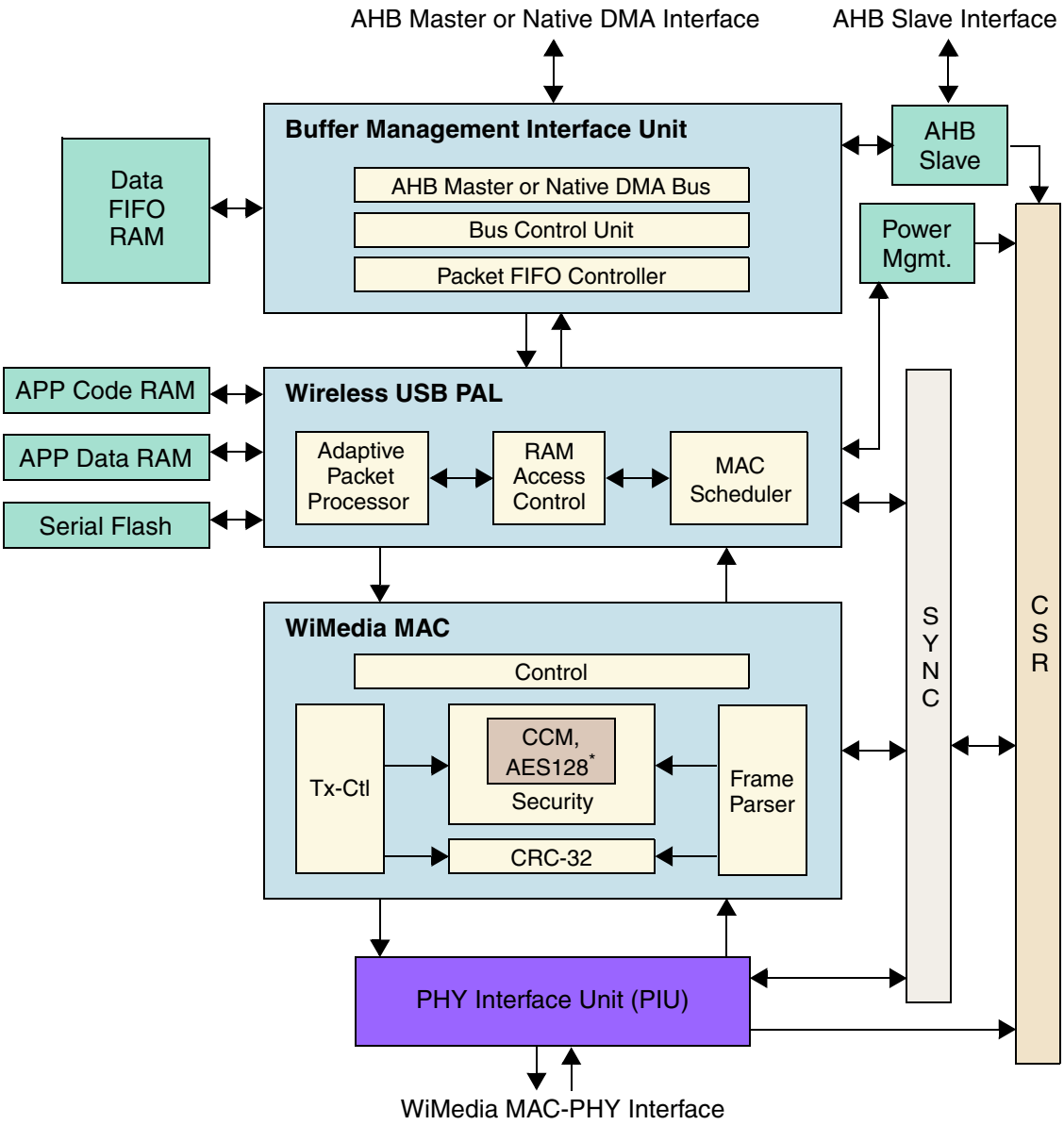
- Supports WiMedia Ultra-Wideband (UWB) Common Radio Platform
- Modular design for power savings in all layers
- Support for MIC generation with UWB AES-128-bit encryption block
- Standard MAC PHY interface for connection to external discrete PHYs or internal integrated PHYs
- Asynchronous clock domains support different PHY frequencies. This allows the use of a separate PHY clock and MAC clocks

Buffer Management Unit (BMU)

- Flexible interface can be configured for high performance and throughput
- AHB Master or Native interface with DMA engine reduces microprocessor loading and maximizes performance
- FIFO sizes are adjustable to tune for performance or die area to focus on throughput or cost

Wireless USB Protocol Adaptation Layer (PAL)

- Protocol Adaptation Layer (PAL) based on Wireless USB from the USB-IF
- Adaptive Packet Processor (APP) allows for post-silicon upgrades to firmware and protocol processing, and additional features (sold separately)
- Device controller includes features for adding CWUSB to a PC peripheral, such as a printer or a portable CE device, such as a camera



The DesignWare dwc_wiusb_device_controller datasheet is available at:

http://www.synopsys.com/dw/ipdir.php?ds=dwc_wiusb_controller

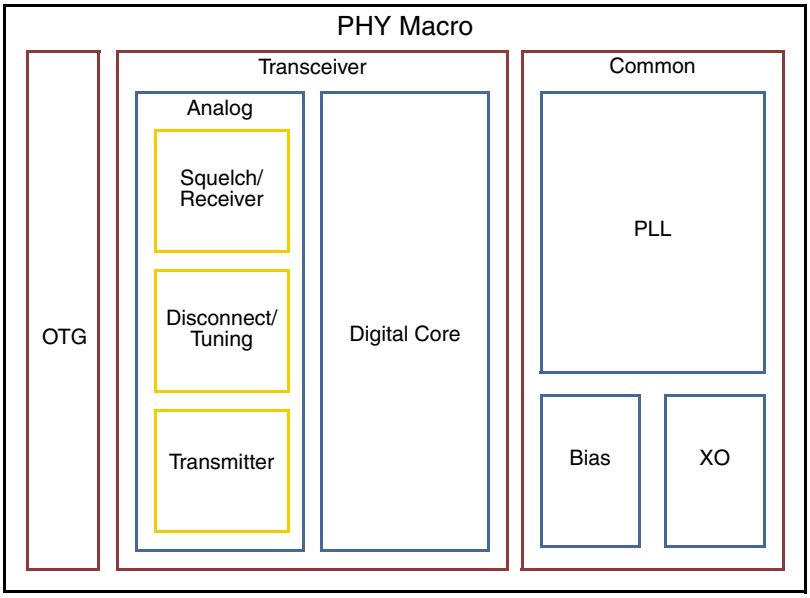
dwc_usb2_nanophy

USB 2.0 nanoPHY

The USB 2.0 nanoPHY provides designers with a complete Physical Layer (PHY) IP solution, designed for low-power mobile and consumer applications such as next-generation handheld game machines, feature-rich smart phones, digital cameras, and portable audio/video players. The DesignWare USB 2.0 nanoPHY IP delivers approximately half the power and die area compared to other solutions, for longer battery life and lower silicon cost. Designed for high yield, the DesignWare USB 2.0 nanoPHY implements architectural features that make it less sensitive to variations in foundry process, device models, package and board parasitics. Other features include the following:

Features

- Complete mixed-signal physical layer for single-chip USB 2.0 OTG and non-OTG applications
- Low power: ~100 mW (during HS packet transmission)
- Small area: ~ 0.6 mm^2
- High yield: Architecture designed to improve key operating margins by having less sensitivity to variations due to foundry process, chip and board parasitics, and process device model variations
- Designed for the latest 55-nm and 65-nm low power (LP) CMOS processes, including shrink geometries
- Low pin count
- USB 2.0 Transceiver Macrocell Interface (UTMI+ Level 3) specification
- 8-bit interface at 60-MHz operation and 16-bit interface at 30-MHz operation
- Hi-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation is compliant with the USB 2.0 OTG Supplement
- Supports all OTG features, including Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Designed for rapid integration with the Synopsys USB 2.0 Hi-Speed OTG controller
- On-chip PLL reduces clock noise and eliminates external clock generator requirement
- Built-in VBUS pulsing and discharge SRP circuitry
- Built-in VBUS threshold comparators
- Supports off-chip charge pump regulator to generate 5-V VBUS signals
- Designed for minimal power dissipation for low-power and bus-powered devices
- Supports Suspend, Resume, and Remote Wakeup modes
- Supports USB 2.0 test modes
- Built-in self test capability for rapid yield and functional testing



The dwc_usb2_nanophy datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_usb2_nanophy.pdf

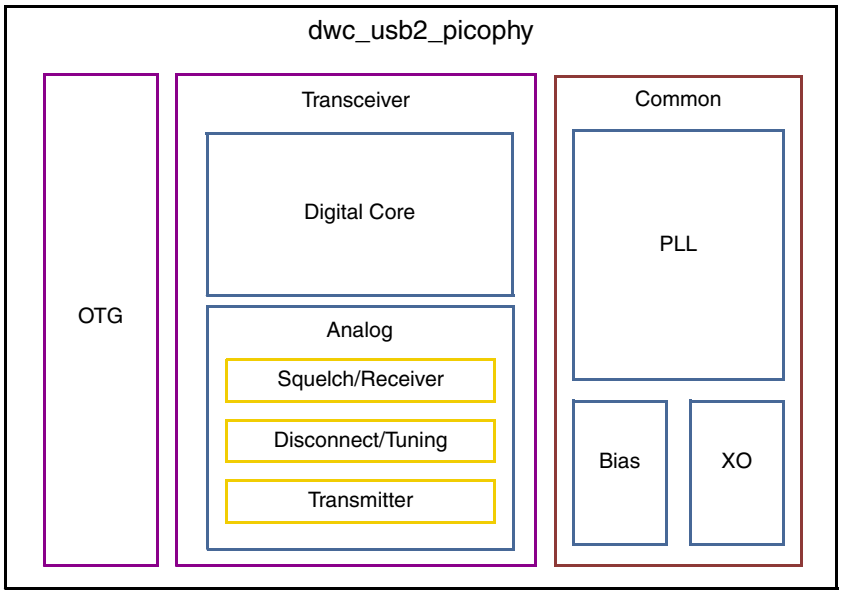
dwc_usb2_picophy
USB 2.0 picoPHY

Optimized for portable applications, the USB 2.0 picoPHY is designed for low power dissipation while active or on standby, small die area for low cost, and process centering for optimal yield and interoperability. The USB 2.0 picoPHY can be implemented as a discrete or integrated physical layer interface for any OTG device that complies with On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification or any host or peripheral application that complies with the USB 2.0 specification.

Other features include the following:

Features

- General features:
  - Implements low power dissipation while active, idle, or on standby
  - Occupies small area
  - Parameter override bits for optimal yield and interoperability
  - High-, full-, and low-speed (Host mode only) termination and signal switching
  - One parallel data interface and clock for high-, full-, and low-speed (Host mode only) USB data transfers
  - Required minimal external components—single resistorand optional single crystal with two capacitors for best operation
  - On-chip PLL to reduce clock noise and eliminate the need for an external clock generator
  - Off-chip charge pump regulator to generate 5 V for Vbus
  - Built-in Self-Test (BIST) circuitry to confirm high-, full-, and low-speed operation
  - Extensive test interface
  - 5v tolerance on D+ and D- lines for 24 hours
  - Optional USB 2.0 picoPHY 1.8-V Regulator
  - Universal Asynchronous Receiver/Transmitter (UART) support to enable the USB 2.0 picoPHY to receive and transmit asynchronous, serial data
- USB 2.0 features
  - 45-Ω termination, 1.5-kΩ pull-up and 15-kΩ pull-down resistors, with support for independent control of the pull-down resistors
  - 480-Mbps high-speed, 12-Mbps full-speed, and 1.5-Mbps low-speed (Host mode only) data transmission rates
  - 8/16-bit unidirectional parallel interfaces for HS, FS, and LS (Host mode only) modes of operation, in accordance with the UTMI+ specification
  - Dual (HS/FS) mode host support
  - Data recovery from serial data on the USB connector
  - SYNC/End-of-Packet (EOP) generation and checking
  - Bit stuffing and unstuffing, and bit-stuffing error detection
  - Non Return to Zero Invert (NRZI) encoding and decoding
  - Bit serialization and deserialization
  - Holding registers for staging transmit and receive data
  - Logic to support suspend, sleep, resume, and remote wakeup operations
  - USB 2.0 test modes
  - Vbus pulsing and discharge Session Request Protocol (SRP) circuit
  - Vbus threshold comparators
  - Battery charging supported to enable devices to draw current in excess of the USB 2.0 specification for charging and/or powering up from dedicated charging ports or charging downstream ports


dwc_usb2_picophy
OTG
Transceiver
Digital Core
Analog
Squelch/Receiver
Disconnect/Tuning
Transmitter
Common
PLL
Bias
XO

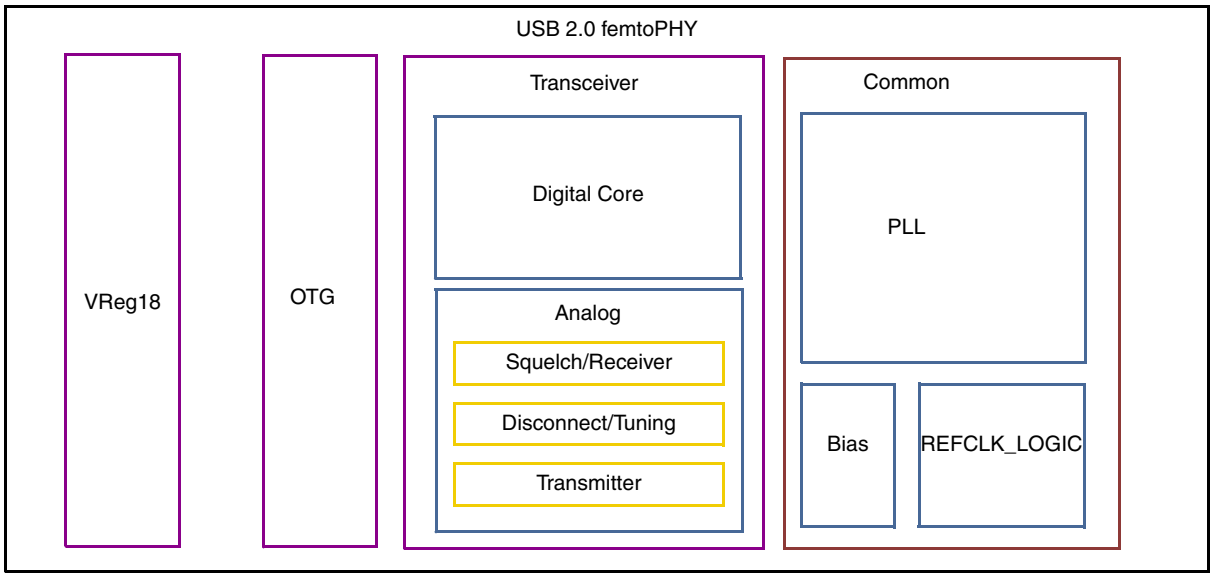
dwc_usb2_femtophy

USB 2.0 femtoPHY

The USB 2.0 femtoPHY provides designers with a complete Physical Layer (PHY) IP solution, designed for low-power mobile and consumer applications such as next-generation handheld game machines, feature-rich smart phones, tablets, digital TVs, and media players. Offering reduced silicon cost and longer battery life, the DesignWare USB 2.0 femtoPHY IP delivers 50% smaller die area and minimizes active and suspend power consumption. The DesignWare USB 2.0 femtoPHY implements the latest USB Battery Charger version 1.2 and USB On-The-Go (OTG) version 2.0 specifications from the USB Implementer's Forum (USB-IF). Other features include the following:

Features

- General features:
  - Implements low power dissipation while active, idle, or on standby
  - Occupies small area
  - Parameter override bits for optimal yield and interoperability
  - High-, full-, and low-speed (Host mode only) termination and signal switching
  - One parallel data interface and clock for high-, full-, and low-speed (Host mode only) USB data transfers
  - Minimal external components requirement—single resistor
  - On-chip PLL to reduce clock noise and eliminate the need for an external clock generator
  - Off-chip charge pump regulator to generate 5 V for Vbus
  - Built-in Self-Test (BIST) circuitry to confirm high-, full-, and low-speed operation
  - Extensive test interface
  - 5v tolerance on D+ and D- lines for 24 hours
  - USB 2.0 femtoPHY 1.8-V Regulator
  - Universal Asynchronous Receiver/Transmitter (UART) support to enable the USB 2.0 femtoPHY to receive and transmit asynchronous, serial data
- USB 2.0 features
  - 45-Ω termination, 1.5-kΩ pull-up and 15-kΩ pull-down resistors, with support for independent control of the pull-down resistors
  - 480-Mbps high-speed, 12-Mbps full-speed, and 1.5-Mbps low-speed (Host mode only) data transmission rates
  - 8/16-bit unidirectional parallel interfaces for HS, FS, and LS (Host mode only) modes of operation, in accordance with the UTMI+ specification
  - Dual (HS/FS) mode host support
  - Data recovery from serial data on the USB connector
  - SYNC/End-of-Packet (EOP) generation and checking
  - Bit stuffing and unstuffing, and bit-stuffing error detection
  - Non Return to Zero Invert (NRZI) encoding and decoding
  - Bit serialization and deserialization
  - Holding registers for staging transmit and receive data
  - Logic to support suspend, sleep, resume, and remote wakeup operations
  - USB 2.0 test modes
  - Vbus pulsing and discharge Session Request Protocol (SRP) circuit
  - Vbus threshold comparators
  - Battery charging supported to enable devices to draw current in excess of the USB 2.0 specification for charging and/or powering up from dedicated charging ports or charging downstream ports



The dwc_usb2_femtophy datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_usb2_femtophy.pdf

dwc_usb_3_0_device

Synthesizable SuperSpeed USB 3.0 Device Controller

The DesignWare SuperSpeed USB 3.0 Device Controller operates as a SuperSpeed USB compliant peripheral. Features include the following:

General Features

- USB-IF certified device
- Verilog-2001 RTL source code
- Software-configurable architecture
- Design trade-offs for area, performance, and power
- Same programming model for SuperSpeed (SS), High-Speed (HS), and Full-Speed (FS)
- LPM protocol in USB 2.0, and U0, U1, U2, and U3 states for USB 3.0
- Dynamic FIFO memory allocation for endpoints
- Descriptor caching and data prefetching used to meet system performance in high-latency systems
- Interrupt moderation
- Clock gating and dual power rail support for low power
- SuperSpeed Inter-Chip (SSIC) and High-Speed Inter-Chip (HSIC) support

Device Features

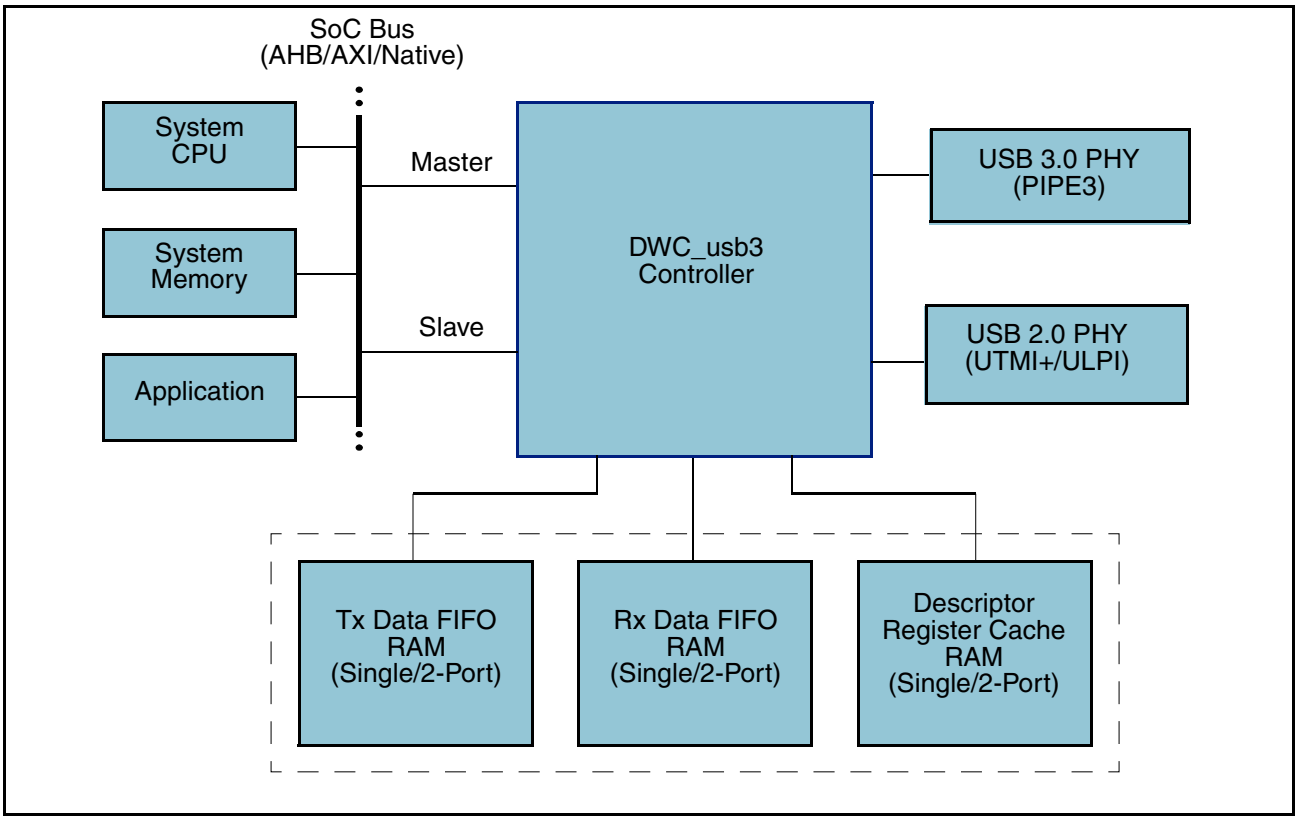
- Supports up to 16 bidirectional endpoints, including control endpoint 0
- Flexible endpoint configuration allows a single area optimized configuration meeting multiple applications/USB set-configuration modes
- Supports simultaneous IN and OUT transfers
- Hardware handles ERDY and burst
- Capability to set up multiple transfers without interrupting the host processor on every transfer
- Stream-based bulk endpoints with controller automatically initiating data movement
- Isochronous endpoints with isochronous data in data buffers or external hardware FIFOs
- External Buffer Control (EBC) feature allows transfers to be setup in external FIFOs
- Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers isochronous, control, and scattered buffering support
- Multiple interrupt support: An endpoint interrupt can be mapped to a selected interrupt line during the endpoint configuration

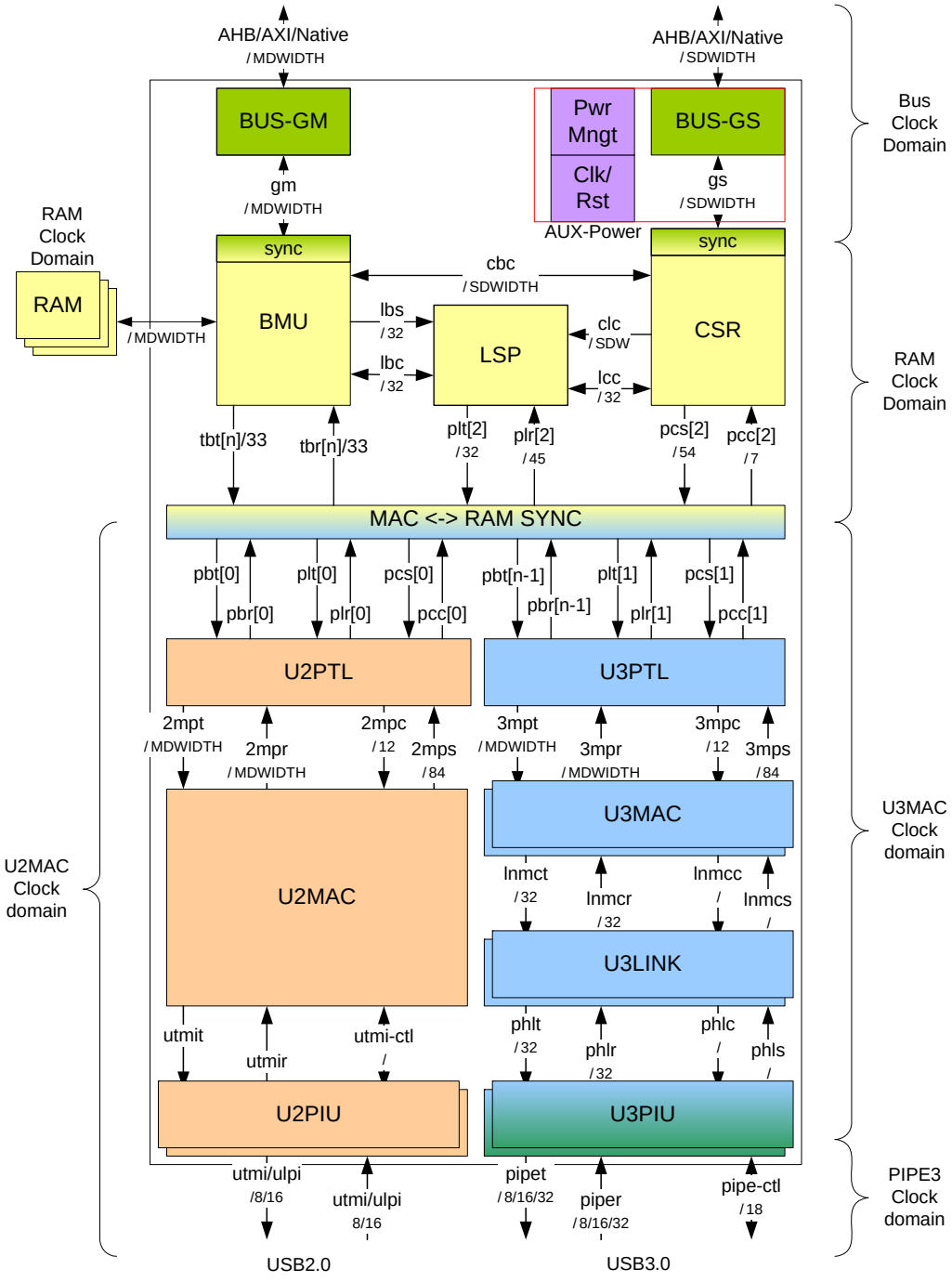
Application Interface Features

- Application interfaces: AHB, AXI, or Native Bus
- Supports 32, 64, or 128-bit data bus, and 32 or 64-bit address bus
- Independent Little or Big Endian (byte invariant) mode selection for both Slave and Master interface
- Independent Endian selection between descriptor and data fetch
- Hardware/software race condition avoidance in systems with bridge
- Concurrent read and write operations to get the best performance of USB 3.0 duplex operation in the AXI bus mode
- AHB Slave interface:
  - Supports all AHB Burst types, including WRAP#
  - Does not generate Split, Retry, or Error responses
- AHB Master interface:
  - Supports Split, Retry, and Error responses
  - Configurable burst type (SINGLE, INCR4, INCR8, INCR16, or INCR)
  - Handles 1KB boundary breakup
- Native interface supports transfer pipeline
- AXI Master interface:
  - Software can select the allowable burst lengths (single, burst 4/8/16/32/64/128/256 as applicable)
  - Handles fixed burst address alignment
  - Supports up to 16 outstanding read/write requests
  - Handles the AXI 4k boundary.
- AXI Slave interface supports all AXI burst types

Debug Features

- CPU read write access to all RAMS
- Most critical state machines' states read through register interface
- FIFO status information visible to software
- Support for upper layer loop back test for testing DMA read and write operation and interrupt generation without any USB traffic
- 64-bit logic analyzer trace port for observing several internal states at the same time


SoC Bus
(AHB/AXI/Native)
System CPU
System Memory
Application
Master
Slave
DWC_usb3 Controller
USB 3.0 PHY (PIPE3)
USB 2.0 PHY (UTMI+/ULPI)
Tx Data FIFO RAM (Single/2-Port)
Rx Data FIFO RAM (Single/2-Port)
Descriptor Register Cache RAM (Single/2-Port)



The dwc_usb_3_0_device datasheet is available at:
https://www.synopsys.com/dw/ipdir.php?c=dwc_usb_3_0_device

dwc_usb_3_0_host

Synthesizable SuperSpeed USB 3.0 Host Controller

The DesignWare SuperSpeed USB 3.0 Host Controller operates as a SuperSpeed USB compliant host. Features include the following:

General Features

- USB-IF certified host
- Verilog-2001 RTL source code
- Software-configurable architecture
- Design trade-offs for area, performance, and power
- Same programming model for SuperSpeed (SS), High-Speed (HS), Full-Speed (FS), and Low-Speed (LS)
- LPM protocol in USB 2.0, and U0, U1, U2, and U3 states for USB 3.0
- Hardware LPM support
- Dynamic FIFO memory allocation for endpoints
- Descriptor caching and data prefetching used to meet system performance in high-latency systems
- Interrupt moderation
- Clock gating and dual power rail support for low power
- SuperSpeed Inter-Chip (SSIC) and High-Speed Inter-Chip (HSIC) support

USB 3.0 xHCI Host Features

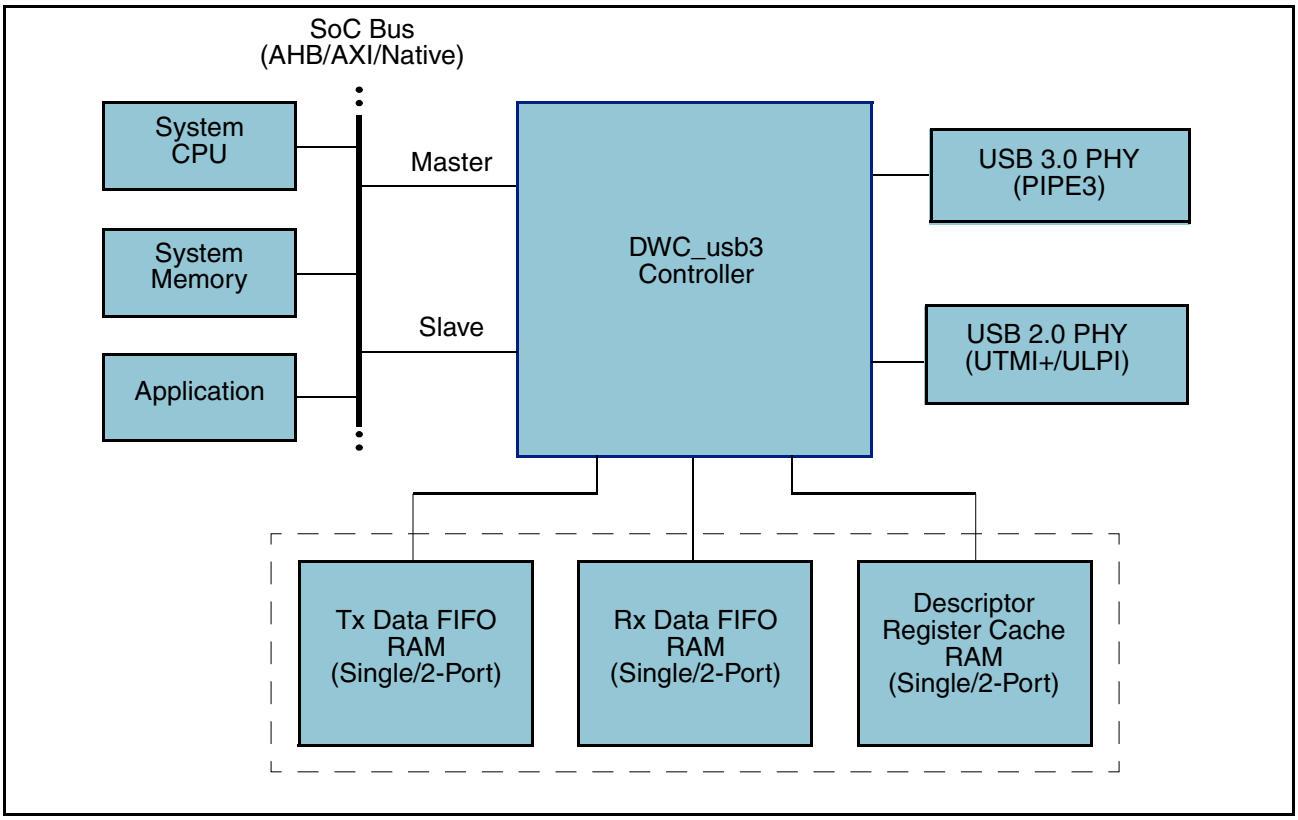
- Supports
  - Up to 127 devices
  - Up to 1024 interrupters
  - Up to 15 USB 2.0 ports and 15 SS ports
  - Up to four SS bus instances, four HS bus instances, and one FS/LS bus instances
  - Standard or open-source xHCI and class drivers
- xHCI 1.0 compatible
- Concurrent IN and OUT transfers to get the full 8 Gbps duplex throughput (interpacket delays and protocol overhead included)
- Concurrent USB 3.0/2.0/1.1 traffic
- Concurrent USB 3.0 transfers on each port (multiple bus instances)

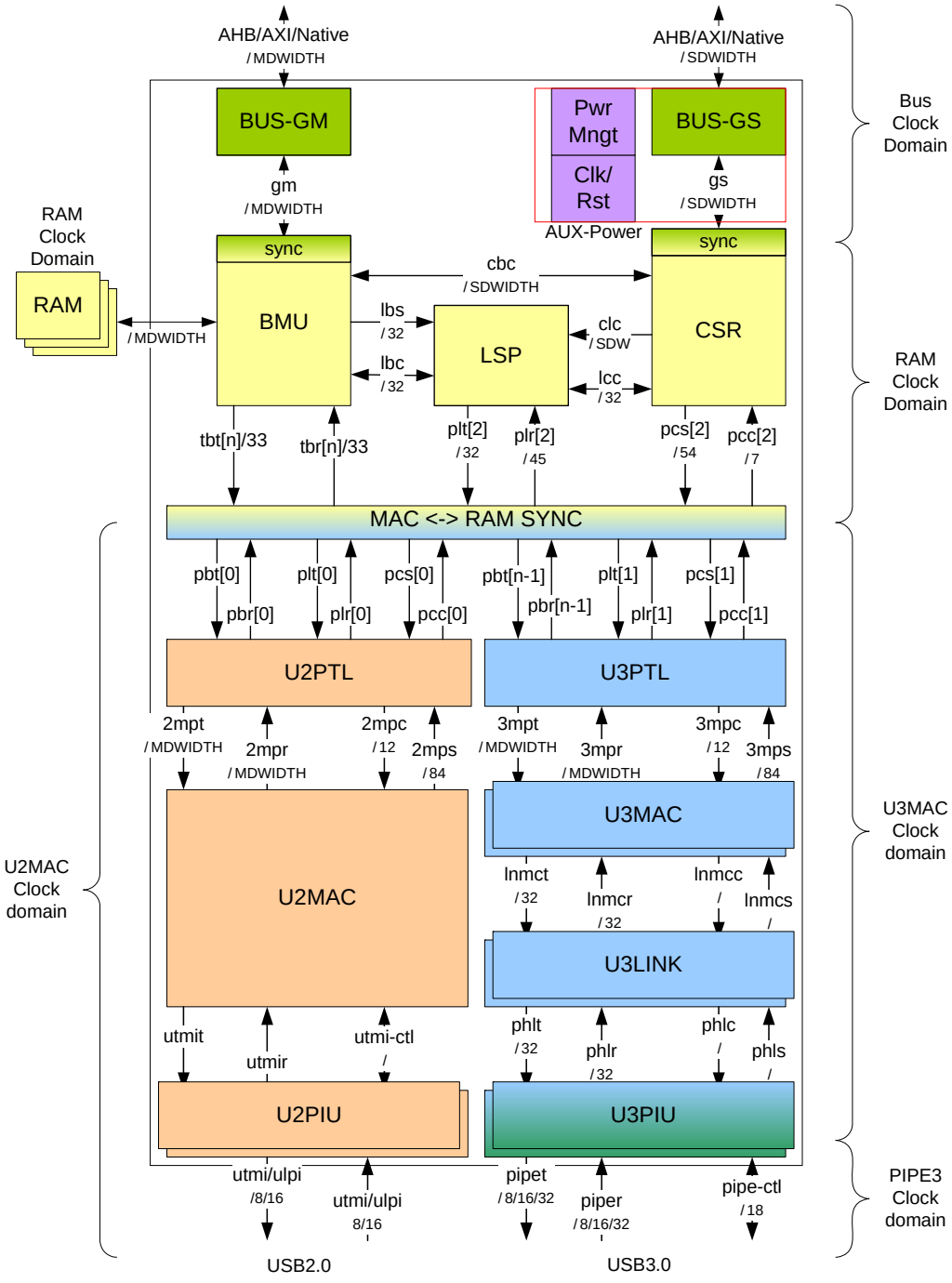
Application Interface Features

- Application interfaces: AHB, AXI, or Native Bus
- Supports 32, 64, or 128-bit data bus, and 32 or 64-bit address bus
- Independent Little or Big Endian (byte invariant) mode selection for both Slave and Master interface
- Independent Endian selection between descriptor and data fetch
- Hardware/software race condition avoidance in systems with bridge
- Concurrent read and write operations to get the best performance of USB 3.0 duplex operation in the AXI bus mode
- AHB Slave interface:
  - Supports all AHB Burst types, including WRAP#
  - Does not generate Split, Retry, or Error responses
- AHB Master interface:
  - Supports Split, Retry, and Error responses
  - Configurable burst type (SINGLE, INCR4, INCR8, INCR16, or INCR)
  - Handles 1KB boundary breakup
- Native interface supports transfer pipeline
- AXI Master interface:
  - Software can select the allowable burst lengths (single, burst 4/8/16/32/64/128/256 as applicable)
  - Handles fixed burst address alignment
  - Supports up to 16 outstanding read/write requests
  - Handles the AXI 4k boundary
- AXI Slave interface supports all AXI burst types

Debug Features

- CPU read write access to all RAMS
- Most critical state machines' states read through register interface
- FIFO status information visible to software
- 64-bit logic analyzer trace port for observing several internal states at the same time


SoC Bus
(AHB/AXI/Native)
System CPU
System Memory
Application
Master
Slave
DWC_usb3 Controller
USB 3.0 PHY (PIPE3)
USB 2.0 PHY (UTMI+/ULPI)
Tx Data FIFO RAM (Single/2-Port)
Rx Data FIFO RAM (Single/2-Port)
Descriptor Register Cache RAM (Single/2-Port)



The dwc_usb_3_0_host datasheet is available at:
https://www.synopsys.com/dw/ipdir.php?c=dwc_usb_3_0_host

dwc_usb_3_0_drd

Synthesizable SuperSpeed USB 3.0 Dual Role Device Controller

The DesignWare SuperSpeed USB 3.0 Dual Role Device Controller is a set of synthesizable building blocks for implementing a complete USB 3.0 DRD interface. Features include the following:

General Features

- USB-IF certified host and device
- Verilog-2001 RTL source code
- Software-configurable architecture
- Design trade-offs for area, performance, and power
- Static Device and Host mode (supports Device or Host mode separately, and not simultaneously)
- Same programming model for SuperSpeed (SS), High-Speed (HS), Full-Speed (FS), and Low-Speed (LS)
- LPM protocol in USB 2.0, and U0, U1, U2, and U3 states for USB 3.0
- Hardware LPM support in host mode
- Dynamic FIFO memory allocation for endpoints
- Descriptor caching and data prefetching used to meet system performance in high-latency systems
- Interrupt moderation
- Clock gating and dual power rail support for low power
- ACA (Accessory Charger Adapter) support
- SuperSpeed Inter-Chip (SSIC) and High-Speed Inter-Chip (HSIC) support

Device Features

- Supports up to 16 bidirectional endpoints, including control endpoint 0
- Flexible endpoint configuration allows a single area optimized configuration meeting multiple applications/USB set-configuration modes
- Simultaneous IN and OUT transfer support
- Hardware handles ERDY and burst
- Capability to set up multiple transfers without interrupting the host processor on every transfer
- Stream-based bulk endpoints with controller automatically initiating data movement
- Isochronous endpoints with isochronous data in data buffers or external hardware FIFOs
- External Buffer Control (EBC) feature allows transfers to be setup in external FIFOs
- Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers, isochronous, control, and scattered buffering support
- Multiple interrupt support: An endpoint interrupt can be mapped to a selected interrupt line during the endpoint configuration

USB 3.0 xHCI Host Features

- Supports
  - Up to 127 devices
  - Up to 1024 interrupters
  - Up to 15 USB 2.0 ports and 15 SS ports
  - Up to four SS bus instances, four HS bus instances, and one FS/LS bus instances
  - Standard or open-source xHCI and class drivers
- xHCI 1.0 compatible
- Concurrent IN and OUT transfers to get the full 8 Gbps duplex throughput (interpacket delays and protocol overhead included)
- Concurrent USB 3.0/2.0/1.1 traffic
- Concurrent USB 3.0 transfers on each port (multiple bus instances)

USB 2.0 OTG Add-On Features

- Session Request Protocol (SRP)
- Host Negotiation Protocol (HNP)
- Filters for OTG-specific PHY interface signals
- Software configurable OTG 2.0 modes of operation
- OTG 2.0 support:
  - ADP (Attach detection Protocol)
  - ACA (Accessory Charger Adapter)

USB 3.0 OTG Add-On Features

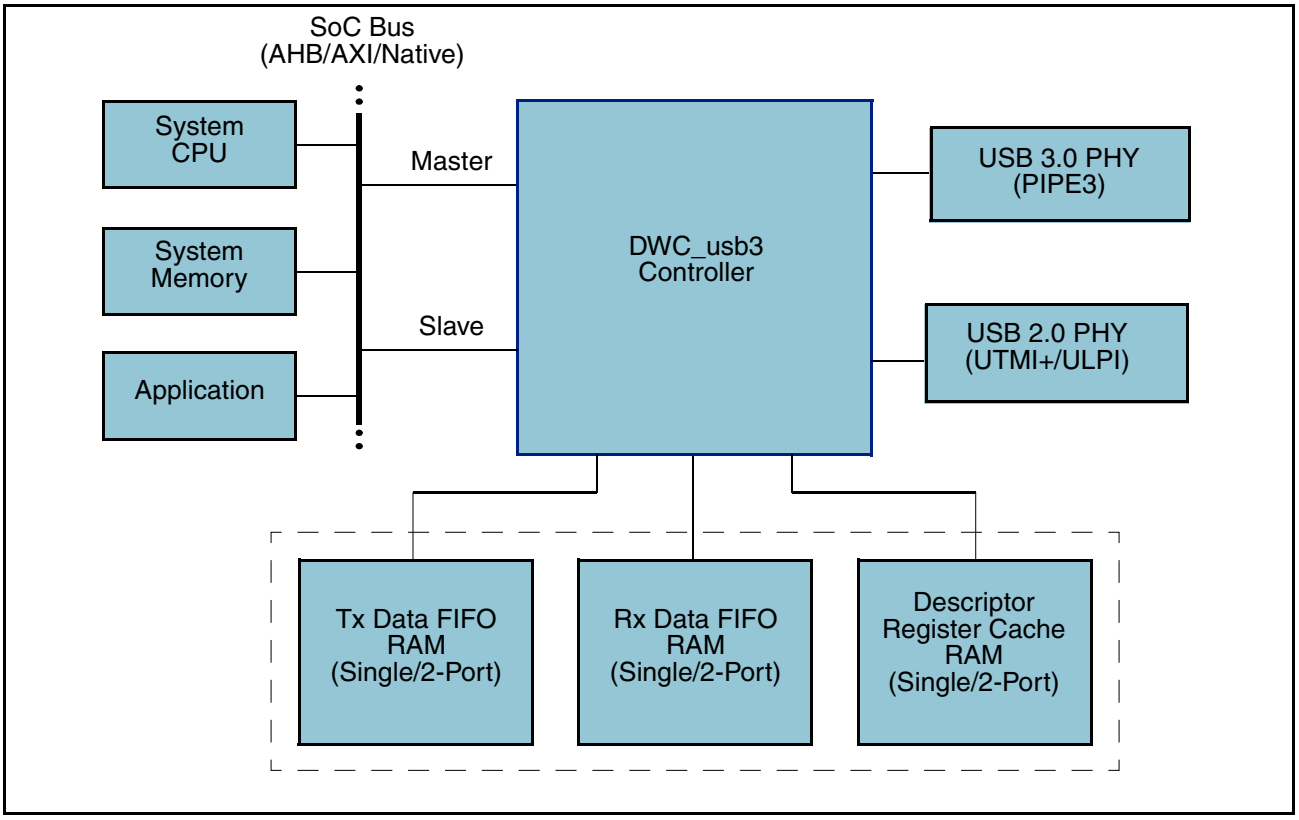
- Session Request Protocol (SRP)
- Host Negotiation Protocol (HNP) in OTG 2.0
- Role Swap Protocol (RSP) in OTG 3.0
- SS, HS, and FS support
- Both categories of targeted hosts: Embedded Hosts and On-The-Go
- Single port only. No support for Multi-port in Host mode
- ADP (Attach Detection Protocol)
- ACA (Accessory Charger Adapter)

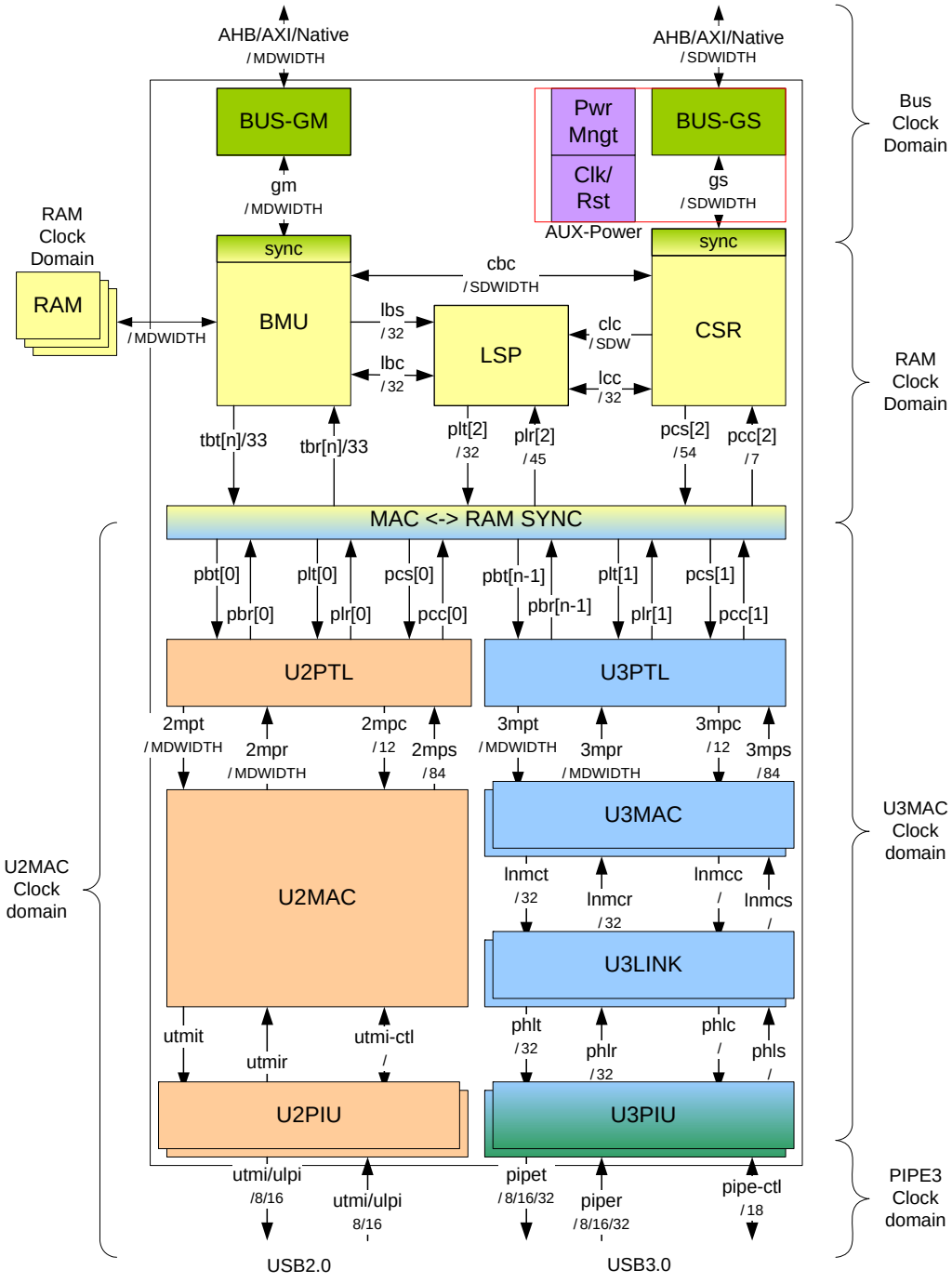
Application Interface Features

- Application interfaces: AHB, AXI, or Native Bus
- Supports 32, 64, or 128-bit data bus, and 32 or 64-bit address bus
- Independent Little or Big Endian (byte invariant) mode selection for both Slave and Master interface
- Independent Endian selection between descriptor and data fetch
- Hardware/software race condition avoidance in systems with bridge
- Concurrent read and write operations to get the best performance of USB 3.0 duplex operation in the AXI bus mode
- AHB Slave interface:
  - Supports all AHB Burst types, including WRAP#
  - Does not generate Split, Retry, or Error responses
- AHB Master interface:
  - Supports Split, Retry, and Error responses
  - Configurable burst type (SINGLE, INCR4, INCR8, INCR16, or INCR)
  - Handles 1KB boundary breakup
- Native interface supports transfer pipeline
- AXI Master interface:
  - Software can select the allowable burst lengths (single, burst 4/8/16/32/64/128/256 as applicable)
  - Handles fixed burst address alignment
  - Supports up to 16 outstanding read/write requests
  - Handles the AXI 4k boundary
- AXI Slave interface supports all AXI burst types

Debug Features

- CPU read write access to all RAMS
- Most critical state machines' states read through register interface
- FIFO status information visible to software
- Support for upper layer loop back test for testing DMA read and write operation and interrupt generation without any USB traffic (in Device Mode)
- 64-bit logic analyzer trace port for observing several internal states at the same time





The dwc_usb_3_0_drd datasheet is available at:
https://www.synopsys.com/dw/ipdir.php?c=dwc_usb_3_0_drd

dwc_usb_3_0_hub

Synthesizable SuperSpeed USB 3.0 Hub Controller

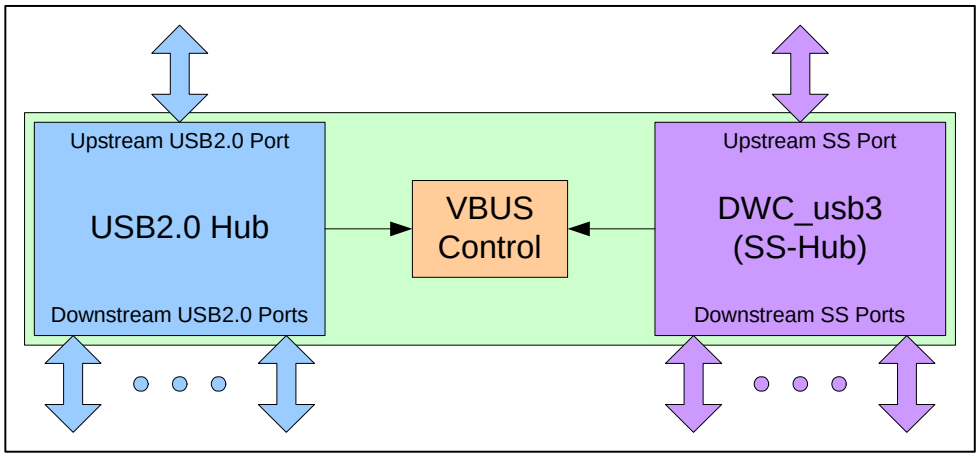
The DesignWare SuperSpeed USB 3.0 Hub Controller is a set of synthesizable building blocks for implementing a complete USB 3.0 hub interface. Features include the following:

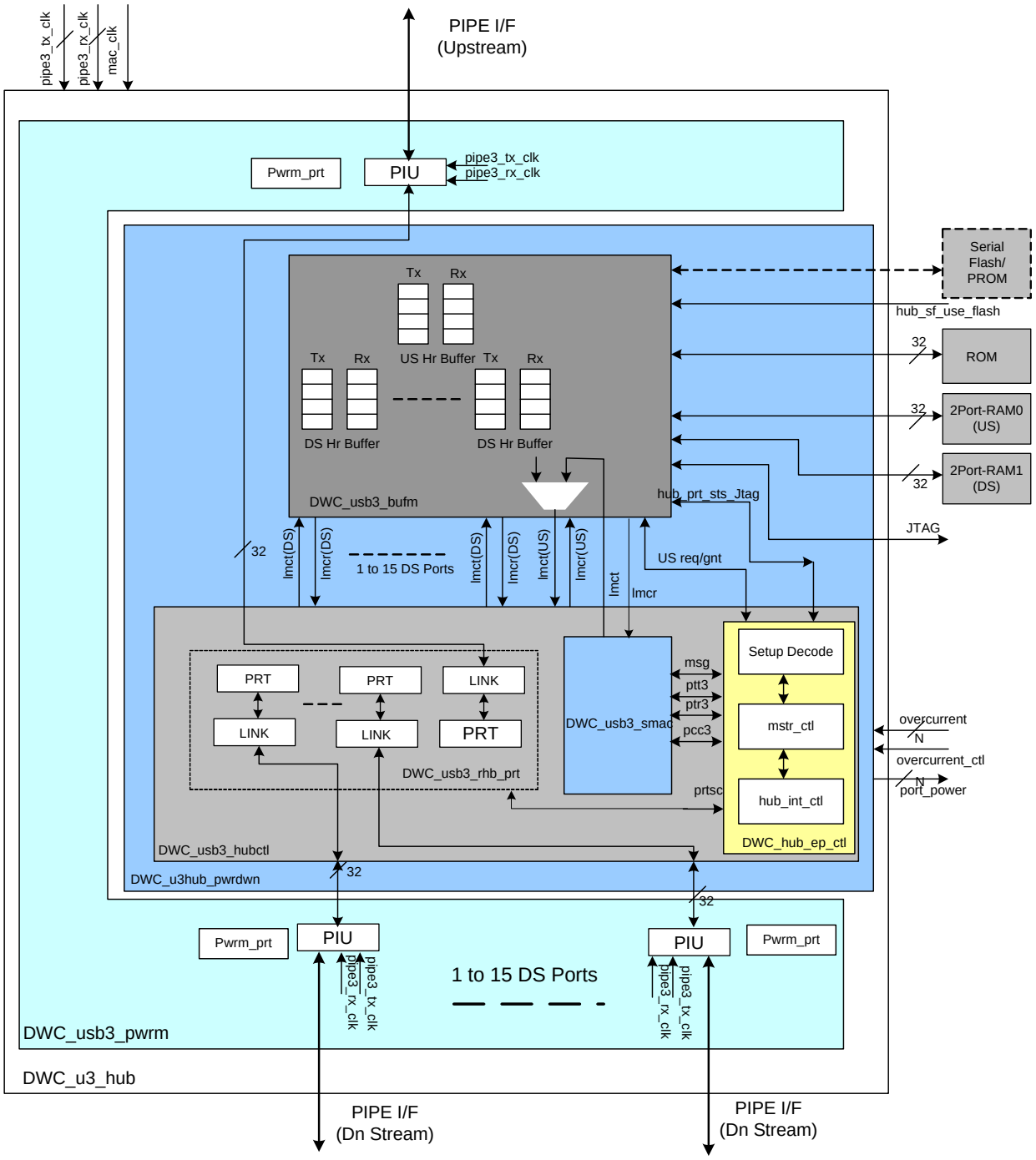
General Features

- Verilog-2001 RTL source code
- Software-configurable architecture
- Design trade-offs for area, performance, and power

USB 3.0 Hub (SuperSpeed Only) Features

- Supports SS only. This can be integrated with an existing USB 2.0 Hub controller to create an USB 3.0 Hub controller
- One upstream port
- 1 to 15 configurable number of downstream ports
- One time configurable software Hub descriptors stored in ROM
- Optional Xilinx Serial-Flash Interface, which overrides the controller. This enables the core to use the descriptors stored in the Xilinx Serial-Flash instead of using the descriptors stored in the ROM
- Optional JTAG port for debug purpose





The dwc_usb_3_0_hub datasheet is available at:
https://www.synopsys.com/dw/ipdir.php?c=dwc_usb_3_0_hub

dwc_usb3.0_femtophy

USB 3.0 femtoPHY IP

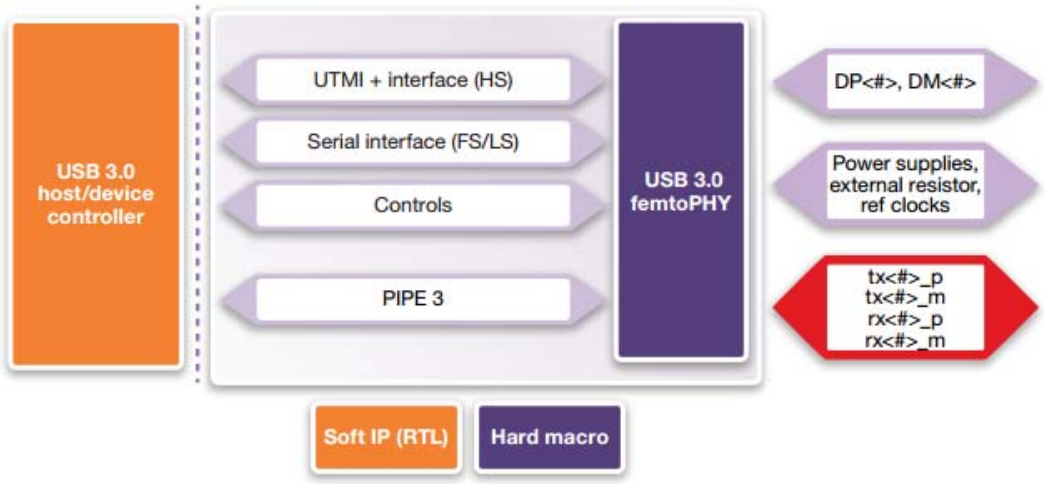
The Synopsys DesignWare® USB 3.0 femtoPHY provides designers with a complete physical (PHY) layer IP solution for low-power mobile and consumer applications, such as digital cameras and networking and storage as well as next-generation, feature-rich smartphones, tablets, digital TVs, and media players requiring high throughput USB capability. Offering reduced silicon cost and longer battery life, the USB 3.0 femtoPHY IP occupies 50% smaller die area and minimizes active and suspend power consumption.

The USB 3.0 femtoPHY implements the latest USB Battery Charging version 1.2 and USB On-The-Go (OTG) specifications from the USB Implementer's Forum (USB-IF). Architected for the industry's most advanced 1.8-V process technologies, the USB 3.0 femtoPHY is designed to minimize effects due to variations in foundry process, device models, packages, and board parasitics.

When combined with the DesignWare Dual-Role Device (DRD), Host, or Device digital controllers and verification IP, the USB 3.0 femtoPHY delivers a complete low-power and small die area solution for advanced system-on-chip (SoC) designs.

Features

- Includes all circuitry needed for operation at all USB speeds (SuperSpeed, High-Speed, Full-Speed, Low-Speed)
- Optimized PHY area (< 0.5 mm^2 macro)
- Low power consumption (~70 mW SuperSpeed, ~50 mW High-Speed)
- Fully compatible with the Synopsys DesignWare USB 3.0 Host, Dual-Role Device, and Device Controllers
- Supports all power management features
- Single reference clock input for all USB speeds
- Wide range of reference clocks supported: 19.2, 20, 24, 25, 26, and 100 MHz
- Integrated 3.3-V-to-2.5/1.8-V regulator in PHY hard macro
- Advanced, built-in diagnostics including SuperSpeed 5-Gbps on-chip "sampling scope"
- Powerful debug capabilities
- IEEE standards 1149.1 and 1149.6 (JTAG) boundary scan for internal visibility and control



The DesignWare USB 3.0 femtoPHY IP Solution datasheet is available at:

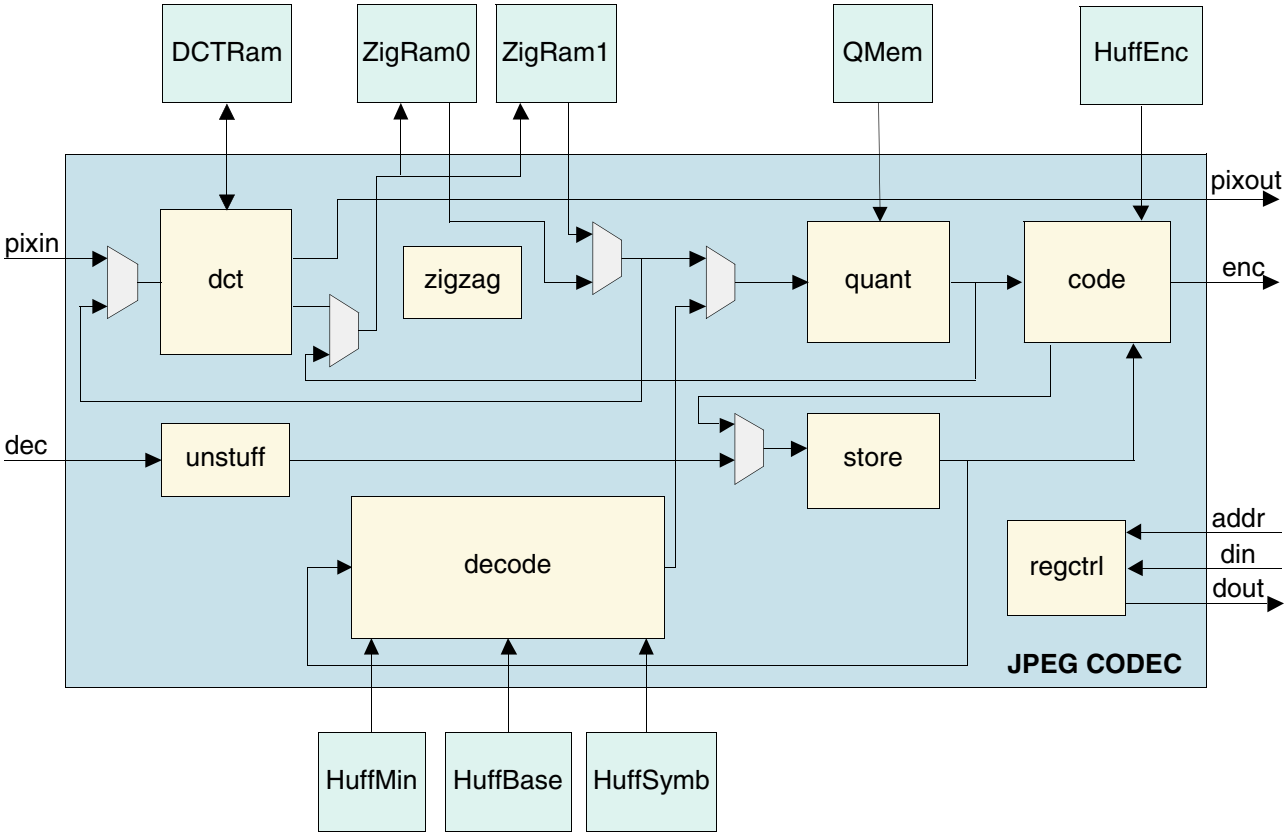
https://www.synopsys.com/dw/doc.php/ds/c/dwc_usb3_femtophy.pdf?fe=y

dwc_jpeg
Synthesizable JPEG CODEC

The Synopsys DesignWare JPEG CODEC is part of an SoC-based multimedia solution that enables fast and simple image compression and decompression. The simplicity of the design allows for easy SoC integration, high-speed operation, and suitability for multimedia and color printing applications. Individual Encoder and Decoder products are available from Synopsys.

Other Features

- 100% baseline ISO/IEC 10918-1 JPEG-compliant
- Verified in hardware
- 8-bit channel pixel depths
- Up to four programmable quantization tables
- Single-clock Huffman coding and decoding
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable Minimum Coded Unit (MCU)
- Encoding/decoding support (non-simultaneous)
- Single-clock per pixel encoding and decoding according to the JPEG baseline algorithm
- Hardware support for restart marker insertion
- Support for single, grayscale components
- Support for up to four channels of component color
- Internal register interface
- Fully synchronous design
- Available as fully functional and synthesizable VHDL or Verilog
- Includes testbench
- Simple external interface
- Four-channel interface
- Low gate count-total gate count is 35K gates
- Stallable design



The dwcore_jpeg_codec datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_jpeg.pdf

DWC_hdmi_rx

HDMI Receiver Controllers

The DesignWare Cores HDMI Receiver Controller includes the DWC_hdmi_rx core and its verification environment. The HDMI RX controller permits digital video, audio, and control data reception transmitted via a HDMI (High-Definition Multimedia Interface). DWC_hdmi_rx includes a High-Bandwidth Digital Content Protection (HDCP) decryption and control unit that enables the reception of content protected material.

In addition, the DWC_hdmi_rx core is used to post-process incoming data with respect to the following:

- Protocol-dependent stream
- Stream de-multiplexing
- Content protection, scheme-related decryption
- Packet assembly and formatting next to video
- Audio output stream formatting

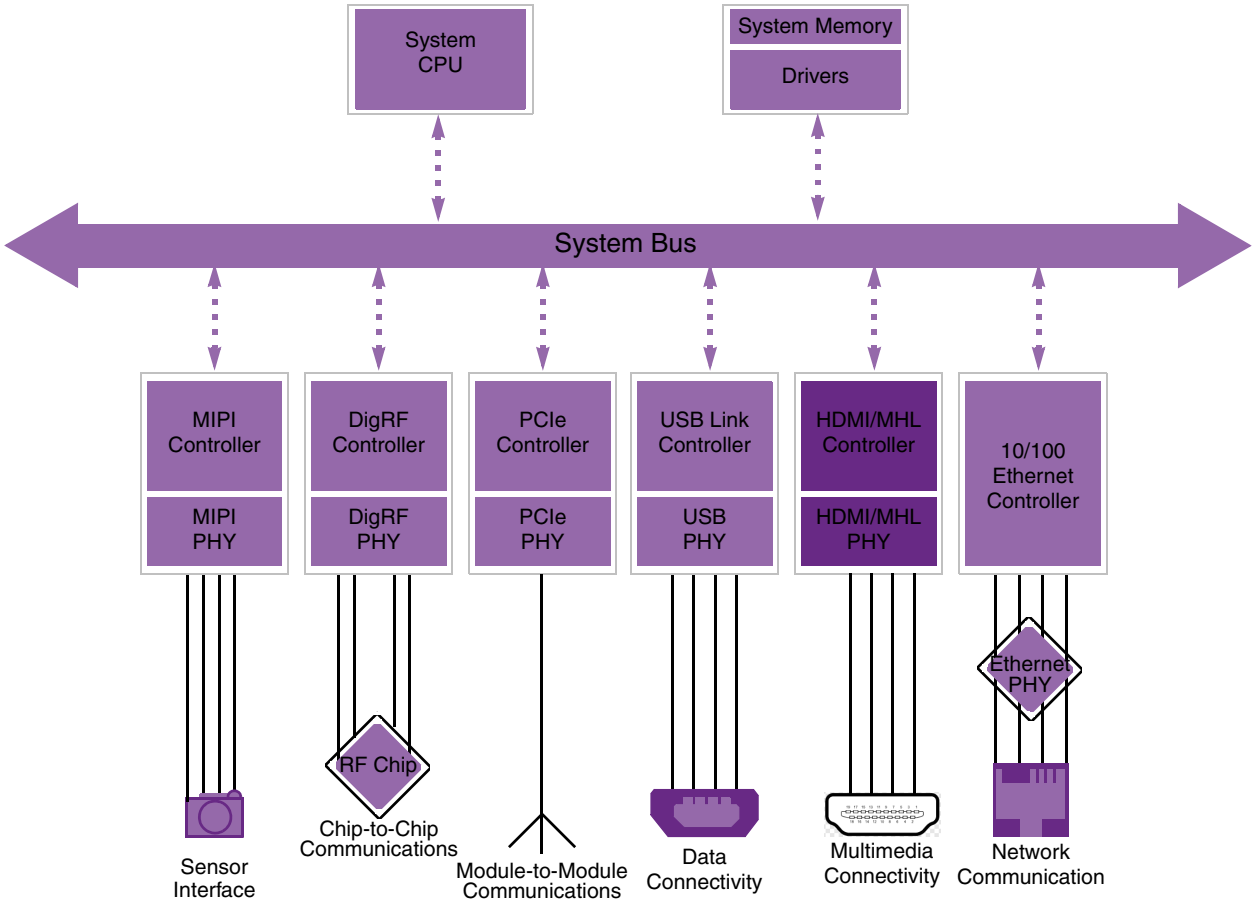
In addition to these native HDMI-/DVI-related tasks, a mode detection unit is provided to allow measurements in non-CEA-861 video modes.

The DWC_hdmi_rx digital core is designed to interface with the Synopsys HDMI 1.4b and 2.0 Receiver Physical Layer (DWC HDMI TX PHY), enabling the integration of a complete HDMI 1.4b and 2.0 Receiver interface.

Features

- HDMI 1.4b- and 2.0-compliant receiver, supporting word data rates up to 600 MHz
- Single-channel DVI 1.0 backward compatibility
- HDCP 1.4 and 2.2
- MHL 2.2
- Video input modes:
  - RGB 4:4:4
    - 8-bit normal color mode
    - 10-, 12-, and 16-bit deep color mode
  - YCbCr 4:2:2 with 8-, 10-, and 12-bit color depth
  - YCbCr 4:4:4
    - 8-bit normal color mode
    - 10-, 12-, and 16-bit deep color mode
  - YCbCr 4:2:0 with 8-, 10-, 12-, and 16-bit color depth (HDMI 2.0)
  - All 3d video formats (HDMI 1.4b)
  - Up to 4K x 2K video formats (HDMI 1.4b)
  - All CEA-861-E video formats (HDMI 1.4b)
  - All CEA-861-F video formats (HDMI 2.0)
- Gamut metadata reception provisions for profiles: P0, P1, P2, and P3
- Audio data reception provisions for:
  - L-PCM
  - L-PCM multi-channel
  - Standard bit-rate compressed audio
  - 1-bit audio (DSD)
  - Compressed 1-bit audio (DST) and high bit-rate (HBR) compressed audio (for example, DolbyTrueHD, DTS HD Master Audio)
  - Multi-stream audio (L-PCM and NL-PCM)[1]
  - One Bit Multistream (DSD)[1]
- PVO interface remapping support for YCbCr 4:2:0 format
- Optional CBUS interface (when MHL supported)
- Optional CEC controller
- Optional HDCP Repeater
- Enhanced clock crossing
- Configurable number of positive-edge-triggered flip-flops connected for data synchronization
- Leda support

1. DWC_HDMI_RX_20 license required



The DesignWare DWC_hdmi_rx datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_hdmi_rx_csds.pdf

DWC_hdmi_tx

HDMI Transmitter Controller

The DesignWare Cores HDMI Transmitter Controller includes the DWC_hdmi_tx core and its verification environment. Synopsys also provides the coreConsultant tool for automated configuration, simulation, and synthesis of the DWC_hdmi_tx core.

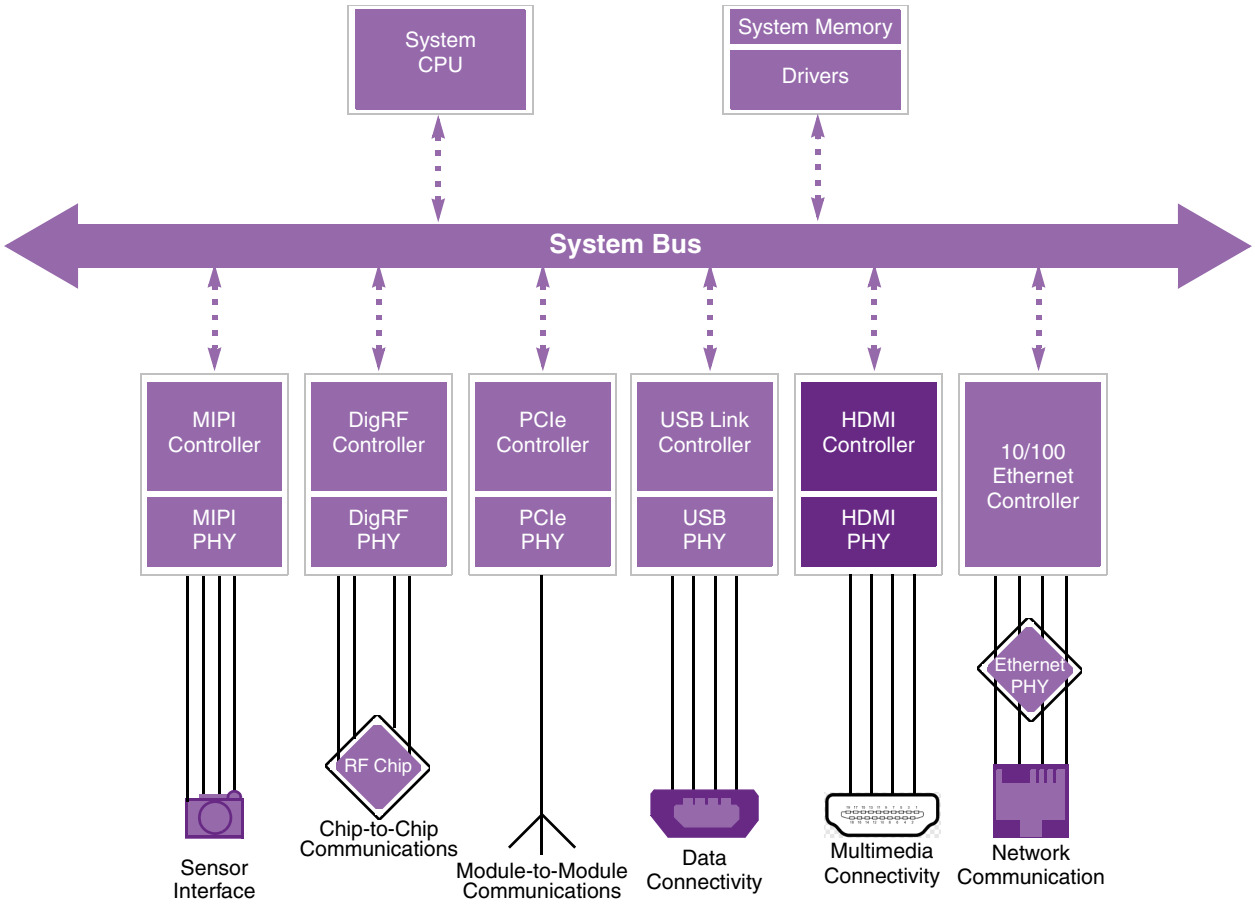
The HDMI TX Controller can be configured with or without a High-bandwidth Digital Content Protection (HDCP) system. If you want HDCP enabled, you need an additional license. The HDMI TX digital core is designed to interface with the Synopsys HDMI Transmitter Physical Layer (DWC HDMI TX PHY), enabling the integration of a complete HDMI Transmitter interface.

Features

- Supported video formats:
  - All CEA-861-E video formats up to 1080p at 60 Hz and 720p/1080i at 120 Hz:
- Optional HDMI 1.4b video formats: (configuration dependent)
  - All CEA-861-E video formats up to 1080p at 120 Hz
  - HDMI 1.4b 4K x 2K video formats
  - HDMI 1.4b 3D video modes with up to 340 MHz (TMDS clock)
- HDMI 2.0 video formats (configuration dependent) – All CEA-861-F video formats
- Supported colorimetry:
  - 24/30/36/48-bit RGB 4:4:4
  - 24/30/36/48-bit YCbCr 4:4:4
  - 16/20/24-bit YCbCr 4:2:2
  - 24/30/36/48-bit YCbCr 4:2:0
  - xvYCC601
  - xvYCC709
- Optional HDMI 1.4b colorimetry:
  - sYCC601
  - Adobe RGB
  - Adobe YCC601
- Optional color space converter (CSC):
  - RGB(4:4:4) to/from YCbCr(4:4:4 or 4:2:2)
- Optional HDMI 1.4b supported Infoframes:
  - Audio infoFrame packet extension to support LFE playback level information
  - AVI infoFrame packet extension to support YCC Quantization range (Limited Range, Full Range)
  - AVI infoFrame packet extension to support Content type (Graphics, Photo, Cinema, Game)
  - NTSC VBI infoframe packet extension to support the carriae of SCTE 127 [29] payloads containing VBI data
- Supported Audio formats:
  - Uncompressed audio formats: IEC60958 L-PCM audio samples
  - Compressed audio formats: IEC61937 compressed non-linear PCM: AC-3, MPEG-1/-2 Audio, DTS®, MPEG-2/-4 AAC, ATRAC, WMA, MAT
  - HBR audio formats: Dolby® True-HD and DTS-HD Master Audio
  - Multistream audio (L-PCM and IEC61937 compressed non-linear PCM)
- Up to 192 kHz IEC60958 audio sampling rate (for IEC61937 compressed audio: up to 1539 kHz for HDMI 2.0 and up to 768 kHz for HDMI 1.4b)
- Pixel clock from 13.5 MHz up to 600 MHz
- Option to remove pixel repetition clock (prepclk) from HDMI TX interface for an easy integration with third-party HDMI TX PHYs
- Flexible synchronous enable per clock domain to enable functional power down modes
- AMBA APB 3.0 register access
- I^2C DDC, EDID block read mode
- SCDC I^2C DDC access
- TMDS Scrambler to enable support for 2160p@60Hz with RGB/YCbCr 4:4:4 or YCbCr 4:2:2
- YCbCr 4:2:0 support to enable 2160p@60Hz at

Features (*continued*)

- YCbCr 4:2:0 support to enable 2160p@60Hz at lower HDMI link speeds
- Advanced PHY testability
- Integrated CEC hardware engine
- Synopsys and external PHY interfaces
- Configurable number of positive-edge-triggered flip-flops connected for data synchronization
- Single-channel DVI 1.0 backward compatibility (dual-link DVI not supported)



The DesignWare DWC_hdmi_tx datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_hdmi_tx_csds.pdf

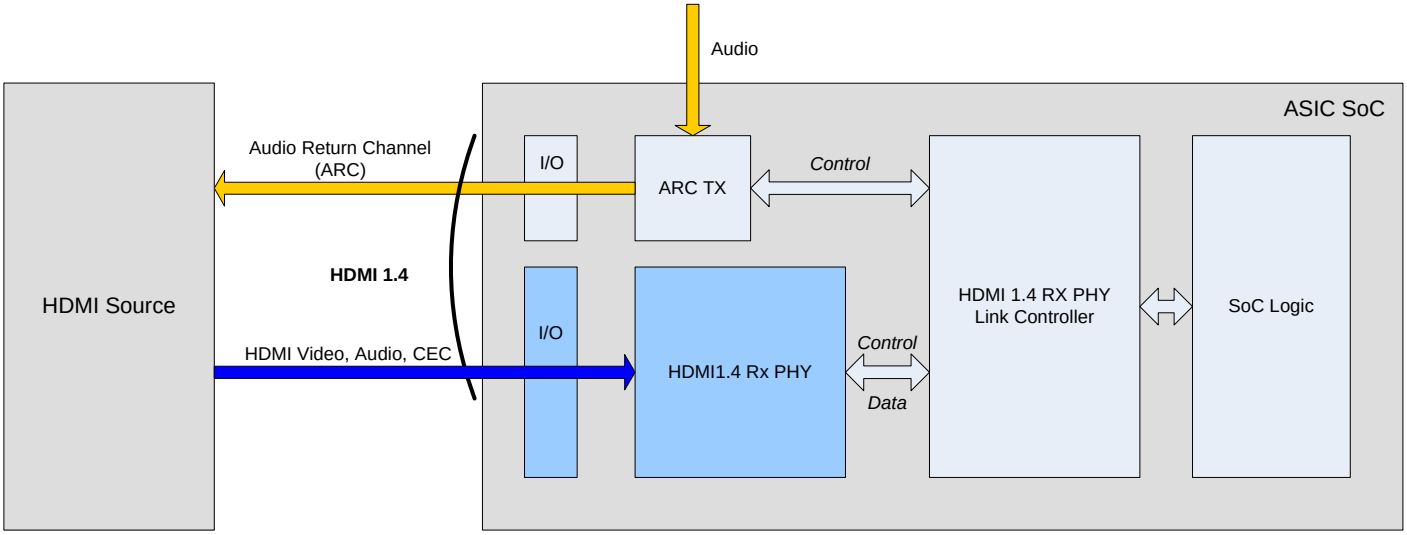
dwc_hdmi_rx_phy

HDMI 1.4 RX PHY IP

The HDMI 1.4 RX PHY IP interface implements the analog front-end of the HDMI receiver, sampling and deserialization of the three data streams and all the digital circuitry for operating mode management, providing a digital interface to the Link Controller. It integrates auto-calibrated input termination resistors and automatic adaptive line equalization to support long cables. An additional clock receiver is included for reference system clock reception.

Features

- Four Levels of Equalization for long cable support and clean signals
- Adaptive equalization in RX core to compensate for the signal attenuation and inter-symbol interference caused by long cables
- Integrated auto-calibrated 50? input termination resistors in RX core
- Support for 5V IO on all nodes (down to 28-nm nodes)
- Aggressive ESD protection Input clock from 25 MHz to 340 MHz range
- Support for 3D formats, 4K x 2K resolution, 720p@100 Hz, 720i@200 Hz, 1080p@60 Hz or 1080i/720i@120 Hz HDTV display resolutions and up to QXGA graphic display resolutions
- Link Controller interface with 24 bit SDR data access, with DATAEN, VERSYNC, HORSYNC and CTRL[3:0] signals (only for HDMI RX PHY Gen2)
- Up to 10.2 Gbps aggregate bandwidth



The DesignWare Cores HDMI 1.4 RX IP Solution datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_hdmi_rx_csds.pdf

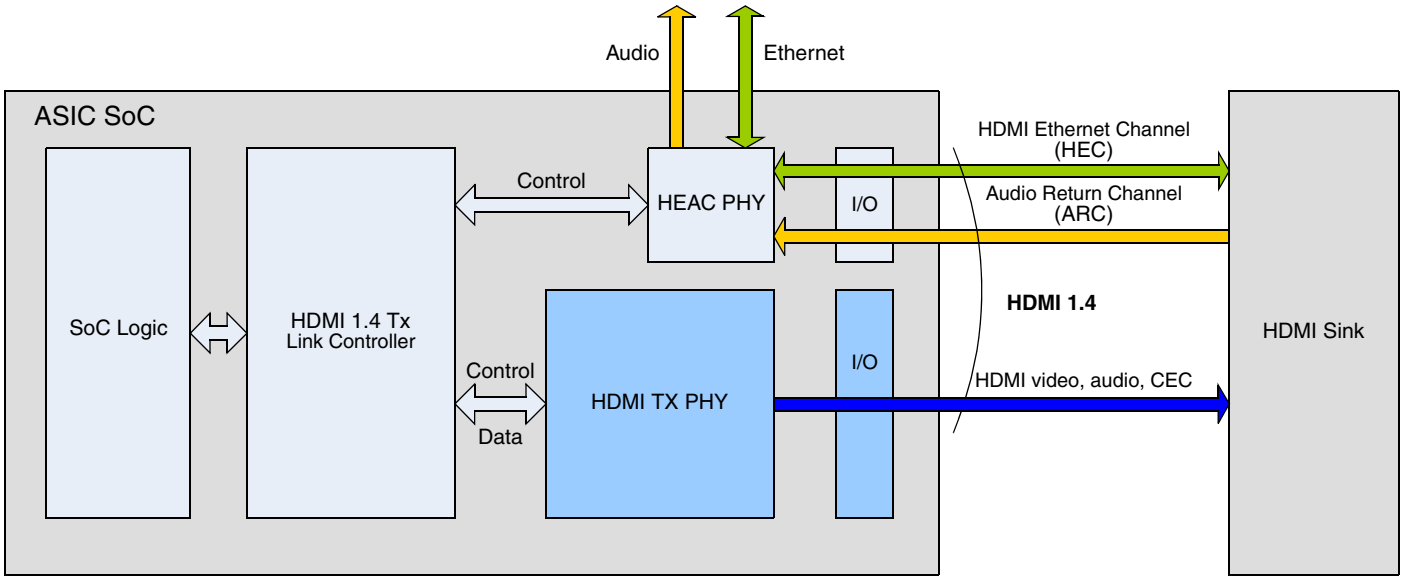
dwc_hdmi14_tx_phy

HDMI 1.4 TX PHY IP

The HDMI 1.4 TX PHY interface is comprised of three line drivers for data transmission and an additional line driver for clock transmission. It is designed to perform the serialization and transmission of video data and control information through an HDMI interface. The HDMI 1.4 TX PHY hard-macro interfaces with the HDMI Link Controller through a common graphic controller interface, supporting up to 30 bit data transfer with data enable. The clock line driver is used for reference clock transmission. The HDMI 1.4 TX PHY is targeted for digital video/audio transmission for high resolution display applications, supporting major display formats up to 3D formats, 4K x 2K resolution and 1080i/p in DTV applications and QXGA in graphic display applications, with True-color or Deep-color resolutions. At maximum pixel rate, the HDMI channel bit rate is 3.4 Gbps, allowing a maximum effective throughput of 8.16 Gbps.

Features

- Compliant with HDMI 1.4 and DVI 1.0 specifications
- 4 Levels of Pre-Emphasis for long cable support and clean signals
- Hot Plug Detect allows changing of cables and components without switching off the entire system
- Support for 5V I/O on all nodes (down to 28-nm nodes)
- Aggressive ESD protection
- Input clock from 25 MHz to 340 MHz range
- Aggregate bandwidth of 10.2 Gbps to support for 3D formats, 4K x 2K resolution, 720p@100 Hz, 720i@200 Hz, 1080p@60 Hz or 1080i/720i@120 Hz HDTV display resolutions and up to QXGA graphic display resolutions
- Link Controller interface with 24 bit SDR data access, with DATAEN, VERSYNC, HORSYNC and CTRL[3:0] signals
- Up to 10.2 Gbps aggregate bandwidth



The DesignWare Cores HDMI 1.4 TX IP Solution datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_hdmi_tx_csds.pdf

dwc_hdmi20_rx_phy

HDMI 2.0 RX PHY IP

The HDMI 2.0 RX PHY IP interface implements the analog front-end of the HDMI receiver, sampling and deserialization of the three data streams and all the digital circuitry for operating mode management, providing a digital interface to the Link Controller. It integrates auto-calibrated input termination resistors and automatic adaptive line equalization to support long cables. An additional clock receiver is included for reference system clock reception.

Features

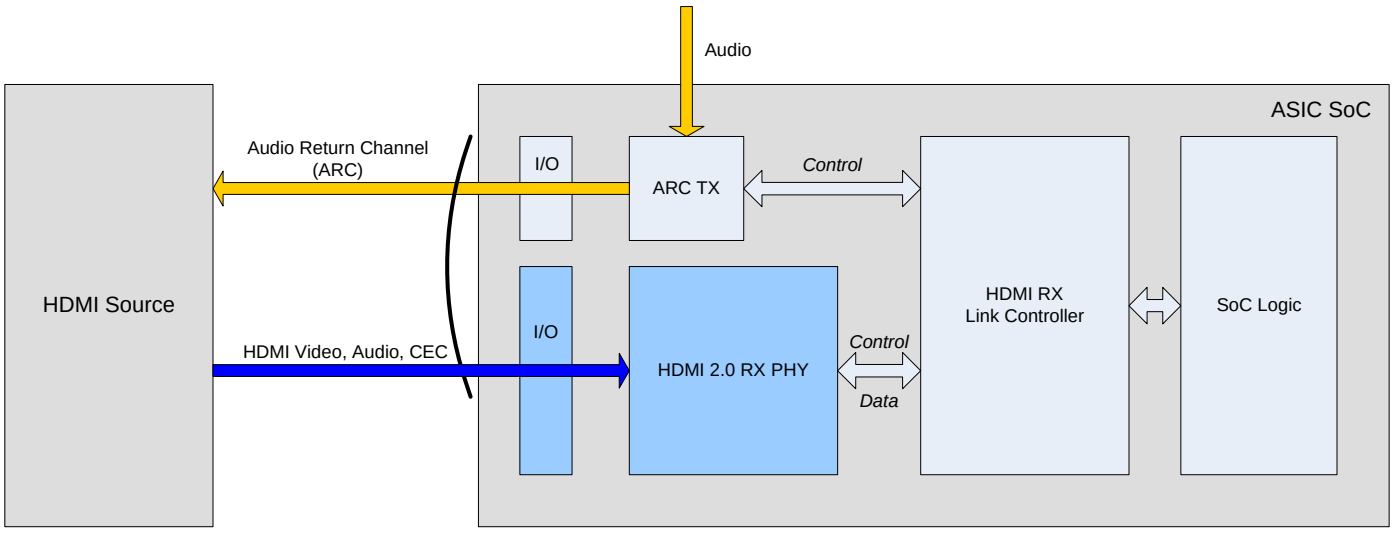
- 25–340 MHz TMDS input clock (on HDMI cable)
- Up to 1080p at 120 Hz and 4k x 2k at 60 Hz HDTV display resolutions and up to QXGA graphic display resolutions
- True-color (24-bit) and Deep-color (30, 36, or 48-bit) color resolution modes
- Up to 18 Gbps total throughput
- I^2C interface for configuration
- JTAG interface for configuration
- Built-in Self-Test (BIST)
- Link controller flexible interface with 30-, 60-, 120-bit SDR data access
- Power collapsing
- Programmable terminations
- ARC TX add-on block
- 5V protection
- Embedded A/D converter and analog testbus for ATE testing
- Built-in pattern generator
- I/O continuity test
- Optimized for low power and small area

Target Applications

- High-end CRT, LCD, or plasma television sets
- Multimedia PC displays
- Video projectors

Technology Processes

- Available in leading process technologies from 90-nm to 28-nm



The DesignWare Cores HDMI 1.4 RX IP Solution datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_hdmi_rx_csds.pdf

dwc_hdmi20_mhl_rx_phy

HDMI-MHL RX PHY

The HDMI-MHL Rx PHY IP can be integrated and configured to operate in HDMI or MHL applications. The PHY can interface with the HDMI 2.0 Rx link controller or the MHL 2.1 Rx link controller, for each mode, respectively. The link controller provides control signals for macro configurability and processes the video data through the TMDS lanes. Analog I/Os interface with the external world.

Features

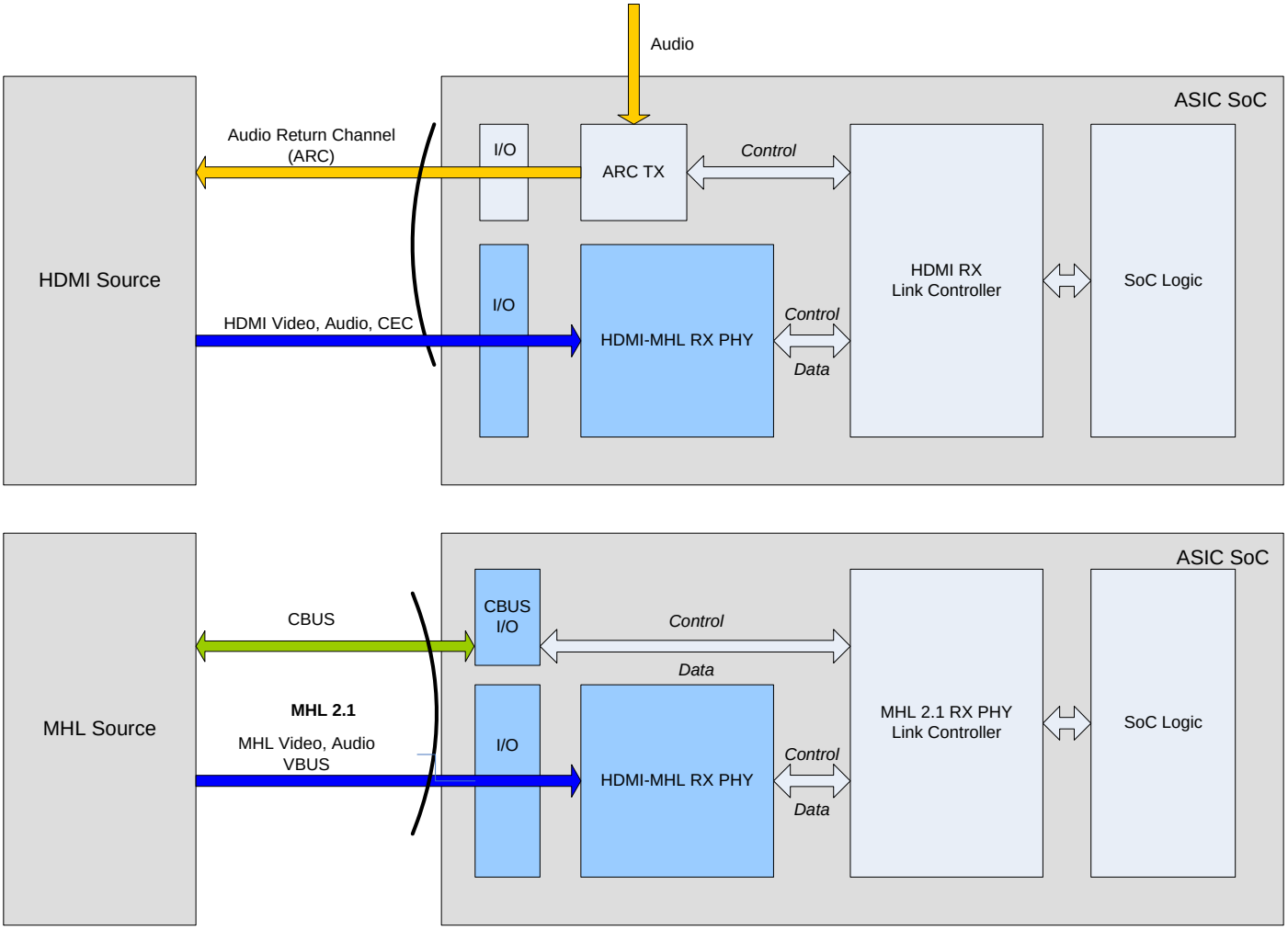
- Standards compliance:
  - MHL 2.1
  - HDMI 2.0
  - DVI 1.0
- 25–340 MHz TMDS input clock (on HDMI cable)
- Up to 1080p at 120 Hz and 4k x 2k at 60 Hz HDTV display resolutions and up to QXGA graphic display resolutions
- True-color (24-bit) and Deep-color (30, 36, or 48-bit) color resolution modes
- Up to 18 Gbps total throughput
- I^2C interface for configuration
- JTAG interface for configuration
- Link controller flexible interface with 30-, 60-, 120-bit SDR data access
- For MHL operation, support for the following:
  - Up to 720p/1080i at 60 Hz for 24-bit mode and support for 1080p at 60 Hz for PackedPixel mode
  - 3-D video formats
  - Up to 2.25 Gbps aggregate bandwidth for 24-bit mode and 3 Gbps aggregate bandwidth for packed pixel mode
  - 25-75 MHz input reference clock for 24-bit mode and 50-150 MHz input reference clock for PackedPixel mode
  - CBUS with add-on block
- Power collapsing
- Programmable terminations
- ARC TX add-on block
- 5V protection
- Embedded A/D converter and analog testbus for ATE testing
- Built-in pattern generator
- Built-in Self-Test (BIST)
- I/O Continuity Test
- Optimized for low power and small area

Target Applications

- High-end CRT, LCD, or plasma television sets
- Multimedia PC displays
- Video projectors

Technology Processes

- Available in leading process technologies from 90-nm to 28-nm



The DesignWare Cores HDMI RX IP Solution datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_hdmi_rx_csds.pdf

dwc_hdmi20_tx_phy

HDMI 2.0 TX PHY IP

The HDMI 2.0 TX PHY interface is comprised of three line drivers for data transmission and an additional line driver for clock transmission. It is designed to perform the serialization and transmission of video data and control information through an HDMI interface. The HDMI 2.0 TX PHY hard-macro interfaces with the HDMI Link Controller through a common graphic controller interface, supporting up to 30 bit data transfer with data enable. The clock line driver is used for reference clock transmission. The HDMI 2.0 TX PHY is targeted for digital video/audio transmission for high resolution display applications, supporting major display formats up to 18 Gbps aggregate bandwidth for advanced 4K x 2K resolution at 60 Hz frame rate and 8-bit per color for a flickerless ultra high-definition experience. At maximum pixel rate, the HDMI channel bit rate is 6.0 Gbps, allowing a maximum throughput of 18.0 Gbps.

Features

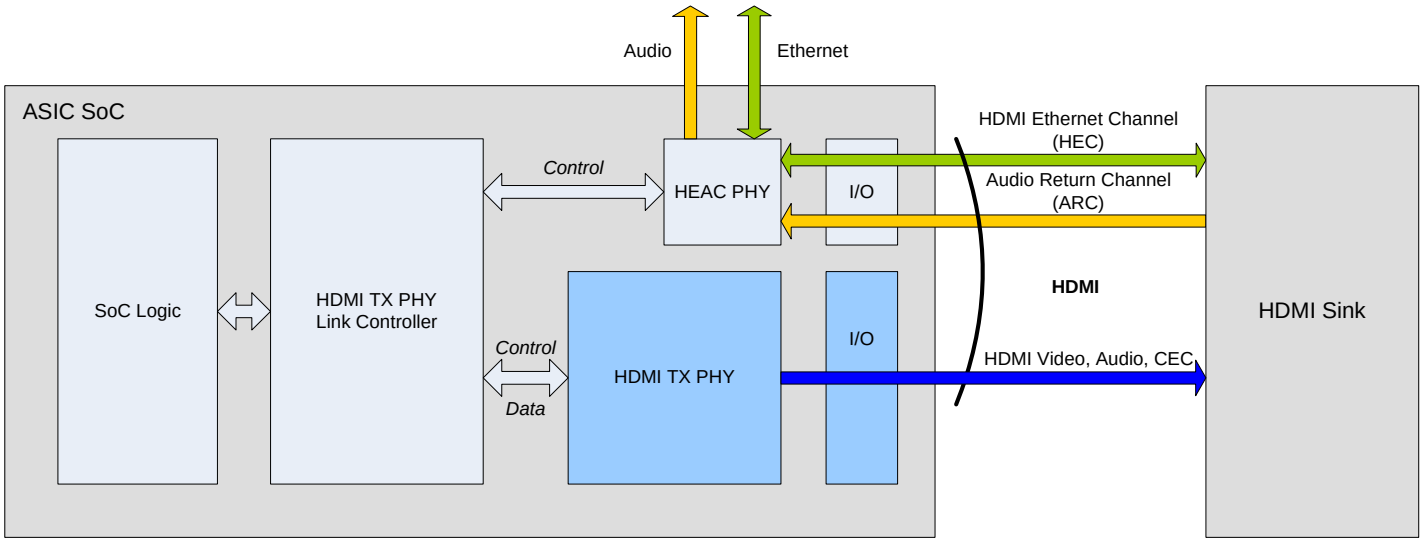
- Single Physical Layer PHY with support for HDMI 2.0 operation
- For HDMI operation, support for the following:
  - Up to 1080p at 120 Hz and 4k x 2k at 60 Hz HDTV display resolutions and up to QXGA graphic display resolutions
  - 3-D video formats
  - Up to 16-bit Deep Color modes
  - Up to 18 Gbps aggregate bandwidth
  - 13.5–600 MHz input reference clock
  - HPD input analog comparator
- 50% duty-cycle output clock
- Link controller flexible interface with 30-, 60- or 120-bit SDR data access
- I2C and JTAG interface for configuration
- Power collapsing
- Driver with features for extra-long cables
  - Pre-emphasis enable
  - Slope boosting
- Programmable source terminations
- Rx sensing
- 5 V protection
- Embedded A/D converter and analog testbus for ATE testing
- Built-in pattern generator
- Built-in Self-Test (BIST)
- I/O Continuity Test
- Optimized pin count, small area and low power to ensure low BOM cost

Target Applications

- DVD players or recorders
- Personal video recorders
- Set-top boxes
- Audio/video receivers
- Game consoles
- Tablets
- Cameras and camcorders

Technology Process

- Available in leading process technologies from 90-nm to 28-nm



The DesignWare Cores HDMI 2.0 TX IP Solution datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_hdmi_tx_csds.pdf

dwc_hdmi20_mhl_tx_phy

HDMI-MHL TX PHY

The HDMI-MHL Tx PHY IP can be integrated and configured to operate in HDMI or MHL applications. The PHY can interface with the HDMI 2.0 Tx link controller or the MHL 2.1 Tx link controller, for each mode, respectively. The link controller provides control signals for macro configurability and processes the video data through the TMDS lanes. Analog I/Os interface with the external world.

Features

- Standards compliance:
  - MHL 2.1
  - HDMI 2.0
  - DVI 1.0
- Single Physical Layer PHY with support for both HDMI and MHL operation
- For HDMI operation, support for the following:
  - Up to 1080p at 120 Hz and 4k x 2k at 60 Hz HDTV display resolutions and up to QXGA graphic display resolutions
  - 3-D video formats
  - Up to 16-bit Deep Color modes
  - Up to 18 Gbps aggregate bandwidth
  - 13.5–600 MHz input reference clock
  - HPD input analog comparator
- For MHL operation, support for the following:
  - Up to 720p/1080i at 60 Hz for 24-bit mode and support for 1080p at 60 Hz for PackedPixel mode
  - 3-D video formats
  - Up to 2.25 Gbps aggregate bandwidth for 24-bit mode and 3 Gbps aggregate bandwidth for packed pixel mode
  - 25-75 MHz input reference clock for 24-bit mode and 50-150 MHz input reference clock for PackedPixel mode
  - VBUS sensing
  - CBUS with add-on block
- 50% duty-cycle output clock
- Link controller flexible interface with 30-, 60- or 120-bit SDR data access
- I2C and JTAG interface for configuration
- Power collapsing
- Driver with features for extra-long cables
  - Pre-emphasis enable
  - Slope boosting
- Programmable source terminations
- Rx sensing
- 5 V protection
- Embedded A/D converter and analog testbus for ATE testing
- Built-in pattern generator
- Built-in Self-Test (BIST)
- I/O Continuity Test
- Optimized for low power and small area

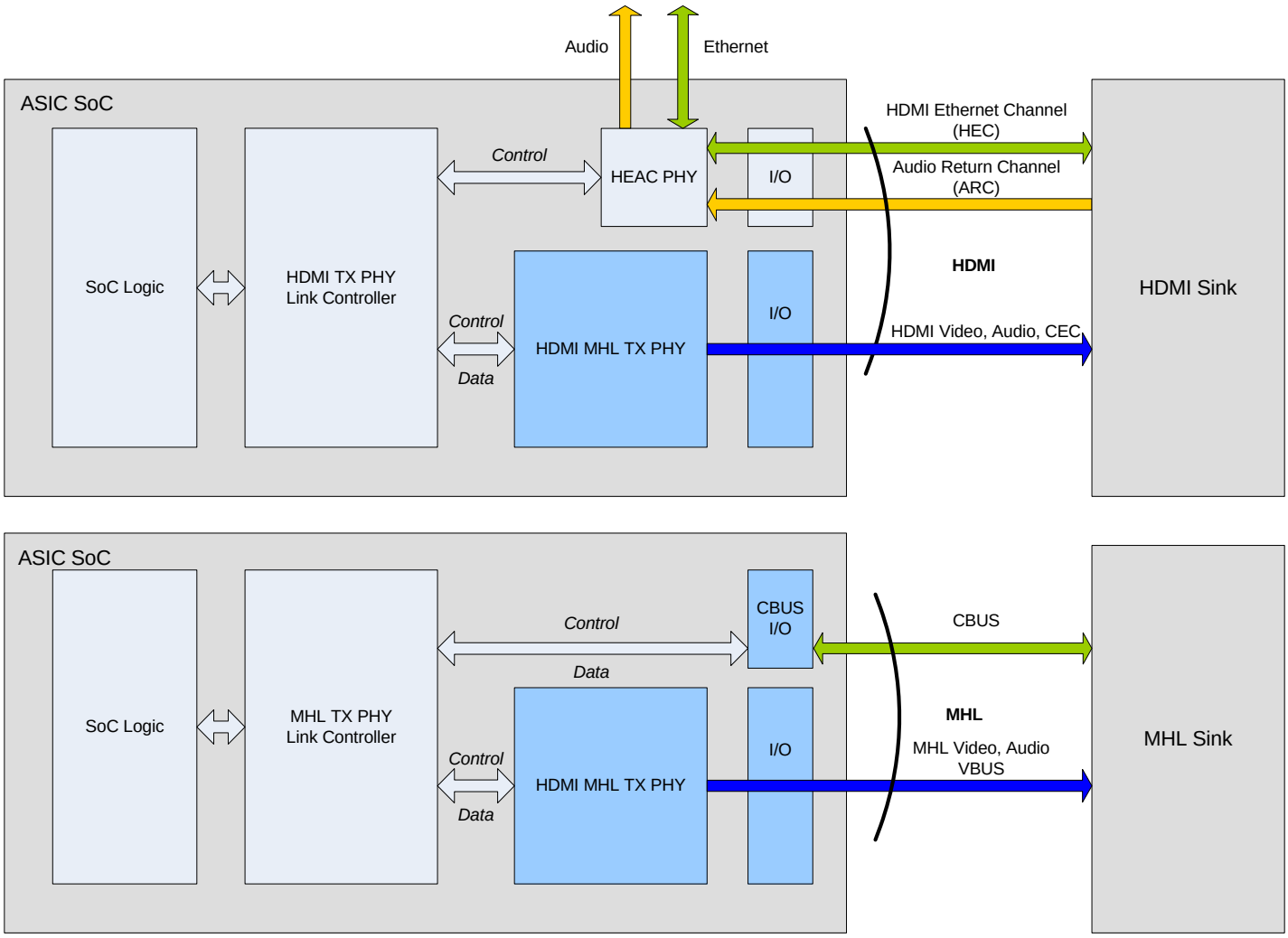
Target Applications

- High-end CRT, LCD, or plasma television sets
- Multimedia PC displays
- Video projectors

Technology Processes

- Available in leading process technologies from 90-nm to 28-nm

dwc_hdmi20_mhl_tx_phy
HDMI-MHL TX PHY



The DesignWare Cores HDMI RX IP Solution datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_hdmi_rx_csds.pdf

dwc_hdmi14_heac_phy

HDMI 1.4 HEAC PHY IP

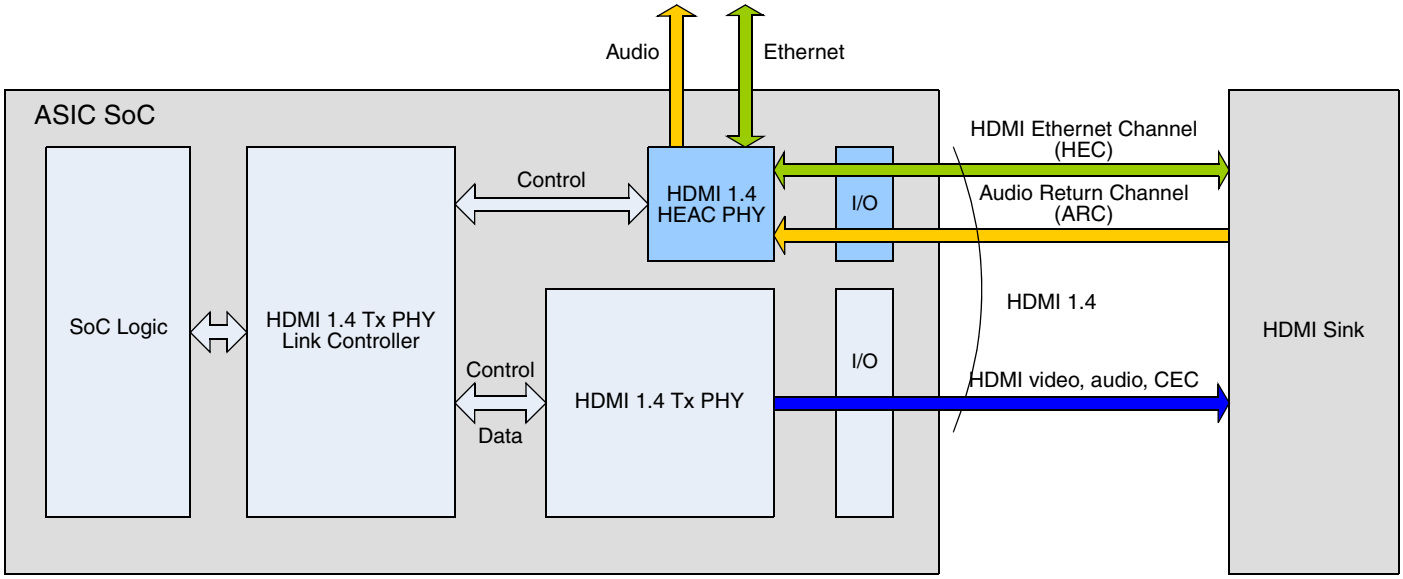
The HDMI Ethernet and Audio Return Channel (HEAC) is one of the latest additions to the HDMI 1.4 specification. This feature enhances the HDMI specification through the addition of a high-speed, full-duplex 100-Mbps data communication link derived from the IEEE 802.3 interface standard 100Base-Tx and a simplex audio data stream interface derived from the IEC60598-1 standard (S/PDIF)—all sharing the same HDMI connector.

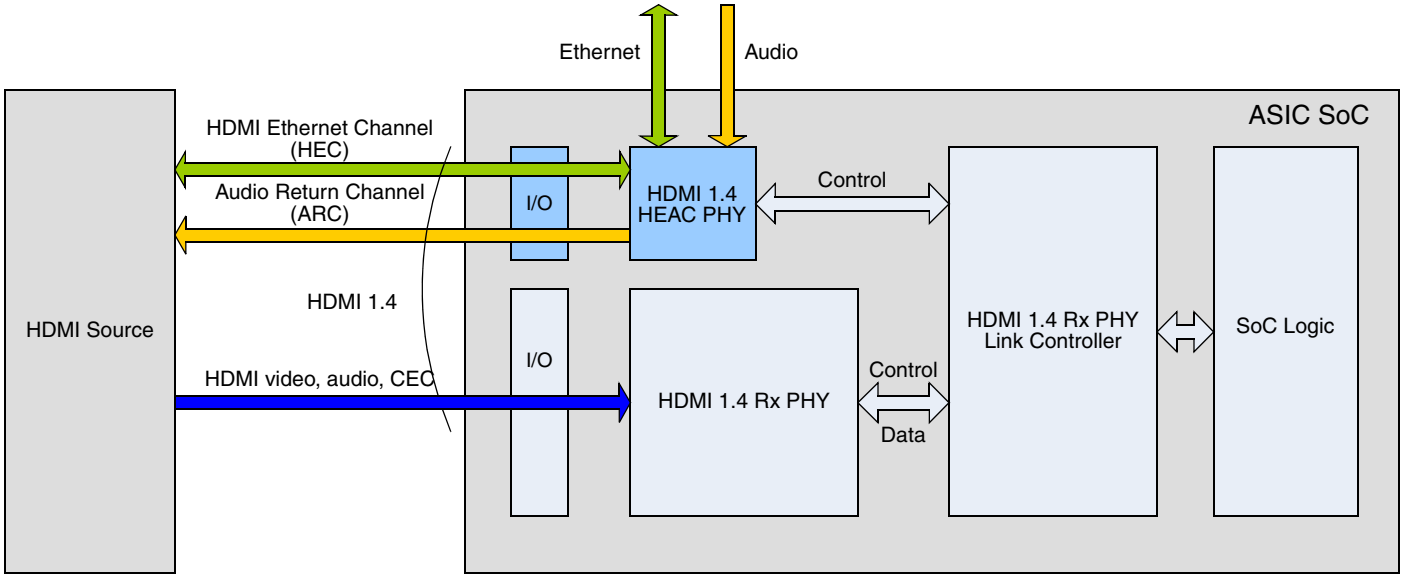
The full-duplex data transmission is defined as HDMI Ethernet Channel (HEC) and the unidirectional audio interface is defined as Audio Return Channel (ARC). The ARC enables audio transmission from an HDMI sink to an HDMI source, enabling a DTV to send a digital audio stream back to an A/V receiver.

This new feature brings to the consumer electronics (CE) equipment increased connectivity without the need for complex interconnection cabling systems. HEAC enables one cable (already in use) to replace three cables.

Features

- Supports duplex 100Base-Tx 100-Mbps data communication using differential signaling (HEC)
- Supports 4.096-Mbps, 5.6448-Mbps and 6.144-Mbps (all ± 1,000 ppm) S/PDIF operating speeds in both Common mode and Single mode (ARC)
- Integrated termination resistors
- Only one external reference resistor required
- Input clock frequency up to 340 MHz for termination resistors calibration
- Self-contained add-on to the HDMI 3D Tx PHY and HDMI 3D Rx PHY
- Small core area
- Low power consumption
- Includes PHY library metal stack options





The DesignWare Cores HDMI 1.4 HEAC IP Solution datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_hdmi_tx_csds.pdf

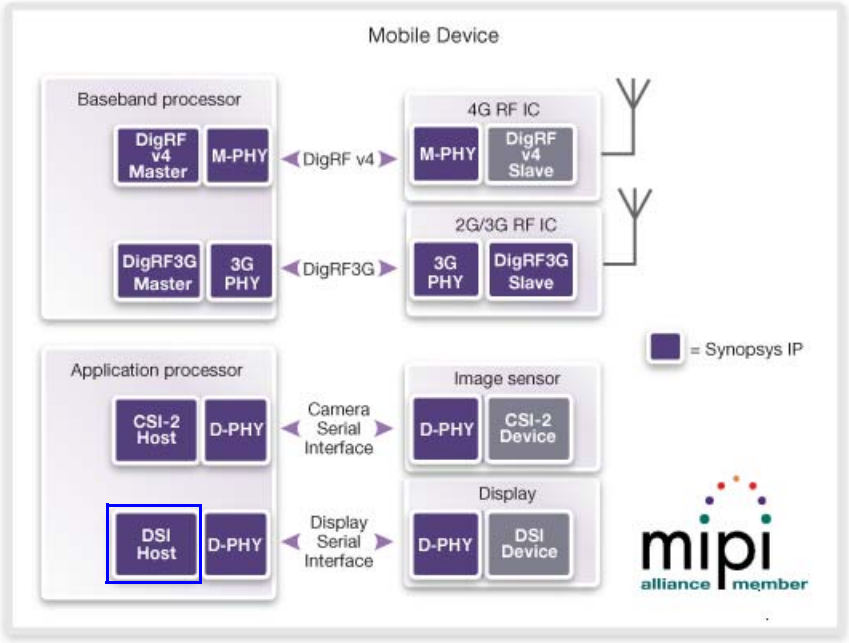
dwc_mipi_dsi_host

MIPI DSI Host Controller

The DesignWare MIPI DSI Host controller implements the DSI protocol on the Host side. The DSI link protocol specification is a part of communication protocols defined by MIPI Alliance standards intended for mobile system chip-to-chip communications. The MIPI DSI Host controller is used to transmit and receive the data to and from a DSI-compliant display. The physical layer is a D-PHY configured as Master. The MIPI DSI Host controller includes the MIPI DSI design and its verification environment. The MIPI DSI Host core is designed to integrate a Synopsys DWC MIPI D-PHY.

Features

- Compliant with MIPI Alliance Specification for Display Serial Interface (DSI), Version 1.01.00 - 21 February 2008.
- Compliant with MIPI Alliance Standard for Display Pixel Interface (DPI-2), Version 2.00 15 September 2005 with Pixel Data bus width up to 24 bits.
- Compliant with MIPI Alliance Standard for Display Bus Interface (DBI-2) Version 2.00 - 29.
- November 2005. Supported DBI types are:
  - Type A Fixed E mode
  - Type A Clocked E mode
  - Type B
- DBI and DPI interface can co-exist but only one can be operational.
- Supports all commands defined in MIPI Alliance Specification for Display Command Set (DCS), Version 1.02.00 - 23 July 2009.
- Supports interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009.
- Supports up to 4 D-PHY Data Lanes.
- Supports Bidirectional Communication and Escape Mode Support through Data Lane 0.
- Supports Multiple Peripheral capability and configurable Virtual Channels.
- Supports the Video Mode Pixel Formats, 16 bpp (5,6,5 RGB), 18 bpp (6,6,6,RGB) packed, 18 bpp.
- (6,6,6,RGB) loosely, 24 bpp (8,8,8,RGB).
- Supports the transmission of all generic commands.
- Supports ECC and Checksum capabilities.
- Supports End of Transmission Packet (EoTp).
- Supports ultra low power mode.
- Has schemes for fault recovery.



The dwc_mipi_dsi_host datasheet is available at:

http://www.synopsys.com/dw/doc.php/ds/c/dwc_mipi_dsi.pdf

dwc_ufshc

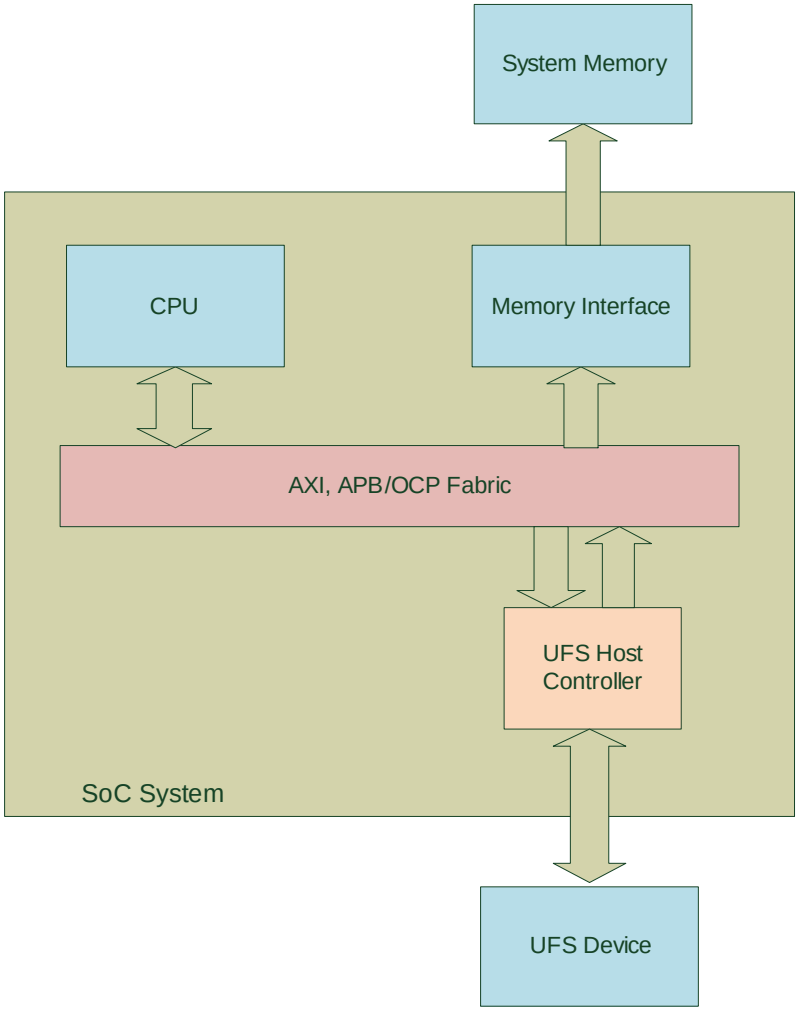
DesignWare UFS Host Controller

The DesignWare UFS Host Controller core is a standard based Serial Interface Engine for implementing a UFS interface in compliance with the UFS Architecture Specification [UFS] and the UFS Host Controller Specification [UFSHCI].

The UFS Host Controller application layer connects to a UniPro^{SM} protocol stack and M-PHY. Both, UniPro protocol stack and M-PHY can be considered part of the UFS Host Controller.

Features

- Scatter/Gather DMA to transfer large data blocks
- Burst transfers to maximize DMA throughput and keep system impact minimal
- Pre-configured for up to 32 task requests
- Pre-configured for up to 8 task management requests
- Ability to perform commands without system host intervention
- Support for the full range of UPIU packets, from 32byte up to 64kB
- 32-bit OCP, AXI, and APB slave interfaces for system host programming access:
  - Only 32-bit access allowed; this removes the need for a little/big endian configuration on this interface.
  - Clock can be individually controlled using the EnableClk_T signal in OCP slave interface.
- 64-bit OCP/64-bit AXI compliant initiator/master interface for DMA controlled data transfer:
  - Clock can be individually controlled using the EnableClk_I signal
  - 1, 2, 4, ..., 256 (power of two) beat bursts to maximize throughput
  - Supports byte enable
- Registered interface with a minimal amount of logic between port and register
- Hierarchical architecture to enable the design for customer owned technology dependent M-PHY
- Fully synchronous synthesizable RTL.
- DFT ready
- Clock gating ready design
- Ability to reuse existing and mature SCSI upper and middle layer software.
- After setup, SCSI commands are executed without requiring any system host intervention.
- With the UniPro stack and M-PHY, provides a high performance and reliable connection to the UFS Flash Memory Device.
- With a UniPro compliant stack, provides direct support for a UniPro compliant physical link layer
- Support for following UFS2.0 features:
  - Higher speed up to HS-G3 (High-Speed Gear 3)
  - Symmetric 2RX-2TX lanes
  - Pre-configured for up to 4 TX/RX lanes
  - Auto-hibernate entry and exit sequence
- Support for all the UniPro 1.6 and M-PHY 3.0 features including:
  - SKIP symbol insertion
  - MK2 extension support
  - Scrambling for EMI mitigation
  - HS-Gear3 adaptation
  - Advanced granularity support



The dwc_ufshc datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_ufs_host.pdf

dwc_mipi_dphy_bd2

MIPI DPHY Bidirectional 2 Lanes

The DWC D-PHY Bidir 2L macro implements the physical layer of bidirectional universal lanes for the MIPI D-PHY interface, stacked in a two-data-lane and one-clock-lane configuration. This IP is reusable for both master and slave applications. The lane modules are full-featured, bi-directional modules with HS-TX, HS-RX, LP-TX, LP-RX, and LP-CD functions, but with no support for HS reverse communication.

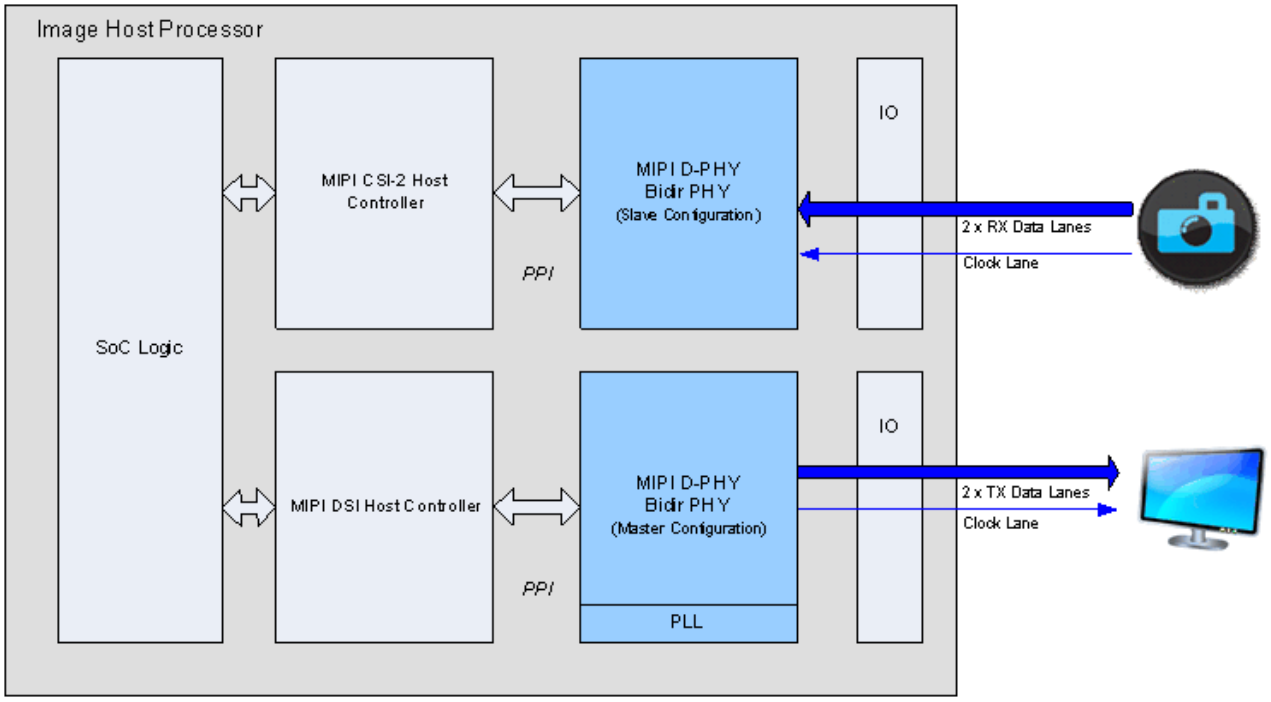
DWC D-PHY Bidir 2L includes a clock multiplier PLL for HS clock generation needed in a master-side application. It is targeted for digital data transmission between a host processor and display drivers or camera interfaces in mobile applications, supporting a maximum effective bit rate of 1.5 Gbps (per lane). The assembled two data lane system enables up to 3 Gbps aggregate communication throughputs, delivering the bandwidth needed for high throughput data transfer.

Given its dual master/slave reusability, DWC D-PHY Bidir 2L builds a highly reliable bidirectional high-speed differential interface for serial data transmission with an additional reduced throughput low-power data transfer mode in the same differential pair-reducing line count and minimizing cable wires and EMI shielding requirements.

Features *

- Attachable PLL clock multiplication unit for master-side functionality
- Flexible input clock reference 5 MHz to 500 MHz
- 50% DDR output clock duty-cycle
- Lane operation ranging from 80 Mbps to 1.5 Gbps in forward direction
- Aggregate throughput up to 3 Gbps with two data lanes
- Protocol peripheral interface (PPI) for clock and data lanes
- Low-power escape modes and ultra low-power state
- 1.8/2.5 V ±10% Analog supply operation
- 0.9-1.1 V ±10% Digital supply operation
- Core Area:
  - For Slave configuration: 0.31-0.532 mm^2
  - For Master configuration: 0.41-0.727 mm^2

* Specifications vary based upon technology



The dwc_mipi_dphy_bd2 datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_mipi_d-phy.pdf

dwc_mipi_dphy_bd4

MIPI DPHY Bidirectional 4 Lanes

The DWC D-PHY Bidir 4L macro implements the physical layer of bidirectional universal lanes for the MIPI D-PHY interface, stacked in a four-data-lane and one-clock-lane configuration. This IP is reusable for both master and slave applications. The lane modules are full-featured, bi-directional modules with HS-TX, HS-RX, LP-TX, LP-RX, and LP-CD functions, but with no support for HS reverse communication.

DWC D-PHY Bidir 4L also includes a clock multiplier PLL for HS clock generation needed in a master-side application. It is targeted for digital data transmission between a host processor and display drivers or camera interfaces in mobile applications, supporting a maximum effective bit rate of 1.5 Gbps (per lane). The assembled four data lane system enables up to 6 Gbps aggregate communication throughputs, delivering the bandwidth needed for high throughput data transfer.

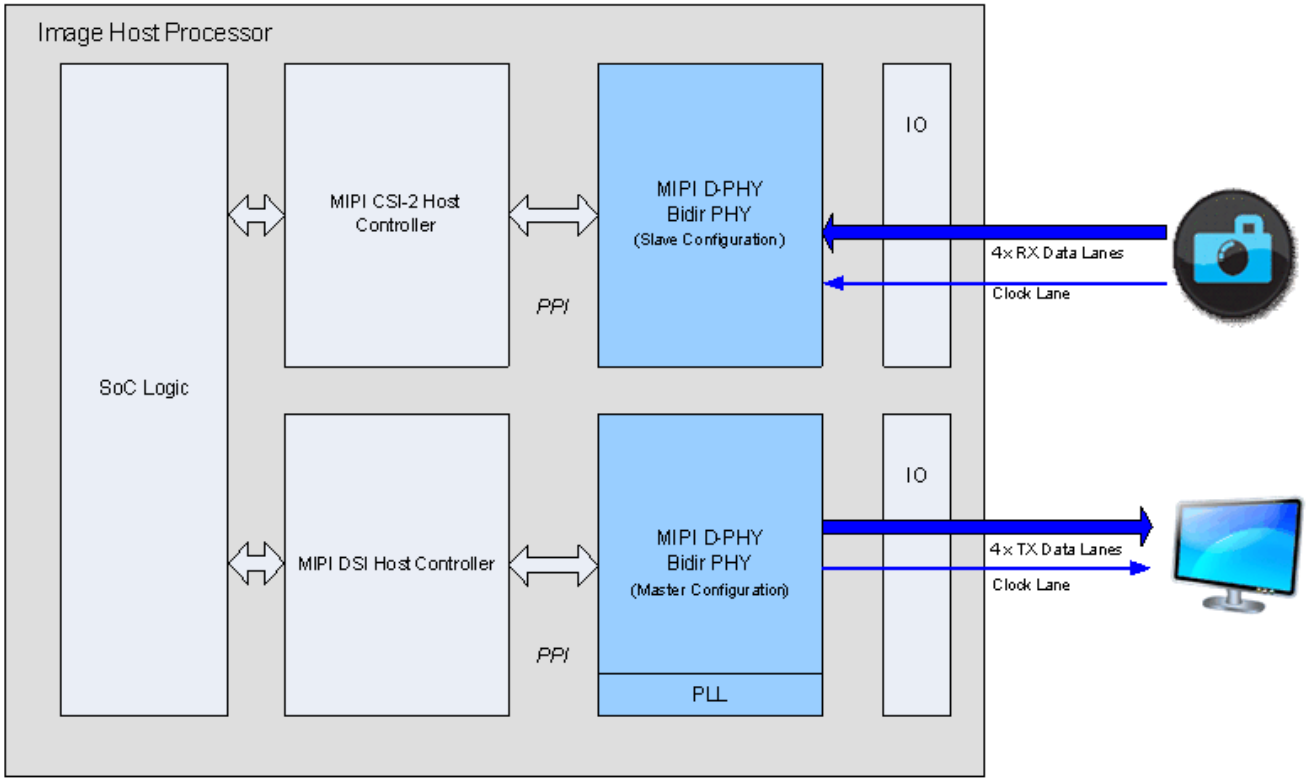
Given its dual master/slave reusability, DWC D-PHY Bidir 4L builds a highly reliable bidirectional high-speed differential interface for serial data transmission with an additional reduced throughput low-power data transfer mode in the same differential pair-reducing line count and minimizing cable wires and EMI shielding requirements.

Features *

- Attachable PLL clock multiplication unit for master-side functionality
- Flexible input clock reference 5 MHz to 500 MHz
- 50% DDR output clock duty-cycle
- Lane operation ranging from 80 Mbps to 1.5 Gbps in forward direction
- Aggregate throughput up to 6 Gbps with four data lanes
- Protocol peripheral interface (PPI) for clock and data lanes
- Low-power escape modes and ultra low-power state
- 1.8/2.5 V ±10% Analog supply operation
- 0.9-1.1 V ±10% Digital supply operation
- Core Area:
  - For Slave configuration: 0.477-0.81 mm^2
  - For Master configuration: 0.576-1.005 mm^2

* Specifications vary based upon technology

dwc_mipi_dphy_bd4
MIPI DPHY Bidirectional 4 Lanes



The dwc_mipi_dphy_bd4 datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_mipi_d-phy.pdf

dwc_mipi_dphy_rx2

MIPI DPHY RX 2 Data Lanes

The DWC D-PHY RX 2 Lanes macro implements the physical layer of universal lanes for the MIPI D-PHY interface, stacked in a two-data- lanes and one-clock-lane configuration. The DWC MIPI D-PHY RX 2L is used for slave applications. The lane modules are unidirectional with HS-RX and LP-RX functions.

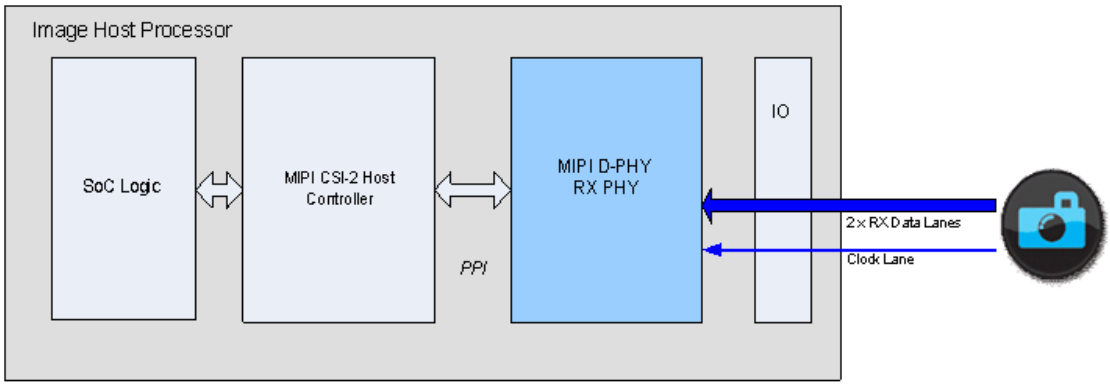
The DWC MIPI D-PHY RX 2L is targeted for the digital data transmission between a camera and host processor interfaces in mobile applications, supporting a maximum effective bit rate of 1.5 Gbps (per lane). The assembled two data lanes system enables up to 6 Gbps aggregate communication throughputs, delivering the bandwidth needed for high throughput data reception.

The DWC MIPI D-PHY RX 2L builds a highly reliable unidirectional high-speed differential interface for serial data reception with an additional reduced throughput low-power data reception mode in the same differential pair-reducing line count. This minimizes the cable wires and EMI shielding requirements.

Features *

- Flexible input clock reference 17 MHz to 27 MHz
- 50% DDR output clock duty-cycle
- Lane operation ranging from 80 Mbps to 1.5 Gbps in forward direction
- Aggregate throughput up to 3 Gbps with two data lanes
- Protocol Peripheral Interface (PPI) for Clock and Data lanes
- Low-Power Escape modes and Ultra Low-power mode supported
- 1.8/2.5 V ± 10% Analog supply operation
- 0.9-1.1 V ± 10% Digital supply operation
- Core Area: 0.24 mm^2

* Specifications vary based upon technology



The dwc_mipi_dphy_rx2 datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_mipi_d-phy.pdf

dwc_mipi_dphy_rx4

MIPI DPHY RX 4 Data Lanes

The DWC D-PHY RX 4 Lanes macro implements the physical layer of universal lanes for the MIPI D-PHY interface, stacked in a four-data- lanes and one-clock-lane configuration. The DWC MIPI D-PHY RX 4L is used for slave applications. The lane modules are unidirectional with HS-RX and LP-RX functions.

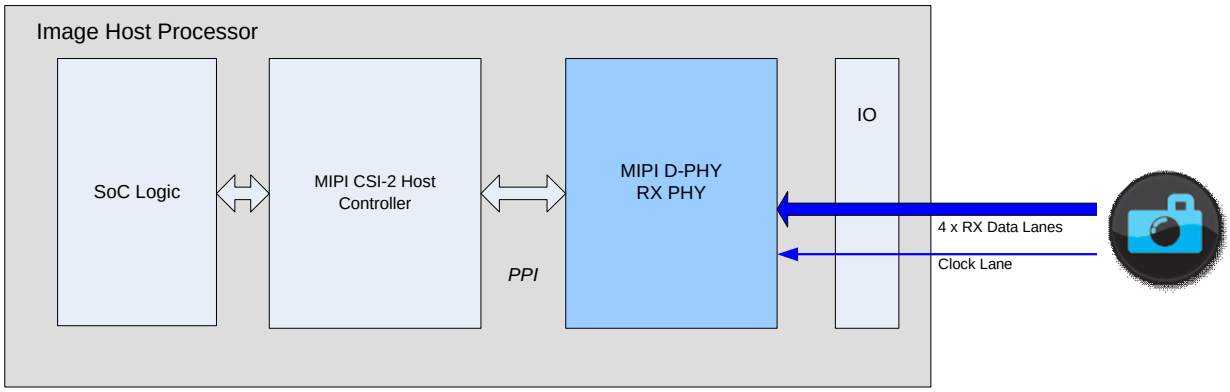
The DWC MIPI D-PHY RX 4L is targeted for the digital data transmission between a camera and host processor interfaces in mobile applications, supporting a maximum effective bit rate of 1.5 Gbps (per lane). The assembled four data lanes system enables up to 6 Gbps aggregate communication throughputs, delivering the bandwidth needed for high throughput data reception.

The DWC MIPI D-PHY RX 4L builds a highly reliable unidirectional high-speed differential interface for serial data reception with an additional reduced throughput low-power data reception mode in the same differential pair-reducing line count. This minimizes the cable wires and EMI shielding requirements.

Features *

- Flexible input clock reference 17 MHz to 27 MHz
- 50% DDR output clock duty-cycle
- Lane operation ranging from 80 Mbps to 1.5 Gbps in forward direction
- Aggregate throughput up to 6 Gbps with four data lanes
- Protocol Peripheral Interface (PPI) for Clock and Data lanes
- Low-Power Escape modes and Ultra Low-power mode supported
- 1.8/2.5 V ± 10% Analog supply operation
- 0.9-1.1 V ± 10% Digital supply operation
- Core Area: 0.39 mm^2

* Specifications vary based upon technology



The dwc_mipi_dphy_rx4 datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_mipi_d-phy.pdf

dwc_mphy_type1_1tx_1rx

MIPI MPHY TYPE1 1Tx1RX

The DWC MIPI Type 1 M-PHY 1 TX/1 RX provides a two-sublink implementation of the MIPI M-PHY interface specification with the following number of lanes:

- one TX
- one RX

The dwc_mphy_type1_1tx_1rx has a fully modular architecture for use with several MIPI standards including:

- LLI
- SSIC
- UFS
- UniPro

The dwc_mphy_type1_1tx_1rx is divided into:

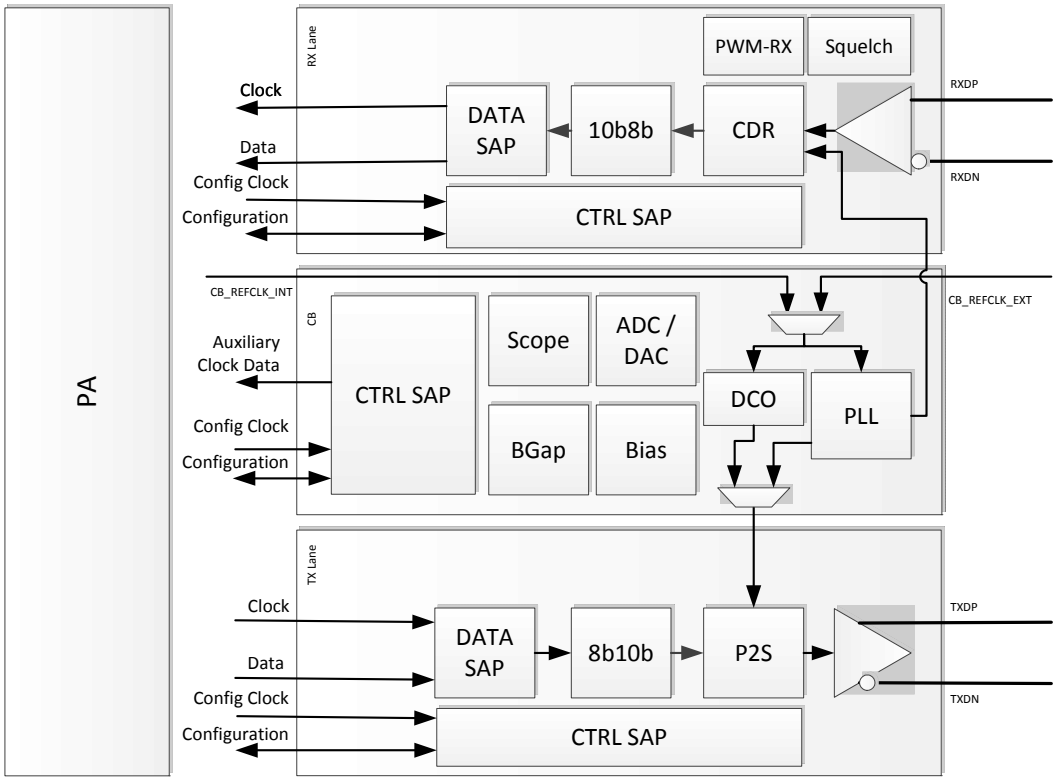
- 1 TX lane – provides one transmission lane
- 1 RX lane – provides one reception lane
- Common block (CB) – provides necessary high-speed clocks for several lanes and support signals

Features *

- M-PHY Type 1 M-PORTs
- Internal (through SoC) and external (through pad) reference clock support: 19.2 MHz, 26 MHz, 38.4 MHz, and 52 MHz
- High-speed G1/2/3, A/B modes
- Up to 4 lanes in M-TX and 4 lanes in M-RX
- Optimized EMI performance through the use of slew-rate control and dithering
- EMI reduction features
- PLL clock multiplication unit for high-speed clock generation (for PHY and controller)
- TX de/pre-emphasis for intricate interconnects
- Quick exit of hibernate and PLL lock time
- Advanced test features
- 1.8/2.5 V ± 10% Analog supply operation
- 0.9-1.1 V ± 10% Digital supply operation

* Specifications vary based upon technology

The following shows the functional block diagram of the DWC MIPI Type 1 M-PHY 1 TX/1 RX.



The dwc_mphy_type1_1tx_1rx datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_mipi_m-phy.pdf

dwc_mipi_mphy_type1_2tx_2rx

MIPI MPHY TYPE1 2Tx2RX

The DWC MIPI Type 1 M-PHY 2 TX/2 RX provides a two-sublink implementation of the MIPI M-PHY interface specification with the following number of lanes:

- two TX
- two RX

The dwc_mphy_type1_2tx_2rx has a fully modular architecture for use with several MIPI standards including:

- LLI
- SSIC
- UFS
- UniPro

The dwc_mphy_type1_2tx_2rx is divided into:

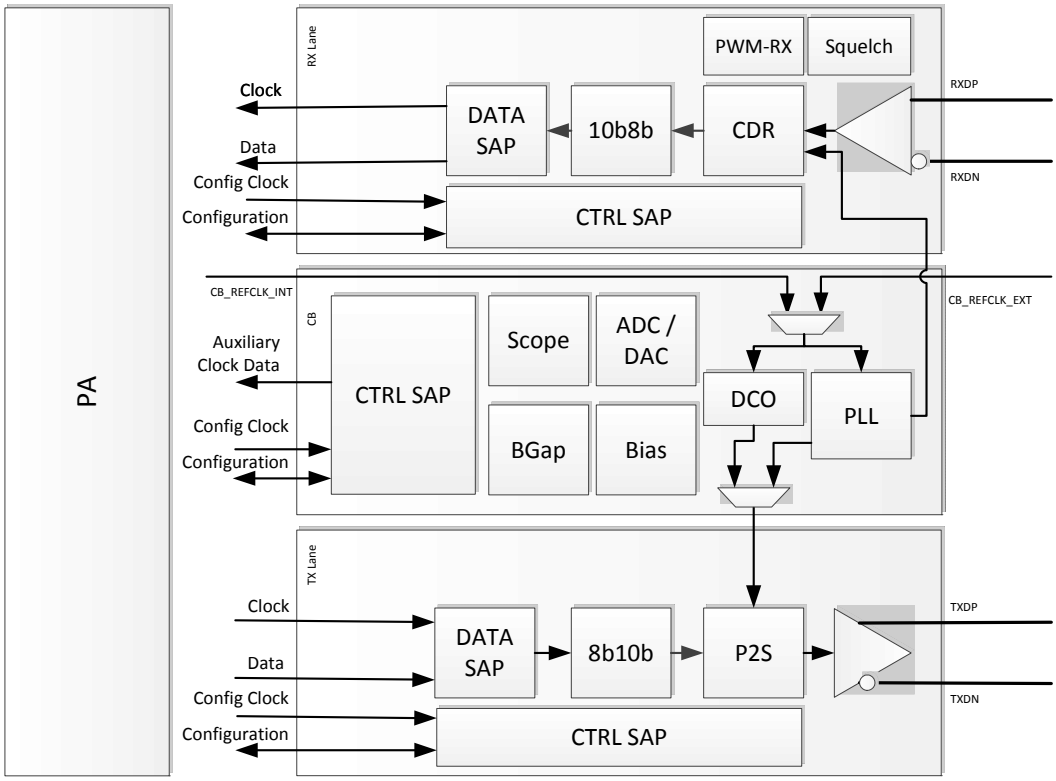
- 2 TX lanes – provides two transmission lanes
- 2 RX lanes – provides two reception lanes
- Common block (CB) – provides necessary high-speed clocks for several lanes and support signals

Features *

- M-PHY Type 1 M-PORTs
- Internal (through SoC) and external (through pad) reference clock support: 19.2 MHz, 26 MHz, 38.4 MHz, and 52 MHz
- High-speed G1/2/3, A/B modes
- Up to 4 lanes in M-TX and 4 lanes in M-RX
- Optimized EMI performance through the use of slew-rate control and dithering
- EMI reduction features
- PLL clock multiplication unit for high-speed clock generation (for PHY and controller)
- TX de/pre-emphasis for intricate interconnects
- Quick exit of hibernate and PLL lock time
- Advanced test features
- 1.8/2.5 V ± 10% Analog supply operation
- 0.9-1.1 V ± 10% Digital supply operation

* Specifications vary based upon technology

The following shows the functional block diagram of the DWC MIPI Type 1 M-PHY 2 TX/2 RX.



The dwc_mphy_type1_2tx_2rx datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_mipi_m-phy.pdf

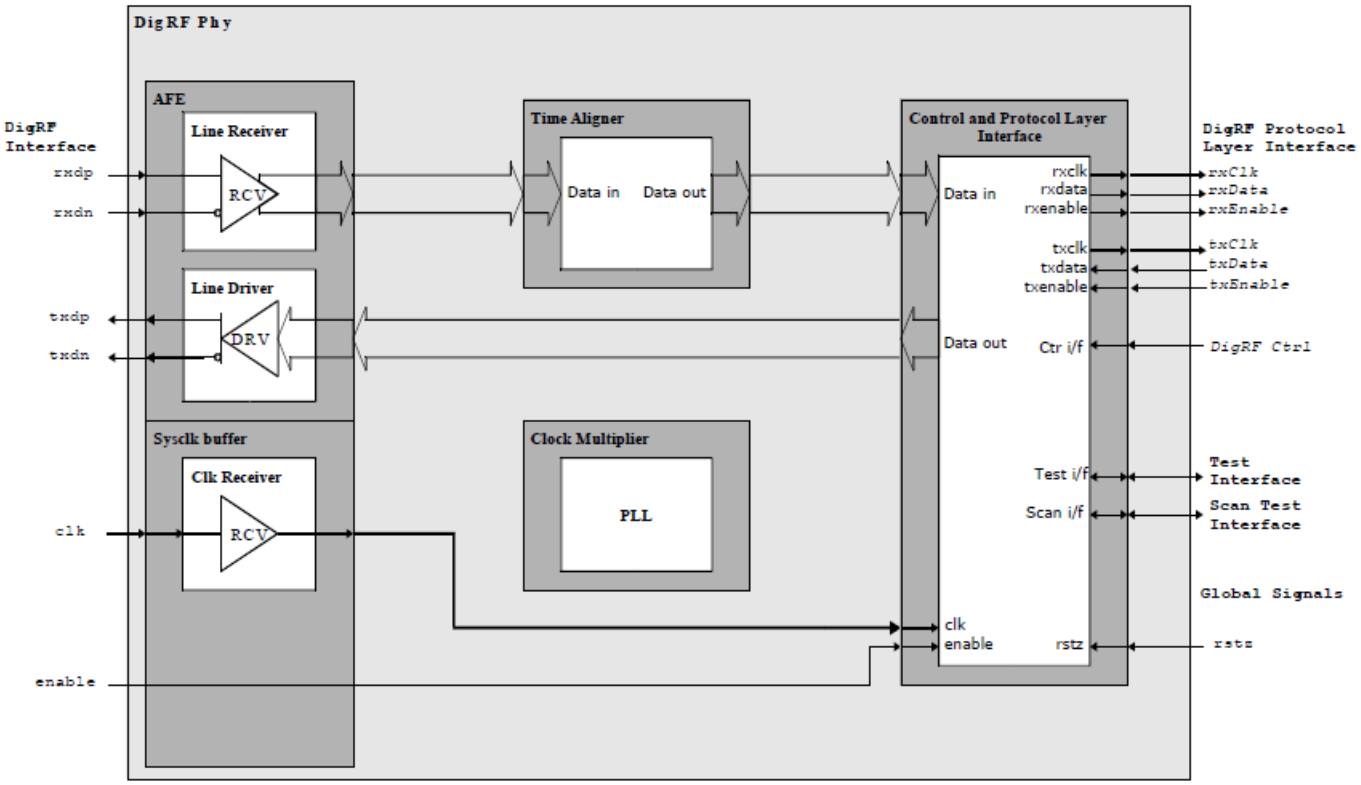
dwc_mipi_digrf

MIPI DigRF 2.5G-3G Physical Layer

The DigRF PHY in an end to end bidirectional serial link using a single interface for transferring data and control information between digital baseband processors and RF ICs in Single or Dual-mode 2.5G/3G Applications. The DigRF Phy implements the physical layer of the DigRF Interface Specification. It implements a DigRF Interface on the line side and a dedicated 3 line clocked serial interface on the protocol interface side. In the transmitting path it receives data, clock and an enable signal in the protocol interface. It than appends the sync field to the received serial data stream and sends is differentially to the DigRF line interface at the output of the line driver. In the opposite direction the differential data stream is received and restored in the line receiver and passed to the CDR block. The re-timed data stream at the output of the CDR is than passed to the next block that looks for, and if detected, captures the frame sync pattern, after what it acquires byte alignment. Than it processes the first three header bits to determine the frame length and generate an enable signal for the protocol interface with the exact frame duration. The received frame is passed to the protocol interface without the sync field.This macro cell implements also all the functionalities needed for clock multiplication, low power modes and test modes. The macro cell can be used in both Digital Baseband Processors and RF ICs applications, recurring to simple top level routing changes.

Features

- Complete PHY for DigRF Interface
- Compliant with DigRF 3G V3.09 spec
- Simple 3 pin clocked serial protocol layer interface
- Supports Low Power Sleep Mode
- Supports Low Power Shutdown Mode
- Built-in functional self test mode (Test Interface)
- 1.8V±10% Analog supply operation
- 1.2V±10% Digital supply operation
- Core Area: 0.32 mm^2
- Power < 25 mW (@1.8V/312MHz Tx/Rx)
- Chartered 65nm LP Digital CMOS process; 1Poly; 5 Metals (Thick Top Metal)



The dwc_mipi_digrf datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_digrf.pdf

dwc_mipi_csi2_host

MIPI CSI-2 Host Controller

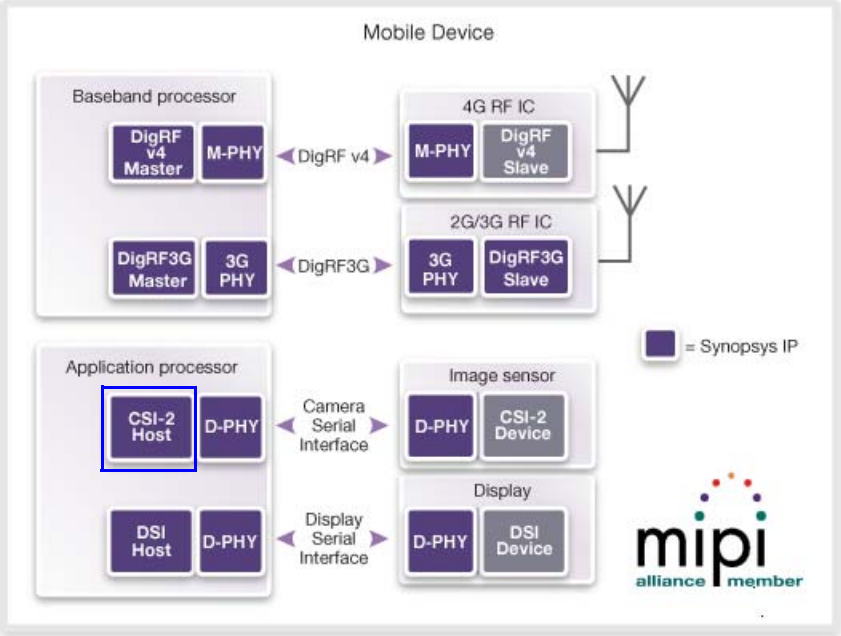
The DesignWare MIPI CSI-2 Host controller implements the CSI-2 protocol. The CSI-2 link protocol specification is a part of communication protocols defined by MIPI Alliance standards intended for mobile system chip-to-chip communications. The CSI-2 specification is specifically targeted for Camera to Image application processor communication.

The MIPI CSI-2 Host controller is used for the reception of data from a CSI-2 compliant camera sensor. A D-PHY configured as Slave acts as the physical layer.

The DesignWare MIPI CSI-2 Host Controller includes the DWC_mipi_csi2_host design and its verification environment. The MIPI CSI-2 Host Controller is designed to integrate a Synopsys MIPI D-PHY.

Features

- Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2), Version 1.00 - 29 November 2005
- Optional support for Camera Control Interface (CCI) through the use of DesignWare Core (DW_apb_i2c)
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009
- Supports up to 4 D-PHY Rx Data Lanes
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- Support for several frame formats such as:
  - General Frame or Digital Interlaced Video with or without accurate sync timing
  - Data type (Packet or Frame level) and Virtual Channel interleaving
- 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification
- Supports all primary and secondary data formats:
  - RGB, YUV and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types
- Error detection and correction at:
  - PHY level
  - Packet level
  - Line level
  - Frame level



The dwc_mipi_csi2_host datasheet is available at:

http://ww.synopsys.com/dw/doc.php/ds/c/dwc_csi2_controller.pdf

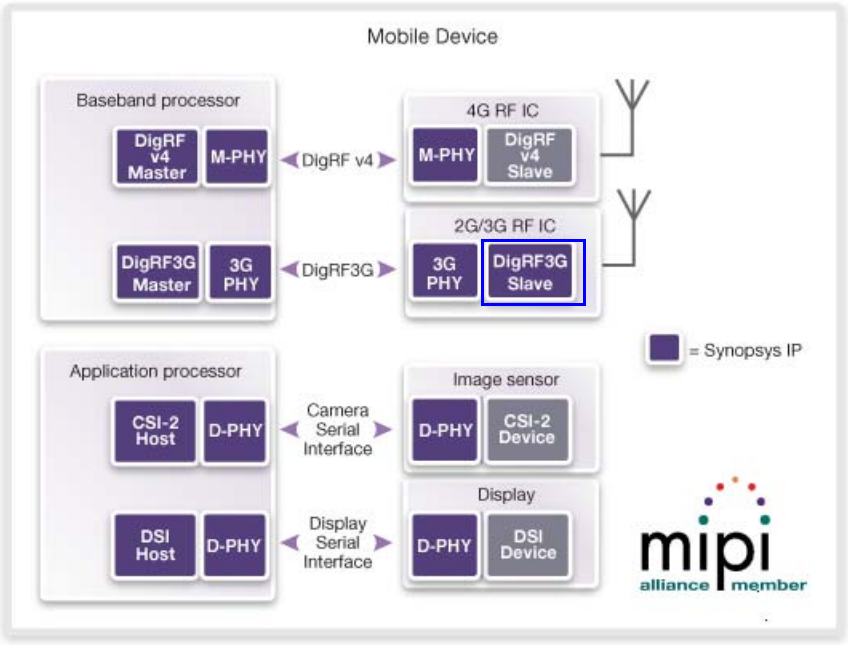
dwc_3g_digrf_slave_controller

MIPI 3G DigRF Slave Controller

The MIPI 3G DigRF Slave Controller IP core implements the protocol layer of a DigRF 3G interface. It makes the interface between the DigRF Physical interface and the RF transceiver internal system side. In the TX path, the controller receives the frame data from the Physical layer. This data is received through the 3-wire (clock, data and enable) serial interface. The controller decodes the header information and, depending on the logical channel type used, directs the payload data to the adequate destination. The DigRF interface control information is locally processed and, if needed, passed to the physical layer through a dedicated control interface. Transceiver register bank data can be accessed for read/write operations using logical channel type 0x02. The DigRF Controller allows full flexibility for the Transceiver to implement register access. An 8-bit parallel interface is provided for this purpose. It is up to the Transceiver logic to interpret the frame payload and provided the read back data, if any. Radio data, 2.5G or 3G, is unpacked and directed to a FIFO interface. In the opposite direction, frame data (header + payload) is received from the link controller through a similar 3-wire interface. The physical layer adds the synchronization pattern field to the received frame and sends all information to the analog line interface. The phy can operate in low speed (sysclk bit rate divided by 4) or high speed (312Mbps) in both directions. Medium speed operation (at sysclk bit rate) is reserved to the link from the Transceiver to the Digital Baseband processor.

Features

- DigRF Controller, RF Transceiver application side, compliant with DigRF 3G V3.09.04 Specification (April, 1, 2008).
- Compliant with SYNOPSYS, INC. Synopsys DigRF Physical Layer
- Simple 3-wire serial DigRF phy interface
- Supports up to 2 RX data streams.
- Supports 1 Tx data stream.
- Implements all Interface Control Logic Channel Management Functions for the RF Transceiver side.
- Performs Frame construction and serialization on the RX path.
- Performs Frame Header decoding and payload routing on the TX path.
- Interface to FIFO memories for frame buffering in Tx and Rx data paths.
- 8 bit parallel interface for Control and Status messages.



The dwc_3g_digrf_slave_controller datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_3g_digrf_slave_controller.pdf

dwc_3g_digrf_master_controller

MIPI DigRF 3G Master Controller

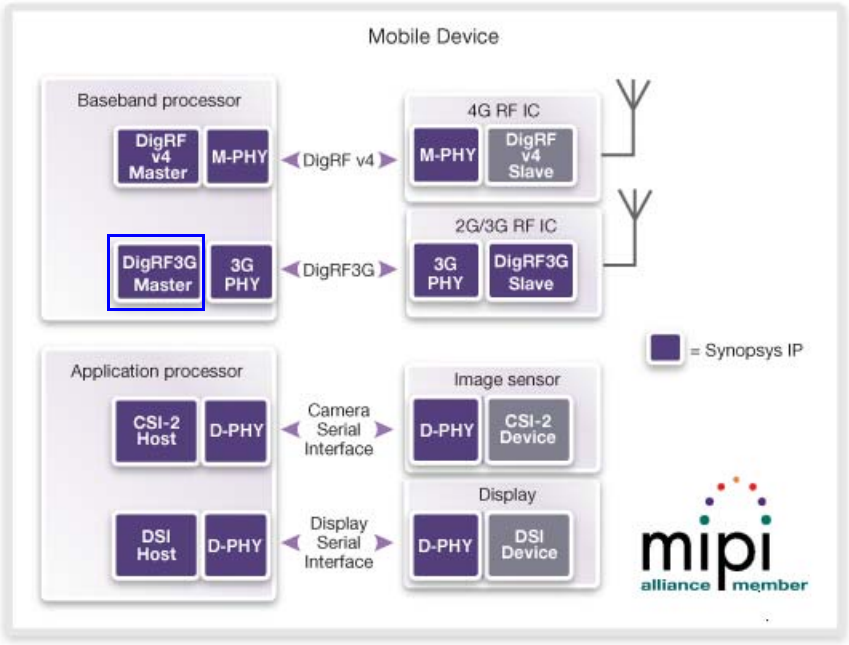
The DigRF 3G Master Controller IP core in conjunction with the Synopsys DigRF PHY provides a complete solution to design a Digital Baseband IC for communicating with a DigRF-compliant Analog Baseband/RF IC.

The DigRF 3G Master Controller is integrated with the Physical Layer based on simple serial interfaces for both transmit and receive channels. In the transmit channel, the DigRF 3G Master Controller implements frame construction and serialization. The receive channel accepts an incoming bit stream and performs header decoding and payload processing. The DigRF 3G Master Controller also has FIFO controllers to allow communication with the 2-port RAMs.

An AMBA-APB slave port is used for configuration of DigRF Physical Layer parameters, and for transmitting commands over the DigRF interface, such as Interface Control Logic Channel Functions, TAS messages, and RFIC Control messages. An interrupt function is provided in order to inform the processor on the completion of certain events. The list of events that can trigger the interrupt function is fully programmable.

Features

- DigRF Dual-Mode 2.5G/3G Controller (BaseBand side)
- Compliant with DigRF 3G Specification version 3.09
- Compatible with Synopsys DigRF Physical Layer
- Implements all Interface Control Logic Channel Functions
- Frame construction and serialization in the Transmit channel
- Header decoding and payload processing in the Receive channel
- 32-bit AMBA-APB slave interface for configuration and control of DigRF Controller and Physical Layer functions
- Programmable Processor Interrupt function
- Supports multi-channel applications
- Supports Basic handset and Local diversity with multiplexed interface configurations



The dwc_3g_digrf_master_controller datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_3g_digrf_master_controller.pdf

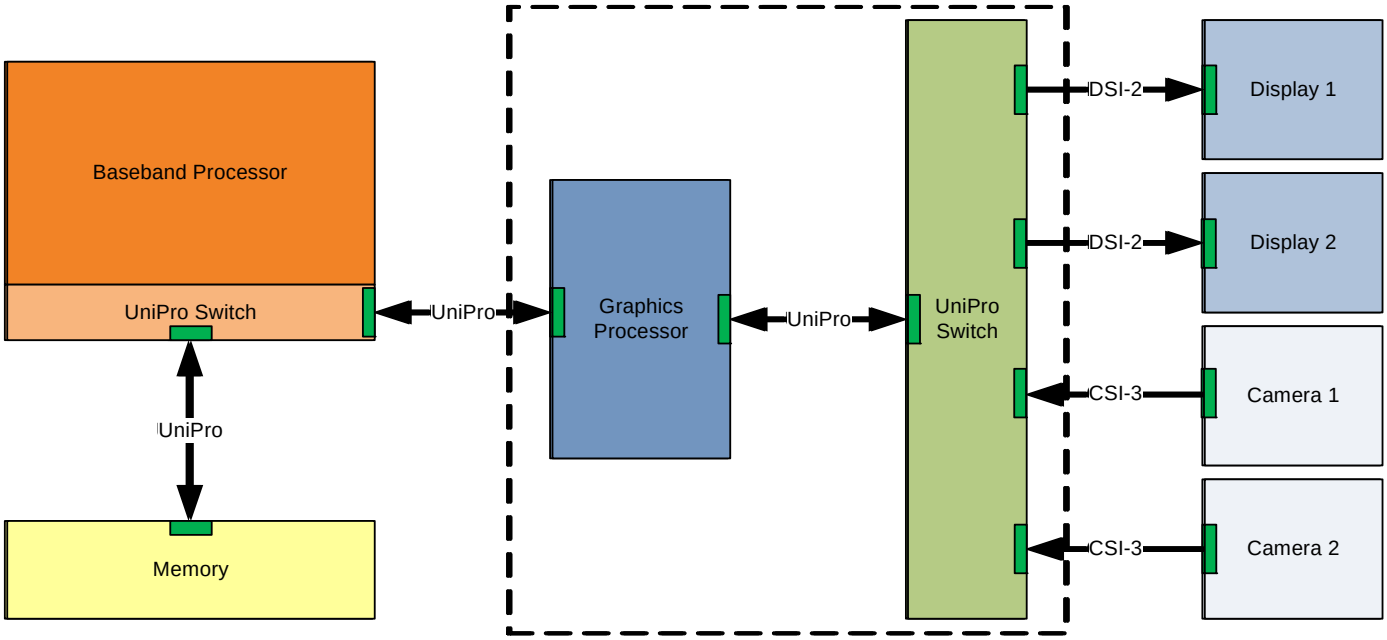
dwc_mipi_unipro

MIPI UniPro

The DWC_mipi_unipro is a MIPI UniPro compliant interface module. It provides the capability to control the UniPro link over MIPI M-PHY modules from one or more generic applications. Because of its generic nature, it is capable of transporting any kind of data between applications like the camera, display, and the memory devices on the same physical link.

Features

- MIPI® M-PHY support with RMMI compliant interface
- Configurable Device Descriptor Block (DDB) settings
- Generic Interface for the applications (CPort for data transfer and APB3/native for configuration)
- Configurable number of CPorts (up to 2048)
- Automatic flow control between the local and the remote Application (CPort end-to-end flow control)
- Automatic flow control between the local and the peer Layer 2 buffers (Layer 2 flow control)
- Reliable transmissions through error detection and automatic retransmission
- Support for up to two Traffic Classes: TC0 and TC1
- Configurable TC1 Traffic Class
- Frame prioritization using pre-emption
- Well-structured clock system (clock domains separated using FIFO structures)
- Parameterizable number of RX and TX M-PHY modules or lanes (one to four in each direction)
- Scalable maximum bandwidth (up to four times 6 Gbps in each direction)
- Configurable system data interface width: 16, 32, 64, or 128 bits
- Minimum restrictions on application clock frequency
- Support for test-modes like scantest
- Configurable number of Layer 4 test features
- Generation and check of Layer 1.5 test pattern
- Access to vendor specific M-PHY attributes



The dwc_mipi_unipro datasheet is available at:

https://www.synopsys.com/dw/doc.php/ds/c/dwc_mipi_unipro.pdf

4 Memory IP

The following Memory IP are briefly described in this section:

Component Name	Component Description	Component Type
DW_memctl	Memory Controller (page 182)	Synthesizable RTL
DW_rambist	Memory Controller (page 183)	Synthesizable RTL

To view the complete DesignWare memory portfolio, refer to the following:

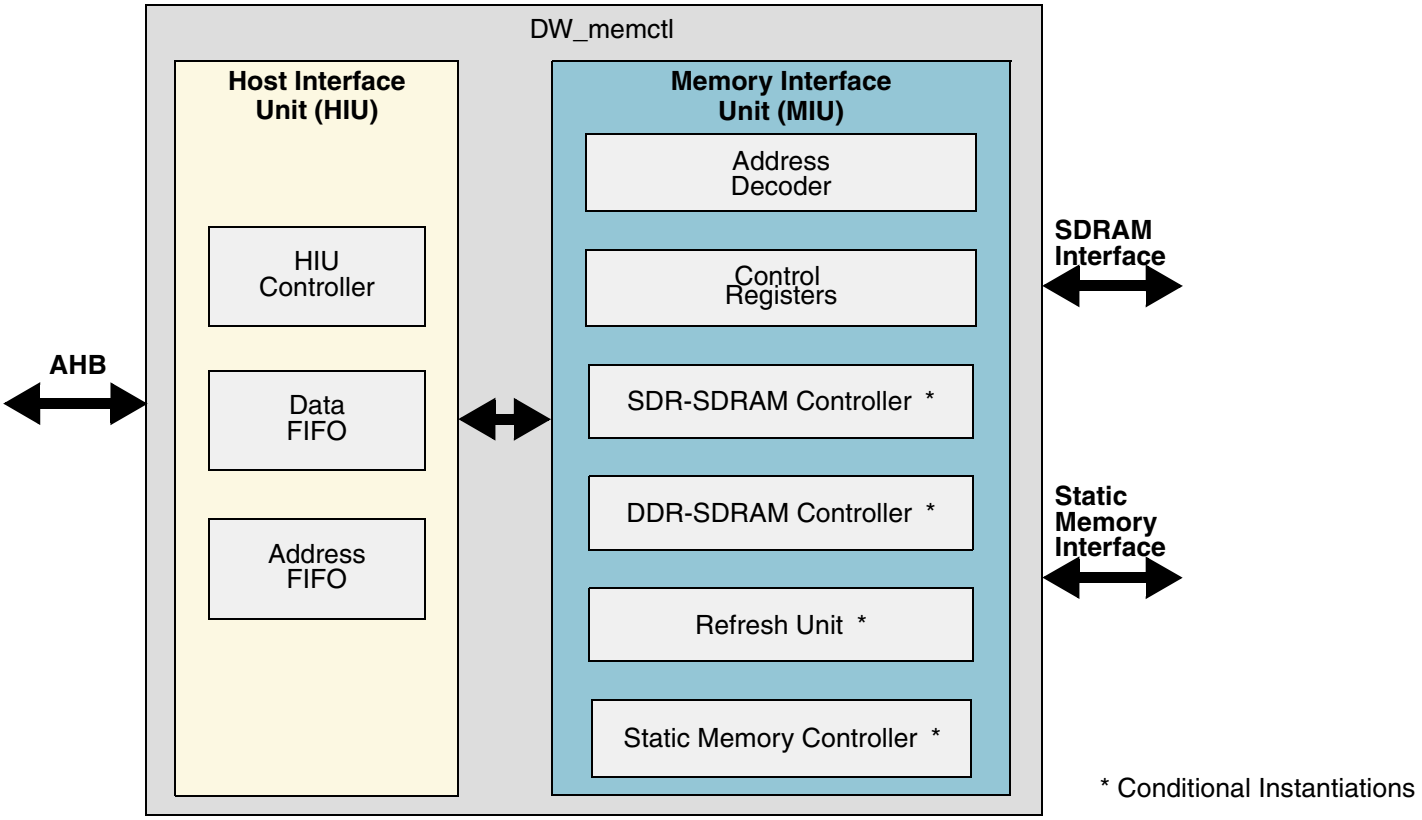
http://www.synopsys.com/dw/dwmm.php

AMBA Compliant

DW_memctl
Memory Controller

- Supports AHB data widths of 32, 64, or 128 bits, AHB address width of 32 bits
- Supports pin-based little- or big-endian modes of operation
- Supports separate or shared memory address and/or data buses between SDRAM and Static memories
- Glueless connection to all JEDEC-compliant SDRAM
- Supports up to 16 SDRAM address bits
- SDR-SDRAM, Mobile-SDRAM, and SyncFlash memory data widths: 16, 32, 64, or 128, with 1:1 or 1:2 ratios with AHB data width. DDR-SDRAMs, memory data width: 8, 16, 32, or 64,with 1:2 or 1:4 ratios with the AHB data width.
- Programmable row and column address bit widths
- Supports 2K to 64K rows, 256 to 32K columns, and 2 to 16 banks
- Supports up to 8 chip selects, with a maximum of 4 GB of address space per chip select
- Supports asynchronous SRAMs, page-mode FLASHes and ROMs
- Supports up to three sets of timing registers
- Supports external “READY” handshake pin to interface non-SRAM-type device

Note: Does not generate split, retry, or error responses on the AHB bus



The *DesignWare DW_memctl MacroCell Databook* is available at:

https://www.synopsys.com/dw/doc.php/iip/DW_memctl/latest/doc/dmctl_db.pdf

AMBA Compliant

DW_rambist

Memory Built-In Self Test

Interfaces

- IEEE 1149.1 TAP controller interface
- Two clock interface, one for a slower TAP I/F, second for at-speed BIST execution
- Optional MUX block that supports either embedded multiplexers inside the memories or user-specified multiplexers
- Flexible configuration for embedded MUX block, providing a better interface to memory control signals with different widths and polarities

Error Diagnostics

- Pause on first and subsequent failures mode, serial debugging
- Failing address and data may be scanned out for examination
- Quick debug mode, continue on failures mode, failing addresses not recorded
- Parallel debug port to observe the failing memory data bits

BIST Tests

- User choice of March LR (14n), March C– (10n) and MATS++ (6n)
- Custom (user-defined) patterns option
- Optional SRAM retention test, (5n + delay), auto pause mechanism
- Selection of background and complement background data patterns
- Default sequence or run-time selection of individual test
- Improved test execution time through reduced memory read/write cycles (each access to synchronous memory occurs in one clock cycle)
- Configuration of Mode Register reset value to provide easy power-up tests
- Higher speed clock frequency

Supported Memories

- Synchronous and asynchronous SRAM
- Asymmetrical pipelining support, up to four stages
- Support for 32 memories per BIST controller
- Highly configurable memory interface to suit most types of memories

Supported Memory Configurations

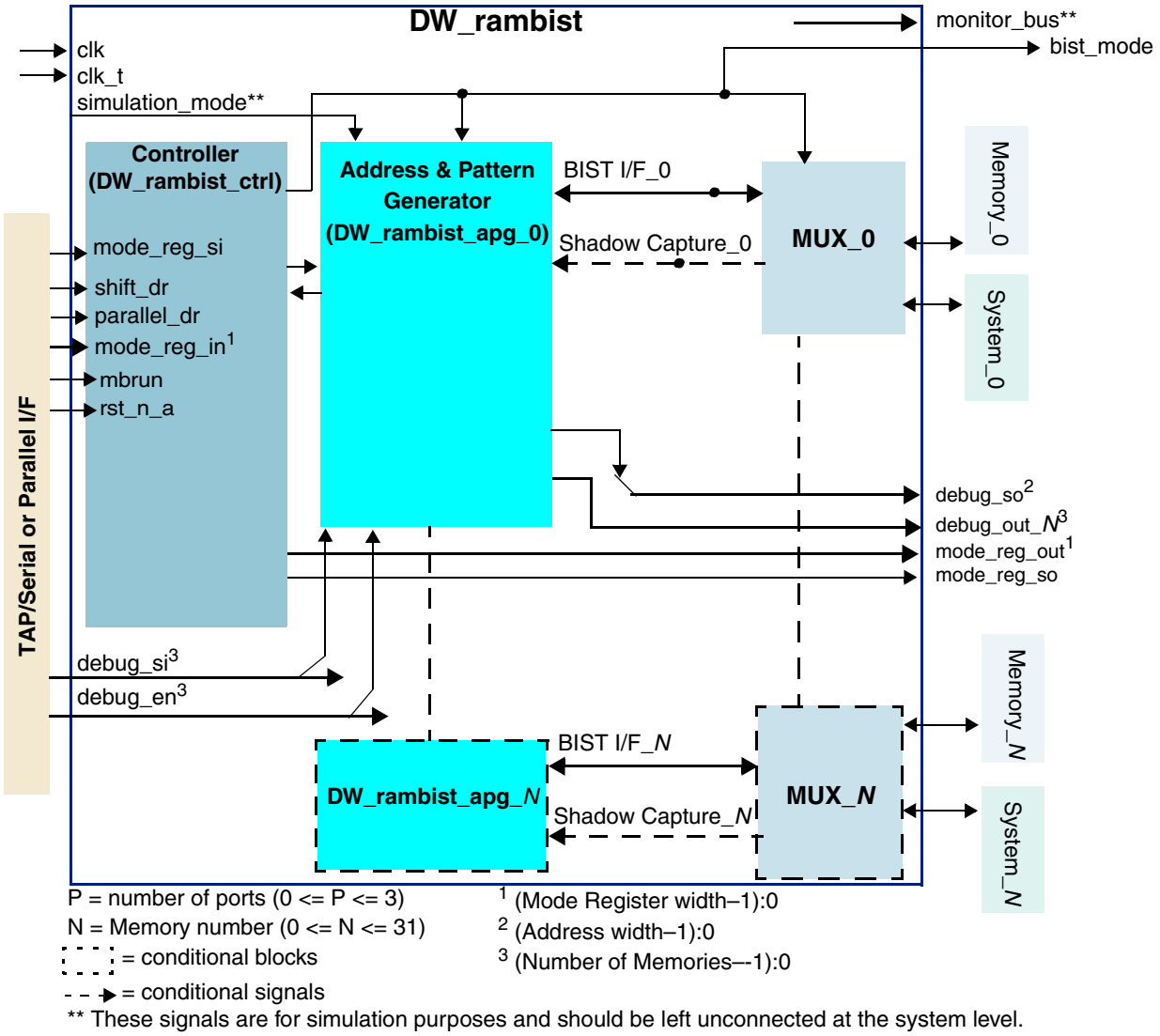
- True at-speed testing of memories in parallel
- Memory array test via single port and multi-port
- Ability to enable/disable testing of individual memories
- Multiple controller scheduling
- Support for incomplete address space

Design for test

- Configuration of shadow logic capture
- Sample script for scan chain creation and connection (part of example design)
- Integration with DFT Compiler, BSD Compiler, and TetraMax

Design for Verifiability

- simulation_mode signal to provide verification of very large configurations and to quickly check system-level interconnection



More information on the DW_rambist MacroCell can be found at:

http://www.synopsys.com/dw/doc.php/ds/i/DW_rambist.pdf

5 Processor Overview

5.1 Microprocessors/Microcontrollers

The components detailed in this section contain a page reference in the following table.

Component Name	Component Description
DWC_n2p	Nios II Processor Core (page 186)
DW_6811	8-bit Microcontroller (page 188)
DW8051	8-bit Microcontroller (page 190)

5.2 ARC Processor Family

The follow page has an overview of ARC Processors: "ARC Processor IP Portfolio" on page 192.

The components detailed in this section contain a page reference in the following table.

Processor Group	Description
ARC HS Family	"ARC HS Family" on page 195
ARC EM Family	"ARC EM Family" on page 196
ARC AS200 Audio Family	"ARC AS200 Audio Family" on page 197
ARC 600 Family	"ARC 600 Family" on page 198
ARC 700 Family	"ARC 700 Family" on page 199

Star IP

DWC_n2p
Nios II Processor Core

The Designware Nios® II Processor from Synopsys, also referred to as DWC_n2p in this document, is an ASIC implementation of Altera's popular Nios® II configurable general-purpose 32-bit RISC processor.

DWC_n2p is a single module that contains an embedded Nios II Processor and additional logic for system level debug through a JTAG interface. Users can specify configuration parameters to optimize the DWC_n2p hardware to match their system requirements.

Features

- Full 32-bit Instruction Set
- Thirty-two 32-bit general purpose registers
- Four external interrupt sources
- Combined instruction and data system port (Von Neumann Architecture)
- Support for a single optional Instruction Tightly Coupled Memory
- Support for up to 4 optional Data Tightly Coupled Memories
- Exported interface for Cache / TCM memories
- Optional exported interface for data cache memories (data cache can be omitted)
- Dynamic branch prediction minimizes taken branch penalty
- 6-stage pipelines to achieve maximum DMIPS/MHz
- 500 DMIPS Performance
- Single instruction barrel shifter
- Single instruction 32 x 32 multiply producing a 32-bit result
- Single instruction 32 x 32 divide producing a 32-bit result
- Embedded hardware-assisted On-Chip Debug (OCD) module enabling start, stop and step
- 5 pin JTAG interface with embedded tap controller for OCD debug
- Embedded JTAG UART for stdio comm.
- Embedded timer module for Nios II software backward compatibility
- Full compatibility with the Nios II Integrated Development Environment

Compatible with software environment based on the GNU C/C++ tool chain and Eclipse

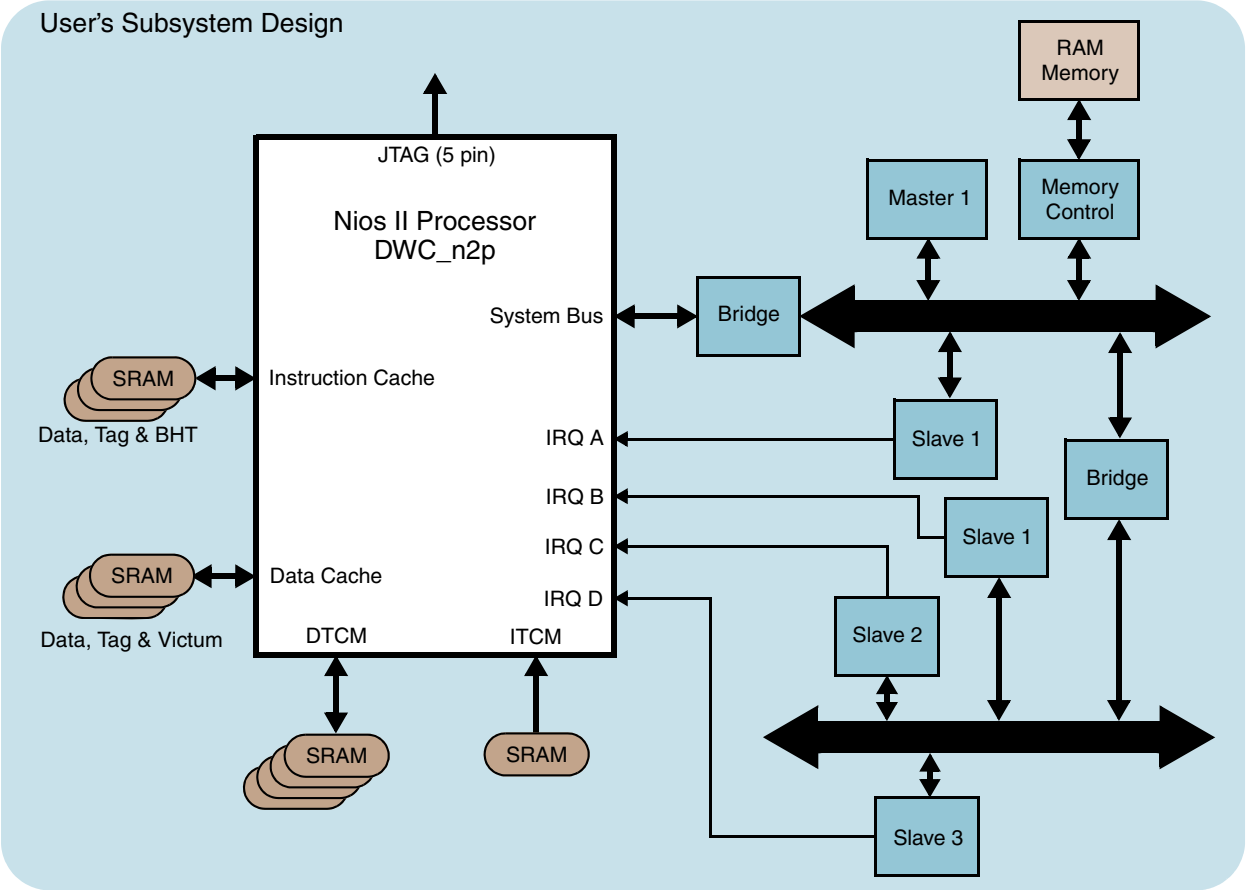
Unsupported NIOS II Features

- No Separate Instruction and Data Master ports (Harvard architecture)
- No Avalon burst protocol (Nios II Processor transfers are issued as single)
- No floating point instructions for single-precision floating point operations
- No instructions for computing 64-bit and 128-bit products
- Data Master system memory port is not removable (needed for OCD)
- No level 2 & level 3 debug support (no support for HW breakpoint and trace)

Key Configurability Options

- Instruction Cache Size: 512 – 64K
- Instruction TCM Interfaces: 0 or 1
- Instruction TCM Size: 512 – 64K
- Allow Data Writes to ITCM: Yes/No
- Number of Data TCM: 0-4
- Data TCM Size: 512 – 64K
- Data Cache Size: 0 – 64K
- Cacheless Option to remove both Data Cache and DTCM
- External Interrupts: 0-4

Configurable Priority Level per Interrupt



5.2.0.1 Nios II FPGA Base Configuration Options

Table 5-1 shows the Nios II FPGA base configuration options:

Table 5-1 Nios II FPGA Base Configuration Options

	Nios II / f Fast Processor	Nios II / s Standard Processor	Nios II / e Economy Processor
Pipeline	6 stage	5 stage	None
Hardware multiplier and barrel shifter	1 cycle	3 cycle	Emulated in software
Branch prediction	Dynamic	Static	None
Instruction cache	Configurable	Configurable	None
Data cache	Configurable	None	None
Custom instructions	Up to 256		

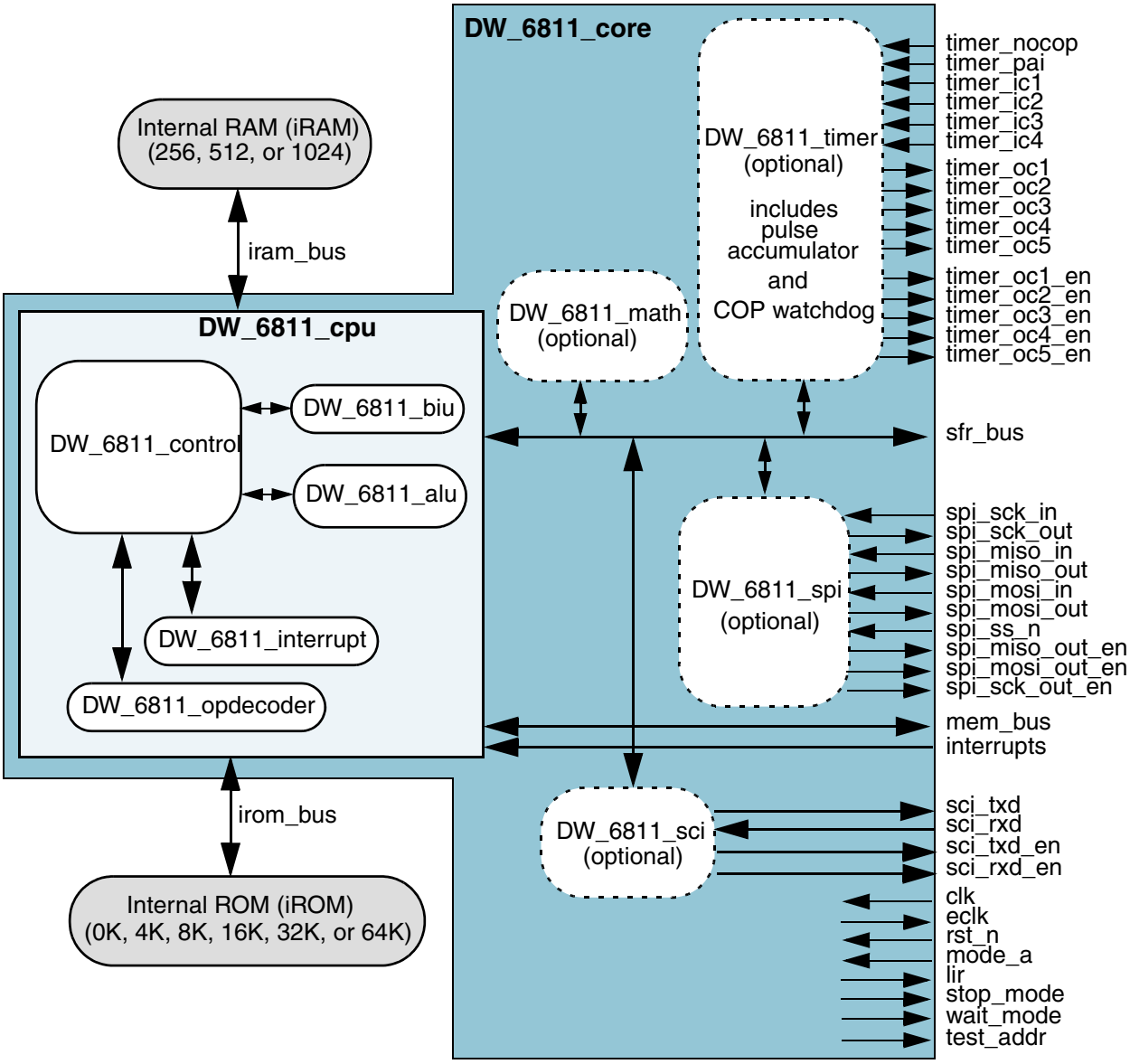
Also see the following web page for additional information:

http://www.altera.com/products/ip/processors/nios2/ni2-index.html

AMBA Compliant

DW_6811
6811 Microcontroller

- Compatibility with industry standard 68HC11 microcontroller:
  - 8-bit CPU with 8-bit/16-bit ALU:
    - Two 8-bit accumulators that can be concatenated to provide 16-bit addition, 16-bit subtraction, 16 x 16 division, 8 x 8 multiplication, shift, and rotate
    - Up to 18 maskable interrupt sources (17 maskable internal interrupts and 1 maskable external interrupt)
    - Power saving STOP and WAIT modes
  - Standard 68HC11 instruction set
- Simple integration of user-defined peripherals through external Special Function Register (SFR) interface, within SFR array space
- Fully synchronous implementation
- A BIU unit to provide control signals for memory and I/O ports:
  - Programmable memory map for internal RAM (iRAM) and SFR array spaces.
  - Parameterized internal ROM (iROM) size
  - De-multiplexed external memory interface
- Optional peripherals:
  - 16-bit timer
    - Three Input Capture (IC) channels
    - Four Output Compare (OC) channels
    - One software selectable IC or OC channel
  - 8-Bit pulse accumulator
  - COP watchdog timer system
  - SPI synchronous serial port, basic or enhanced (SPI or SPI+)
  - SCI UART, basic or enhanced (SCI or SCI+)
  - Up to 3 external reset/interrupt sources
  - Up to 17 internal interrupt sources



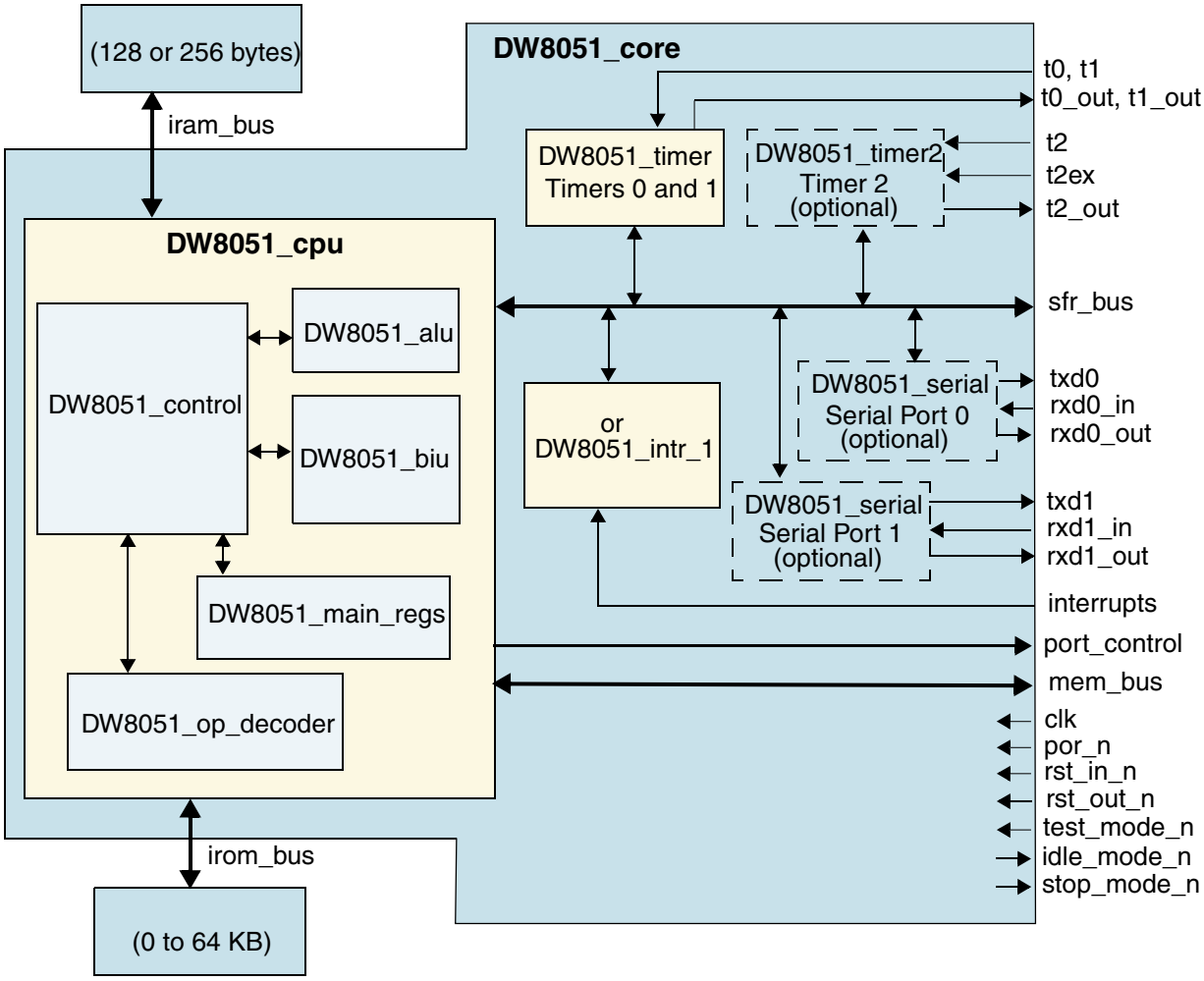
The *DesignWare DW_6811 MacroCell Databook* is available at:

http://www.synopsys.com/dw/ipdir.php?ds=dw_microcontrollers

AMBA Compliant

DW8051
8051 Microcontroller

- Compatible with industry-standard 803x/805x:
  - Standard 8051 instruction set
  - Optional full-duplex serial ports selectable through parameters
  - Optional third timer selectable through parameter
  - Control signals for standard 803x/805x I/O ports
- High–speed architecture:
  - Four clocks per instruction cycle
  - 2.5X average improvement in instruction execution time over the standard 8051
  - Runs greater than 300 MHz in 90 nanometer process technology.
  - Wasted bus cycles eliminated
  - Dual data pointers
- Parameterizable internal RAM address range
- Parameterizable internal ROM address range
- Simple integration of user-defined peripherals through external Special Function Register (SFR) interface
- Enhanced memory interface with 16-bit address bus
- Variable length MOVX to access fast/slow RAM peripherals
- Fully static synchronous design



The *DesignWare DW_8051 MacroCell Databook* is available at:

http://www.synopsys.com/dw/ipdir.php?ds=dw_microcontrollers

6 ARC Processor IP Portfolio

6.1 Introduction

Synopsys' DesignWare® ARC® Processors are a family of 32-bit CPUs that SoC designers can optimize for a wide range of uses, from deeply embedded to high-performance host applications in a variety of market segments. Designers can differentiate their products by using patented configuration technology to tailor each ARC processor instance to meet specific performance, power and area requirements. The DesignWare ARC processors are also extendable, allowing designers to add their own custom instructions that dramatically increase performance. Synopsys' ARC processors have been used by over 170 customers worldwide who collectively ship more than 1 billion ARC-based chips annually.

All DesignWare ARC processors utilize a 16-/32-bit ISA that provides excellent performance and code density for embedded and host SoC applications. The RISC microprocessors are synthesizable and can be implemented in any foundry or process, and are supported by a complete suite of development tools.

DesignWare ARC processors are supported by a variety of 3rd-party tools, operating systems and middleware from leading industry vendors, including members of the ARC Access Program.

Also see the following web page for additional information:

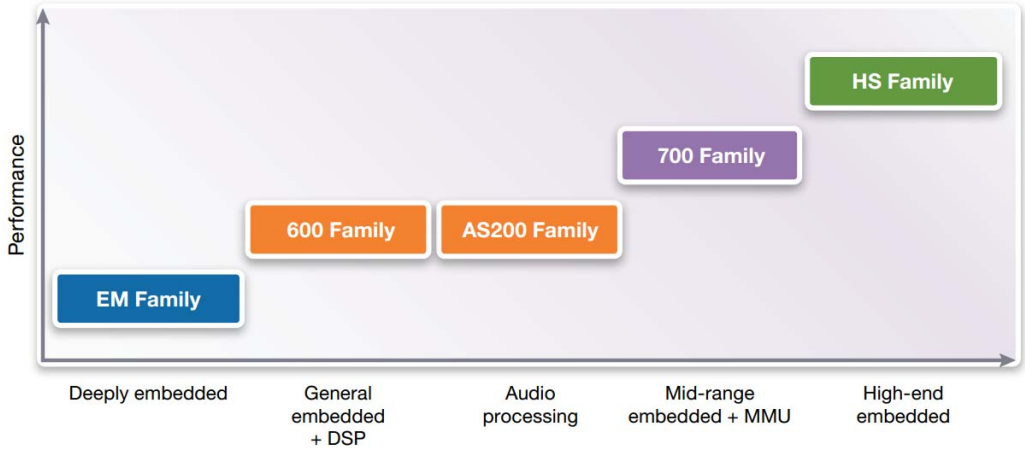
http://www.synopsys.com/IP/ProcessorIP/ARCProcessors/Pages/default.aspx

6.2 Processor Families Overview

Synopsys' DesignWare® ARC® Processor IP includes the ARC HS, ARC EM, ARC 600 and ARC 700 families of 32-bit processor cores, as well as the ARC AS211 and AS221 audio processors and optimized software audio codecs.

The following families of ARC processors are available:

- ARC HS Family
- ARC 700 Family
- ARC 600 Family
- ARC EM Family
- ARC AS200 Audio Family



ARC processor cores are based on a flexible and proven instruction set architecture (ISA) with features optimized for a broad range of embedded and deeply embedded applications:

- Performance-efficient designs deliver maximum performance while consuming a minimum amount of power and silicon area
- Highly configurable processors can be performance- and power-optimized for each instance on an SoC while sharing a common programming model
- Extensible ISA supports user-defined custom instructions, enabling integration of users' proprietary hardware to accelerate application-specific tasks
- Streamlined system integration through the ability to closely couple memory and directly map peripherals to the core, reduce system latency and cost

6.2.1 ARC HS Family

The ARC HS Family includes the HS34 Processors and HS36 Processors. The HS34 supports Close Coupled Memory (CCM) while the HS36 adds up to 64KB of instruction and data caches. The processors are optimized for high performance with power efficiency (DMIPS/mW) and area efficiency (DMIPS/mm2), making them ideally suited for embedded applications with very high speed data and signal processing requirements. The HS Processors are available in dual-core and quad-core versions for applications that require even higher performance.

6.2.2 ARC 700 Family

The ARC 700 Family includes the ARC 710D, ARC 725D and ARC 770D Processors. The processors, which can run at more than 1 GHz in a 40G process, are ideal for embedded applications and tasks where high performance and low power consumption is required. The ARC 700 Family supports single-cycle CCMs for instructions and data, as well as configurable I-cache and D-cache. Optional DSP and floating point capabilities enable designers to address a wide range of signal processing requirements with a single processor, simplifying the design, lowering silicon-area and enabling faster debug of the chip. The ARC 770D features a full memory management unit (MMU) and is designed specifically to improve execution performance for embedded applications running Linux.

6.2.3 ARC 600 Family

The ARC 600 Family includes the ARC 601, ARC 605, ARC 610D and ARC 625D Processors. The ARC 600 Processors target embedded applications where enhanced DSP performance with small size and low power consumption is required. The addition of support for an advanced XY memory architecture enables efficient DSP processing with fast access to algorithm coefficients stored in dedicated X and Y memories. This enables low power and efficient processing of audio data and other digital signals and information. The ARC 600 Family includes flexible memory options such as single-cycle CCMs for instructions and data, as well as configurable I-cache and D-cache. The optional floating point extension enables additional signal processing capabilities for single- and double-precision floating point calculations with minimal additional area and power consumption.

6.2.4 ARC EM Family

The ARC EM Family includes the ARC EM4, ARC EM6 and ARC EM SEP Processors. The ARC EM4 supports instruction and data CCMs and the EM6 adds instructions and data caches. The ultra-compact cores feature excellent code density, small size and very low power consumption making them ideal for power-critical and area-sensitive embedded and deeply embedded applications. The dynamic power consumption of the ARC EM4 core can be as low as 4µW/MHz, particularly well-suited for battery-powered applications. ARC EM SEP is designed for use in ISO 26262 safety-compliant automotive applications, combining a highly efficient and compact processor with integrated hardware safety features and an ASIL D ready certified compiler to help enable automotive designers to achieve ISO 26262 safety compliance. The ARC EM SEP also features detailed ISO 26262 compliant safety documentation.

6.2.5 ARC AS200 Audio Family

The ARC AS200 Family includes the AS211SFX and AS221BD Audio Processors. These processors feature powerful audio DSP capabilities and support a broad portfolio of certified audio codecs and post-processing software from a range of popular standards including Dolby®, DTS®, Microsoft® and SRS. The AS211SFX Audio Processor is an excellent solution for consumer, portable and mobile applications including portable audio players, digital cameras, media players and digital TV where lowest power and smallest area are required. The AS221BD Processor is a dual-core processor designed for high-performance, multi-channel HD audio and Blu-ray Disc™ applications.

ARC HS Family

High-speed 32-bit processors for high-end embedded applications

The ARC HS Family includes the HS34 Processors and HS36 Processors. The HS34 supports Close Coupled Memory (CCM) while the HS36 adds up to 64KB of instruction and data caches. The processors are optimized for high performance with power efficiency (DMIPS/mW) and area efficiency (DMIPS/mm2), making them ideally suited for embedded applications with very high speed data and signal processing requirements. The HS Processors are available in dual-core and quad-core versions for applications that require even higher performance.

HS34 – High-performance, cacheless processor for real-time control

HS36 – High performance processor with up to 64KB of instruction and data caches

See the following web page for additional information:

http://www.synopsys.com/IP/ProcessorIP/ARCProcessors/arc-hs/Pages/default.aspx

Key Features

- 10-stage pipeline based on ARCv2 ISA
- Up to 1MB instruction and data close coupled memory (CCM)
- 64-bit loads and stores
- IEEE 754-compliant floating point unit
- Native ARM® AMBA® AXI ™ and AHB™ interfaces
- Single-, dual- and quad-core configurations

Example Applications

- Solid state drive (SSD) controller
- Home gateways
- Digital TV
- Baseband control
- Set-top box
- Home networking

ARC EM Family

Ultra-compact, ultra low-power processors for deeply embedded applications

The ARC EM Family includes the ARC EM4, ARC EM6 and ARC EM SEP Processors. The ARC EM4 supports instruction and data CCMs and the EM6 adds instructions and data caches. The ultra-compact cores feature excellent code density, small size and very low power consumption making them ideal for power-critical and area-sensitive embedded and deeply embedded applications. The dynamic power consumption of the ARC EM4 core can be as low as 4µW/MHz, particularly well-suited for battery-powered applications. ARC EM SEP is designed for use in ISO 26262 safety-compliant automotive applications, combining a highly efficient and compact processor with integrated hardware safety features and an ASIL D ready certified compiler to help enable automotive designers to achieve ISO 26262 safety compliance. The ARC EM SEP also features detailed ISO 26262 compliant safety documentation.

EM4 – Ultra-compact, cacheless processor

EM6 – Ultra-compact processor core with up to 32KB of instruction and data caches

EM SEP – Ultra-compact processor for automotive safety-compliant applications

See the following web page for additional information:

http://www.synopsys.com/IP/ProcessorIP/ARCProcessors/ARCEM/Pages/default.aspx

Key Features

- 3-stage pipeline based on ARCv2 ISA, featuring high code density
- Up to 1MB instruction and data close coupled memory (CCM), 2MB on EM SEP
- Very small size - less than 10K gates
- Shadow registers for fast context switch
- Enhanced sleep modes
- Native ARM® AMBA® AHB™, AHB-Lite™, and BVCI interfaces

Example Applications

- Solid state device controllers
- Power management
- Smart appliances
- Advanced driver assistance systems
- Sensor control
- Wearable devices

ARC AS200 Audio Family

Efficient single/dual core audio processors, optimized codecs

The ARC AS200 Family includes the AS211SFX and AS221BD Audio Processors. These processors feature powerful audio DSP capabilities and support a broad portfolio of certified audio codecs and post-processing software from a range of popular standards including Dolby®, DTS®, Microsoft® and SRS. The AS211SFX Audio Processor is an excellent solution for consumer, portable and mobile applications including portable audio players, digital cameras, media players and digital TV where lowest power and smallest area are required. The AS221BD Processor is a dual-core processor designed for high-performance, multi-channel HD audio and Blu-ray Disc™ applications.

AS211SFX – Compact, low-power audio processor with up to 32KB of instruction and data caches

AS221BD – Dual-core, high-performance audio processor

ARC Audio Codecs – Extensive portfolio of certified encoders and decoders for ARC audio processors

See the following web page for additional information:

http://www.synopsys.com/dw/ipdir.php?ds=arc_audio_processors

Key Features

- 5-stage pipeline
- Dual MAC with 80-bit accumulator
- AMBA XXI or BVCI interfaces
- ARC XY Advanced DSP solution
- ARC-optimized audio codecs support Dolby, DTS, Microsoft, SRS technologies and more

Example Applications

- Portable audio players
- Digital TV, set-top boxes
- Sound bars
- Multi-channel HD
- Wireless headsets and speakers

ARC 600 Family

General purpose embedded processor cores with DSP capabilities

The ARC 600 Family includes the ARC 601, ARC 605, ARC 610D and ARC 625D Processors. The ARC 600 Processors target embedded applications where enhanced DSP performance with small size and low power consumption is required. The addition of support for an advanced XY memory architecture enables efficient DSP processing with fast access to algorithm coefficients stored in dedicated X and Y memories. This enables low power and efficient processing of audio data and other digital signals and information. The ARC 600 Family includes flexible memory options such as single-cycle CCMs for instructions and data, as well as configurable I-cache and D-cache. The optional floating point extension enables additional signal processing capabilities for single- and double-precision floating point calculations with minimal additional area and power consumption.

601 – Low-power cacheless processor with instruction and data CCMs

605 – Low-power cacheless processor with instruction and data CCMs and power management unit

610D – Low-power cacheless processor with instruction and data CCMs, as well as DSP features

625D – Low-power processor with DSP features and up to 32KB of instruction and data caches

See the following web page for additional information:

http://www.synopsys.com/IP/ProcessorIP/ARCProcessors/ARC600/Pages/default.aspx

Key Features

- 5-stage pipeline based on ARCv1 ISA
- Up to 512KB instruction and 256KB data close coupled memory (CCM)
- AMBA AXI or BVCI interfaces
- JTAG debug interface + optional SmarRT trace debug
- Optional XY DSP and FPX floating point extensions

Example Applications

- Solid state device controllers
- Personal audio players
- Wireless LANs
- Industrial control
- Security encryption/decryption

ARC 700 Family

Efficient 32-bit processors for mid-range embedded and host applications

The ARC 700 Family includes the ARC 710D, ARC 725D and ARC 770D Processors. The processors, which can run at more than 1 GHz in a 40G process, are ideal for embedded applications and tasks where high performance and low power consumption is required. The ARC 700 Family supports single-cycle CCMs for instructions and data, as well as configurable I-cache and D-cache. Optional DSP and floating point capabilities enable designers to address a wide range of signal processing requirements with a single processor, simplifying the design, lowering silicon-area and enabling faster debug of the chip. The ARC 770D features a full memory management unit (MMU) and is designed specifically to improve execution performance for embedded applications running Linux.

710D – Cacheless CPU/DSP processor for real-time control

725D – Efficient CPU/DSP processor with up to 64KB of instruction and data caches

770D – CPU/DSP processor with MMU and Linux acceleration package

See the following web page for additional information:

http://www.synopsys.com/IP/ProcessorIP/ARCProcessors/ARC700/Pages/default.aspx

Key Features

- 7-stage pipeline based on ARCv1 ISA
- Up to 512KB instruction and 256KB data close coupled memory (CCM)
- Dynamic branch prediction for high throughput
- AMBA AXI or BVCI interfaces
- JTAG debug interface + optional SmarRT trace debug

Example Applications

- Digital TV
- Network devices
- Set-top box
- Network attached storage (NAS)
- Embedded Linux-based devices

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