SYNOPSYS®

DesignWare Building Block IP

Release Notes

DWBB_201506.0 Release for Design Compiler

Supported DC Synthesis Releases:
See Table 1-2 on page 5.

Supported Synplify FPGA Releases:
See Table 1-3 on page 6.

DWBB_201506.0
K-2015.06
June 2015

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Release Notes: Building Block IP

This document contains the latest information about the Synopsys DesignWare Building Block DWBB_201506.0 IP Release for Design Compiler (DC), Synplify Pro (FPGA) and VCS MX. This library of IP was previously called the DesignWare Foundation (DWF) Library. The older DWF nomenclature appears in licensing and file naming. This release is based on the K-2015.06 Synthesis release.

This document also contains release information for Building Block IP in FPGA synthesis (Synplify tools).

The following lists the topic described in this document:

- "Features and Changes in Version DWBB_201506.0 / K-2015.06" on page 4
- "Known Problems and Limitations" on page 4
- "DWBB Version Compatibility with Tool Versions" on page 5
  - "Design Compiler Compatibility" on page 5
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1.1 Features and Changes in Version DWBB_201506.0 / K-2015.06

This section lists DWBB IP additions/updates for the current release. This section also describes the release information and issues related to using Building Block IP with Synopsys Synplify Premier and Synplify Premier with Design Planner tools.

- Removed EST download and installation procedures from this and other documents
- This is a bug fix release.

Table 1-1 STARs Resolved in DWBB_201506.0 (K-2015.06)

STAR ID	Type	Description
9000872804	Bug	DW_ln creates garbled message when op_width exceeds legal range (2 to 60)
9000862271	Bug	DW_sincos has values that are larger than 1 ulp error for several configurations

1.2 Known Problems and Limitations

STAR ID	Type	Description
See "STARs on the Web" on page 16 for the latest information about current pending issues.		

- The simulation models for **DW_pulseack_sync** and **DW_data_sync_na** do not support configurations with the *tst_mode* parameter set to 2, which is supported by the component.
- The auto-swapping feature of preferred flip-flops in the synthesis flow for some DesignWare Synchronizers and FIFOs is initially correct, but due to downsizing during subsequent DC optimization, the preferred flip-flops are replaced with smaller cells. There will be an enhancement in a future release to avoid optimization of these "preferred flops."
- When using **DW_ecc** with more than 1000 data bits, Design Compiler may encounter a fatal error unless the Tcl variable, hdlin_while_loop_iterations, is set to a high enough value before compiling. The following is an example of the command to use before the compile_ultra is executed.

```
set hdlin_while_loop_iterations 8200
```

This issue will be resolved in a future release of the DesignWare Library.

1.3 DWBB Version Compatibility with Tool Versions

Attention View this document on the Synopsys website for the latest compatibility information: http://www.synopsys.com/dw/doc.php/doc/dwf/manuals/dwbb_relnotes.pdf

1.3.1 Design Compiler Compatibility

Table 1-2 shows which DWBB IP releases work with the supporting Design Compiler releases:

Table 1-2 DesignWare Building Block Release Compatibility

Building Block IP Release	2015.06 DC	2014.09 -SP5 DC	2014.09 -SP4 DC	2014.09 -SP3 DC	2014.09 -SP2 DC	2014.09 -SP1 DC	2014.09 DC	2013.12 -SP5 DC	2013.12 -SP4 DC	2013.12 -SP3 DC	2013.12 -SP2 DC	2013.12 -SP1 DC	2013.12 DC	2013.03 -SP5 DC	2013.03 -SP4 DC	2013.03 -SP3 DC
DWBB_201506	Bundled															
DWBB_201409.5		Bundled														
DWBB_201409.4			Bundled													
DWBB_201409.3				Bundled												
DWBB_201409.2					Bundled											
DWBB_201409.1						Bundled										
DWBB_201409.0							Bundled									
DWBB_201312.5								Bundled								
DWBB_201312.4									Bundled							
DWBB_201312.3										Bundled						
DWBB_201312.2											Bundled					
DWBB_201312.1												Bundled				
DWBB_201312.0													Bundled			
DWBB_201303.5														Bundled		
DWBB_201303.4															Bundled	
DWBB_201303.3																Bundled

1.3.2 Synplify FPGA Synthesis Tool Compatibility

Table 1-3 shows which DWBB IP releases work with the Synplify Premier releases:

Table 1-3 DesignWare Building Block / Synplify Premier Release Compatibility

Building Block IP Release / (DC Bundled)	Synplify Premier Release								
	2015.03	2014.09 -SP2	2014.09 -SP1	2014.09	2014.03	2013.09 -SP1	2013.09	2013.03 -SP1	2012.09 -SP1
DWBB_201.506 / K-2015.06	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201409.5 / J-2014.09-SP5	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201409.4 / J-2014.09-SP4	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201409.3 / J-2014.09-SP3	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201409.2 / J-2014.09-SP2	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201409.1 / J-2014.09-SP1	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201409.0 / J-2014.09	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201312.5 / I-2013.12-SP5	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201312.5 / I-2013.12-SP5	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201312.4 / I-2013.12-SP4	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201312.3 / I-2013.12-SP3	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201312.2 / I-2013.12-SP2	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201312.1 / I-2013.12-SP1	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201312.0 / I-2013.12	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201303.5 / H-2013.03-SP5	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201303.4 / H-2013.03-SP4	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201303.3 / H-2013.03-SP3	✔	✔	✔	✔	✔	✔	✔	✔	✔

1.3.3 VCS MX Compatibility

The DWBB_201506.0 Building Block IP release works with VCS MX.

1.4 Features and Changes in Previous Versions (History)

1.4.1 DWBB_201409.4 / J-2014.09-SP5

This section describes the release information and issues related to using Building Block IP with Synopsys Synplify Premier and Synplify Premier with Design Planner tools.

- This is a bug fix release.

Table 1-4 STARs Resolved in DWBB_201409.5 (J-2014.09-SP5)

STAR ID	Type	Description
9000878133	Bug	The **DW_div_seq_sim.vhd** module is not in sync with the modeling of corruption detection in the Verilog version.

1.4.2 DWBB_201409.4 / J-2014.09-SP4

This section describes the release information and issues related to using Building Block IP with Synopsys Synplify Premier and Synplify Premier with Design Planner tools.

- Updated simulation models for DW_8b10b_dec and DW_8b10b_enc to be compatible with Native Low Power features of VCS.
- This is a bug fix release.

Table 1-5 STARs Resolved in DWBB_201409.4 (J-2014.09-SP4)

STAR ID	Type	Description
9000853770	Bug	Designs containing instance(s) of **DW_fp_exp** resulting in INCONCLUSIVE result from Formality.
9000851903	Bug	When configured without an input register (in other words, when the parameter *input_mode* is set to 0), the Verilog simulation models for components **DW_div_seq**, **DW_mult_seq** and **DW_sqrt_seq** are overly pessimistic in generating error messages based on changes on the operand input(s).
9000864335	Bug	The **DW_fifo_2c_df** datasheet has incorrect parameter limits for *ram_depth* and *width*.

1.4.3 DWBB_201409.3 / J-2014.09-SP3

This section describes the release information and issues related to using Building Block IP with Synopsys Synplify Premier and Synplify Premier with Design Planner tools.

- DesignWare Developers Guide document updated for new attributes in SLDB
- This is a bug fix release.

Table 1-6 STARs Resolved in DWBB_201409.3 (J-2014.09-SP3)

STAR ID	Type	Description
9000628477	Bug	Elaboration-time latch inferences observed when synthesizing **DW_arb_rr**

Table 1-6 STARs Resolved in DWBB_201409.3 (J-2014.09-SP3) (Continued)

STAR ID	Type	Description
9000729139	Bug	Modulo operator when using DC command “set_message_info -id UID-95 -stop_on” causing error (cla, cla2 and cla3 implementations of **DW_div**)
9000813521	Enhance	**DW_exp2** simulation model does not support op_width range 39-60 (only 2-38). Note: upper range is now support only for Verilog model in Synopsys VCS

1.4.4 DWBB_201409.2 / J-2014.09-SP2

- This is a bug fix release.

Table 1-7 STARs Resolved in DWBB_201409.2 (J-2014.09-SP2)

STAR ID	Type	Description
9000732052 9000731628	Bug	Incorrect *err_mode* parameter description on Verilog simulation model for **DW_fifo_s2_sf**. The datasheet description is correct.
9000813903	Bug	**DW_fp_div** has 1ulp rounding error for some operand pairs when the configuration uses *sig_width*=29.

1.4.5 DWBB_201409.1 / J-2014.09-SP1

- This is a bug fix release.

Table 1-8 STARs Resolved in DWBB_201409.1 (J-2014.09-SP1)

STAR ID	Type	Description
9000782646	Bug	The ‘str’ implementation of **DW_fp_div** provides incorrect results for output z and status inexact bits with some operand pairs when `a/b` remainder = 0. The output `z` may show 1 ulp error, but only when rnd is 1, 3, or 4. The status inexact bit incorrectly becomes '1' at all rnd modes with some operand pairs when there is no remainder.

1.4.6 DWBB_201409.0 / J-2014.09

- This is a bug fix release.

1.4.7 DWBB_201312.5 / I-2013.12-SP5

- The following new component was added to the DWBB Library:
  - DW_ram_2r_2w_s_dff - Synchronous Write, Asyncronous Read, 4-port (2 read/2 write) Flip-Flop based RAM

- This is a bug fix release. The following table shows the STARs fixed in DWBB_201312.5 release:

Table 1-9 STARs Resolved in DWBB_201312.5 (I-2013.12-SP5)

STAR ID	Type	Description
9000744388	Bug	**DW_tap** and **DW_tap_uc** remove redundant clock-phase logic on TCK path.
9000758151	Bug	Remove invalid mx2 implementation from **DW01_bsh** datasheet.

1.4.8 DWBB_201312.4 / I-2013.12-SP4

- This is a bug fix release. The following table shows the STARs fixed in DWBB_201312.4 release:

Table 1-10 STARs Resolved in DWBB_201312.4 (I-2013.12-SP4)

STAR ID	Type	Description
9000741261	Bug	Mismatch between simulation and synthesis in the **DW_div_ seq** component. This issue also affects **DW_mult_seq** and **DW_sqrt_seq** components.

1.4.9 DWBB_201312.3 / I-2013.12-SP3

- This is a bug fix release. The following table shows the STARs fixed in DWBB_201312.3 release:

Table 1-11 STARs Resolved in DWBB_201312.3 (I-2013.12-SP3)

STAR ID	Type	Description
9000702931	Bug	Fatal with datapth gating enabled
9000712371	Bug	**DW_log2** datasheet contains incorrect instance of DW_lp_multifunc
9000736629	Bug	Incorrect functionality of **DW_data_qsync_lh**

1.4.10 DWBB_201312.2 / I-2013.12-SP2

- Components **DW02_cos**, **DW02_cos** and **DW02_sincos** are now obsolete. Use the **DW_sincos** component for all designs going forward. The datasheets for these components are marked obsolete.
- Update to HDL-120 message to include loader node information.
- This is a bug fix release. The following table shows the STARs fixed in DWBB_201312.2 release:

Table 1-12 STARs Resolved in DWBB_201312.2 (I-2013.12-SP2)

STAR ID	Type	Description
9000720958	Bug	**DW_fp_sincos** component datasheet and simulation model removal of *arch=2* parameter that references "obsolete" **DW02_sincos** component.
9000712371	Bug	**DW_log2** datasheet contains incorrect instance of **DW_lp_multifunc**.
9000708193	Enhance	Details required on how push and pop clock frequencies can be varied within the **DW_fifoctl_2c_df**, **DW_fifo_2c_df** and **DW_asymfifoctl_2t_df** components.

Table 1-12 STARs Resolved in DWBB_201312.2 (I-2013.12-SP2) (Continued)

STAR ID	Type	Description
9000585947	Enhance	Provide methodology for pre-computing **DW_ecc** checkbits for parameterizable width.

1.4.11 DWBB_201312.1 / I-2013.12-SP1

- This is a bug fix release. The following table shows the STARs fixed in DWBB_201312.1 release

Table 1-13 STARs Resolved in DWBB_201312.1 (I-2013.12-SP1)

STAR ID	Type	Description
9000690530	Bug	Synthetic_library settings result in UISN-65 error message
9000688940	Bug	Discrepancy between simulation model and actual synthesized netlist and document for **DW_fifo_s2_sf**.

1.4.12 DWBB_201312.0 / I-2013.12

- The following new components have been added to the DWBB Library:
  - DW_div_sat - Combinational Divider with Saturation
  - DWF_dp_mult_comb - Combined Unsigned/Signed Multiply
  - DWF_dp_mult_comb_sat - Combined Unsigned/Signed Multiply and Saturate
  - DWF_dp_mult_ovfldet - Multiply and Overflow Detection
  - DWF_dp_mult_sat - Combined Unsigned/Signed Multiply and Saturate
- This is a bug fix release. The following table shows the STARs fixed in DWBB_201312.0 release

Table 1-14 STARs Resolved in DWBB_201312.0 (I-2013.12)

STAR ID	Type	Description
9000685189	Bug	DW_pl_reg datasheet needs to be updated to indicate max stages = 1024

1.4.13 DWBB_201303.5 / H-2013.03-SP5

- Descriptions for 'pparch' and 'apparch' implementation of DW02_mult, DW02_multp, DW_square, and DW_squarep have been enhanced in the component datasheets.
- This is a bug fix release. The following table shows the STARs fixed in DWBB_201303.5 release.

Table 1-15 STARs Resolved in DWBB_201303.5 (H-2013.03-SP5)

STAR ID	Type	Description
9000663666	Bug	The Verilog simulation model of the **DW_div** component generates an incorrect remainder not correctly sign-extended when input b=0, tc=1 and *b_width* >=2**a_width*.
9000655497	Bug	Inconsistency between synthesis and simulation model of the **DW_arb_dp** component when synchronous reset is used and *output_mode=0*.

Table 1-15 STARs Resolved in DWBB_201303.5 (H-2013.03-SP5) (Continued)

STAR ID	Type	Description
9000661751	Bug	Inconsistency between synthesis and simulation model of the **DW_arb_sp** component when synchronous reset is used and *output_mode=0*.
9000668457	Bug	Incorrect simulation model behavior in the **DW_arb_dp** component when synchronous reset is used and *output_mode=0*.
9000668458	Bug	Incorrect simulation model behavior in the **DW_arb_sp** component when using synchronous reset and *output_mode=0*.
9000661687	Bug	When trying to asynchronously reset the **DW_tap_uc** in the absence of `tck`, gate level simulations show undefined value (Xs) on the outputs.
9000661688	Bug	The Verilog simulation model of the **DW_sync** component could cause a race condition due to declaration of a derived constant (F_SYNC_TYPE_INT) as a wire.

1.4.14 DWBB_201303.4 / H-2013.03-SP4

- This is a bug fix release. The following table shows the STARs fixed in DWBB_201303.4 release.

Table 1-16 STARs Resolved in DWBB_201303.4 (H-2013.03-SP4)

STAR ID	Type	Description
9000629609	Bug	The Verilog simulation model of the **DW_asymfifoctl_s2_sf** component has an incorrect Default Value of 0 set for the *rst_mode* parameter.

1.4.15 DWBB_201303.3 / H-2013.03-SP3

- The 'rpl' implementation of DW_div was moved to the standard library to support divide, remainder, modulus, and rotate operaters for DC-Expert without consuming a designware license.
- This is a bug fix release. The following table shows the STARs fixed in DWBB_201303.3 release.

Table 1-17 STARs Resolved in DWBB_201303.3 (H-2013.03-SP3)

STAR ID	Type	Description
9000637593	Enhance	Using VHDL ror/rol functions is not fully supported in the standard library.
9000634390	Bug	The 'str' implementation of DW_fp_mult causes DC to crash when *sig_width=2.*

1.4.16 DWBB_201303.2 / H-2013.03-SP2

- This is a bug fix release. The following table shows the STARs fixed in DWBB_201303.2 release.

Table 1-18 STARs Resolved in DWBB_201303.2 (H-2013.03-SP2)

STAR ID	Type	Description
9000629609	Bug	For **DW_asymfifoctl_s2_sf**, default *rst_mode* parameter value between simulation and synthesis models differ.

Table 1-18 STARs Resolved in DWBB_201303.2 (H-2013.03-SP2) (Continued)

STAR ID	Type	Description
9000625421	Bug	**DW_div** “cla3” implementation causes DC fatal error during mapping optimization when using “set hdlin_keep_signal_name {user_driving}” There is no fatal when default value “all_driving” is used.
9000621343	Bug	**DW_fp_mac** has an error with 'huge status bit' when *ieee_compliance*=1
9000621342	Bug	**DW_fp_dp2** has an error with 'huge status bit' when *ieee_compliance*=1

1.4.17 DWBB_201303.1 / H-2013.03-SP1

- **DW_div** enhanced with new implementations: **cla3** and **mlt**. See the DW_div Datasheet for details.
- This is a bug fix release. The following table shows the STARs fixed in DWBB_201303.1 release.

Table 1-19 STARs Resolved in DWBB_201303.1 (H-2013.03-SP1)

STAR ID	Type	Description
9000615535	Bug	The output of the **DW_thermdec** may be inverted (depending on the design constraints and cells available in the target technology library) when the *width* parameter is set to an odd value.
9000617967	Bug	The **DW_fp_dp2** component provides incorrect results during the operation (-0) + (-0) in all rounding modes.
9000617968	Bug	The **DW_fp_mac** component provides incorrect results during the operation (-0) + (-0) in all rounding modes.
9000600055	Bug	The default value of *ieee_compliance* parameter of **DW_fp_mult** VHDL simulation model is inconsistent with other DW components.
9000605068	Bug	The Verilog simulation model of **DW_fifoctl_2c_df** component has a race condition on the 'next_almost_empty_d_tmp' signal.

1.4.18 DWBB_201303.0 / H-2013.03

- This is a bug fix release. The following table shows the STARs fixed in the DWBB_201303.0 release.

Table 1-20 STARs Resolved in DWBB_201303.0 (H-2013.03)

STAR ID	Type	Description
9000600054	Bug	Default value of the parameter *ieee_compliance* in the VHDL entity file, **DW_fp_invsqrt**.vhd had incorrect default value which affected the behavior of the VHDL simulation model **DW_fp_invsqrt**_sim.vhd when *ieee_compliance* is not specified.
9000600055	Bug	Default value of the parameter *ieee_compliance* in the VHDL entity file, **DW_fp_mult**.vhd had incorrect default value which affected the behavior of the VHDL simulation model **DW_fp_mult**_sim.vhd when *ieee_compliance* is not specified.

1.5 Obsoleted IP for New Designs

DesignWare Building Block IP components are occasionally removed from the library. The process of removing components occurs in three stages over a period of at least two years.

1.5.0.1 Stage 1: Notification of Obsoleted IP

The first stage in obsoleting IP is a notification that the IP will not be supported in the future. You can still simulate and synthesize the IP, but a warning is issued during simulation.

There is currently no DesignWare Building Block IP at this stage.

1.5.0.2 Stage 2: Notification of Obsoleted Simulation Models

The second stage of the IP obsolescence is to remove the simulation model from the library. This occurs approximately 1 year from the time of the announcement that a particular IP is being obsoleted for new designs. Simulation is not possible, but synthesis of old designs still is possible

There is currently no DesignWare Building Block IP at this stage.

1.5.0.3 Stage 3: Notification of Obsoleted Synthesis Models

The third and final stage of the IP obsolescence process is to remove the remaining synthesis model from the library. This occurs approximately 2 years from the time of the announcement that a particular IP is being obsoleted for new designs. Simulation and synthesis is not possible.

The following DWBB IP is at stage 3 of obsolescence: **DW02_sincos**, **DW02_sin**, and **DW02_cos**.

1.5.0.4 Notification of Obsoleted Synthesis Implementations

There are no recent obsoleted synthesis implementations.

1.6 Installation

DesignWare Building Block IP is installed with your DC synthesis release. If you install a patch to DC, refer to "When to Run the Reanalysis Scripts" on page 14.

1.6.1 How Can I Tell Which DWBB Version Is Installed?

One way to view which DesignWare Building Block IP library you currently have installed on your UNIX system is to issue the following command:

```
% cat $SYNOPSYS/dw/version
```

The string that is returned looks something like this:

```
K-2015.06-DWBB_201506.0
```

The "K-2015.06" portion indicates the Synthesis base release. The "DWBB_201506.0" portion indicates the DesignWare Building Block IP release, which uses the YYYYMM.S format. In this example, the year (YYYY) is 2014, the month (MM) is 09 (September) and the service pack release is 3 (SP3).

To determine which DWBB Library version is installed over VCS MX, issue the following command:

```
% cat $VCS_HOME/dw/version
```

The string that is returned is displayed similar to the following:

```
X-XXXXX-DWBB_201506.0 #(DC version scheme - K-2015.06)
```

1.6.2 Installation of Building Block IP for FPGA Synthesis

Building Block IP installation for FPGA synthesis is the same process as for DC. For details, refer to "Installation" on page 14. You can use an existing DC installation without modification for FPGA synthesis, as long as the version is compatible (see Table 1-3 for version compatibility).

1.6.3 Version Label for Technical Support

For future reference, a file exists under $SYNOPSYS/dw called 'version', which contains the release version label. You need to know this label when contacting Synopsys technical support.

1.6.4 When to Run the Reanalysis Scripts

There are two special script files included with each DWBB release that reanalyze your DWBB IP source files. When run, the dw_analyze_syn.csh or dw_analyze_sim.csh script reanalyzes all existing DC and VCS MX components in your $SYNOPSYS/dw/ or $VCS_HOME/dw/ tree to ensure compatibility with newer versions of Synopsys Synthesis releases.

You must run the appropriate script for either of the following situations:

- When you receive a patch to DC that does not include DWBB IP, or if you add another tool after DC installation, you must do the following:

```
setenv SYNOPSYS path
set path = (${SYNOPSYS}/platform/syn/bin $path)
setenv LM_LICENSE_FILE ${SYNOPSYS}/admin/license/key:$LM_LICENSE_FILE
cd $SYNOPSYS/dw/scripts
./dw_analyze_syn.csh
egrep -i 'warning|error' $SYNOPSYS/dw_analyze_syn.*.log
```

- When you receive a patch to VCS MX that does not include DWBB IP, or if you add another tool after VCS MX installation, you must do the following for every target platform:

```
set path = (${VCS_HOME}/platform/bin $path) # VCS MX
setenv LM_LICENSE_FILE ${VCS_HOME}/admin/license/key:$LM_LICENSE_FILE
cd $VCS_HOME/dw/scripts
./dw_analyze_sim.csh
egrep -i 'warning|error' $VCS_HOME/dw_analyze_sim.log
```

path is the directory location where DesignWare Building Block IP and Synopsys synthesis and simulation tools have been installed, (for, example, "/synopsys/H-2013.03" or "/synopsys/VCS_mxversion").

platform is one of the following: sparc64, sparcOS5, linux, or any supported platform.

The reanalyze_sim.csh script is also available, along with dw_analyze_sim.csh. It is a simple reanalyze script that is independent of versions and the installation location of DWBB IP.

1.7 Documentation

1.7.1 DesignWare Building Block IP Datasheets and Manuals

PDF files containing the complete set of current DesignWare Building Block IP datasheets and manuals exist in the directory, $SYNOPSYS/dw/doc. The latest documentation is also available on the Synopsys website at the following location:

http://www.synopsys.com/dw/dwlibdocs.php

You can also find the documentation for a specific Building Block component by:

1. Using "Search for IP" field to find your desired DWBB component
2. Click on the "More Information..." link provided
3. Click on the Documentation: "Show Documents..." link to view the document list
4. Click on the document title to display the specific document

1.7.2 FPGA Synthesis Documentation

For a "QuickStart" on using Building Block IP with Synplify Premier tools for FPGA synthesis, refer to "Using DesignWare Building Block IP in FPGA Synthesis" in the *DesignWare Building Block IP User Guide*.

For Synplify Premier tool and FPGA synthesis information, see the *Synopsys FPGA Synthesis User Guide.*

1.8 Getting Help

1.8.1 STARs on the Web

You can view a complete list of problem reports for this product, including problems identified after product release, by accessing the STAR report on the Web. Note that you must have a SolvNet ID in order to view STAR reports.

You can access STAR reports for any component via the IP Search web page:

http://www.synopsys.com/dw/ipsearch.php

1.8.2 Filing Synopsys Technical Action Requests (STARs)

Synopsys records any reported problems or enhancement requests in an internal database called the Synopsys Technical Action Request (STAR) system. To file a STAR, provide the following information to Synopsys Customer Support:

- Your company name and site ID number.
- Your name or the name of the person to contact about the problem.
- Your company address, phone number, and fax number.
- A detailed description of the problem.
- The full text of any error messages, including numbers that appear at the end of messages.
- The name and version number of the tool with the problem. To obtain the version number, invoke the tool and read the copyright header.
- A test case that demonstrates the problem, which you can send using electronic mail or tape.

1.8.3 Requesting New IP and Submitting Ideas

To request new DesignWare Building Block IP, visit the DesignWare Web site http://www.designware.com or send e-mail to designware25@synopsys.com. You can also call the Synopsys Support Center at 1-800-245-8005 or at 1-650-584-4013.

1.8.4 Searching PDF Files

You can search for a text string within a single PDF document or entire document set using the Search feature of Adobe Reader (formerly Acrobat Reader).

You can also search through an individual PDF file located on a web server or on your local file system; however, in order to search through a collection of PDF files, those files must reside on your local file system.

In addition, many collections of PDF files provided by Synopsys are preconfigured with a search index file called INDEX.PDX, which enables even faster search operations. The Adobe Reader locates the INDEX.PDX file automatically for use in the next search operation.