**VE527 Computer-Aided Design of Integrated Circuits**

**Written Assignment Five Solution**

1. (10%) What is the function for the following ROBDD?



**Solution**: .

2. (10%) How many input patterns , where , will satisfy the following BDD (i.e., let the function of this BDD be 1)?



**Solution**: There are 10: (1,0,-,-), (0,-,1,-), (0,-,0,1).

3. (40%) A simple comparator takes two 2-bit unsigned binary numbers and and compares their magnitude. Its output if and only if is GREATER THAN . For example, since , the output . However, for and , since they are equal, the output .

Draw the ROBDD for the output of the 2-bit comparator. Suppose the variable ordering is (i.e., is the closest to the root and is the farthest away from the root).

What does the ROBDD look like for the variable ordering ?

**Solution**:

For the order , the initial BDD is



After simplification, we get



For the order , the initial BDD is



After simplification, we get



4. (18%) Consider the function expressed in the CNF form:

where , , , ,   
, , , . Assume that we have decided . Make this assignment and then run Boolean constraint propagation (BCP) by applying the unit clause rule. You should continue BCP **until** you cannot make any additional progress on the formula. What is your conclusion after BCP and simplification? If the CNF is still unresolved, show the final CNF.

**Solution**:

With , we have

, , , , , , ,   
.

From , we have . Then, we get

, , , , , , , .

From , we have . Then, we get . unSAT!

5. (10%) BDDs operating on general Boolean logic, and SAT solvers operating on CNF clause lists, are both techniques that we can use to work with complex logic. But they each have different capabilities. Which of the following statements are true about each respective technology? Select the correct ones.

1. We can use a BDD to find ALL satisfying assignments of a Boolean function.
2. We can use SAT to find a satisfying assignment of a Boolean function.
3. SAT solvers and BDD packages may not always work for any Boolean function.
4. SAT solvers and BDD packages will always work for any Boolean function.
5. We can use a BDD to find a satisfying assignment of a Boolean function.
6. A SAT solver allows us to perform many manipulations on a set of Boolean functions, such as AND, OR, NOT, XOR, XNOR, etc.
7. A BDD package allows us to perform many manipulations on a set of Boolean functions, such as AND, OR, NOT, XOR, XNOR, etc.
8. Suppose we have two gate level hardware implementations of some function, call them F and G. We want to check if the hardware for F produces identical outputs as the hardware for G. We can do this using BDDs, but we cannot do this using a SAT solver.
9. Suppose we have two gate level hardware implementations of some function, call them F and G. We want to check if the hardware for F produces identical outputs as the hardware for G. We can do this using a SAT solver, but we cannot do this using BDDs.

**Solution**: a, b, c, e, g.

6. (12%) As we talked in lecture, we can apply SAT to check if two different gate-level implementations and of a logic function are identical. In this problem, we will try a trivial example. We want to compare whether is identical to . The figure below shows the gate-level circuit on which we can ask the SAT question to see whether and are identical. We have also labeled two internal nodes as and as shown below. Write the CNF formula that is satisfiable if and only if the gate-level circuit below is satisfiable.   
**Hint**: apply the gate consistency function discussed in class.

Suppose F(x,y) = x and G(x,y) = x+xy. The connectivity of network to check if F and G are the same is as follows:

The network has two primary inputs x and y; one primary output r; two internal wires p and q; and three internal gates from G1 to G3.

G1 is an AND gate having two inputs and one output. Its two inputs connect to primary inputs x and y, and its output connects to internal wire p.

G2 is an OR gate having two inputs and one output. Its two inputs connect to primary inputs x and internal wire p, and its output connects to internal wire q.

G3 is an XOR gate having two inputs and one output. Its two inputs connect to primary inputs x and internal wire q, and its output connects to primary output r.


**Solution**:

CNF for the entire circuit is