VAN-CHAN NGO

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SUMMARY

My research activities aim at building reliable and secure computer systems by developing formal frameworks which guarantee that software satisfies formally its specification, especially embedded safety-critical software such as automotive, avionic, and health-care applications. The construction of a formal framework involves the research and knowledge of principles of programming languages, compiler design and development, and formal methods including model checking, theorem proving, and static analysis for providing formal assurances that the specification is fulfilled.

EDUCATION

INRIA, Rennes, France *August 2014*
Ph.D in Computer Science & Engineering
Programming Language, Compiler, and Formal Verification of Embedded and Safety-Critical Systems
First Class Honors

Université de Grenoble, Verimag, Grenoble, France *June 2008*
Masters in Computer Science & Engineering
Embedded Software and Systems
French Government Scholarship, Évariste Galois Program

Hanoi University of Technology, Hanoi, Vietnam *July 2005*
Engineer Degree in Computer Engineering
Information Systems and Communication, Centre of Talented Training - PFIEV
First Class Honors with Congratulations of the Ministry of Education

EXPERIENCE

Carnegie Mellon University *2016 - Present*
Research Fellow, Computer Science *Pittsburgh, PA, US*

· Automatic symbolic resource bound (e.g., time and memory) analysis of functional and imperative programs for detecting security vulnerability including time side-channel attacks, stack overflow, etc
· Static analysis for probabilistic programs, e.g., automatic symbolic expected resource bound analysis such as execution time and memory usage

INRIA France *2014 - 2015*
R&D Engineer *Rennes, France*

· Formal verification of probabilistic SystemC models using Statistical Model Checking
· Probabilistic temporal assertion-based verification of SystemC models

INRIA France *2011 - 2014*
Research Assistant *Rennes, France*

· Formal verification of the highly optimizing and industrial synchronous compiler, Signal, which is used in model-based design of real-time and safety-critical systems
· Using translation validation approach to prove the preservation of clock semantics, data dependencies and value-equivalence for source code and the compiled programs using several techniques including model checking, theorem proving, graph transformation

Tech Propulsion Lab USA *2010 - 2011*
Software Architect *Saigon Branch, Vietnam*

· Design and development of embedded mobile software on iOS and Android platforms
· Project management in the mobile development department

IBM Zurich Lab and ZISC *2008 - 2010*
Research Assistant *Zurich, Switzerland*

· Formally verifying and certifying the design of secure boot processes in IBM AIX mainframes
· Formalizing the boot process and its security properties using the language of the model checker Spin, Promela.

Verimag Lab *2007 - 2008*
Internship *Grenoble, France*

· Automated verification framework to prove formally the IND-CPA security property of asymmetric encryption schemes
· The framework represents the encryption schemes as *frame* in cryptographic π-calculus, and formalize the IND-CPA property as a equivalent relation between two frames

IBM Vietnam *2006 - 2007*
Senior Software Engineer *Hanoi, Vietnam*

· Working on text search engine of the IBM data base management DB2

FPT Software *2005 - 2006*
Software Engineer *Hanoi, Vietnam*

· Working on embedded systems for navigation

Security Systems, MISOFT *2003 - 2005*
Software Developer *Hanoi, Vietnam*

· Developing a distributed firewall as an operation system based on the package filtering library and the Linux kernel in C++ and Python

Hanoi University of Technology *2000 - 2003*
Tutor *Hanoi, Vietnam*

· Student teaching in Mathematics and Physics

TECHNICAL STRENGTHS

· **Programming Languages**. Strong knowledge: C/C++, OCaml - Familiarity: Assembly, Java, Python
· **Toolchains**. Strong knowledge: GCC, LLVM Compiler Infrastructure
· **Formal Methods & Modeling Languages**. Strong knowledge: Synchronous Languages, Logics and Temporal Logics, Model Checking, Theorem Proving, Static Analysis - Familiarity: Verilog, SystemC
· **Formal Method Tools**. SPIN, SMV, UPAAL, PRISM, SMC Plasma Lab, Yices, Z3, Coq, Frama-C
· **Embedded Software Development**. Familiarity: AVR, Arduino, RTLinux, FreeRTOS

LANGUAGES

English - Advance   **French** - Advance   **Vietnamese** - Mother-tongue

AWARDS

Ph.D scholarship, INRIA France
DEA scholarship from the French government, Université de Grenoble, France
Masters scholarship from the Italian government, Politecnico di Milano, Italy
Masters scholarship from SamSung company, ICU-KAIST, South Korea
Scholarships from Hanoi University of Technology for excellent academic results