BrainScaleS-2 Single Chip System (SGA2 Milestone 9.2.1)

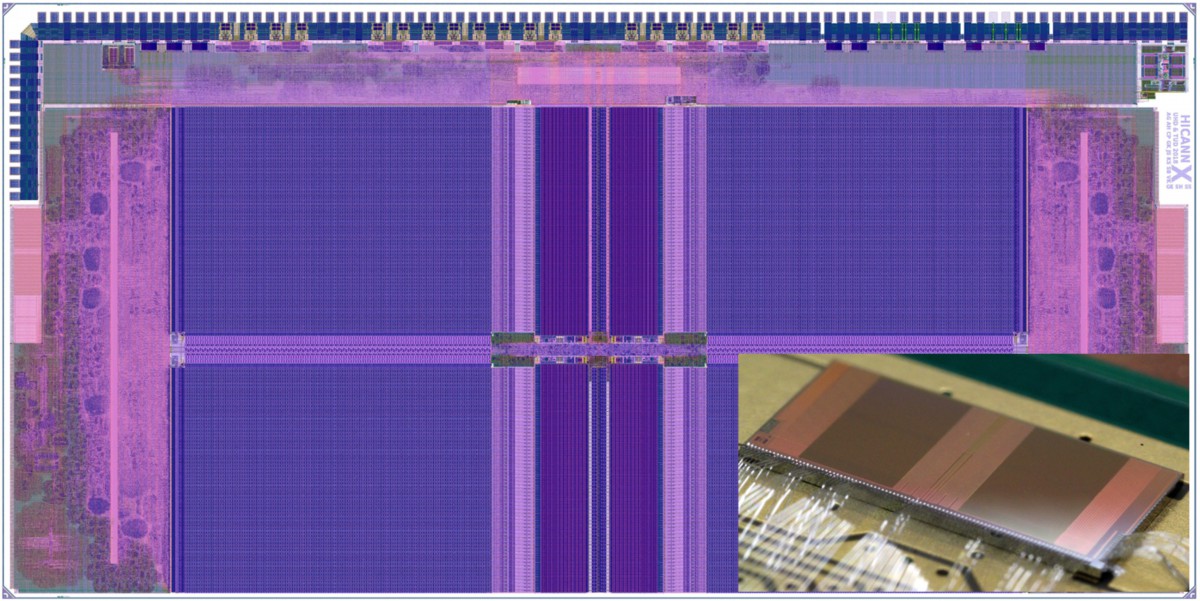


Figure 1: Layout drawing (large image) and chip photograph (small insert) of the HICANN-X microchip. The HICANN-X is the first full-size prototype of the BrainScaleS-2 system. It contains 128k plastic synapses and 512 neurons and operates at an acceleration factor of 1000 compared to biological real-time.

|  |  |  |  |
| --- | --- | --- | --- |
| Project Number: | 785907 | Project Title: | Human Brain Project SGA2 |

|  |  |
| --- | --- |
| Document Title: | BrainScaleS 2 single chip system |
| Document Filename: | HBP\_SGA2\_SP9\_MS9.2.1.docx |
| Milestone Number: | SGA2 MS9.2.1 (MS366) |
| Deliverable Type: | Report |
| Work Package(s): | WP9.2 |
| Dissemination Level: | CO = Confidential |
| Planned Delivery Date: | SGA2 M12 / 31 March 2019 |
| Actual Delivery Date: | SGA2 M12 / 22 March 2019 |

|  |  |
| --- | --- |
| Authors: | Johannes Schemmel, UHEI (P 47) |
| Compiling Editors: |  |
| Contributors: |  |
| SciTechCoord Review: |  |

|  |  |
| --- | --- |
| Abstract: | The status of the BrainScaleS-2 single chip system. |
| Keywords: | BrainScaleS-2, neuromorphic computing, single chip system |

**Introduction**

During SGA2 the BrainScaleS (BSS) second generation system will be developed further from small prototypes to the full-scale chip version ready for wafer-scale integration in SGA3. There are two versions of these full-scale chips planned, named HICANN-X and HICANN-DLS. HICANN-X is the first iteration and serves two purposes: first, test all features of the neuromorphic network core scaled to their final size, and second, provide a single, or small multiple, -chip(s) platform for early users of the second BrainScaleS generation, BrainScaleS-2 (BSS-2).

BSS-2 offers significant improvements regarding plasticity and multi-compartment modeling, which are not present in BSS-1. It contains a fully embedded-MIPS compatible RISC CPU with a custom SIMD accelerator for plasticity calculations, configuration, environment simulation, slow-control and debugging support. Therefore, the complexity of the BSS-2 system is significantly higher that BSS-1.

# Status of the Single Chip System

To operate an HICANN-X chip, a single-chip system has been developed, consisting of:

* a chip-carrier printed-circuit board
* an interface board to the BrainScaleS single-chip test platform
* a new FPGA firmware for said test platform
* software extensions to the different tiers of the BrainScaleS software infrastructure, to support all hardware changes and new features, especially the new integrated parallel processing core (plasticity processing unit, PPU)

All components have been completed and are ready for commissioning of the single-chip BSS-2 platform. Detailed informations can be found in the SGA2 month 12 compound deliverable (D9.6.1) as well as in the SGA2 SP9 deliverable software upgrade for BrainScaleS-2 (D9.2.1).

The HICANN-X microchip was received from manufacturing in December 2018. Initial tests showed no measurable functionality, not even leakage currents from the IOs to the supply could be observed. Further inspection of the production database showed that all IO filler cells were missing. Therefore, a second production run was necessary and we are currently (March 2019) waiting for the corrected chips to arrive for testing.

Regarding the cause of the problem, one has to know how the generation of the production database is distributed between the manufacturer, the channel partner, and the customer. Due to the sensitivity of the intellectual property involved, the manufacturer, in our case TSMC, does not trust the customer with the design data of their library cells, instead, they provide the customers with black-boxed library cells only. The channel partner, in our case the IMEC location of the Europractice-IC-service in Belgium, gets the complete data from TSMC to fill it in after they received the layout from their customers.

The IO ring, which contains the circuits interfacing the inner parts of the chip, the core, with the external world, consists of different kinds of such library cells, which are placed automatically by the design software. Due to the fact that the design data is not available to the customer, the software places the black-boxed cells instead, which contain only information about the interconnections of the cells to the bond-pads and the core.

The problem with the black-boxed cells IMEC provided to us in the case of the HICANN-X chip is their missing lateral, ring-internal connections. The IO ring cells are edge-connected to form a continuous string of IO cells. In the case that there are gaps for geometrical reasons, the software inserts IO filler cells. Theses filler cells contain a set of metal stripes to connect two adjacent IO cells with each other, but they contain no connections to the core or to bond pads at all.

Unfortunately, the cells provided by IMEC do not model these internal connections, like, for example other manufactures, namely UMC which did the manufacturing of BSS-1, do. The black-boxed IO filler cells we have received from IMEC therefore contain nothing at all. They are only a placeholder at certain coordinates in the layout for the later processing done at IMEC. Due to this fact it was not possible for our verification software to detect the fact that they got lost in the last processing step generating the database for IMEC, which contained only the IO cells themselves. Doing all recommended steps, we read in the database and rechecked, but no warnings were flagged, since it is impossible to detect missing black-box IO fillers with the process design kit provided by IMEC to us.

This procedure, which makes it impossible for customers to detect dropped or moved IO filler cells by their suite of automated checks, is the recommended procedure of IMEC and they declined any responsibility. Being dependent on them for our research, we therefore had to accept their decision and had to do a rerun on our own budget. They gave us a 15% discount due to the importance of the HBP project, though.

To avoid a repetition of the observed failure for the second manufacturing pass and to take into account the fact that the replaced black-box cells in the IO ring are not checked for continuity at IMEC, we arranged with IMEC to get the metal-backend layout data of the processed database, i.e. the data IMEC would send to the manufacturer, but only for the metal layers, not the transistors. This allows us to check continuity at least manually, which is obviously not how we think this should be done, but in the case of the HICANN-X chip should be sufficient to ensure a correct IO ring. We would strongly suggest that IMEC switches to a more professional procedure, one that does not shift all risks to the customer.

The single chip system will be delayed approximately 5 months and the manufacturing of the HICANN-DLS chip has to be moved to SGA3 due to lack of money for an additional chip production.