PROCESSOR_51

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ABSTRACT

Processor_51, an alias for the NYU-6463 Processor, is a 32bit Processor designed completely using VHDL. The processor has a specialized Instruction Set Algorithm and supports both sequential. We have implemented the RC5 Encryption Algorithm using the instructions of this ISA.

HARDWARE USED

Digilent Nexys 4 DDR Board

Family : Artix7
Device : XC7A100T
Package : CSG324
Speed Grade : -1

SOFTWARE USED

Xilinx ISE Project Navigator
Purpose : VHDL Modelling

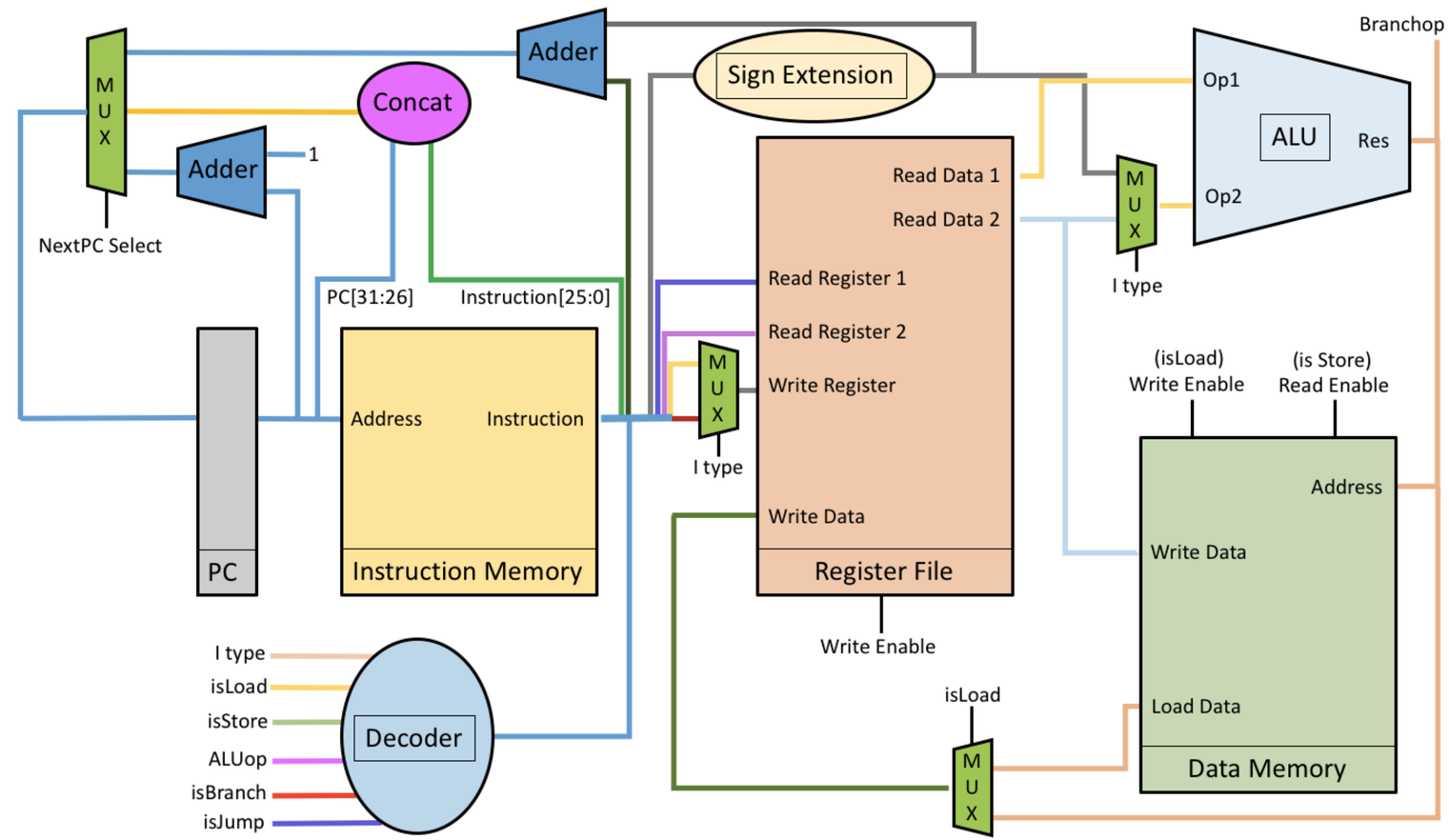
Digilent Adept
Purpose : Programming the FPGA

Python 2.7
Purpose : Assembler

FEATURES

Speed	83.918 MHz
Instruction per Cycle (IPC)	1 instruction
Instruction per Second (IPS)	83.918 Million
ALU Operations	Arithmetic : add, subtract Logical : or, nor, and Compare : bne, beq, blt Shift : shl, shr
ISA	3 address
Instruction Length	32bits
Instruction Memory	2 KB
Register File	32 32bit Registers
Data Memory	2 KB
Assembler (Convert Assembly to Machine Code)	Yes

ARCHITECHTURE



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