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| **Equivalence Class Design** | | | | | | | | | |
| **Valid EC** |  |  |  |  | | **Invalid EC** | |  |  |
| **EC ID** | **Condition** | | | |  | **EC ID** | **Condition** | | |
| Ec01 | Lock = : 1 <= < 35 | | | |  | Ec07 | Lock = : < 1 | | |
| Ec02 | Lock = : 35 <= <= 70 | | | |  | Ec08 | Lock = : 70 < | | |
| Ec03 | Stock = : 1 <= < 40 | | | |  | Ec09 | Lock = : < 1 | | |
| Ec04 | Stock = : 40 <= <= 80 | | | |  | Ec10 | Lock = : 80 < | | |
| Ec05 | Barrel = : 1 <= < 45 | | | |  | Ec11 | Lock = : < 1 | | |
| Ec06 | Barrel = : 45 <= <= 90 | | | |  | Ec12 | Lock = : 90 < | | |
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| **Test Case Design and Test Results** | | | | | | | | | | | | | |
|  |  | | | |  |  |  |  | |  |  | | |
| **Project Name:** | Commission Program | | | | | | | **Project ID:** | | Lab5 | | | |
| **Test Strategy:** | Strong Robust Equivalence Class Testing | | | | | | | **Designer:** | | Chanrungrueang jantavara | | | |
| **Test Environment:** | | **JUnit5** | | | | | | | | | | | |
|  |  | | | |  |  |  |  | |  |  | | |
| **Test Case ID** | **Input** | | | **Expected Result** | | | | | **Actual Result** | | | **Status (Pass/Fail/No run)** |
| Lock | Stock | Barrel |
| TC01 | 1 | 1 | 1 | 1000 | | | | | 0 | | | Fail |
| TC02 | 1 | 1 | 45 | 20500 | | | | | 20500 | | | Pass |
| TC03 | 1 | 1 | 0 | -1 | | | | | 0 | | | Fail |
| TC04 | 1 | 1 | 91 | -1 | | | | | 43500 | | | Fail |
| TC05 | 1 | 40 | 1 | 21900 | | | | | 33600 | | | Fail |
| TC06 | 1 | 40 | 45 | 43900 | | | | | 55600 | | | Fail |
| TC07 | 1 | 40 | 0 | -1 | | | | | 33100 | | | Fail |

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| **Test Case ID** | **Input** | | | **Expected Result** | **Actual Result** | **Status (Pass/Fail/No run)** |
|  |  |  |
| TC08 | 1 | 40 | 91 | -1 | 78600 | Fail |
| TC09 | 1 | 0 | 1 | -1 | 0 | Fail |
| TC10 | 1 | 0 | 45 | -1 | 19600 | Fail |
| TC11 | 1 | 0 | 0 | -1 | 0 | Fail |
| TC12 | 1 | 0 | 91 | -1 | 42600 | Fail |
| TC13 | 1 | 81 | 1 | -1 | 70500 | Fail |
| TC14 | 1 | 81 | 45 | -1 | 92500 | Fail |
| TC15 | 1 | 81 | 0 | -1 | 70000 | Fail |
| TC16 | 1 | 81 | 91 | -1 | 115500 | Fail |
| TC17 | 35 | 1 | 1 | 29100 | 18900 | Fail |
| TC18 | 35 | 1 | 45 | 51100 | 40900 | Fail |
| TC19 | 35 | 1 | 0 | -1 | 18400 | Fail |
| TC20 | 35 | 1 | 91 | -1 | 63900 | Fail |
| TC21 | 35 | 40 | 1 | 52500 | 54000 | Fail |

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| **Test Case ID** | **Input** | | | **Expected Result** | **Actual Result** | **Status (Pass/Fail/No run)** |
|  |  |  |
| TC22 | 35 | 40 | 45 | 74500 | 76000 | Fail |
| TC23 | 35 | 40 | 0 | -1 | 53500 | Fail |
| TC24 | 35 | 40 | 91 | -1 | 99000 | Fail |
| TC25 | 35 | 0 | 1 | -1 | 18000 | Fail |
| TC26 | 35 | 0 | 45 | -1 | 40000 | Fail |
| TC27 | 35 | 0 | 0 | -1 | 17500 | Fail |
| TC28 | 35 | 0 | 91 | -1 | 63000 | Fail |
| TC29 | 35 | 81 | 1 | -1 | 90900 | Fail |
| TC30 | 35 | 81 | 45 | -1 | 112900 | Fail |
| TC31 | 35 | 81 | 0 | -1 | 90400 | Fail |
| TC32 | 35 | 81 | 91 | -1 | 135900 | Fail |
| TC33 | 0 | 1 | 1 | -1 | 0 | Fail |
| TC34 | 0 | 1 | 45 | -1 | 19900 | Fail |
| TC35 | 0 | 1 | 0 | -1 | 0 | Fail |
| TC36 | 0 | 1 | 91 | -1 | 42900 | Fail |

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| **Test Case ID** | **Input** | | | **Expected Result** | **Actual Result** | **Status (Pass/Fail/No run)** |
|  |  |  |
| TC37 | 0 | 40 | 1 | -1 | 33000 | Fail |
| TC38 | 0 | 40 | 45 | -1 | 55000 | Fail |
| TC39 | 0 | 40 | 0 | -1 | 32500 | Fail |
| TC40 | 0 | 40 | 91 | -1 | 78000 | Fail |
| TC41 | 0 | 0 | 1 | -1 | 0 | Fail |
| TC42 | 0 | 0 | 45 | -1 | 19000 | Fail |
| TC43 | 0 | 0 | 0 | -1 | 0 | Fail |
| TC44 | 0 | 0 | 91 | -1 | 42000 | Fail |
| TC45 | 0 | 81 | 1 | -1 | 69900 | Fail |
| TC46 | 0 | 81 | 45 | -1 | 91900 | Fail |
| TC47 | 0 | 81 | 0 | -1 | 69400 | Fail |
| TC48 | 0 | 81 | 91 | -1 | 114900 | Fail |
| TC49 | 71 | 1 | 1 | -1 | 40500 | Fail |
| TC50 | 71 | 1 | 45 | -1 | 62500 | Fail |
| TC51 | 71 | 1 | 0 | -1 | 40000 | Fail |
| **Test Case ID** | **Input** | | | **Expected Result** | **Actual Result** | **Status (Pass/Fail/No run)** |
|  |  |  |
| TC52 | 71 | 1 | 91 | -1 | 85500 | Fail |
| TC53 | 71 | 40 | 1 | -1 | 75600 | Fail |
| TC54 | 71 | 40 | 45 | -1 | 97600 | Fail |
| TC55 | 71 | 40 | 0 | -1 | 75100 | Fail |
| TC56 | 71 | 40 | 91 | -1 | 120600 | Fail |
| TC57 | 71 | 0 | 1 | -1 | 39400 | Fail |
| TC58 | 71 | 0 | 45 | -1 | 61600 | Fail |
| TC59 | 71 | 0 | 0 | -1 | 39100 | Fail |
| TC60 | 71 | 0 | 91 | -1 | 84600 | Fail |
| TC61 | 71 | 81 | 1 | -1 | 112500 | Fail |
| TC62 | 71 | 81 | 45 | -1 | 134500 | Fail |
| TC63 | 71 | 81 | 0 | -1 | 112000 | Fail |
| TC64 | 71 | 81 | 91 | -1 | 157500 | Fail |

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| **Scenario ID** | **Scenario Name** | **Test Case#** | **Pass** | **Fail** | **No run** | **Block** | **Remark** | **Defect ID** |
| EC-Lab5-01 | Commission Program | 64 | 1 | 63 | 0 | 0 |  |  |
| **รวม** | | 64 | 1 | 63 | 0 | 0 |  |  |