Computer System Design

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Variant number: 9

1 Screen shots of obtained simulation waveforms:

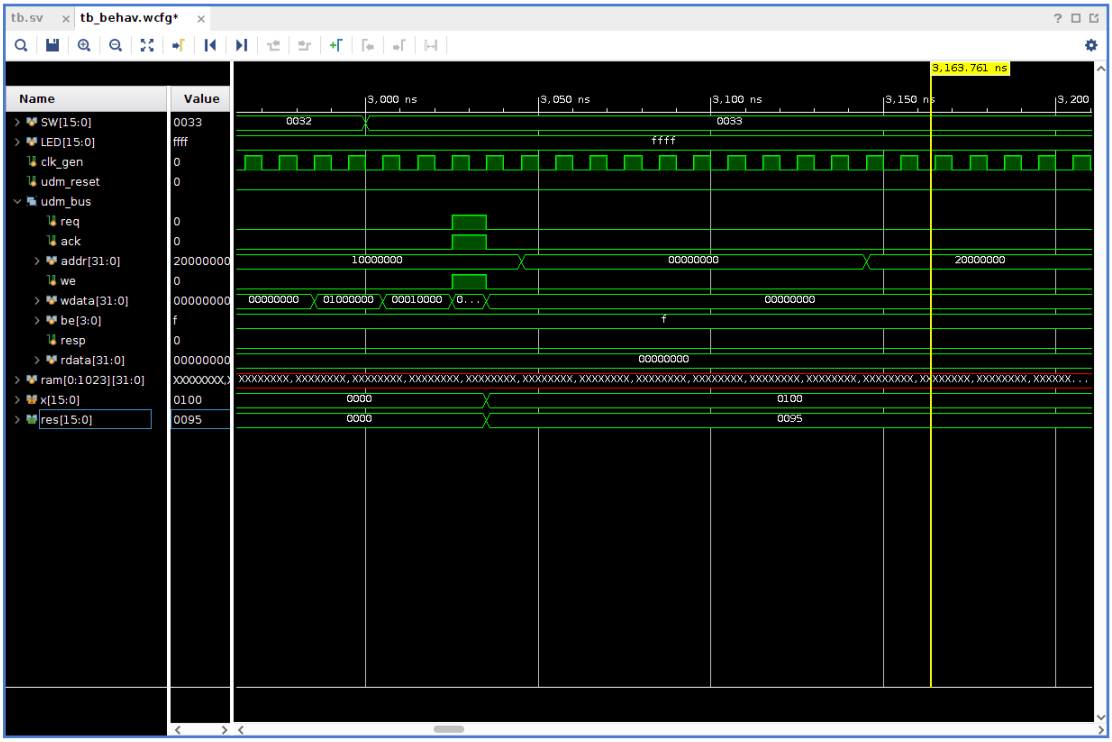

Figure 1: simulation waveform

2 Report on module characteristics:

2.1 Timing:

TNS: -7.235 ms

WNS: -111.038 ns

2.2 Module's performance:

Clock frequency: 10ns(100 MHz clock) + 111ns(WNS) + 7(WNS) = 128ns

Initiation interval: 1 clock cycle for combinational implementation; 128ns.

Bandwidth: 1 op/cycle; 1 / 128ns = 7.8125Mop/second

Latency: 1 clock cycle; 128ns

2.3 HW resources:

LUTs: 888

FFs: 0

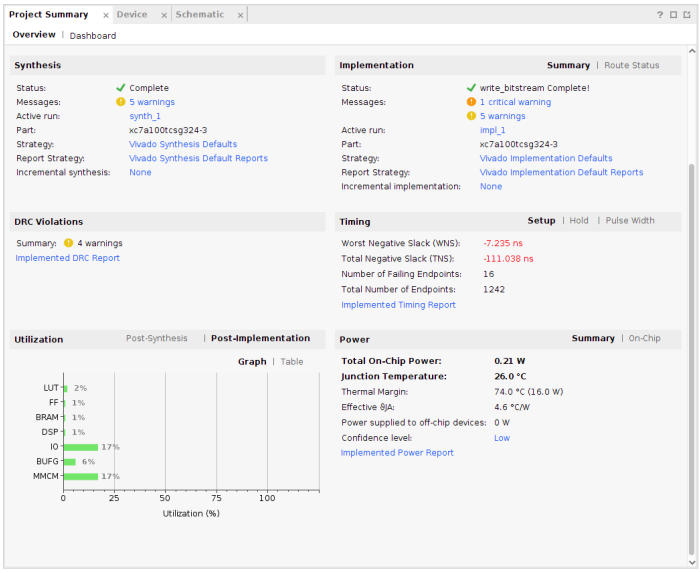

Figure 2: TNS and WNS

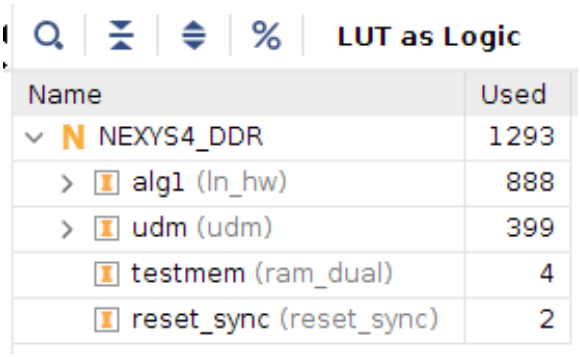

Figure 3: LUTs of the module

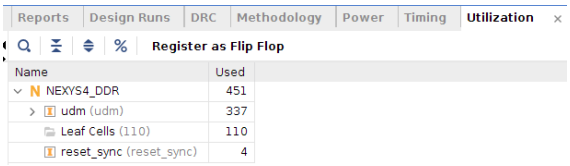

Figure 4: FFs of the module

3 Comments on achieved characteristics:

The design has achieved the task of variant 9 but has failed in timing closure. This is due to the combinational circuit I used to implement the task which results that the entire computation is finished in one clock cycle. The number of flip flop in this module is 0. I think this is because I did not implement any register in my Verilog code. The LUTs are quit many because of the wires I implement in the module are a large amount. I tried to use sequential logic to finish the task but failed at reading output. In the failed case, the output of the result is always XXXXXX. I will try to figure it out and update my implementation.