

Computer System Design

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Variant number: 9

1 Screenshot of obtained simulation waveforms:

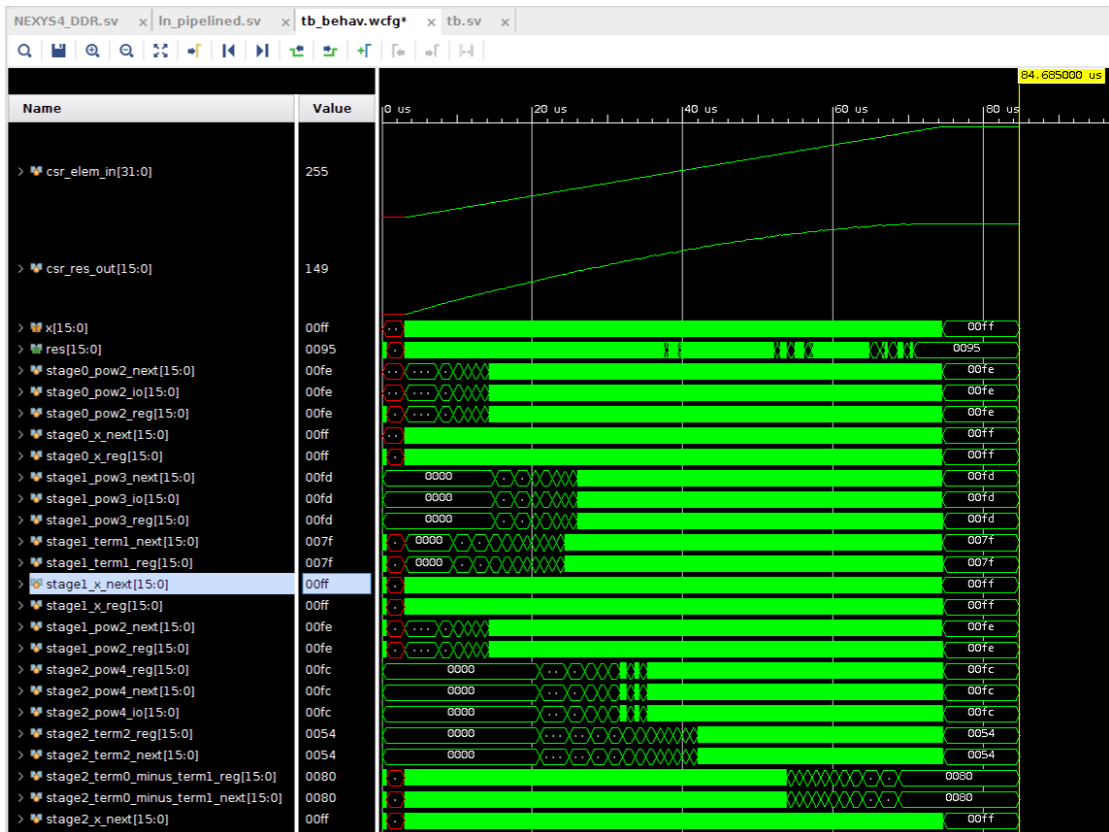


Figure 1: simulation waveform

2 Report on module characteristics:

2.1 Timing:

2.1.1 TNS: 0 ns

2.1.2 WNS: 2.379 ns

2.2 Module's performance:

2.2.1 Clock frequency: 10 ns (100 MHz)

2.2.2 Initiation Interval: 1 clock cycle; 10ns

2.2.3 Throughput: 1 op / cycle; 100Mop / second

2.2.4 Latency: 5 clock cycles; 50ns

2.3 HW resources

2.3.1 LUTs: 832

2.3.2 FFs(registers): 140

2.4 Evaluate top achievable frequency for the designed implementations:

The implementation failed to meet the time constraint when the `sys_clk_pin` is set to 9 ns. So, I think it works only at 10 ns or more than this.

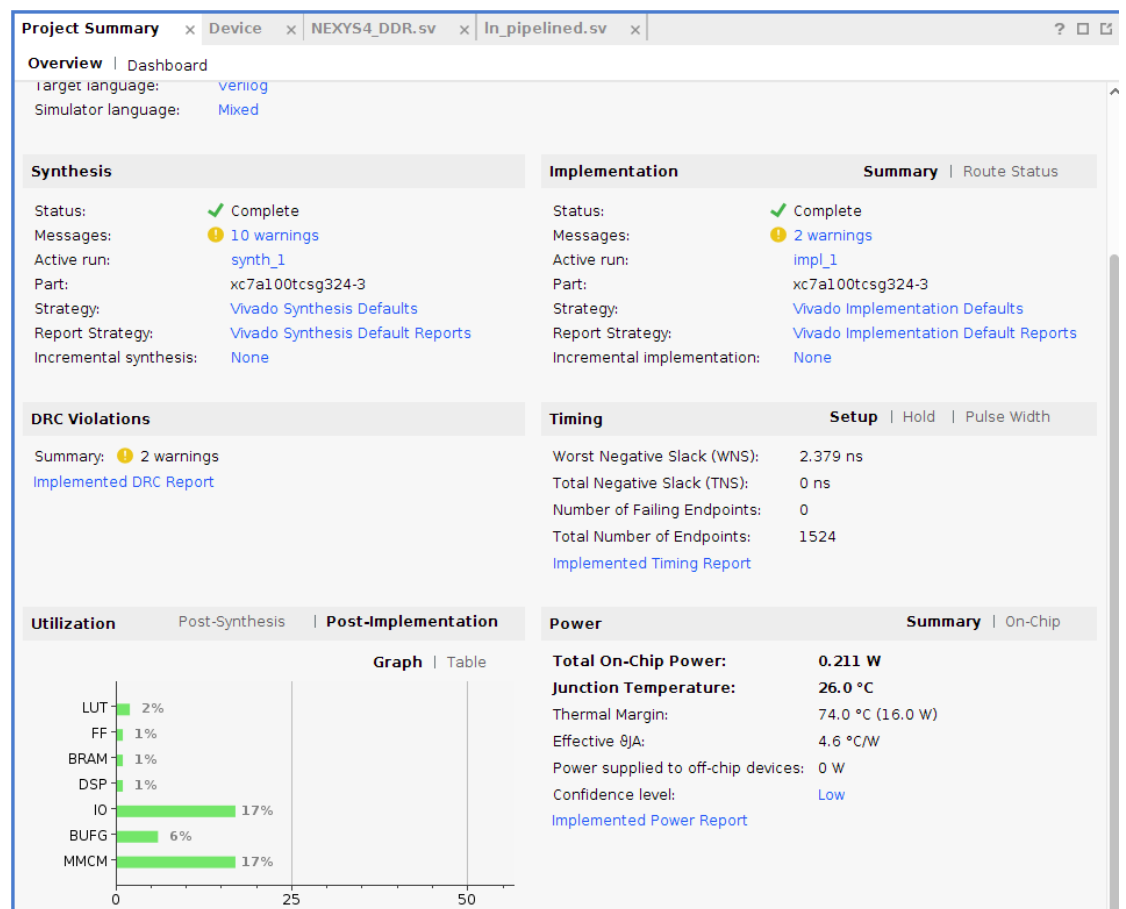


Figure 2: TNS and WNS

Name	Used
▼ N NEXYS4_DDR	591
> I udm (udm)	337
I ln_inst (ln_pipeline)	140
Leaf Cells (110)	110
I reset_sync (reset_sync)	4

Figure 3: FFs of the module

Name	Used
▼ N NEXYS4_DDR	1237
▼ I ln_inst (ln_pipeline)	832
I pow3 (fix16_8mult_0)	287
I pow2 (fix16_8mult)	246
I pow4 (fix16_8mult_1)	240
Leaf Cells (59)	59
> I udm (udm)	399
I testmem (ram_dual)	4
I reset_sync (reset_sync)	2

Figure 4: LUTs of the module

SYNTHESIZED DESIGN - synth_1 | xc7a100tcs324-3

Device: Timing Constraints

▼ Clocks (3)

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Src
1	sys_clk.pin	10.000	0.000	4.500	<input type="checkbox"/>	[get_ports CLK100MHz]	sys_clk.vdc	sys^
3	sys_clk.pin	9.000	0.000	4.500	<input checked="" type="checkbox"/>	[get_ports CLK100MHz]	NEXYS4_DDR.vdc	sys^

All Constraints

Properties

Select an object to see properties

Timing

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): -5.792 ns	Worst Hold Slack (WHS): 0.053 ns	Worst Pulse Width Negative Slack (WPWS): 2.500 ns
Total Negative Slack (TNS): -1985.407 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 1316	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 1461	Total Number of Endpoints: 1461	Total Number of Endpoints: 584

Timing constraints are not met.

Figure 5: implementation failed at 9 ns

3 Comments on achieved characteristics:

The timing closure is successful since the pervious design has been updated to the pipelined one. The whole task of counting Taylor series is divided into 5 stages and each stage can be completed in a single clock cycle. It requires 5 clock cycles to finish the computation. Since these stages can be overlapped, we can pass new computation each cycle and achieve top throughput of 100 Mop / second. However, there remains some questions I haven't figure out yet. On the one hand, I don't know why when clock cycle is set to 9 ns and the design failed the time closure. On the other hand, I can only superficially evaluate the power consumption. I will try to make a good understand of these problems.

The remaining questions from lab1 are solved. Output X means unstable in the Verilog language, and I finish the task using sequential logic.

4 Schedule of designed pipeline

c-step number	operation
0	compute pow2
1	compute pow3, term1
2	compute pow4, term2, term0_minus_term1
3	compute term3, term0_minus_term1_plus_term2
4	compute y

Table 1: Schedule for pipelined implementation

5 Microarchitectural diagram

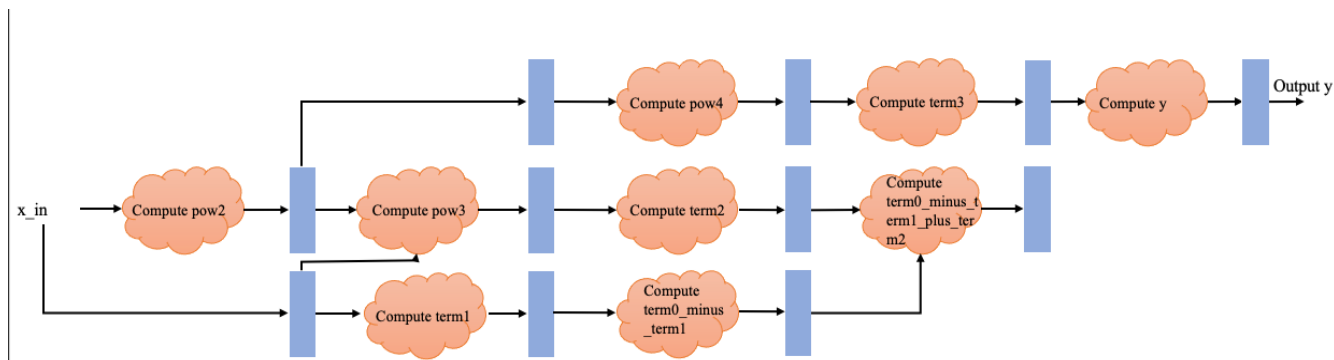


Figure 6: Microarchitectural diagram for fully pipelined implementation

6 Power consumption evaluation

Figure 2 shows the Total On-chip Power consumption is 0.211 W. Figure 7 shows that *NEXYS4_DDR* consumes 0.113 W while the *ln_inst* which I designed consumes 0.001 W

across all utilizations.

Utilization	Name	Clocks (W)	Signals (W)	Data (W)	Clock Enable (W)	Set/Reset (W)	Logic (W)	BRAM (W)	DSP (W)	Clock Manager (W)	MMCM (W)	I/O (W)
0.113 W (54% of total)	NEXYS4_DDR											
> 0.106 W (50% of total)	sys_clk (sys_clk)	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.106	0.106	<0.001
> 0.003 W (2% of total)	udm (udm)	0.002	0.001	0.001	<0.001	<0.001	0.001	<0.001	<0.001	<0.001	<0.001	<0.001
> 0.002 W (1% of total)	testmem (ram_dual)	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.002	<0.001	<0.001	<0.001	<0.001
0.001 W (1% of total)	Leaf Cells (147)											
> 0.001 W (1% of total)	ln_inst (ln_pipelined)	0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
> <0.001 W (<1% of total)	reset_sync (reset_sync)	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001

Figure 7: power consumption of the design