Computer System Design

陈浩东 Chen Haodong

232320029

2023.9.19

Variant number: 9

1. Verify functional correctness in simulation

The function is correct as shown in Figure 1. $LED[31:0]$ in Figure 1 approves the correct output value of ln function, the program works as intended. Now, measure the number of clock cycles needed to execute the program by various CPU configurations, and the results is shown in Table 1. Figure 2 shows the design latency of $riscv\_5stage$, simulation frequency set in the testbench is 140Mhz clock, so 157.124 ns equals to around 22 clock cycles. For my example, the waveform simulation outputs of each $riscv$ stage are put in the appendix.

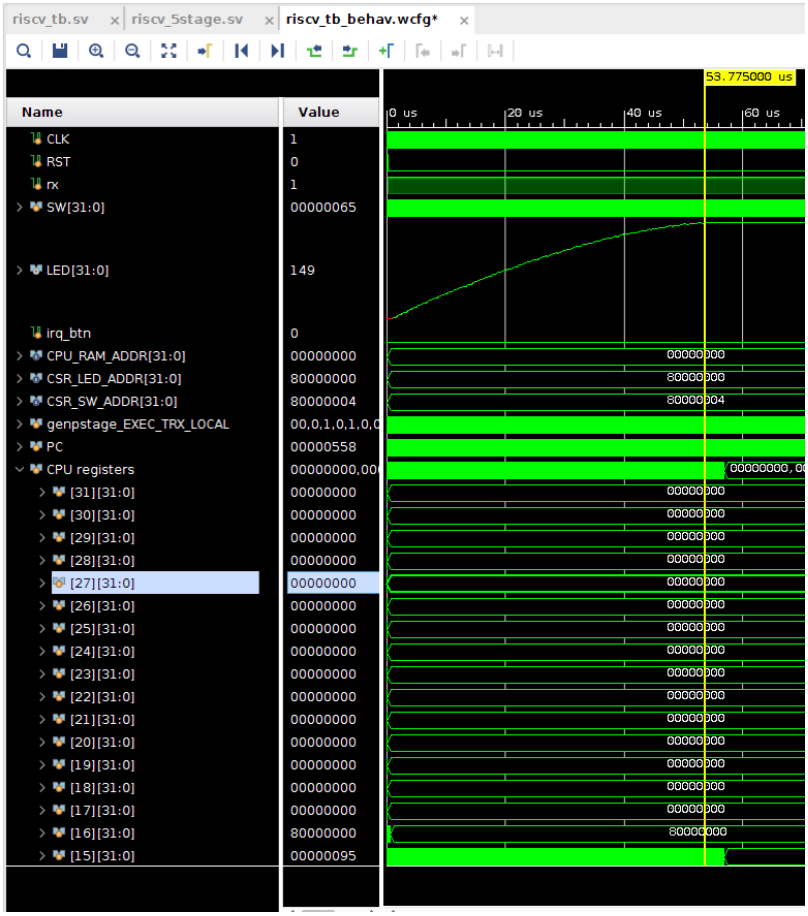

Figure 1: simulation waveform

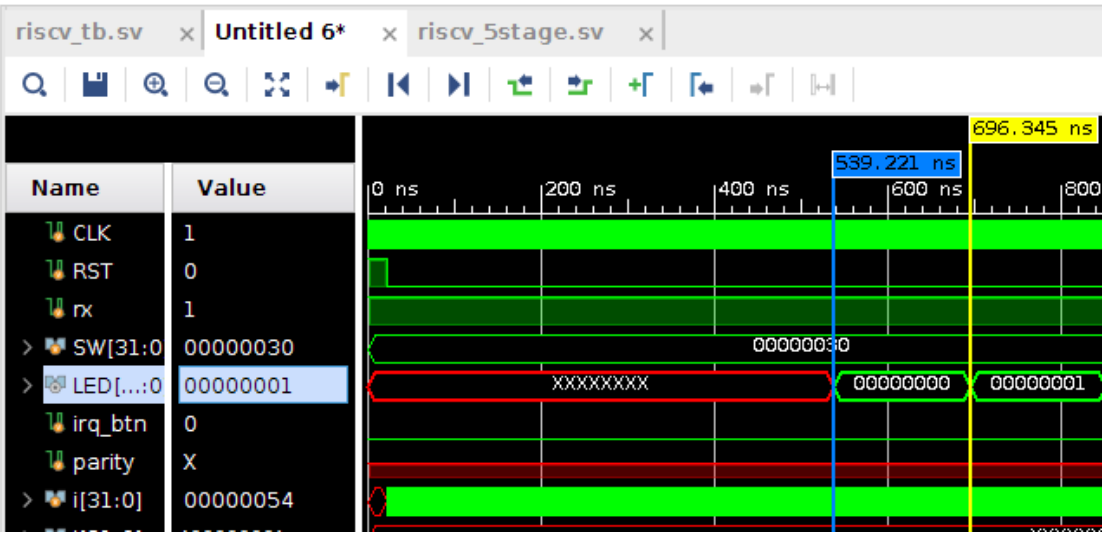

Figure 2: design latency of riscv_5stage

CPU configuration	Latency, clock cycles
riscv_1stage	42
riscv_2stage	24
riscv_3stage	33
riscv_4stage	24
riscv_5stage	22
riscv_6stage	23

Table 1: Performance (in clock cycles) of software implementations based on various CPU configurations

2. Implement the design and collect metrics of the implementation

Characteristics of provided *sigma_tile* configurations are shown in Table 2. The program outputs of each element in Table 2 are shown in the appendix.

CPU configuration	Frequency, MHz	LUTs	FFs
riscv_1stage	70	2835	1665
riscv_2stage	70	3193	1766
riscv_3stage	80	3200	1920
riscv_4stage	140	3565	2198
riscv_5stage	140	3739	2273

riscv_6stage	150	3937	2406

Table 2: Characteristics of provided *sigma_tile* implementations

3. Analyze performance of implementations

The absolute performance values of target functionality implementations based on various CPU configurations is shown in table 3.

CPU configuration	Latency, ns
riscv_1stage	600
riscv_2stage	343
riscv_3stage	413
riscv_4stage	171
riscv_5stage	157
riscv_6stage	153

Table 3: Absolute performance of target functionality implementations based on various CPU configurations

4. Appendix:

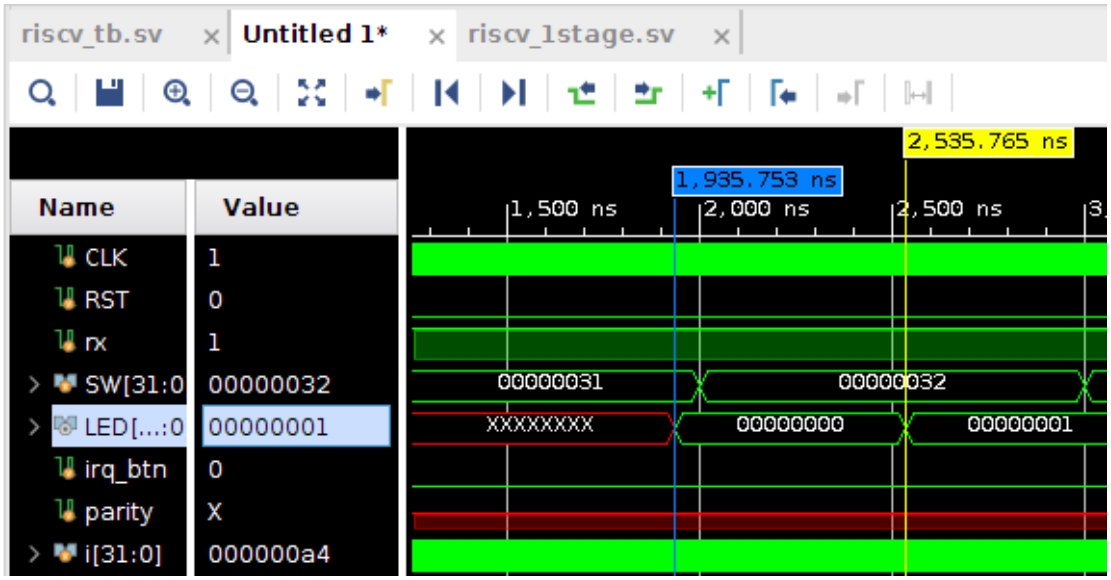

Figure 3: design latency of riscv_1stage

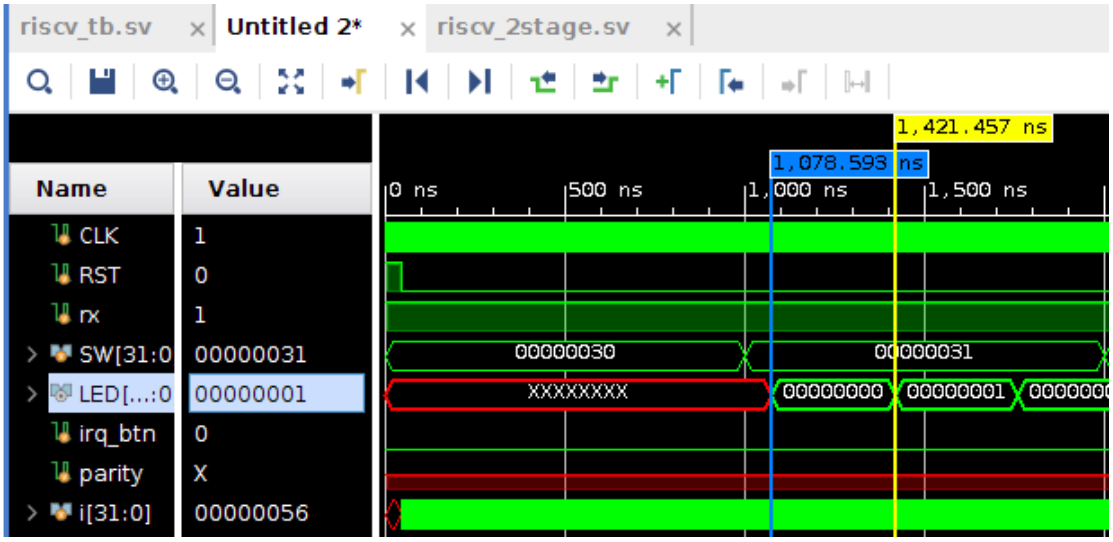

Figure 4: design latency of riscv_2stage

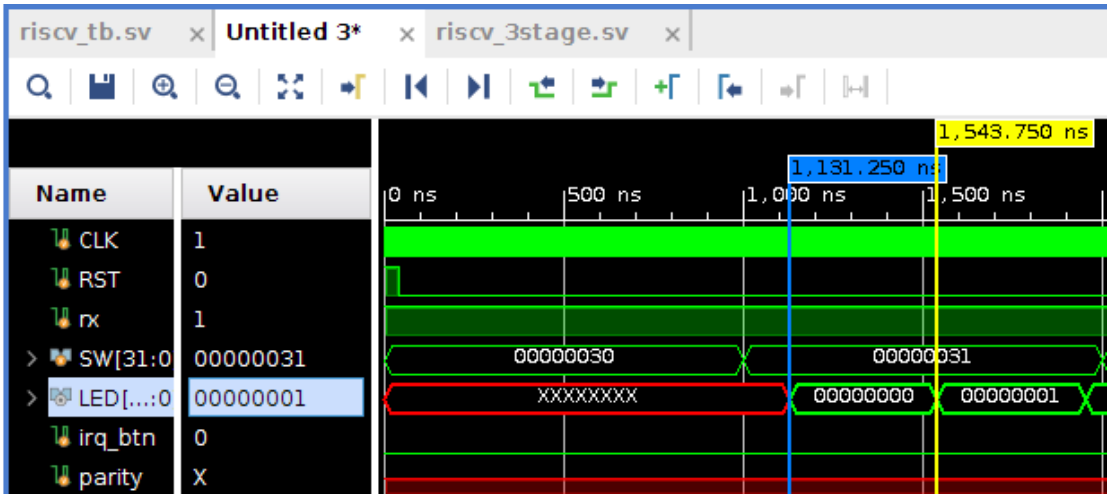

Figure 5: design latency of riscv_3stage

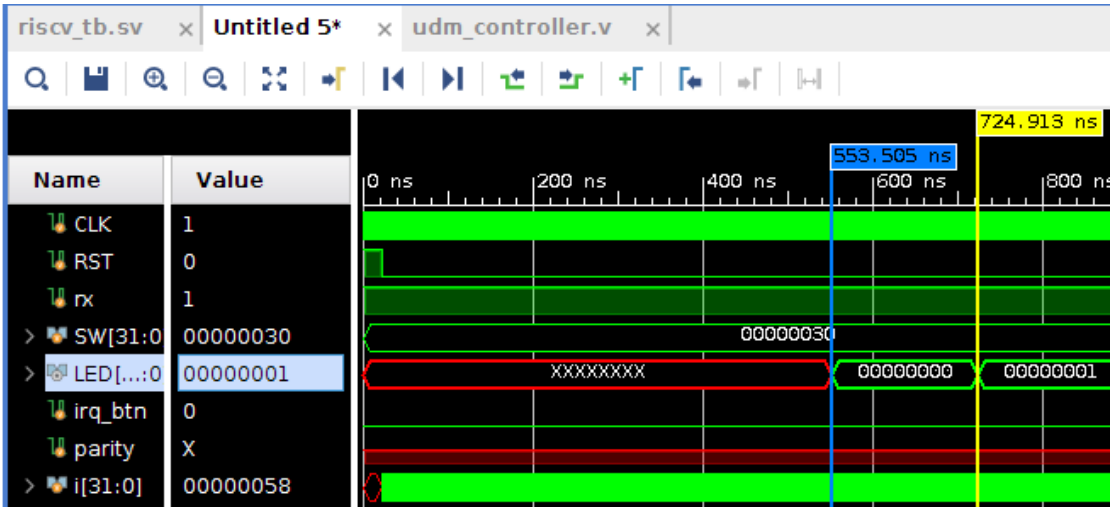

Figure 6: design latency of riscv_4stage

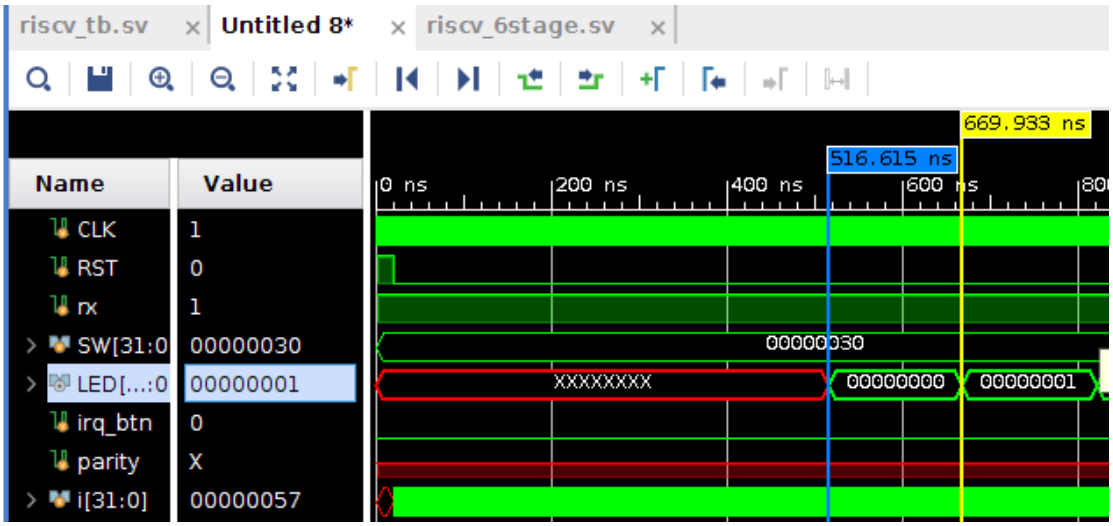

Figure 7: design latency of riscv_6stage

Name	Slice LUTs (63400)	Slice Registers (126800)
NEXYS4_DDR	3289	2111
sigma (sigma)	3288	2111
debouncer (debounce	28	23
reset_sync (reset_syn	2	4
sigma_tile (sigma_tile)	2835	1665
arb_cpu (arb_2m3s	101	6
genexu_MUL_DIV (g	334	231
irq_adapter (irq_ad	31	24
ram (ram_dual_mer	109	53
riscv (riscv_1stage)	2214	1227
sfr (sfr)	44	124
udm (udm)	423	338
sys_clk (sys_clk)	0	0

Figure 8: LUTs and FFs of *riscv_1stage sigma_tile*

Name	Slice LUTs (63400)	Slice Registers (126800)
NEXYS4_DDR	3636	2212
sigma (sigma)	3635	2212
debouncer (debounce	28	23
reset_sync (reset_syn	2	4
sigma_tile (sigma_tile)	3193	1766
arb_cpu (arb_2m3s	6	6
genexu_MUL_DIV (g	353	231
irq_adapter (irq_ad	30	24
ram (ram_dual_mer	110	53
riscv (riscv_2stage)	2555	1328
sfr (sfr)	137	124
udm (udm)	412	338
sys_clk (sys_clk)	0	0

Figure 9: LUTs and FFs of *riscv_2stage sigma_tile*

Hierarchy

Name	Slice LUTs (63400)	Slice Registers (126800)
NEXYS4_DDR	3603	2366
sigma (sigma)	3602	2366
debouncer (debounce	28	23
reset_sync (reset_sync	2	4
sigma_tile (sigma_tile)	3200	1920
arb_cpu (arb_2m3s)	5	6
genexu_MUL_DIV (ge	339	231
irq_adapter (irq_ada	30	24
ram (ram_dual_mem	126	53
riscv (riscv_3stage)	2588	1482
sfr (sfr)	110	124
udm (udm)	372	338
sys_clk (sys_clk)	0	0

Figure 10: LUTs and FFs of *riscv_3stage sigma_tile*

Name	Slice LUTs (63400)	Slice Registers (126800)
NEXYS4_DDR	3966	2644
sigma (sigma)	3965	2644
debouncer (debounce	28	23
reset_sync (reset_syn	2	4
sigma_tile (sigma_tile	3565	2198
arb_cpu (arb_2m3s	4	6
genexu_MUL_DIV (g	413	231
irq_adapter (irq_ad	26	24
ram (ram_dual_mer	126	53
riscv (riscv_4stage)	2882	1760
sfr (sfr)	112	124
udm (udm)	370	338
sys_clk (sys_clk)	0	0

Figure 11: LUTs and FFs of *riscv_4stage sigma_tile*

Hierarchy

Name	Slice LUTs (63400)	Slice Registers (126800)
NEXYS4_DDR	4144	2719
sigma (sigma)	4143	2719
debouncer (debounce	28	23
sigma (sigma)	2	4
sigma_tile (sigma_tile)	3739	2273
arb_cpu (arb_2m3s)	21	6
genexu_MUL_DIV (ge	357	231
irq_adapter (irq_ada	28	24
ram (ram_dual_mem	150	53
riscv (riscv_5stage)	3086	1835
sfr (sfr)	95	124
udm (udm)	374	338
sys_clk (sys_clk)	0	0

Figure 12: LUTs and FFs of *riscv_5stage sigma_tile*

Name	Slice LUTs (63400)	Slice Registers (126800)
NEXYS4_DDR	4338	2852
sigma (sigma)	4337	2852
debouncer (debounce	28	23
reset_sync (reset_syn	2	4
sigma_tile (sigma_tile)	3937	2406
arb_cpu (arb_2m3s	33	6
genexu_MUL_DIV (g	285	231
irq_adapter (irq_ada	30	24
ram (ram_dual_mem	158	53
riscv (riscv_6stage)	3330	1968
sfr (sfr)	99	124
udm (udm)	370	338
sys_clk (sys_clk)	0	0

Figure 13: LUTs and FFs of *riscv_6stage sigma_tile*