九齊科技股份有限公司
Nyquest Technology Co., Ltd.

DATA SHEET

NX12F / NX13F (EF Series)

32-bit Audio SoC for SBC / MIDI Playback & Voice Changer / Recording / Recognition

Version 1.3

May 30, 2022

Revision History

Version	*Date*	*Description*	*Modified Page*
1.0	2021/9/30	Initial release.	-
1.1	2021/11/29	1. Replace SSOP-24 by SSOP-28. 2. Replace PA1 by PA2 for SOP-16 packages.	5, 6, 8, 10, 11, 13, 15, 16, 17, 35, 36, 38
1.2	2021/12/24	1. Revise I_{HALT} with typical and maximum values. 2. Revise DC/AC characteristics.	6, 11, 26 26, 27
1.3	2022/5/30	1. Revise I_{HALT} / I_{SB} values. 2. Correct SPI0_VDD capacitance to 1uF. 3. Revise ALT# for programming pins. 4. Modify AGC gain control. 5. Add application circuit for Port C as GPIO.	6, 11, 26 15 16, 17 24 32

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1. 概述

NX12Fx5xA / NX13Fx5xA 是基於 32 位元 MCU 的高品質 Speech/MIDI 系統單晶片處理器，特別設計用來處理數位語音相關的功能。NX12Fx5xA / NX13Fx5xA 源自 NX1 OTP 系列, 其在 Speech/MIDI 播放、錄變音、以及離線式語音識別等各方面的應用，早已廣為業界所採用。NX12Fx5xA / NX13Fx5xA 為新一代的 EF (Embedded Flash，嵌入式快閃記憶體) 系列，用來彌補一次性燒錄 OTP 之不足，並且將 ICE 偵錯功能直接集成在量產晶片之中，使得開發流程更加地簡化、順暢。相較於掩膜 (Mask ROM) 產品而言，NX12Fx5xA / NX13Fx5xA 則具有絕佳的 MOQ 和交期的優勢。

NX12Fx5xA / NX13Fx5xA 採用記憶體映射架構，最高可以定址到 16MB，包含記憶體 (EF/RAM)、週邊、以及 SPI Flash 的儲存空間 (支援 Bank 擴充以及指令/資料模式)。由於 DSP 演算法以及硬體規格的提升，NX12Fx5xA / NX13Fx5xA 支援 SBC (Sub-Band Coding, 子帶編碼)，相較於傳統式的 ADPCM 演算法，除了更高的壓縮率之外，在音質上也大幅超越傳統的語音水準！CPU 內建 ILM/DLM 本地匯流排，當在 48MHz 最高系統頻率時，可以達到 50+ DMIPS 的優異表現。NX12Fx5xA / NX13Fx5xA 內建單一週期乘法器及七週期除法器，再加上 32 位元 MCU 的高性能運算，可以用來實現豐富的 16 和絃 MIDI。所有的資料，包括 SBC / MIDI 檔案、音色波表 (Wavetable)、XIP 本地執行程式、以及一般使用者的資料，除了內建的 EF 之外，也都可以存放到 SPI Flash。

內建 48MHz 高頻以及 32KHz 低頻的雙時脈設計，可讓使用者在 Normal / Standby / Halt 模式之間切換以求取最佳的功耗/效能比、抑或在低耗能情況下，作為計時之用途。NX12Fx5xA / NX13Fx5xA 系列包含單晶片以及將 SPI Flash 合封的封裝產品，除了內建 2Mb 的 EF（嵌入式快閃記憶體）之外，也可以藉由合封或外接的 SPI Flash 來擴充記憶體大小。

NX12Fx5xA / NX13Fx5xA 涵蓋了大量實用的功能：4 組 16 位元的計時器 (Timer)；最多 8 通道硬體 PWM-IO 輸出；8 通道、12 位元的 SAR 類比數位轉換器 (ADC)，可以支援具備前置放大器、AGC/PGA 的差動式 MIC 輸入，以及各式類比感測元件輸入；14 位元的數位類比轉換器 (DAC) 外接功放，或者選擇內建的 Σ-Δ PWM 來直接驅動喇叭；每根 I/O 管腳獨立控制、可作為多功能用途的 GPIO；支援 38KHz/57KHz/125KHz/500KHz 載波傳輸的紅外發射 (IR TX) 或 QFID 應用；SPI0 用來控制外部的 SPI Flash，可選擇內建的 3.3V LDO 來供電，並支援 Single/Dual/Quad I/O 模式以及 XIP (e**X**ecute **I**n **P**lace，在地執行程式) 功能；SPI1 則可外接 2.4GHz RF 或其他 SPI 從元件；I2C 硬體介面；UART可作為 ISP（在系統燒錄）的來源，串列傳輸的介面,或者用來連接超級終端作為簡易的除錯工具；NFC tag 則可當作 ISP的來源並與手機、平板交換資料。

NX12Fx5xA / NX13Fx5xA 系列除了可用 C 語言在 *NYIDE* 環境下開發，提供客戶更多的控制度來滿足較複雜的產品開發以外，更將高階的 *Q-Code* 語言移植到 32 位元 MCU，不僅提供簡單易用和高生產力的開發環境，更把握了產品構想及時實現的重要性。NX12Fx5xA / NX13Fx5xA 內建仿真線路，可以在實際量產的晶片進行程式除錯，以完成原型的演示，並進而直接量產。在大量生產的時候，可以使用 ICP (In-Circuit Programming，在線燒錄) 的功能，方便客戶先組裝 PCBA 再進行燒錄 EF 以及量產板上的 SPI Flash。 另外，透過 ISP 的功能，客戶則可以在成品上做到程式以及內容的更新。

NX12Fx5xA / NX13Fx5xA 系列提供多種封裝型式來滿足各式多樣化的應用：Dice、SOP-16、SSOP-28、LQFP-32 以及合封 SPI Flash 的小型 SOP-16 / SSOP-28 多晶片封裝 (MCP, Multi-Chip Package)。

2. 功能

- 寬廣的工作電壓： 2.0V ~ 5.5V
  - SPI Flash 由內建 LDO 3.3V 供電。
  - CPU 最高速度 48MHz 運行時，最低工作電壓為 2.0V。
- 32 位元 CPU 內核
  - Andes N705-S，性能相當於 ARM Cortex-M0+。
  - 最高 CPU 頻率：48MHz，搭配 1 個等待狀態 (wait-state) 的高速 24MHz EF 存取，可達 50+ DMIPS。
  - 單一指令週期快速乘法器，七指令週期快速除法器。
  - 本地指令/資料記憶體匯流排。
- 共 6 個母體，包括單芯片以及合封 SPI Flash 的 MCP（多芯片封裝）。

P/N	VDD	RAM	EF	SPI Flash	Duration (Sec) 8Kbps	Duration (Sec) 16Kbps	I/O	SPI 0	SPI 1	I²C	UART	16-bit Timer	PWM-IO	12-bit SAR ADC	MIC	Dual Clock	DAC	Power Amp.	VR	Package
NX12FS51A	2.0V ~ 5.5V	10KB	2Mb	-	197	98	25 10 22 25	v - v v	v v v v	v - v v	v	4	8 3 8 8	8 1 6 8	v	v	14-bit	Σ-Δ PWM	v	Dice SOP-16 SSOP-28 LQFP-32
NX12FM52A	2.0V ~ 5.5V	10KB	2Mb	4Mb	721	360	10 21	- -	v v	- v	v	4	4	1 8	v	v	14-bit	Σ-Δ PWM	v	SOP-16 SSOP-28
NX12FM54A	2.0V ~ 5.5V	10KB	2Mb	16Mb	2,294	1,147	10 21	- -	v v	- v	v	4	4	1 8	v	v	14-bit	Σ-Δ PWM	v	SOP-16 SSOP-28
NX13FS51A	2.0V ~ 5.5V	10KB	2Mb	-	197	98	25 10 22 25	v - v v	v v v v	v - v v	v	4	8 3 8 8	8 1 6 8	v	v	14-bit	Σ-Δ PWM	-	Dice SOP-16 SSOP-28 LQFP-32
NX13FM52A	2.0V ~ 5.5V	10KB	2Mb	4Mb	721	360	10 21	- -	v v	- v	v	4	4	1 8	v	v	14-bit	Σ-Δ PWM	-	SOP-16 SSOP-28
NX13FM54A	2.0V ~ 5.5V	10KB	2Mb	16Mb	2,294	1,147	10 21	- -	v v	- v	v	4	4	1 8	v	v	14-bit	Σ Λ PWM	-	SOP-16 SSOP-28

Table 1 NX12Fx5xA / NX13Fx5xA 選型表

- 雙時脈操作，內建 I_HRC (48MHz) 和 I_LRC (32,768Hz) 振盪器。 (出廠精準度調校：I_HRC @ +/-0.5%, I_LRC @ +/-1.5%)
- 三種工作模式可隨系統需求調整電流消耗：正常 (Normal) / 待機 (Standby) / 睡眠 (Halt)，在睡眠模式下，典型耗電流 @ 4.5uA。
- 內建 8 階低電壓檢測器 (LVD)：3.6V, 3.4V, 3.2V, 3.0V, 2.8V, 2.4V, 2.2V, 2.0V，出廠調校至 +/-3% 精準度。
- 內建低壓復位功能 (LVR)。
- 四組具備各式時鐘源的 16 位下數計時器 (Timer0 / Timer1 / Timer2 / Timer3)。
- 內建 14 位元 DAC (數位類比轉換器)，可以外接功放。
- 內建 13 位元 Σ-Δ PWM 功放, 可以直接驅動喇叭。
- 最多 25 根 I/O 管腳，除了上拉電阻大小以 byte 為單位選擇以外，每根管腳之組態皆可由暫存器個別位元控制，並可經由暫存器設定多功能用途。
- SPI0 主模式，內建 3.3V LDO 以連接 SPI Flash
  - 高達 24MHz 時脈。
  - 支援 32 位元模式，可定址超過 128Mb。

- 支援數據模式以及 XIP 模式 (在地執行程式)。
- 支援 x1 / x2 / x4 I/O 模式 (Single / Dual / Quad)。

- SPI1 主模式，與 SPI0 共用 3.3V LDO
  - 高達 24MHz 時脈。
- 支援 IR TX (可選任一 Timer, 0 ~ 3)
- 支援實時時鐘 (RTC)：可選 16.384KHz / 1.024KHz / 64Hz / 2Hz 中斷。
- 支援看門狗 (WDT) 計時：可選 188ms / 750ms 重置。
- 支持 NFC Tag
  - 相容 ISO-14443A 之 NFC 操作，可以在供電情況下和手機/平板作雙向通訊
- 支持 ISP (In-System Programming，在系統燒錄)
  - 來源: UART，NFC Tag
  - 目的地: EF, SPI Flash（經由程式控制）
  - ISP boot 程式保護機制
- 支援硬體 UART
  - 全雙工 TX/RX，具 4-level FIFO
  - 傳輸率（Baud Rate）支持 115,200 / 230,400 / 1M bps
- 支援硬體 I2C
  - 主/從模式
  - 100KHz / 400KHz / 1MHz 時鐘
  - 4-byte FIFO
- 兩組 PWM-IO 產生器 (PWMA / PWMB)
  - 每組最多 4 個獨立的 PWM-IO 通道 (PWMA0 ~ PWMA3 / PWMB0 ~ PWMB3)。
  - 每組 PWM-IO 產生器擁有一個具備各式時鐘源的 16 位元計時器 (可獨立當作一般計時器使用) 。
  - 每根 PWM-IO 管腳具有獨立的 16 位元脈寬暫存器。
- 支援電容式觸摸感測（CapTouch Sensor）
  - 所有的 PA 腳位皆可選擇作為觸摸鍵
- ADC (類比數位轉換器)
  - 八通道 (具自動切換通道功能)，12 位元 SAR ADC。
  - 可由計時器下溢 (Timer0 / 1 / 2) 或軟件觸發。
  - Ch0 具有 4-level FIFO，與 MIC 輸入共用。
  - 配備 Analog LDO 獨立供電：可選 3.3V @ 3-Battery，或 2.3V @ 2-Battery。
- 內建 MIC 控制線路
  - 差動輸入，2 級前置放大器，可選自動或程式增益控制 (AGC / PGA)。

- 支援 EF 安全保護機制。
- 簡單易用的開發環境
  - 高階的 *Q-Code* 程式。
  - 進階的 *NYIDE* C-Module 程式。
  - 內建兩根管腳的 OCD（On-Chip Debugger）仿真線路，支援 Q-Code / C-Module 源代碼仿真。
  - 多用途 NX_Programmer 作為仿真以及 EF/SPI Flash 之燒錄。
  - Smart Writer 作為封裝片量產之 EF/SPI Flash 代燒，或者 ICP（在線燒錄）之用途。
  - 6 根管腳的燒錄介面 (VDD, VSS, PD1/ICE_DAT, PD0/ICE_CLK, PA12, RSTB/PA8)。
- 基於軟件的 Speech/MIDI 編解碼器，語音識別，以及各式演算法
  - ADPCM 編解碼：4通道，每採樣點 4位元 / 5位元。
  - SBC 編解碼：2通道，4.5K ～ 32Kbps（位元速率），最高頻寬 16KHz。
  - MIDI 解碼：最多16通道 (32KHz 輸出採樣率)。
  - 聲音特效：變速不變調、變調不變速、機器人聲音、回音、實時變聲等等。
  - 語音識別：基於音素的離線式語音識別應用（僅限 NX12Fx5xA）
- 支援 16 倍頻超採樣濾波器。
- 出貨形態
  - 裸片 (Dice)。
  - 封裝片
    - 單晶片：SOP-16 / SSOP-28 / LQFP-32。
    - 多晶片 (與 4Mb / 16Mb SPI Flash 合封)：SOP-16 / SSOP-28。

1. GENERAL DESCRIPTION

The NX12Fx5xA / NX13Fx5xA is a 32-bit MCU based high-quality speech/MIDI SoC, which is specially designed for various audio-related DSP applications. Its predecessor, the NX1 OTP series, has been well accepted in the market for numerous applications like long-duration speech/MIDI synthesis, voice changer, and stand-alone voice recognition. The NX1 Embedded Flash (EF) series follows the same architecture but uses EF to replace the OTP memory core and embeds OCD (On-Chip Debugger) at production chips to make the project development much easier than ever. As compared with mask ROM counterparts, the NX12Fx5xA / NX13Fx5xA got absolute advantage over MOQ and lead time.

The NX12Fx5xA / NX13Fx5xA got memory-mapped architecture, which can address up to 16MB space that includes memory (EF / RAM), register files, peripheral and SPI Flash (that supports Bank for expansion and Instruction / Data modes). The highly compressed SBC (Sub-Band Coding) is achieved with greatly enhanced quality & much less memory size compared against traditional ADPCM coding due to the incorporation of efficient DSP algorithms as well as the upgrade of H/W spec. By incorporating Instruction / Data local buses, 1-cycle multiplier and 7-cycle divider for the 32-bit N705-S core, it reaches outstanding performance of 50+ DMIPS when the system clock runs at 48MHz. The S/W-based MIDI synthesizer can reach more than 16-ch polyphonic channels, with all data including SBC / MIDI files, wavetable timbres, XIP (eXecutable In Place) program code and general user data stored in the embedded Flash and/or external SPI Flash memory.

The dual clock design with built-in 48MHz I_HRC and 32KHz I_LRC gives users the freedom to switch among Normal / Standby / Halt modes for the balance of power consumption and performance or to keep the time under low power condition. The NX12Fx5xA / NX13Fx5xA series got single-chip packages as well as MCP (Multi-Chip Package) that integrates SPI Flash inside the low-pin count packages. Set aside the 2Mb EF inside the NX12Fx5xA / NX13Fx5xA, users can select different SPI Flash density of the pin-compatible MCP bodies or using external SPI Flash to expand the memory easily.

There are various useful features inside the NX12Fx5xA / NX13Fx5xA: Four sets of 16-bit Timers; up to 8-ch H/W PWM-IO pins; 8-channel, 12-bit SAR ADC that supports differential MIC input with 2-stage of pre-amplifiers & AGC / PGA, and various kinds of sensors; 14-bit DAC to connect with external power amplifier or built-in Σ-Δ PWM amplifier to drive speaker directly; independently configurable GPIO per pin with alternate functions; IR TX that supports 38KHz / 57KHz / 125KHz / 500KHz carrier for Infrared or QFID applications; SPI0 with embedded LDO to connect to external SPI Flash; SPI1 for connecting with 2.4GHz RF module or other SPI devices; I2C H/W interface; UART for ISP (In System Programming), serial communication, or debugging via Hyper-Terminal; NFC tag for ISP or data exchange with iDevices.

The NX12Fx5xA / NX13Fx5xA supports C language programming that provides customers with more controllability over complicated projects. Besides, it also brings Q-Code (High-level script programming) to 32-bit MCU that provides customers with an easy-to-use, highly productive development environment for quick realization of product concepts. The NX12Fx5xA / NX13Fx5xA is embedded with On-Chip Debugger, which can provide ICE functionality on the actual production chip. Moreover, it allows for ICP (In-Circuit

Programming) to change code / content right on the target board and ISP (In-System Programming) that makes possible on-board re-programming and code/content updates in the system.

Various package forms are available for the NX12Fx5xA / NX13Fx5xA: Dice, SOP-16, SSOP-28, LQFP-32, and MCP with SPI Flash to fit in diversified application needs.

2. FEATURES

- Wide Operating Voltage: 2.0V ~ 5.5V
  - SPI Flash is powered by embedded 3.3V LDO.
  - Min. operating voltage is 2.0V for max. CPU clock @ 48MHz.
- 32-bit CPU core
  - Andes N705-S, like ARM Cortex-M0+.
  - Max. CPU clock @ 48MHz, up to 50+ DMIPS w/ 1 wait-state @ EF access.
  - 1-cycle fast multiplier, 7-cycle fast divider.
  - Instruction Local Memory & Data Local Memory employed.
- There are six Single-Die and MCP (Multi-Chip Package) parts for the NX12Fx5xA / NX13Fx5xA.

P/N	VDD	RAM	EF	SPI Flash	Duration (Sec) 8Kbps	Duration (Sec) 16Kbps	I/O	SPI 0	SPI 1	I²C	UART	16-bit Timer	PWM-IO	12-bit SAR ADC	MIC	Dual Clock	DAC	Power Amp.	VR	Package
NX12FS51A	2.0V ~ 5.5V	10KB	2Mb	-	197	98	25 10 22 25	v - v v	v v v v	v - v v	v	4	8 3 8 8	8 1 6 8	v	v	14-bit	Σ-Δ PWM	v	Dice SOP-16 SSOP-28 LQFP-32
NX12FM52A	2.0V ~ 5.5V	10KB	2Mb	4Mb	721	360	10 21	- -	v v	- v	v	4	4	1 8	v	v	14-bit	Σ-Δ PWM	v	SOP-16 SSOP-28
NX12FM54A	2.0V ~ 5.5V	10KB	2Mb	16Mb	2,294	1,147	10 21	- -	v v	- v	v	4	4	1 8	v	v	14-bit	Σ-Δ PWM	v	SOP-16 SSOP-28
NX13FS51A	2.0V ~ 5.5V	10KB	2Mb	-	197	98	25 10 22 25	v - v v	v v v v	v - v v	v	4	8 3 8 8	8 1 6 8	v	v	14-bit	Σ-Δ PWM	-	Dice SOP-16 SSOP-28 LQFP-32
NX13FM52A	2.0V ~ 5.5V	10KB	2Mb	4Mb	721	360	10 21	- -	v v	- v	v	4	4	1 8	v	v	14-bit	Σ-Δ PWM	-	SOP-16 SSOP-28
NX13FM54A	2.0V ~ 5.5V	10KB	2Mb	16Mb	2,294	1,147	10 21	- -	v v	- v	v	4	4	1 8	v	v	14-bit	Σ Λ PWM	-	SOP-16 SSOP-28

Table 1 Product Line-Up of NX12Fx5xA / NX13Fx5xA

- Built-in oscillators for I_HRC (48MHz) and I_LRC (32,768Hz), accuracy trimmed to +/-0.5% for I_HRC and +/-1.5% for I_LRC.
- Power management to support 3 operating modes per system requirement: Normal / Standby / Halt modes. At Halt mode, the typical current consumption is 4.5uA.
- 8-level LVD (Low Voltage Detection): 3.6V, 3.4V, 3.2V, 3.0V, 2.8V, 2.4V, 2.2V, 2.0V. Trimmed @ 3.3V to +/-3% accuracy.
- Built-in LVR (Low Voltage Reset) function.
- Four Timers (Timer0 / Timer1 / Timer2 / Timer3), each Timer consists of a 16-bit down-counter with various clock sources.
- Built-in 14-bit resolution DAC output for driving speaker via external power amplifier
- Built-in 13-bit Σ-Δ PWM power amplifier to drive speaker directly
- Up to 25 pins of GPIO
  - Bit configurable for every I/O pin by register control, except byte-defined strength of pull-up resistors
  - Multi-function pins via register control

- SPI Flash interface supported @ SPI0 with embedded 3.3V LDO
  - Master mode
  - Up to 24MHz clock speed
  - 32-bit mode supported to address beyond 128Mb
  - Support Data mode and XIP mode (eXecute In Place)
  - Support Single / Dual / Quad I/O modes of SPI Flash
- SPI master @ SPI1 supported with embedded 3.3V LDO shared with SPI0
  - Up to 24MHz clock speed
- IR TX supported (via any Timer, 0 ~ 3)
- RTC with optional 16.384KHz / 1.024KHz / 64Hz / 2Hz interrupts
- WDT (Watch-Dog Timer) supported with optional 188ms / 750ms reset periods
- NFC Tag supported
  - ISO-14443A compliant NFC operation while powered to communicate in both directions with iDevices
- ISP (In-System Programming) supported
  - Source: UART, NFC Tag
  - Destination: EF, SPI Flash (via program control)
  - ISP boot code protected from accidental erasure
- UART H/W supported
  - Full-duplex TX/RX with 4-level FIFO
  - Baud rates @ 115,200 / 230,400 / 1M bps
- I2C H/W supported
  - Master / Slave mode
  - 100KHz / 400KHz / 1MHz Clock
  - 4-byte FIFO
- Up to two PWM-IO Generators
  - Each generator with 4 PWM-IO pins (PWMA0 ~ PWMA3 / PWMB0 ~ PWMB3)
  - Each generator got one 16-bit timer, which could be used as a general timer
  - Independent 16-bit duty cycle register per PWM-IO pin
- CapTouch sensor supported
  - All pins of PA port are optional as CapTouch sensing pads
- ADC (Analog Digital Conversion)
  - 8-ch (with auto scan mode), 12-bit resolution SAR ADC
  - Trigger by underflow of Timer0 / 1 / 2, or by software
  - Ch0 with 4-level FIFO shared with MIC input for voice processing

- Embedded with dedicated analog LDO: optional output at 3.3V @ 3-battery, or 2.3V @ 2-Battery.

- Built-in MIC control circuitry
  - Differential input MIC with 2-stage of pre-amplifiers and optional AGC or PGA for gain control
- Support EF Security Lock mechanism to prevent programmed data from being read out
- Easy-to-use Development Environment
  - High-level *Q-Code* programming supported
  - Advanced C-Module programming supported
  - 2-pin OCD (On-Chip Debugger) supported with source-level debugging for both Q-Code and C-Module
  - Multi-purpose NX_Programmer for ICE debugging and programming of EF / SPI Flash
  - Smart Writer used in MP for EF/SPI Flash pre-programming @ packages, or ICP @ target boards
  - 6-pin programming interface (VDD, VSS, ICE_DAT, ICE_CLK, PA12, RSTB/PA8) supported
- S/W-based Speech/MIDI Codec, Voice Recognition, & various algorithms supported
  - ADPCM Codec (Adaptive Differential PCM): 4 channels, 4-bit / 5-bit per sample
  - SBC Codec (Sub-Band Coding): 4.5K ~ 32Kbps, max. 16KHz bandwidth, up to 1-ch record & 2-ch playback
  - MIDI: up to 16-channel polyphonic melody @ 32KHz Output Sample Rate
  - Voice Effects: speed / pitch change, robotic sound, echo, real-time voice changer, etc.
  - Voice Recognition: phoneme-based for stand-alone VR applications (only for NX12Fx5xA)
- Noise filter @ 16x up-sampling supported
- Shipping Form
  - Dice
  - Package
    - ✧ Single-Die: SOP-16 / SSOP-28 / LQFP-32
    - ✧ MCP (with 4Mb / 16Mb SPI Flash): SOP-16 / SSOP-28

3. BLOCK DIAGRAM

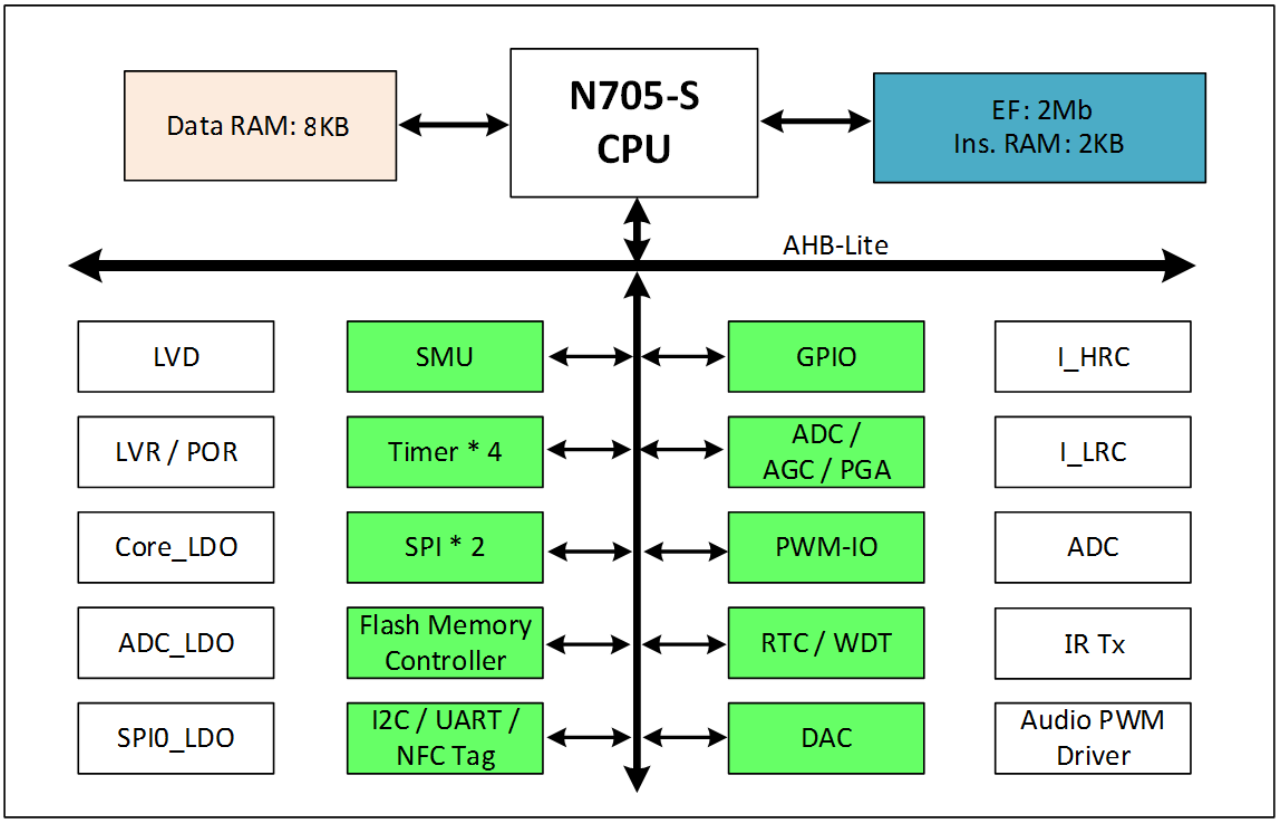


Figure 1 Block Diagram of NX12Fx5xA / NX13Fx5xA Series

4. PAD / PIN DESCRIPTION

Pad Name	Alt #	Type	SOP-16	SSOP-28	SSOP-28	LQFP-32	Dice	Pad Description
Part No.	-	-	NX12Fx5xAS16 NX13Fx5xAS16	NX12FS51AU28 NX13FS51AU28	NX12FM5xAU28 NX13FM5xAU28	NX12FS51AQ32 NX13FS51AQ32	NX12FS51A NX13FS51A	-
Power								
VDD	0	P	●	●	●	●	●	Power input
ADC_VDD	0	AP	●	●	●	●	●	Analog power output for connecting with 0.1uF cap.
VDD_PWM	0	P			●	●	●	Power for DAC and audio PWM driver.
SPI0_VDD	0	P	●	●	●	●	●	Power output for SPI Flash. Connect with 1uF cap.
VSS	0	P	●	●	●	●	●	Ground
VSS_PWM	0	P					●	Ground for DAC and audio PWM driver
VSS_ADC	0	AP					●	Ground for analog circuits
PWM / DAC								
PWM1 / DAC	0	O	●	●	●	●	●	Audio PWM driver output 1 or DAC output by register.
PWM2	0	O	●	●	●	●	●	Audio PWM PA output 2
Port A								
PA0	0	I/O			●	●	●	GPIO pin PA0
AIN0	3	AI			●	●	●	Analog input 0
PA1	0	I/O			●	●	●	GPIO pin PA1
IR0	1	O			●	●	●	IR Tx output from Timer0
AIN1	3	AI			●	●	●	Analog input 1
PA2	0	I/O	●	●	●	●	●	GPIO pin PA2
IR1	1	O	●	●	●	●	●	IR Tx output from Timer1
INT0	2	I	●	●	●	●	●	External INT0
AIN2	3	AI	●	●	●	●	●	Analog input 2
PA3	0	I/O		●	●	●	●	GPIO pin PA3
TM0	1	I		●	●	●	●	External input for Timer0 / Timer1
INT1	2	I		●	●	●	●	External INT1
AIN3	3	AI		●	●	●	●	Analog input 3
PA4	0	I/O		●	●	●	●	GPIO pin PA4
SDA	1	I/O		●	●	●	●	SDA pin of I2C
AIN4	3	AI		●	●	●	●	Analog input 4
PA5	0	I/O		●	●	●	●	GPIO pin PA5
SCL	1	O		●	●	●	●	SCL pin of I2C
AIN5	3	AI		●	●	●	●	Analog input 5
PA6	0	I/O		●	●	●	●	GPIO pin PA6
TX	1	O		●	●	●	●	TX pin of UART
AIN6	3	AI		●	●	●	●	Analog input 6
PA7	0	I/O		●	●	●	●	GPIO pin PA7
RX	1	I		●	●	●	●	RX pin of UART

Pad Name	Alt #	Type	SOP-16	SSOP-28	SSOP-28	LQFP-32	Dice	Pad Description
Part No.	-	-	NX12Fx5xAS16 NX13Fx5xAS16	NX12FS51AU28 NX13FS51AU28	NX12FM5xAU28 NX13FM5xAU28	NX12FS51AQ32 NX13FS51AQ32	NX12FS51A NX13FS51A	-
AIN7	3	AI		•	•	•	•	Analog input 7
RSTB/PA8	0	I, I/O	•	•	•	•	•	RSTB (default) or GPIO pin by option. Since this pin is RSTB by default upon power up, so that it can't be set at low level when powered on.
CSB	-	I	•	•	•	•	•	Programming I/F
PA12	0	I/O	•	•	•	•	•	GPIO pin PA12
PWMA0	1	O	•	•	•	•	•	PWMA0 output pin
SPI1_CSB	2	O	•	•	•	•	•	CSB pin of SPI1
MISO	-	O	•	•	•	•	•	Programming I/F
PA13	0	I/O	•	•	•	•	•	GPIO pin PA13
PWMA1	1	O	•	•	•	•	•	PWMA1 output pin
SPI1_CLK	2	O	•	•	•	•	•	CLK pin of SPI1
PA14	0	I/O	•	•	•	•	•	GPIO pin PA14
PWMA2	1	O	•	•	•	•	•	PWMA2 output pin
SPI1_MOSI	2	O	•	•	•	•	•	MOSI pin of SPI1
PA15	0	I/O		•	•	•	•	GPIO pin PA15
PWMA3	1	O		•	•	•	•	PWMA3 output pin
SPI1_MISO	2	I		•	•	•	•	MISO pin of SPI1
Port B								
PB0	0	I/O		•		•	•	GPIO pin PB0
PWMB0	1	O		•		•	•	PWMB0 output pin
SPI0_IO1	2	O		•		•	•	IO1 / MISO pin of SPI0
PB1	0	I/O		•		•	•	GPIO pin PB1
PWMB1	1	O		•		•	•	PWMB1 output pin
SPI0_CSB	2	O		•		•	•	CSB pin of SPI0
PB2	0	I/O		•		•	•	GPIO pin PB2
PWMB2	1	O		•		•	•	PWMB2 output pin
SPI0_CLK	2	O		•		•	•	CLK pin of SPI0
PB3	0	I/O		•		•	•	GPIO pin PB3
PWMB3	1	O		•		•	•	PWMB3 output pin
SPI0_IO0	2	I/O		•		•	•	IO0 / MOSI pin of SPI0
PB4	0	I/O		•	•	•	•	GPIO pin PB4
NFC_LA	1	I		•	•	•	•	NFC Antenna terminal A
SPI0_IO2	2	I/O		•	•	•	•	IO2 pin of SPI0
TM1	3	I		•	•	•	•	External input for Timer2 / Timer3
PB5	0	I/O		•	•	•	•	GPIO pin PB5
NFC_LB	1	O		•	•	•	•	NFC Antenna terminal B
SPI0_IO3	2	I/O		•	•	•	•	IO3 pin of SPI0

Pad Name	Alt #	Type	SOP-16	SSOP-28	SSOP-28	LQFP-32	Dice	Pad Description
Part No.	-	-	NX12Fx5xAS16 NX13Fx5xAS16	NX12FS51AU28 NX13FS51AU28	NX12FM5xAU28 NX13FM5xAU28	NX12FS51AQ32 NX13FS51AQ32	NX12FS51A NX13FS51A	-
Port C								
PC0	0	I/O	●	●	●	●	●	GPIO pin PC0
IR2	1	O	●	●	●	●	●	IR Tx output from Timer2
MICP	3	AI	●	●	●	●	●	MIC+
PC1	0	I/O	●	●	●	●	●	GPIO pin PC1
IR3	1	O	●	●	●	●	●	IR Tx output from Timer3
MICN	3	AI	●	●	●	●	●	MIC-
PC2	0	I/O	●	●	●	●	●	GPIO pin PC2
VMIC	3	AO	●	●	●	●	●	MIC bias voltage output
PC3	0	I/O			●	●	●	GPIO pin PC1
OPO	3	AO			●	●	●	Output pin of 2nd stage Pre-Amp
Port D								
PD0	0	I/O	●	●	●	●	●	GPIO pin PI0
TX	3	O	●	●	●	●	●	TX pin of UART
ICE_CLK	-	O	●	●	●	●	●	Clock pin of ICE port
SCL	-	I	●	●	●	●	●	Programming I/F
PD1	0	I/O	●	●	●	●	●	GPIO pin PI1
RX	3	I	●	●	●	●	●	RX pin of UART
ICE_DAT	-	I/O	●	●	●	●	●	Data pin of ICE port
SDA	-	I/O	●	●	●	●	●	Programming I/F

Pad Type: P = Digital Power, I = Input, O = Output, I/O = Input / Output, AI = Analog Input, AO = Analog output, AP = Analog Power.

5. FUNCTIONAL DESCRIPTION

5.1 Memory Organization

The memory map is depicted in Figure 2 Memory Map of the NX12Fx5xA / NX13Fx5xA Series. The Embedded Flash, RAM, function registers, and interrupt vectors, are all memory mapped. The embedded flash size is 256KB, including AP code (255.5KB) and interrupt vectors (0.5KB). There are 2KB of Ins. RAM and 8KB of Data RAM associated with the N705-S processor for running the program @ EF / SPI Flash. The Ins. RAM is mainly used for routines related to FMC operation so that it can still work while EF is being erased. For example, the talk-back application that utilizes EF as the memory to record the voice input would use Ins. RAM to serve the INT routine for receiving data from MIC continuously even when EF is erased in parallel. For applications that requires no FMC operations, the Ins. RAM could be used as Data RAM, which would add up to 10KB.

Total addressing space is 16MB, while SPI flash is mapped within 0x80_0000 ~ 0x9F_FFFF (2MB space) with bank support for XIP and data storage expansion.

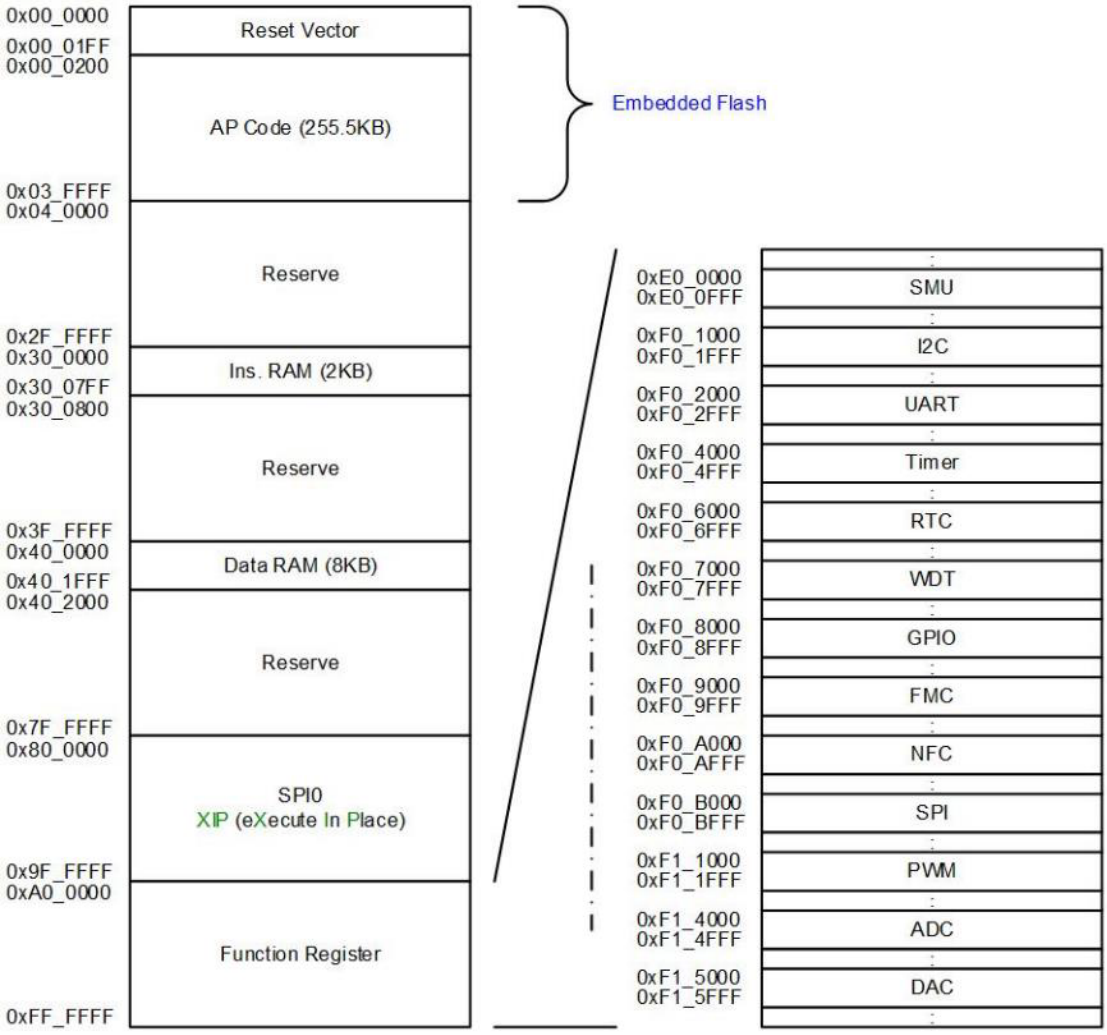


Figure 2 Memory Map of the NX12Fx5xA / NX13Fx5xA Series

5.2 Clock Generator

The clock generator consists of 2 clock sources:

- Built-in high clock (I_HRC): Output frequency is 48MHz with 1 wait-state @ EF access.
- Built-in low clock (I_LRC): Output frequency is 32,768Hz.

These two internal oscillators, I_HRC and I_LRC, are trimmed to achieve +/-0.5% and +/-1.5% accuracy, respectively.

5.3 Operating Mode

The NX12FX5XA / NX13FX5XA provides three kinds of operating modes to tailor for various kinds of applications while saving power consumption. These operating modes are normal mode, standby mode and halt mode.

Normal mode is designated for high-speed, high-performance operation. At standby mode, the NX12FX5XA / NX13FX5XA stops almost all operations, except peripheral blocks with clock source from I_LRC, and wake-up periodically to serve scheduled routines. At halt mode, it stops all operations, waiting for external events to wake it up.

When the NX12FX5XA / NX13FX5XA is powered up, there is a delay of 32mS before user's code is executed to ensure proper operation. Besides, the SPI Flash needs another 15mS to get power stabilized after SPI0_VDD is turned on. Therefore, there is a total of 50mS or so before any attempt to access the data stored inside the SPI Flash.

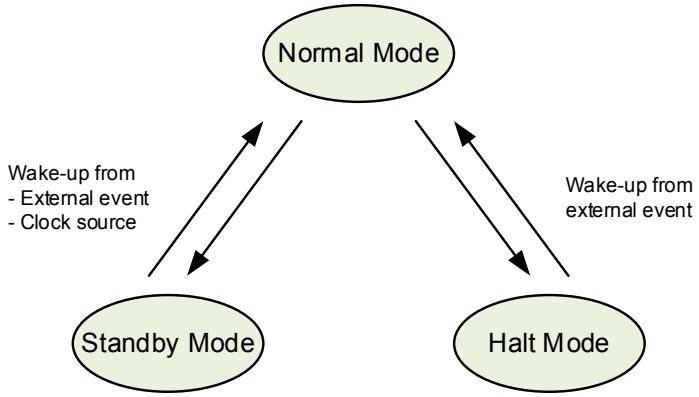


Figure 3 Operating Modes

5.4 Interrupt

Interrupt signals are directly connected to the N705-S processor. The interrupt priority is controlled by the processor. Each interrupt is assigned with 2 bits to represent 4 possible priority levels ranging from 0

(highest) to 3 (lowest). The hardware compares the priority level first: the smaller the priority level, the higher the priority. With the same priority, the lower the interrupt number, the higher the priority.

5.5 Peripherals

5.5.1 I/O Port

Up to 25 GPIO pins are available. These are shared multiple function pins under control of the alternate multiple function registers. A total of 25 pins are arranged in 4 ports named with Port A (PA), Port B (PB), Port C (PC), and Port D (PD). The PA port has 13 pins, PB port 6 pins, PC port 4 pins, and PD port 2 pins.

Each pin can be configured as input or output, weak / strong pull-high resistor and can wake up CPU upon I/O state changes from halt mode.

5.5.2 SPI

There are two SPI masters supported. One is the SPI0 that is dedicated for connecting with an external SPI flash device to store most of the data used for various applications like speech (ADPCM, SBC, or CELP), melody (including MIDI file and wavetable timbres), and user's general data storage. With single/dual/quad I/O modes supported, the SPI flash can run up to 24MHz clock. Together with the XIP capability (e**X**ecute **I**n **P**lace), users can extend the program code @ EF to the SPI Flash with a descent performance for many applications. The other is the SPI1 master with single I/O mode, which can be used to interface with popular devices like 2.4GHz RF for a wireless connectivity.

The SPI0 / SPI1 is generally powered by the SPI0_VDD, which is an LDO (Low Drop-Out) regulator rated at 26mA sourcing capability & 140uA quiescent current consumption. It is used under normal mode for read / erase / write operations to the external SPI Flash. This LDO is turned off by default to save power consumption when not in operation.

5.5.3 I^2C

The I^2C (Inter-Integrated Circuit) master/slave controller support the following features.

- Standard-mode (100 Kb/s), Fast-mode (400 Kb/s) and Fast-mode Plus (1 Mb/s) protocols
- Programmable Master/Slave mode
- Support 7-bit and 10-bit addressing mode
- Support general call address
- Auto clock stretching

5.5.4 UART

The NX12FX5XA / NX13FX5XA provides the UART (Universal Asynchronous Receiver Transmitter) module, which is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols such as RS-232.

- Support 5 to 8 bits per character
- Support 1, 1.5 and 2 STOP bits
- Support even, odd and stick parity bits
- Support programmable baud rate
- Support detection of parity error, framing error and data overrun

5.5.5 PWM-IO

The NX12FX5XA / NX13FX5XA has 2 sets of PWM-IO generators (PWMA / PWMB), each with four PWM-IO outputs (PWMA0 ~ PWMA3, PWMB0 ~ PWMB3). Every four PWM-IO output pins share a common 16-bit PWM-IO timer, while each PWM-IO output pin has its own duty register.

- Four PWM-IO outputs share a 16-bit timer
- Programmable divider as the clock source of timer
- 16 bits for PWM's duty cycle

5.6 Timer

The NX12FX5XA / NX13FX5XA has four 16-bit timers: TIMER0 / TIMER1 / TIMER2 / TIMER3, which can be used as a trigger source for DAC / Audio PWM / ADC / IR / Software CapTouch or as a function of time delay, clock generation, etc.

- Programmable source of timer clock
- 16-bit counter for each timer

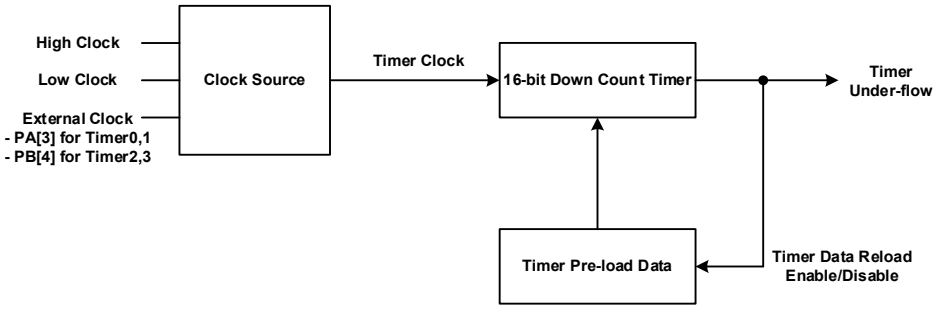


Figure 4 Timer Block Diagram

5.7 Software CapTouch

The NX12FX5XA / NX13FX5XA supports S/W-based CapTouch on all PA pins for applications that require no very low standby current with wake-up on CapTouch feature. The power consumption of each S/W-based CapTouch might not low enough to meet the strict battery life criterion, but it's still useful for many applications virtually without the increase of BOM cost.

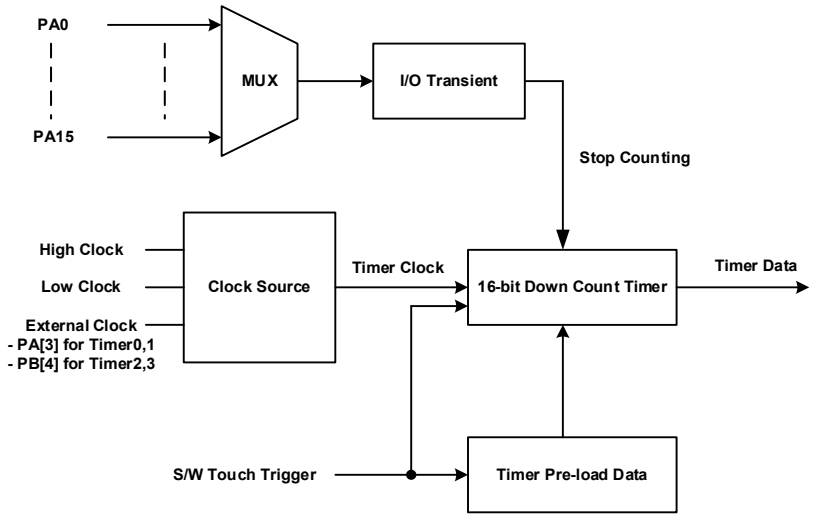


Figure 5 Software CapTouch Block Diagram

5.8 IR TX

The NX12FX5XA / NX13FX5XA provides a programmable IR carrier, whose frequency can be generated by assigning suitable counter values to the 16-bit timer.

- Support output stop value at 0 or 1.
- Support 16 bits reload data to adjust IR's frequency.
- The lowest frequency is I_HRC divided by 65535, which is 732Hz @ I_HRC=48MHz.

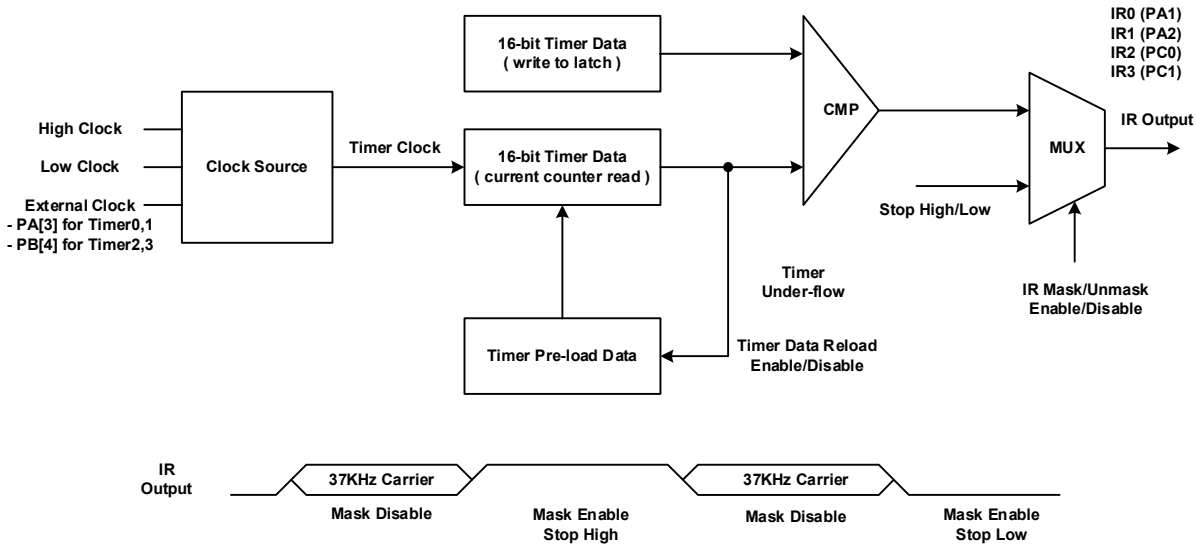


Figure 6 IR TX Block Diagram

5.9 RTC

As the name implies, the RTC (Real-Time Clock) is generally used to keep the time, with the clock source from an internal built-in I_LRC (trimmed to 32,768Hz with +/-1.5% accuracy). The RTC supports periodic time tick interrupts with 4 options: 16.384KHz, 1.024KHz, 64Hz, 2Hz.

5.10 WDT

The Watchdog Timer (WDT) is used to perform a system reset when the system is not responding at all. There are two period options for the WDT to generate a reset: 188ms / 750ms.

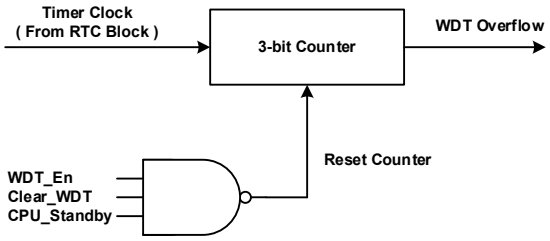


Figure 7 WDT Block Diagram

5.11 ADC

The NX12FX5XA / NX13FX5XA provide one 12-bit Analog-to-Digital converter that supports up to eight input channels. The A/D converter supports both single and continuous scan mode. It can be started by software or TIMER trigger.

- Provide 4-level FIFO or data registers for each channel.
- Auto scan mode can be used to get 4/3/2 channel's data automatically.

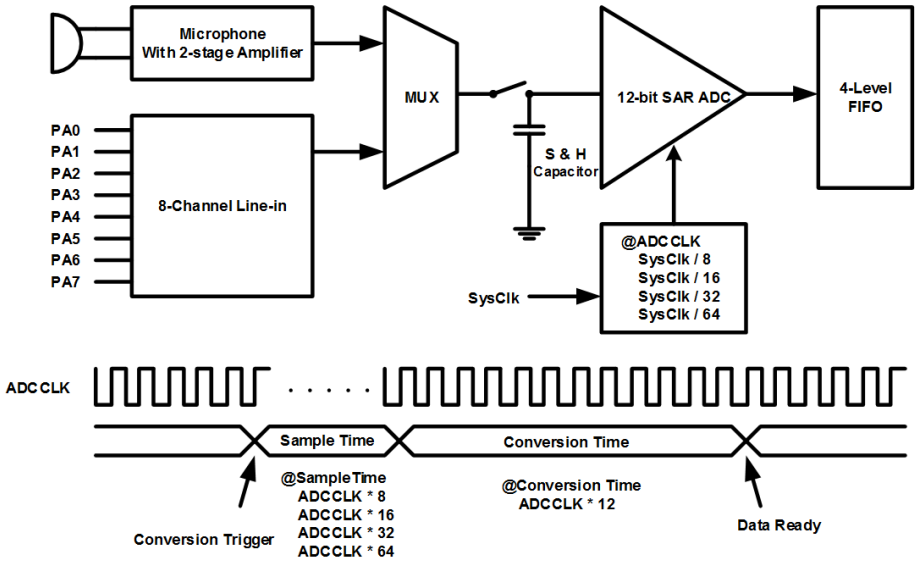


Figure 8 ADC Block Diagram

5.12 AGC & PGA

For applications with microphone input, there are two kinds of gain control: one is the AGC (Auto Gain Control), the other is the PGA (Programmable Gain Adjustment). For AGC, the 1st stage gain of pre-amplifier is controlled by the AGC along with parameters configured via register control, while the 2nd stage gain of pre-amplifier is controlled by S/W program. For PGA, the 1st stage pre-amplifier gain could be selected as 15x or 30x, while the gain of 2nd stage of pre-amplifier is controlled by S/W program. For more details, please refer to User's Manual for NX12Fx5xA / NX13Fx5xA.

Depending on the MIC sensitivity, distance between user and MIC, and component value of application circuit, overall PGA gain of the 2-stage pre-amplifiers might vary accordingly. Please refer to User's Manual for NX12Fx5xA / NX13Fx5xA for more details.

5.13 DAC & Audio PWM Driver

The NX12Fx5xA / NX13Fx5xA provides two data buffers with 4-level FIFO each and one 14-bit Digital-to-Analog converter with interpolation function. It can be started by software or TIMER trigger.

- Provide 4-level FIFO per channel as data buffer
- Provide hardware up-sampling (interpolation) function
- Support mixing mode for two-channel data applications

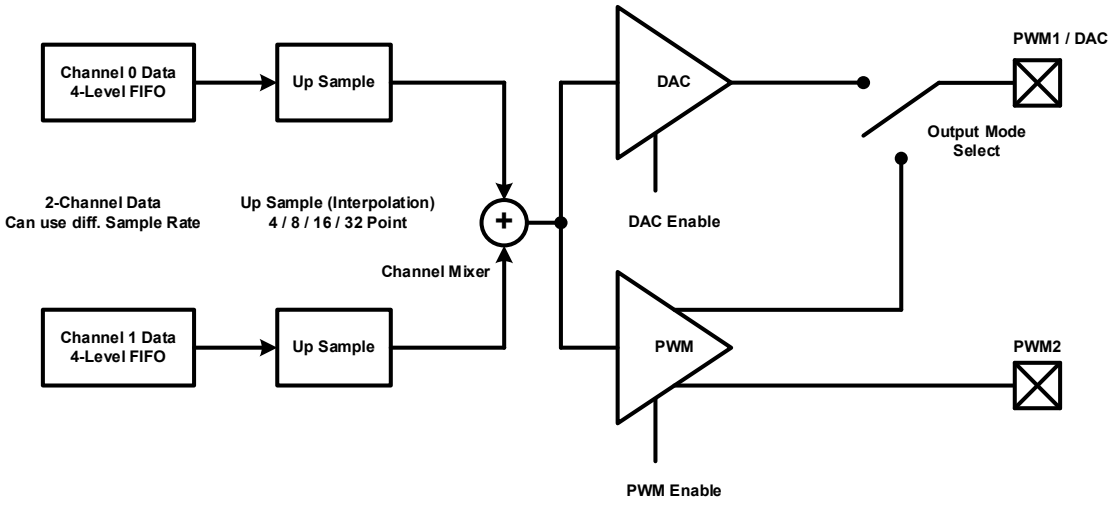


Figure 9 Block Diagram of DAC and Audio PWM Driver

5.14 LVD

The LVD (Low Voltage Detector) is trimmed to +/-3% accuracy for the user to detect the battery voltage @ VDD pin. When the VDD voltage falls below the specified LVD level, the LVD_Flag will be set as HIGH.

LVD_SEL[2:0]	Voltage
111	3.6V
110	3.4V
101	3.2V
100	3.0V
011	2.8V
010	2.4V
001	2.2V
000	2.0V

Table 2 LVD voltage select

5.15 Options

Users may select different options depending on the application requirement. There are several options that users may select for the NX12Fx5xA / NX13Fx5xA series, as shown in Table 3 User Options.

Item	Name	Options
1	Reset Pin (PA8)	1. Reset Pin (default) 2. GPIO
2	LVR (Halt Mode)	1. LVR Enable at Halt Mode 2. LVR Disable at Halt Mode (default)
3	VDD Voltage	1. 4.5V (ADC_VDD @ 3.3V, default) 2. 3.0V (ADC_VDD @ 2.3V)
4	WDT	1. WDT Enable (default) 2. WDT Disable
5	Ins. RAM (IRAM)	1. IRAM Enable 2. IRAM Disable (default)
6	Input Voltage (V_{IH}/V_{IL})	1. 0.7VDD/0.3VDD (default) 2. 0.5VDD/0.2VDD
7	SPI0 Functions	1. GPIO (default) 2. SPI
8	SPI0 IO Mode	1. Single/Dual (default) 2. Quad
9	SPI1 Functions	1. GPIO (default) 2. SPI
10	Voice Output	1. PWM (default) 2. DAC
11	PWM Current	1. Normal (default) 2. Large 3. Ultra

Table 3 User Options

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

Symbol	Parameter	Rated Value	Unit
V_{DD} - V_{SS}	Supply voltage	-0.5 ~ +7.5	V
V_{IN}	Input voltage	V_{SS} - 0.3 ~ V_{DD} + 0.3	V
T_{OP}	Operating Temperature	0 ~ +70	°C
T_{ST}	Storage Temperature	-25 ~ +85	°C

6.2 DC Characteristics

(T_A=25ºC, unless otherwise specified)

Symbol	Parameter		V_{DD}	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating voltage		-	2.0		5.5	V	-
I_{HALT}	Halt Current		3		4		uA	CPU stop, all functions off, Disable SPI0_VDD[1]
			4.5		4.5			
			3		5		uA	LVR on at halt mode
			4.5		5.5			
I_{SB}	Standby Current		3		5.5		uA	CPU stop, all functions off, RTC on, LVR on, Disable SPI0_VDD
			4.5		6			
I_{OP}	Operating Current	Normal Mode	3		7		mA	CPU_CLK = 48MHz, 1 wait-state, Enable SPI0_VDD, No load
			4.5		7			
R_{PH}	Pull High Resistor (Input current)	Strong (100KΩ)	3		100		KΩ	V_{IN} = 0V
			4.5		60			
		Weak (1MΩ)	3		1,000			
			4.5		600			
I_{OH}	Normal drive current (Normal GPIO)		3		-9		mA	V_{OH} = VDD - 1.0V, SPI mode (Power from SPI0_VDD, 3.3V)
			4.5		-13			
	SPI mode drive current (SPI0 PB[0:5])		3		-14			
			4.5		-17			
	SPI mode drive current (SPI1 PA[12:15])		3		-14			
			4.5		-17			
I_{OL}	Normal sink current		3		12		mA	V_{OL} = 1.0V,

Symbol	Parameter	V_{DD}	Min.	Typ.	Max.	Unit	Condition
	(Normal GPIO)	4.5		20			SPI mode (Power from SPI0_VDD, 3.3V)
	Large sink current (Normal GPIO)	3		23			
		4.5		35			
	SPI mode sink current (SPI0 PB[0:5])	3		14			
		4.5		16			
	SPI mode sink current (SPI1 PA[12:15])	3		14			
		4.5		16			
I_{PWM}	Audio PWM Output Current[2]	3		150		mA	1KHz Sine wave, THD+N @ 1%, Load = 8Ω
		4.5		250			
ΔF/F	I_HRC trim accuracy	3	-0.5		0.5	%	$\frac{Fosc - Ftyp}{Ftyp}$[3]

[1] LDO @ SPI0_VDD is rated at 26mA for read / erase / write operation to the SPI Flash @ Normal mode.

[2] The current is represented in the form of effective power, which is bigger than playback under practical conditions.

[3] Ftyp = 48MHz, which is the nominal clock of I_HRC.

6.3 ADC Characteristics

(ADC_V_{DD}=3.3V, T_A=25ºC, unless otherwise specified)

Symbol	Characteristics	Min.	Typ.	Max.	Unit
V_{INL}	ADC Sensor Input Voltage Range from PA[7:0]	V_{SS} - 0.3		ADC_V_{DD} + 0.3	V
V_{INM}	ADC Microphone Input Voltage Range	V_{SS} - 0.3		ADC_V_{DD} + 0.3	V
B_{RES}	Resolution of ADC			12	Bit
ENOB	Effective Number of Bits		10.1		Bit
INL	Integral Non-Linearity of ADC		2.5 ~ -2.4		LSB
DNL	Differential Non-Linearity of ADC		2.3 ~ -1.0		LSB
F_{CONV}	AD Conversion Rate		44.1		KHz

6.4 DAC Characteristics

(V_{DD}=3V, T_A=25ºC, unless otherwise specified)

Symbol	Characteristics	Min.	Typ.	Max.	Unit	Condition
B_{RES}	Resolution of DAC			14	Bit	-
THD+N	THD+N (Vin = -3 dBFS)		-55.3		dBr A	No load
DR	Dynamic Range (Vin = -60 dBFS)		-77.7		dBr A	
SNR	Noise at No Signal (Vin = -90 dBFS)		-97.6		dBr A	

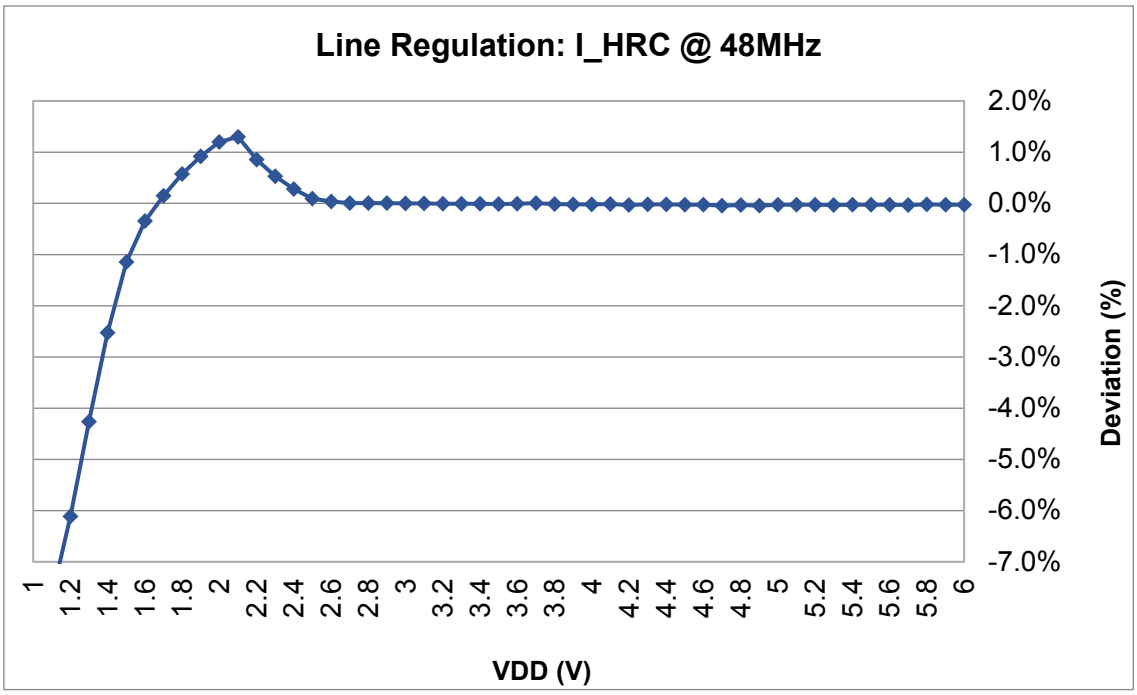
6.5 Audio PWM Characteristics

(V_{DD}=5.5V, T_A=25ºC, unless otherwise specified)

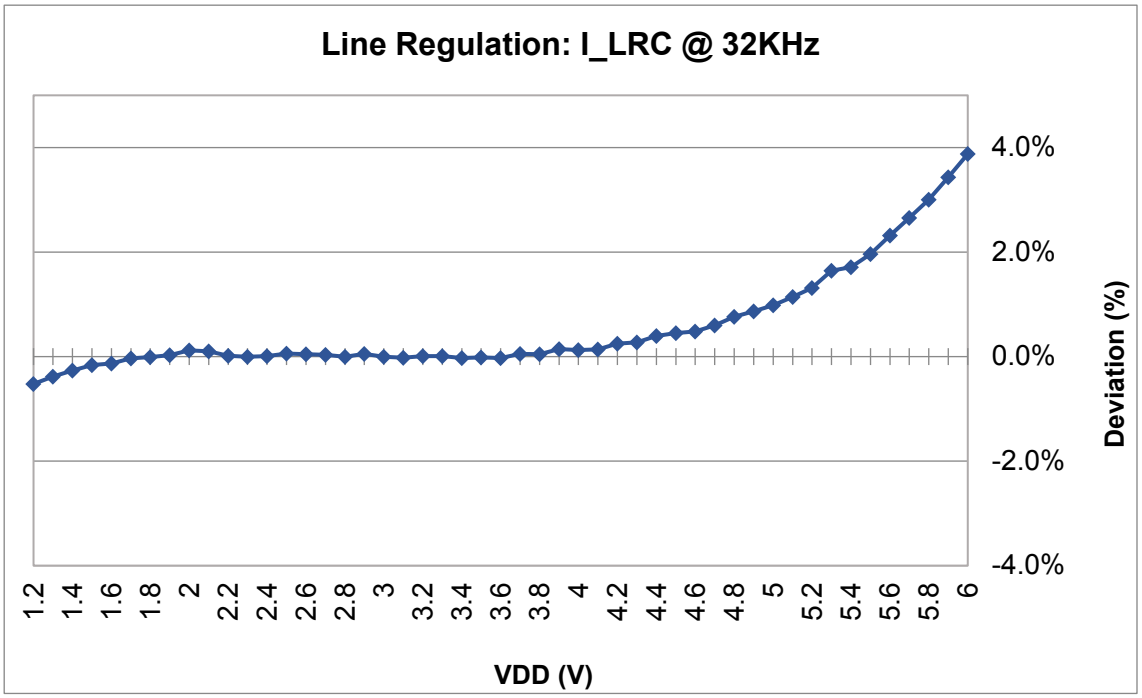
Symbol	Characteristics	VDD	Min.	Typ.	Max.	Unit	Condition
THD+N	THD+N (Vin = -3 dBFS)	-		-66.4		dBr A	No load
DR	Dynamic Range (Vin = -60 dBFS)	-		-82.1		dBr A	
SNR	Noise at No Signal (Vin = -90 dBFS)	-		-126.4		dBr A	
P_O	Output Power	3V		200		mW	Load = 8Ω, THD+N @ 1%
		4.5V		500		mW	Load = 8Ω, THD+N @ 1%

6.6 Frequency vs. Voltage

6.6.1 I_HRC

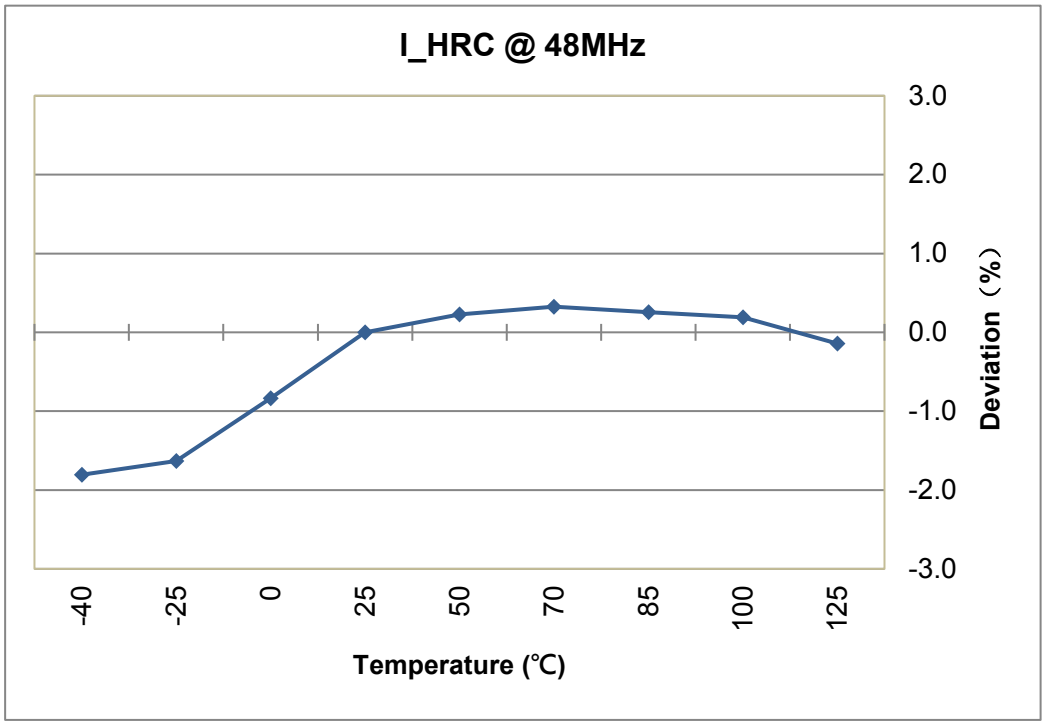


6.6.2 I_LRC

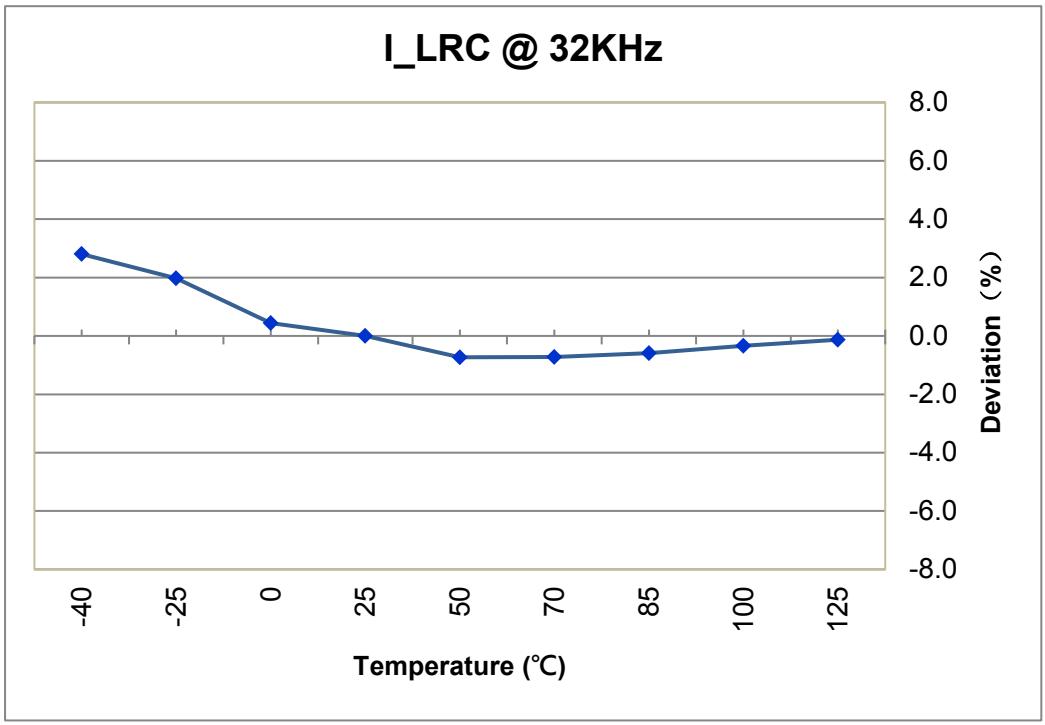


6.7 Frequency vs. Temperature

6.7.1 I_HRC

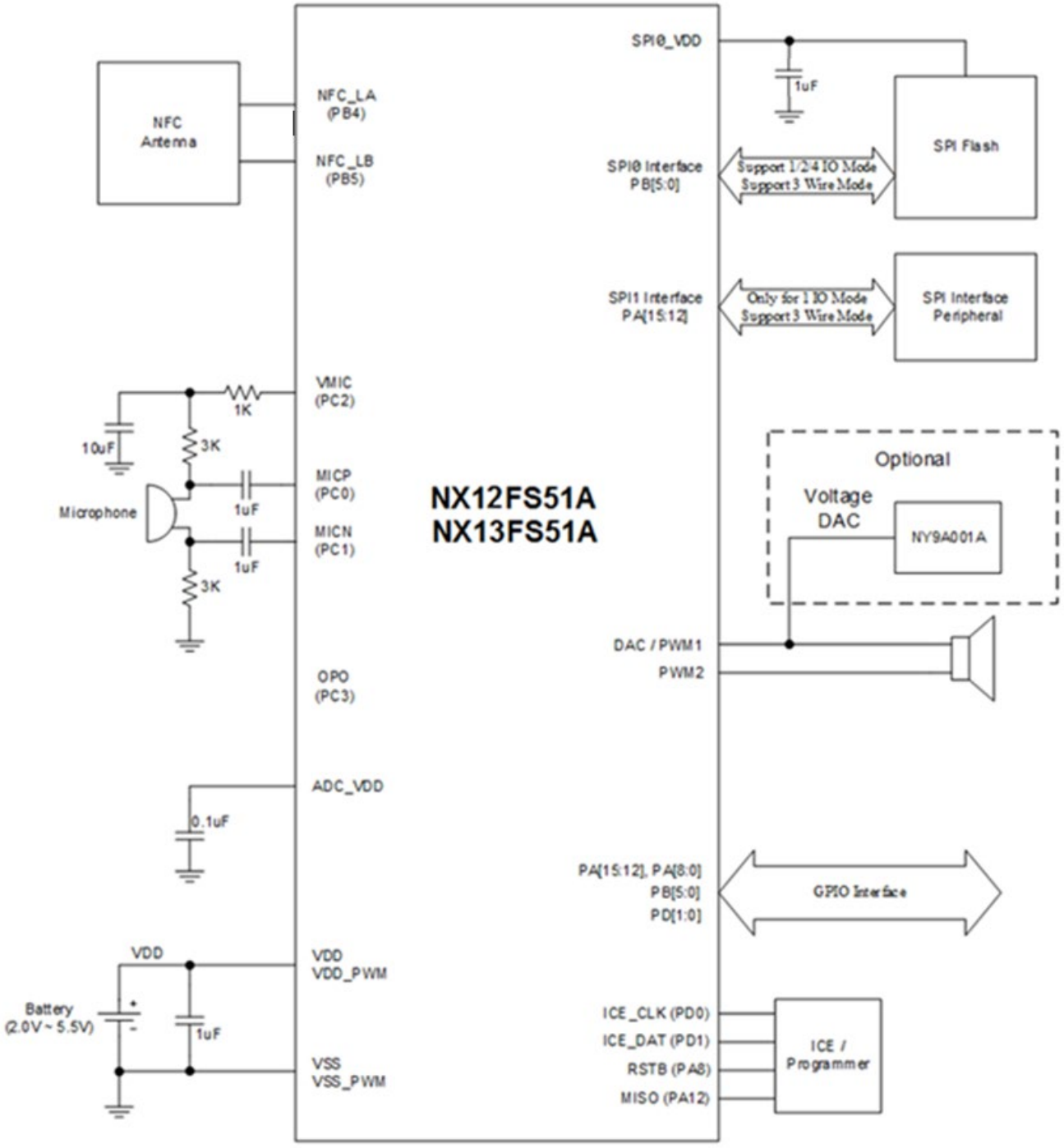


6.7.2 I_LRC

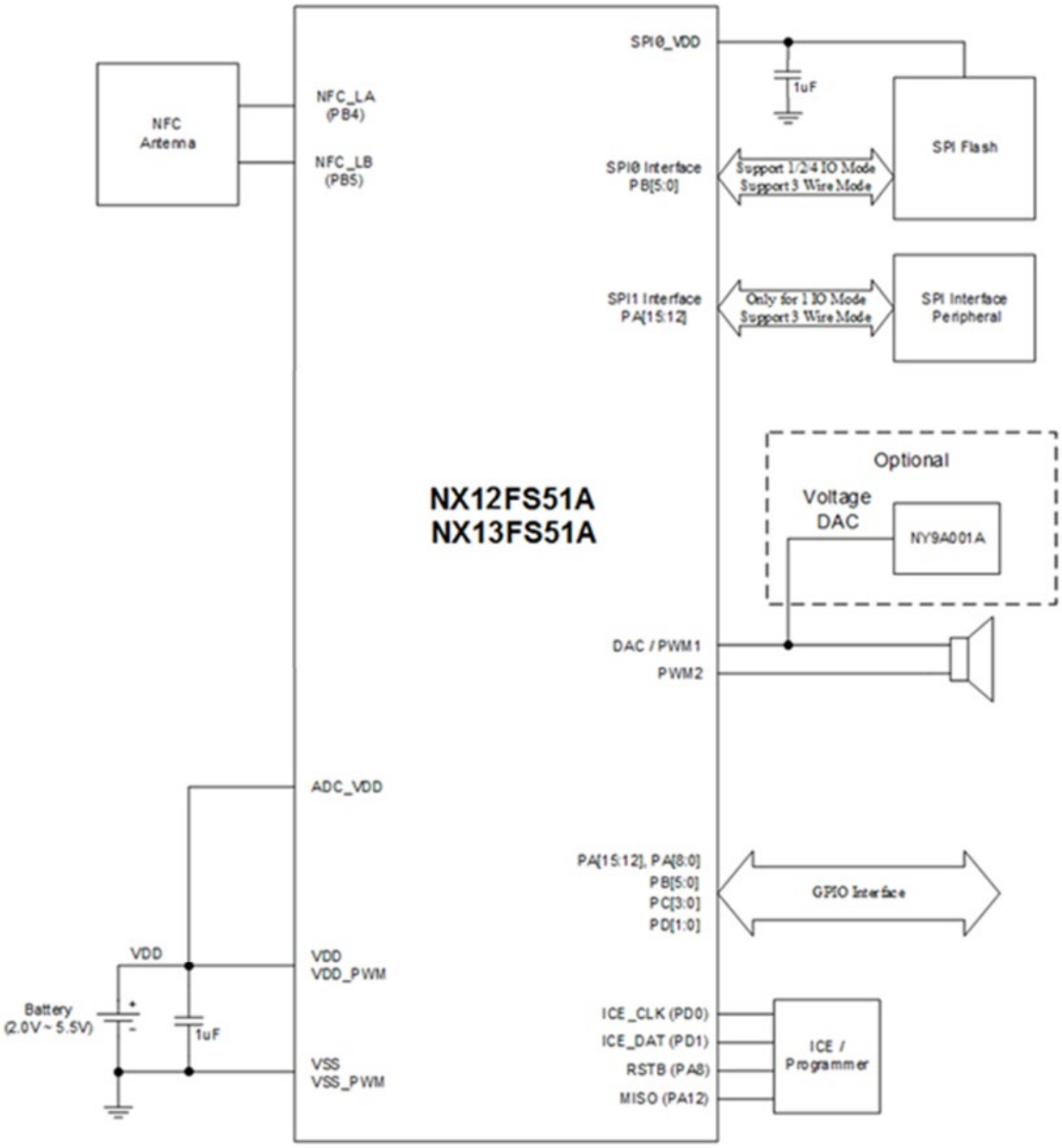


7. APPLICATION CIRCUIT

7.1 Port C for MIC input



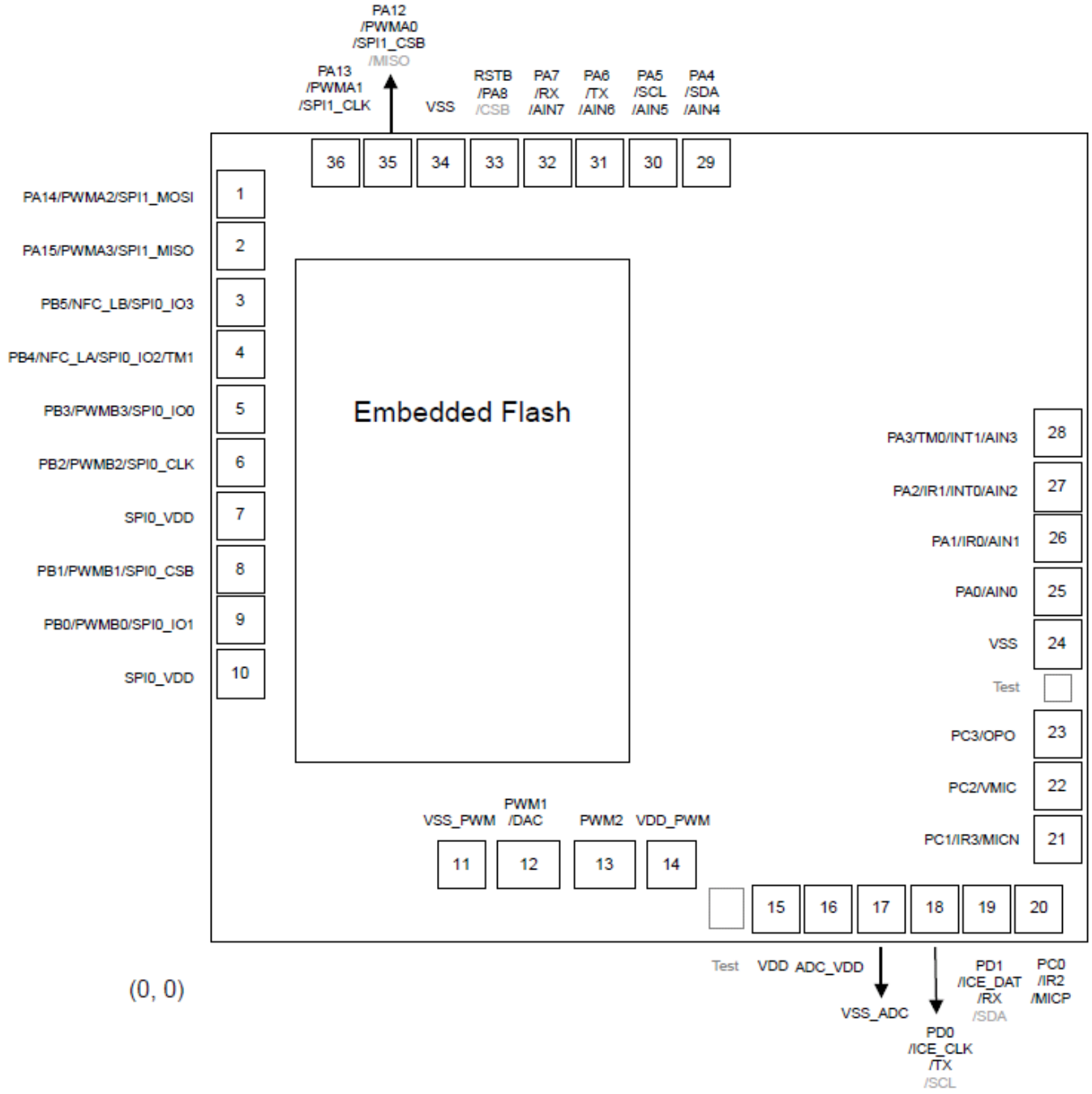
7.2 Port C for GPIO



Note 1: If Port C is used for I/O applications, ADC_VDD must be disabled from F/W and connected to VDD.

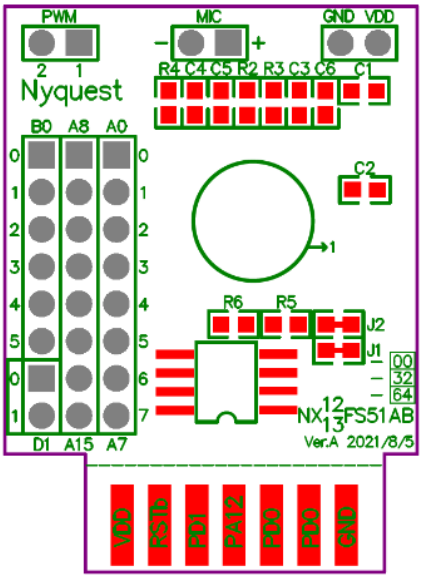
Note 2: If ADC used, LDO is recommended for VDD / ADC_VDD in order to have better ADC accuracy.

8. DIE PAD DIAGRAM

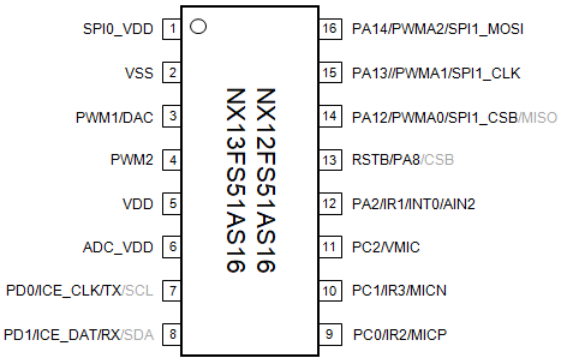


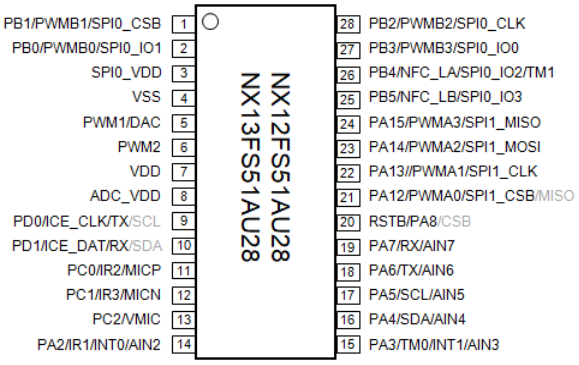
9. COB PIN ASSIGNMENT

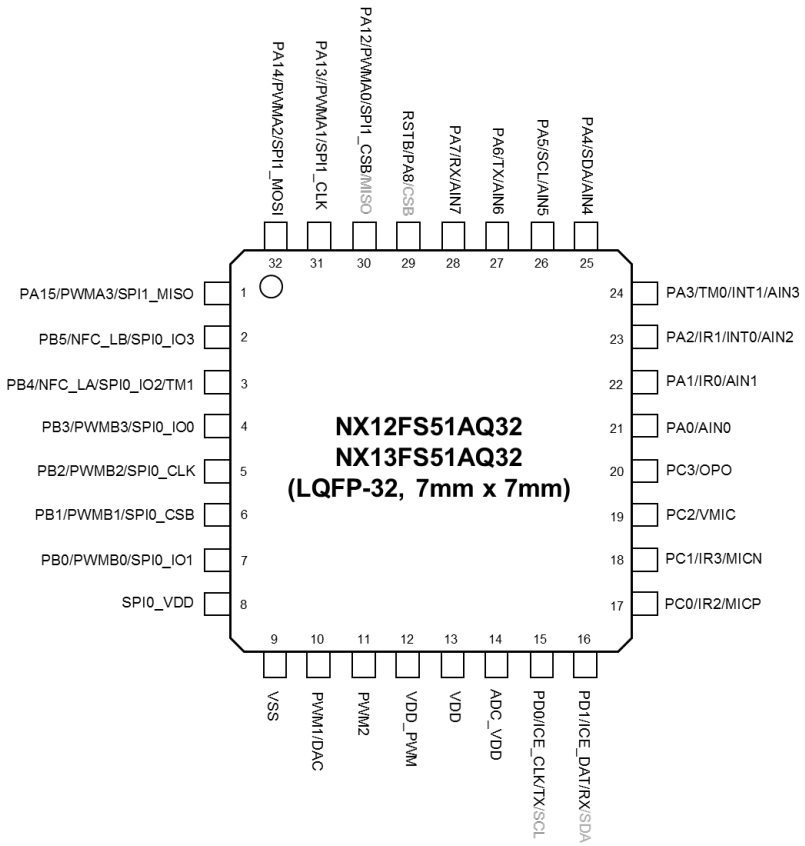
NX12FS51AB / NX13FS51AB

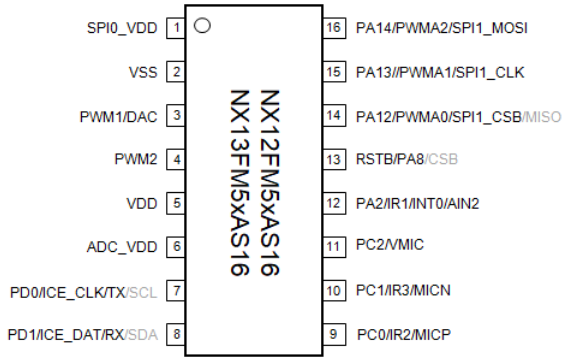


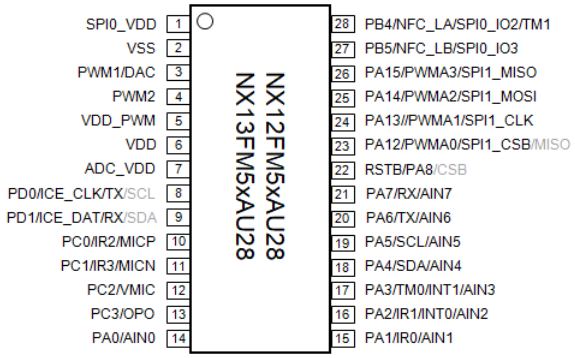
10. PACKAGE PIN ASSIGNMENT





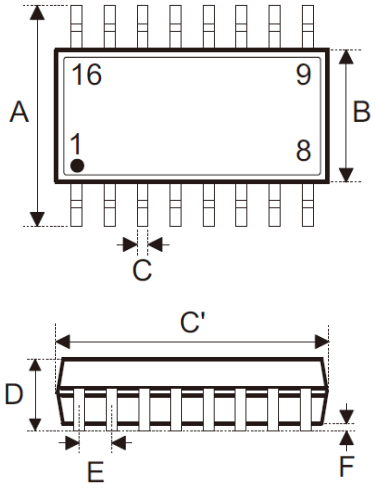






11. PACKAGE DIMENSION

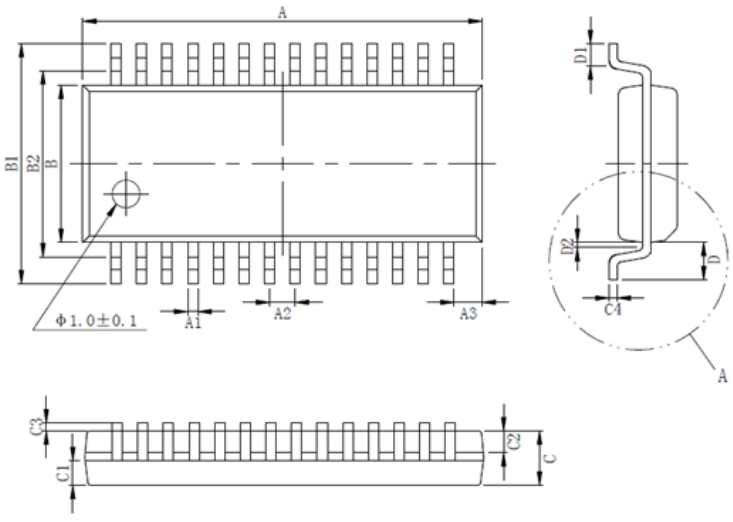
11.1 SOP-16 (150mil, 1.27mm pin pitch)



	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A		0.236 BSC			6.00 BSC	
B		0.154 BSC			3.90 BSC	
C	0.012	-	0.020	0.31	-	0.51
C'		0.390 BSC			9.90 BSC	
D	0.065	-	0.069	1.64	-	1.75
E		0.050 BSC			1.27 BSC	
F	0.004	-	0.010	0.10	-	0.25
G	0.016	-	0.050	0.40	-	1.27
H	0.004	-	0.010	0.10	-	0.25
α	-	-	8°	-	-	8°

Note: For 16-pin SOP IC, 50 units per tube.

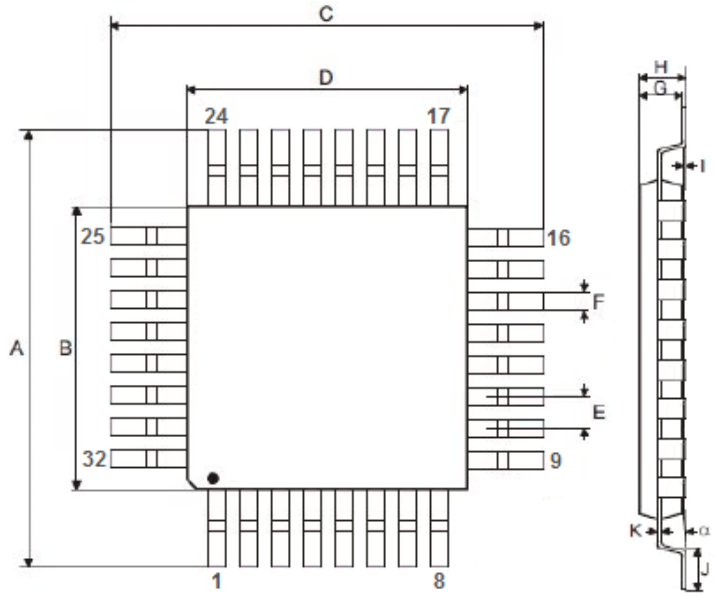
11.2 SSOP-28 (150mil, 0.635mm pin pitch)



Symbol	Dimension (mm)	
	MIN	MAX
A	9.80	10.00
A1	0.254 TYP	
A2	0.635 TYP	
B	3.85	3.95
B1	5.84	6.24
C	1.40	1.60
C1	0.61	0.71
C3	0.05	0.25
D	1.05 TYP	
D1	0.40	0.70
D2	0.15	0.25

Note: For 28-pin SSOP IC, 50 units per tube.

11.3 LQFP-32 (7mm x 7mm)



	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.346	-	0.362	8.80	-	9.20
B	0.272	-	0.280	6.90	-	7.10
C	0.346	-	0.362	8.80	-	9.20
D	0.272	-	0.280	6.90	-	7.10
E	-	0.031	-	-	0.80	-
F	0.013	-	0.017	0.32	-	0.43
G	0.053	-	0.057	1.35	-	1.45
H	-	-	0.063	-	-	1.60
I	0.002	-	0.008	0.05	-	0.20
J	0.020	-	0.028	0.50	-	0.70
K	0.005	-	0.006	0.13	-	0.16
α	-	4°	-	-	4°	-

12. ORDERING INFORMATION

P/N	*Shipping Form*	*Remark*
NX12FS51A / NX13FS51A	Dice	Blank EF data
NX12FS51AQ / NX13FS51AQ	Dice	Pre-Programmed EF data (unit: wafer)
NX12FS51AW / NX13FS51AW	Wafer	Blank EF data
NX12FS51AQW / NX13FS51AQW	Wafer	Pre-Programmed EF data (unit: wafer)
NX12FS51AB / NX13FS51AB	COB	28.0mm x 38.6mm (with V-Cut)
NX12FS51AS16 / NX13FS51AS16	SOP-16	150 mil, 1.27mm pitch
NX12FS51AU28 / NX13FS51AU28	SSOP-28	150 mil, 0.635mm pitch
NX12FS51AQ32 / NX13FS51AQ32	LQFP-32	7mm x 7mm, 0.8mm pitch
NX12FM52AS16 / NX13FM52AS16	SOP-16 (MCP)	150 mil, 1.27mm pitch
NX12FM52AU28 / NX13FM52AU28	SSOP-28 (MCP)	150 mil, 0.635mm pitch
NX12FM54AS16 / NX13FM54AS16	SOP-16 (MCP)	150 mil, 1.27mm pitch
NX12FM54AU28 / NX13FM54AU28	SSOP-28 (MCP)	150 mil, 0.635mm pitch