Homework #1

Course: CSE4010-01 Computer Architecture

Professor Juho Kim

March 12, 2021

1. Submission

- Submission Deadline: **March 19, 2021, 11:59 pm (Submit at Cyber Campus)** (20 percent reduction per day for late submissions and no credit after 3 days)
- Write solving processes and answers on a blank white paper, scan it and submit it as a **PDF file.**
- The filename should be **HW1_STUDENT-ID_NAME.pdf**

  (ex. HW1_20219999_홍길동.pdf)
- **WARNING**:
  - Students who copy other's homework will get zero point for this assignment.
  - Submission without any solving processes will get zero points.
  - Submission with another form rather than pdf will have a 3 points reduction of the total score.
  - Submission with the wrong file name will have 3 points reduction of total score.
  - Before submission, please check whether your solving processes and answers are clear enough to read. (No credit will be given if your work is illegible)

2. Reference

- Lecture notes
- Patterson and Hennessy, Computer Organization and Design 4th (ARM Edition), Morgan Kaufmann, 2010

1. Consider four different processors P1, P2, P3, and P4 executing the same instruction set with the clock rates and CPIs given in the following table.**(35pts)**

Processor	Clock Rate	CPI
P1	1.5 GHz	1.0
P2	2 GHz	1.5
P3	4 GHz	2.5
P4	3 GHz	2.0

1-1 Which processor has the highest performance?

1-2 If the processors each execute a program in 5 seconds, find the number of cycles and the number of instructions

1-3 We are trying to reduce the time by 20% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

For problems below, use the information in the following table.

Processor	Clock Rate	No. instructions	Time
P1	1.5 GHz	30×10^9	12 s
P2	2 GHz	40×10^9	10 s
P3	4 GHz	90×10^9	8 s
P4	3 GHz	60×10^9	6 s

1-4 Find the IPC(instruction per cycle) for each processor.

1-5 Find the clock rate for P1 that reduces its execution time to that of P3.

1-6 Find the number of instructions for P2 that reduces its execution time to that of P4.

2. Consider three different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table.**(30pts)**

	Clock Rate	**CPI Class A**	**CPI Class B**	**CPI Class C**	**CPI Class D**
P1	2 GHz	1	2	3	4
P2	3 GHz	2	2	2	2
P3	4 GHz	2	1	3	1

2-1 Given a program with 10^9 instructions divided into classes as follows: 30% class A, 20% class B, 40% class C and 10% class D, which implementation is faster?

2-2 What is the global CPI for each implementation?

2-3 Find the clock cycles required for all three cases.

The following table shows the number of instructions for a program

Arith	**Store**	**Load**	**Branch**	**Total**
600	100	200	100	1000

2-4 Assuming that arith instructions take 2cycles, store 5cycles, load 4cycle, and branch 3cycles, what is the execution time of the program in a 4GHz processor?

2-5 Find the CPI for the program.

2-6 If the number of load instructions can be reduced by on-half, what is the speed-up and the CPI?

3. The following table show the increase in clock rate and power of five generations of processors.**(10pts)**

Processor	Clock Rate	Power	Voltage
P1	200 MHz	30 W	5
P2	500 MHz	60 W	5
P3	1 GHz	80 W	3
P4	3 GHz	100 W	2
P5	2.5 GHz	95 W	1

3-1 What is the geometric mean of the ratios between consecutive generations for both clock rate and power?

3-2 Find the average capacitive loads, assuming a negligible static power consumption

4. Suppose we have developed new versions of a processor with the following characteristics.**(15pts)**

Version	Voltage	Clock Rate
Version 1	9 V	2 GHz
Version 2	6 V	3 GHz

4-1 By how much has the dynamic power been reduced if the capacitive load does not change?

4-2 Assuming that the capacitive load of version 2 is 60% the capacitive load of version 1, find the voltage for version 2 if the dynamic power of version 2 is reduced by 20% from version 1

Supposing that the industry trends show that a new process generation scales as follows

Capacitance	Voltage	Clock Rate	Area
1.5	$1/2^{-1/5}$	$2^{2/5}$	$2^{-1/3}$

4-3 By what factor does the dynamic power scales?

5. The following table shows manufacturing data for a processor.**(10pts)**

Wafer Diameter	Dies Per Wafer	Defects per unit area	Cost per Wafer
20	100	0.025 defects/cm^2	20

5-1 If the number of dies per wafer is increased by 20% and the defects per area unit increased by 30%, find the die area and yield.

(Calculate π as 3)