Homework #5

Course: CSE4010-01 Computer Architecture

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May 26, 2021

1. Submission

- Submission Deadline: **June 1, 2021, 11:59 pm (Submit at Cyber Campus)** (20% deduction per day. No credit after 3days)
- Write solving processes and answers on a blank white paper, scan it and submit it as a **PDF file.**
- The filename should be **HW5_STUDENT-ID_NAME.pdf**

  (ex. HW5_20219999_홍길동.pdf)
- **WARNING**:
  - Students who copy other's homework will get zero point for this assignment.
  - Submission without any solving processes will get zero points.
  - Submission with another form rather than pdf will have a 3 points reduction of the total score.
  - Submission with the wrong file name will have 3 points reduction of total score.
  - Before submission, please check whether your solving processes and answers are clear enough to read. (No credit will be given if your work is illegible)
  - All works must be hand-written.(50% reduction for typed submissions)

2. Reference

- Lecture notes

- Patterson and Hennessy, Computer Organization and Design 4th (ARM Edition), Morgan Kaufmann, 2010

1. Assume that main memory accesses take 70ns and that memory accesses are 36% of all instructions. The following table shows data for L1 caches attached to each of two processors, P1 and P2. **(25pts)**

	L1 size	**L1 miss rate**	**L1 hit time**
P1	8KB	4.3%	0.96ns
P2	16KB	3.4%	1.08ns

1-1 Assuming that the L1 hit time determines the cycle times for P1 and P2, what are their respective clock rates?

1-2 What is the AMAT(Average Memory Access Time) for each of P1 and P2?

1-3 Assuming a base CPI of 1.0, what is the total CPI for each of P1 and P2? Which processor is faster?

2. For a direct-mapped cache design with 32-bit address, the following bits of the address are used to access the cache**.(10pts)**

Tag	**Index**	**Offset**
31-12	11-15	4-0

2-1 What is the cache line size (in words)?

2-2 How many entries does the cache have?

3. Calculate the improvement in performance of interleaving compared to 1, 2, and 4 word block size.**(25pts)**

Block size		1 word
Memory bandwidth		1 word
Miss rate (at each block size)	1 word	25%
	2 words	15%
	4 words	10%
Memory access per instruction		1.2
Cache miss penalty		8
CPI(without cache miss)		2
Basic memory organization - 1 cycle for send address - 6 cycles for access time/word - 1 cycle to send a word of data		

3-1 What is CPI for base machine using one word block?

Assuming that block size is increased up to 2,

3-2 What is CPI for CPI with interleaving?

3-3 What is CPI for CPI without interleaving?

Assuming that block size is increased up to 4,

3-4 What is CPI for CPI with interleaving?

3-5 What is CPI for CPI without interleaving?

4. A direct mapped cache was designed with 8 blocks and 1 word/block. **(20pts)**

4-1 When this cache is used, fill the blanks in the below table.

Word Address	Binary Address	Hit/Miss	Cache block
22			
26			
22			
26			
16			
3			
16			
18			

4-2 What will be the shape of cache after completion of 4-1?

Index	Valid	Tag	Data
000			
001			
010			
011			
100			
101			
110			
111			

5. Assume that the miss rate of an instruction cache is 2% and the miss rate of the data cache is 4%. If a processor has a CPI of 2 without any memory stalls and the miss penalty is 100 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. (Assume that the frequency of all loads and stress is 36%) **(10pts)**

6. For the below conditions, how much faster $CPU_{time\ with\ ideal\ cache}$ than $CPU_{time\ with\ stall}$? **(10pts).**

- I-cache miss rate = 3%
- D-cache miss rate = 5%
- Miss penalty = 120 cycles for all misses
- Base CPI (ideal cache) = 2
- Load & Store are 40% of instructions