I. synchronous sequential circuits are governed by clock signals.

However, Asynchronous sequential circuits aren't driven by clock, they're governed by time-delay devil

In Short, Synchronous Soquential system's state is updated at discrete times.

Asynchronous Sequential System's state is updated at any time.

2.

B.(a) 101110010001011. → 508B

3.

4.

$$(c) 0 = 0000002$$

(e) 6-bit two's complement termet's range is 32~31. out of range.

5.

6.

(e)
$$5um = 110010$$
 $(-26+12=-14)$

7,

abc	be	b'c)	ac]	手	(atc)	(a'+b+c')	9
000	0	0	0	0	0	1	0
001	0	1	0	1	1	1	1
010	1	ь	10	1	0	1	0
011	0	0	0	0	1	1	1
100	0	O	0	10	1	1	1
101	0	1	11	11	1	0	0
110	1	0	0	1.	1	1	1
111	0	0	1	1	1	'	1

(b) f=ab+ac'+a'bd' g= ad'ta'kta'bd'

abcd	06	00	0,99,	4	09,	abc	a'bd'	9
0000	0	0	0	D	0	0	0	0
0001	0	6	10	0	0	0	0	0
0010	0	0	0	10	0	0	0	0
0011	0	0	0	0	0	0	0	ь
0100	1	0	1	1	0	0	1	1
0101	1	0	0	1	0	0	0	0
0110	1	0	1	1	0	1	1	1
0111	1	0	0	1	0	I	0	1
	0	1	0	1	1	0	0	1
	0	1	0	1	0	0	0	0
	0	0	0	0	1	0	0	1
	0	0	0	0	1000		0	0
1011					0	0	0	1
1100	0	1	0	-	13		-	0
11 01	0	1	0	1	0	0	0	
7.01					1	0	0	1
11 10	0	0	٥	0	10	D	0	0
1111	0	0	0	0	, 0			

8.

EN 2,5 + 27,5 + 275

= 12+ 755 + 759

2/2+27 (y'+y) (pistributive Law)

= 12+ 22.1

5 (x+'x)

1.7

(commutative Law)

(x+x'=1)

(Distributive Law)

(X+ X' = 1)

(b) x'y'z' +x'y'z+ xy'z+ xyż

= 214 (5+2) + xyz + xyz (5+x) (6)

(1='x+x) '5ex +5'ex + 10'E'x =

= y'x' + y'xz+ xyz' (commutative

= y'(x'+xz)+xyz' (distributive

= " (x+x) (2+x)) +x12

(distributive Law Y+Y2=(X+Y)(AZ)

= y'.1.(x'+2)+ xy2)

= y'(x'+2) + xy2'

(x+y+z) (x+y+z') (x+y+z) (x+y+z')

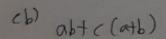
=> x +y ... redundancy law (AVB) (A+B) (A+B) =A

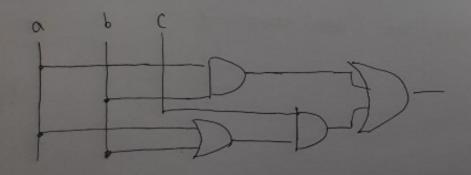
('5+'b+k)(5+, (htt) (htt)

b x+y' ... redundancy law (A+B)(A+B')=A

('etx) (etx) .:

= 2 ... redundarcy law (AHB) (A+B')=A





10

(a)

(6)

sine X·X' = 0 ,

= a'b'c' ta'c'd + abd +6c'd+ ab'c+ acd