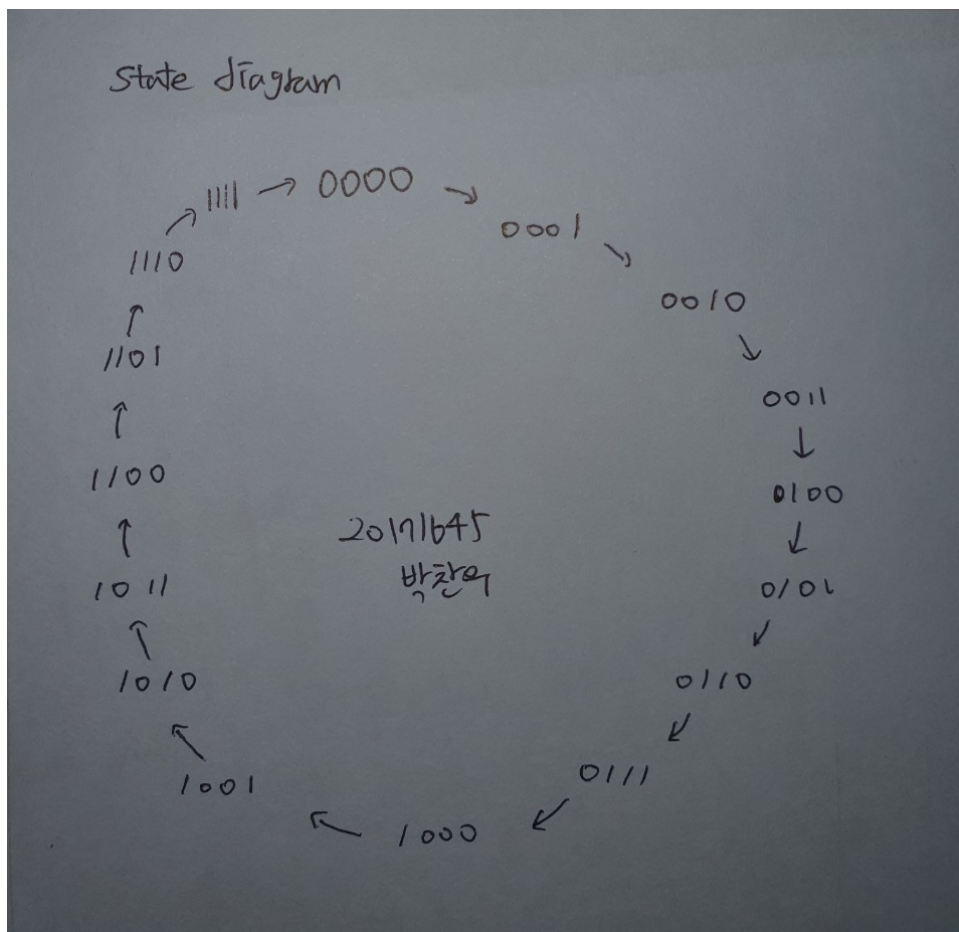


State diagram



Excitation Table of D flip-flop

Excitation table

D flip-flop

Q	Q _{next}	D
0	0	0
0	1	1
1	0	0
1	1	1

From this excitation table,
 State Table of synchronous counter using
 D flip-flops is

DCBA	D'C'B'A'	Dd	Dc	Db	Da
0000	0001	0	0	0	1
0001	0010	0	0	1	0
0010	0011	0	0	1	1
0011	0100	0	1	0	0
0100	0101	0	1	0	1
0101	0110	0	1	1	0
0110	0111	0	1	1	1
0111	1000	1	0	0	0
1000	1001	1	0	0	1
1001	1010	1	0	1	0
1010	1011	1	0	1	1
1011	1100	1	1	0	0
1100	1101	1	1	0	1
1101	1110	1	1	1	0
1110	1111	1	1	1	1
1111	0000	0	0	0	0

From this table, get Karnaugh Map

Karna map

$D_d \backslash BA$	00	01	11	10
DC				
00	0	0	0	0
01	0	0	1	0
11	1	1	0	1
10	1	1	1	1

$D_c \backslash BA$	00	01	11	10
DC				
00	0	0	1	0
01	1	1	0	1
11	1	1	0	1
10	0	0	1	0

$D_b \backslash BA$	00	01	11	10
DC				
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$D_a \backslash BA$	00	01	11	10
DC				
00	1	0	0	1
01	1	0	0	1
11	1	0	0	1
10	1	0	0	1

So

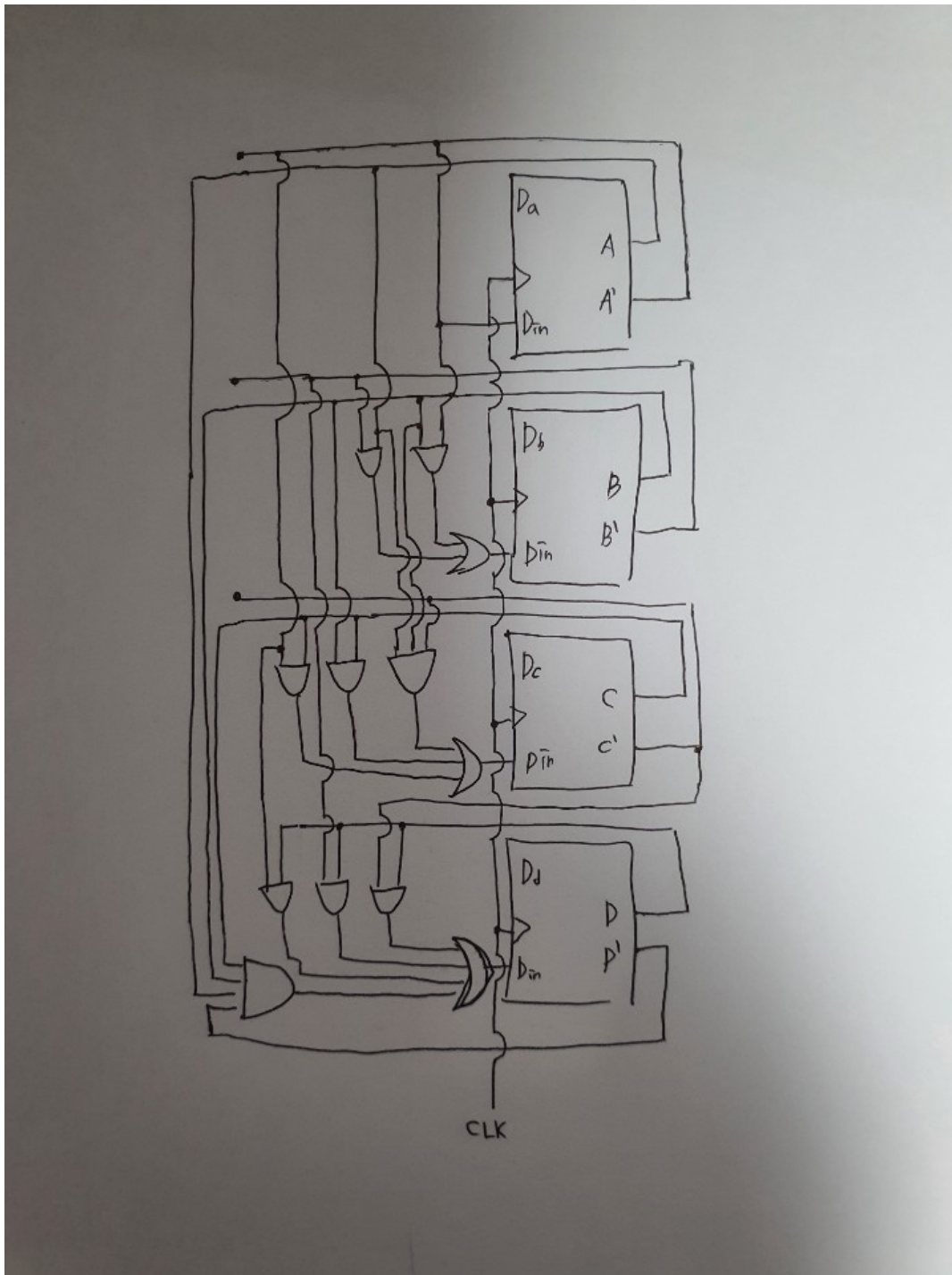
$$D_d = DC' + DB' + DA' + D' CBA$$

$$D_c = CB' + CA' + C'BA$$

$$D_b = B'A + BA'$$

$$D_a = A'$$

draw Circuit Diagram



Redesign with JK flip-flops. State Diagram is same as before, and Excitation table of JK flip-flop is

Execution table
JK Flip-Flop

Q	Q _{next}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Karnaugh map

so State Table of synchronous counter using JK flip-flops is

DCBA	D'C'B'A'	Jd	Kd	Jc	Kc	Jb	Kb	Ja	Ka
0000	0001	0	x	0	x	0	x	1	x
0001	0010	0	x	0	x	1	x	x	1
0010	0011	0	x	0	x	x	0	1	x
0011	0100	0	x	1	x	x	1	x	1
0100	0101	0	x	x	0	0	x	1	x
0101	0110	0	x	x	0	1	x	x	1
0110	0111	0	x	x	0	x	0	1	x
0111	1000	1	x	x	1	x	1	x	1
1000	1001	x	0	0	x	0	x	1	x
1001	1010	x	0	0	x	1	x	x	1
1010	1011	x	0	0	x	x	0	1	x
1011	1100	x	0	1	x	x	1	x	1
1100	1101	x	0	x	0	0	x	1	x
1101	1110	x	0	x	0	1	x	x	1
1110	1111	x	0	x	0	x	0	1	x
1111	0000	x	1	x	1	x	1	x	1

by this table, get Karnaugh map

Karna map

$$J_d$$

$DC \backslash BA$	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	x	x	x	x
10	x	x	x	x

$$J_d = CBA$$

$$K_d$$

$DC \backslash BA$	00	01	11	10
00	x	x	x	x
01	x	x	1	x
11	0	0	1	0
10	0	0	0	0

$$K_d = CBA$$

$$J_c$$

$DC \backslash BA$	00	01	11	10
00	0	0	1	0
01	x	x	x	x
11	x	x	x	x
10	0	0	1	0

$$J_c = BA$$

$$K_c$$

$DC \backslash BA$	00	01	11	10
00	x	x	x	x
01	0	0	1	0
11	0	0	1	0
10	x	x	x	x

$$K_c = BA$$

$$J_b$$

$DC \backslash BA$	00	01	11	10
00	0	1	x	x
01	0	1	x	x
11	0	1	x	x
10	0	1	x	x

$$J_b = A$$

$$K_b$$

$DC \backslash BA$	00	01	11	10
00	x	x	1	0
01	x	x	1	0
11	x	x	1	0
10	x	x	1	0

$$K_b = A$$

$$J_a$$

$DC \backslash BA$	00	01	11	10
00	1	x	x	1
01	1	x	x	1
11	1	x	x	1
10	1	x	x	1

$$J_a = 1$$

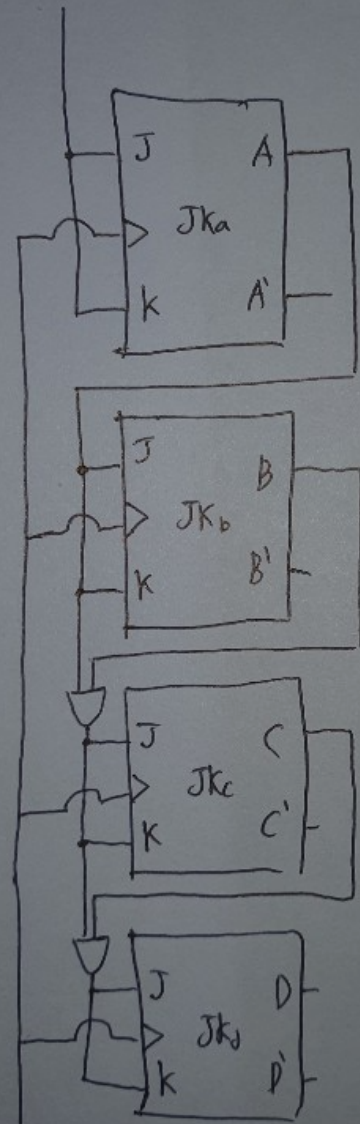
$$K_a$$

$DC \backslash BA$	00	01	11	10
00	x	1	1	x
01	x	1	1	x
11	x	1	1	x
10	x	1	1	x

$$K_a = 1$$

draw Circuit Diagram

Logic 1



CLK

Redesign with T flip-flops. State Diagram is same as before, and Excitation table of T flip-flop is

Excitation table
T flip-flop

Q	Qnext	T
0	0	0
0	1	1
1	0	1
1	1	0

so State Table of synchronous counter using T flip-flops is

DCBA	D'C'B'A'	Td	Tc	Tb	Ta
0000	0001	0	0	0	1
0001	0010	0	0	1	1
0010	0011	0	0	0	1
0011	0100	0	1	1	1
0100	0101	0	0	0	1
0101	0110	0	0	1	1
0110	0111	0	0	0	1
0111	1000	1	1	1	1
1000	1001	0	0	0	1
1001	1010	0	0	1	1
1010	1011	0	0	0	1
1011	1100	0	1	1	1
1100	1101	0	0	0	1
1101	1110	0	0	1	1
1110	1111	0	0	0	1
1111	0000	1	1	1	1

by this table, get Karnaugh map

Karna map

$$T_d$$

$D_C \backslash BA$	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	0	0	1	0
10	0	0	0	0

$$T_d = CBA$$

$$T_c$$

$D_C \backslash BA$	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	0	0	1	0
10	0	0	1	0

$$T_c = BA$$

$$T_b$$

$D_C \backslash BA$	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	0	1	1	0
10	0	1	1	0

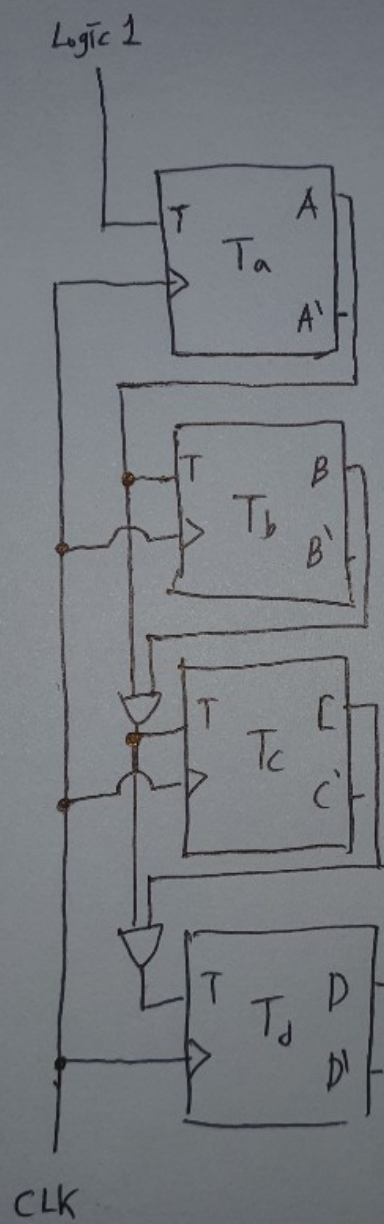
$$T_b = A$$

$$T_a$$

$D_C \backslash BA$	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$$T_a = 1$$

draw Circuit Diagram



모든 사진자료는 자필로 직접 작성했습니다.

