Graduate Thesis

Design of Gate Driver Circuit Using a-IGZO TFT for High Reliability Display System

Chan Young Park

Sung Kyun Kwan University, College of Information and Communication
Electrical and Electronic Engineering Department, NEMS

Design High Reliability Oxide TFT Gate Driver Circuit

a-IGZO TFT

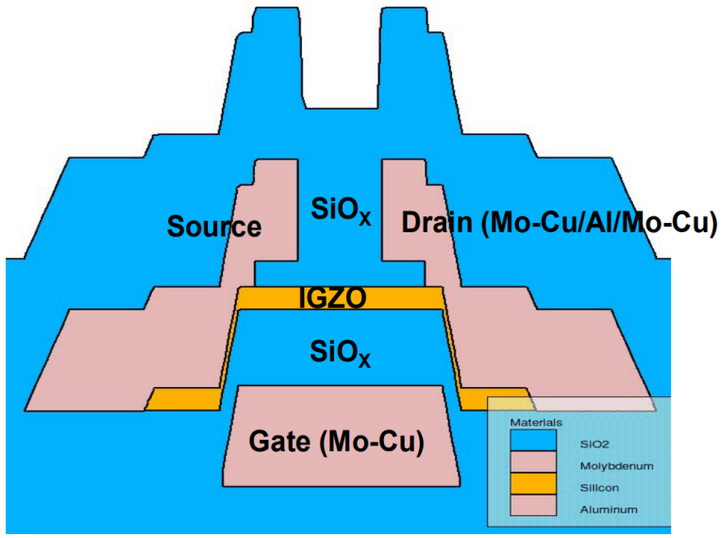
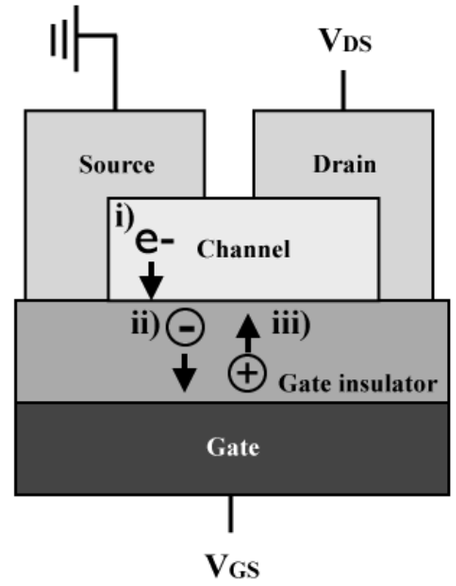
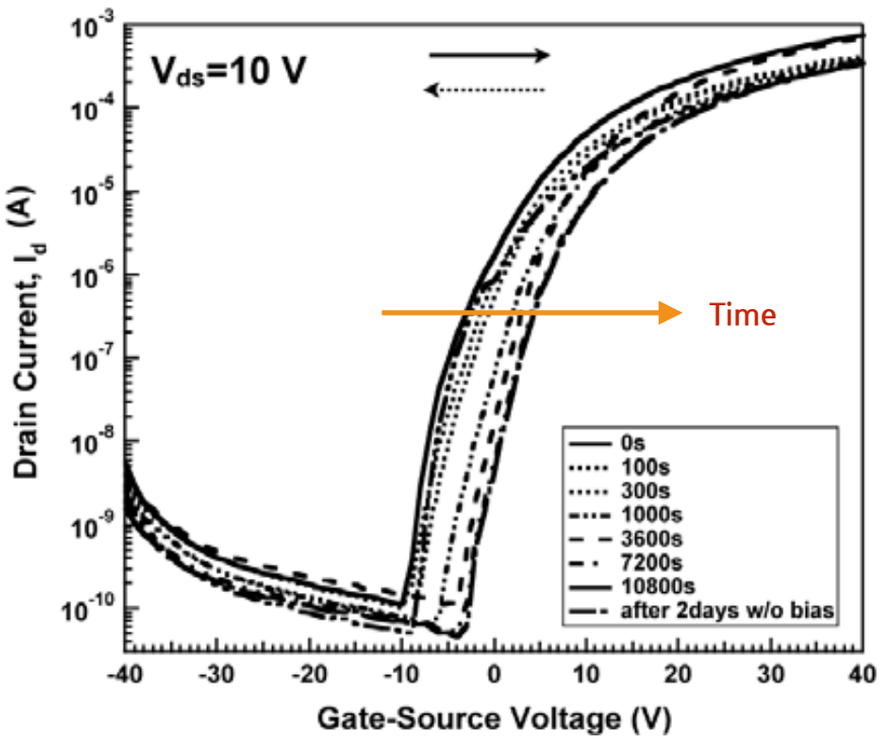


Figure shows schematic cross-sectional view of the fabricated a-IGZO TFT. The IGZO TFTs in this work have an inverted-staggered and etch-stopper structure, and are fabricated by the following steps. First, a 100 nm thick MoCu gate is patterned on a glass substrate, and then a gate insulator of 110 nm thick SiO2 is deposited by plasma-enhanced chemical vapor deposition (PECVD). Next, an active layer of a-IGZO (In:Ga:Zn = 1:1:1) whose thickness is 65nm is formed by a sputtering, and its channel area is protected by an etch-stopper layer of SiO2 to prevent the back channel from being damaged during an etching process of a-IGZO. In sequence, a source/drain of MoCu/Al/ MoCu is patterned, and then the device is passivated by 300 nm thick PECVD SiO2 and a thick organic layer consecutively. The pad size of the device is 150X300 μm^2





Cross-sectional view of an n-channel TFT subjected to a positive gate bias. Three possible instability mechanisms are indicated, all of which would lead to time-dependent **changes in V_{ON}**

Figure illustrates three type of charge migration:
(i) electron trapping at or near the channel-insulator towards the gate-insulator interface
(ii) negative ion migration within the insulator towards the gate-insulator interface
(iii) positive ion migration within the insulator towards the channel-insulator interface

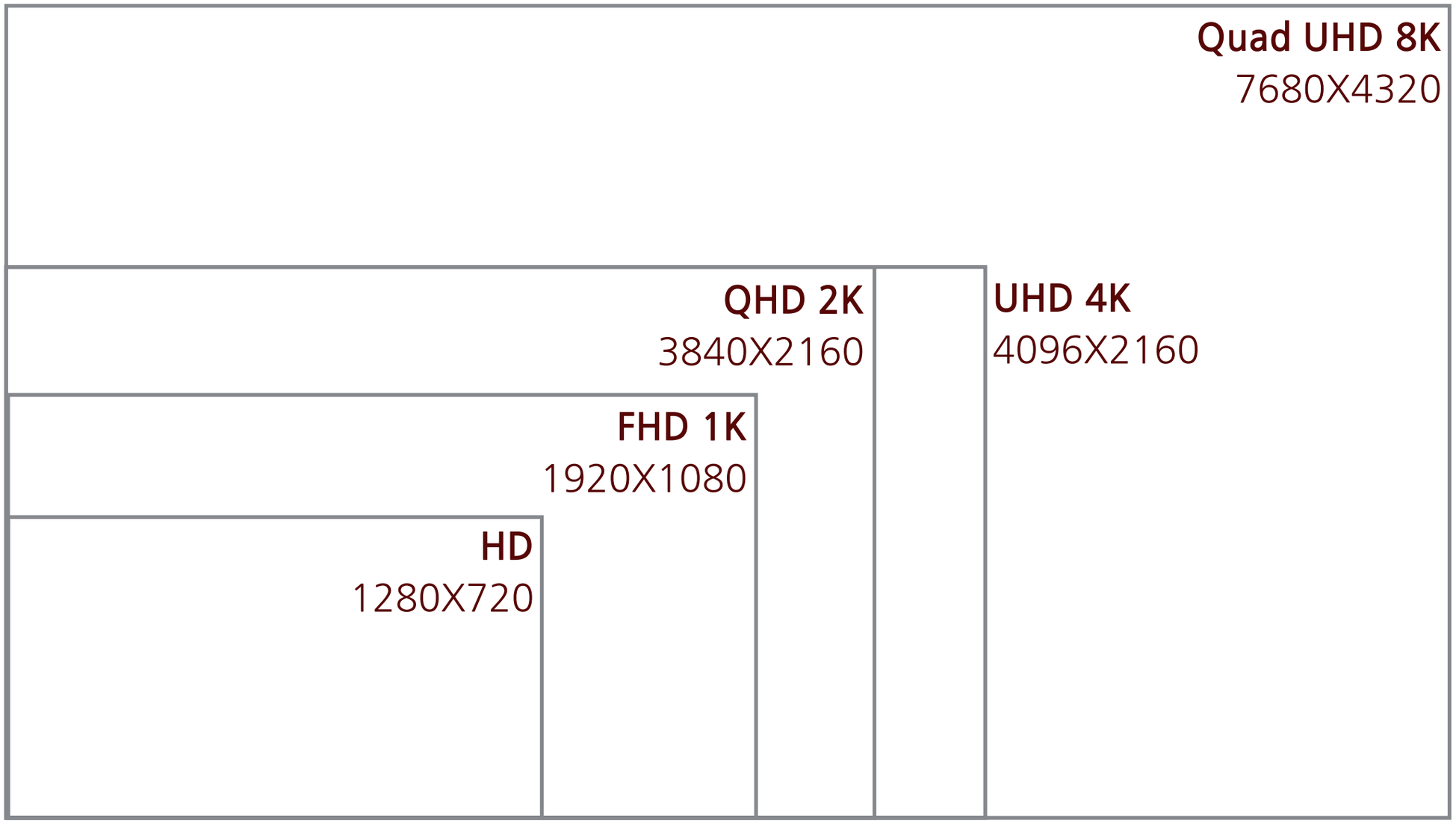
all of which could conceivably occur in an operating n-channel TFT and which would give **rise to a V_{ON} shift**.

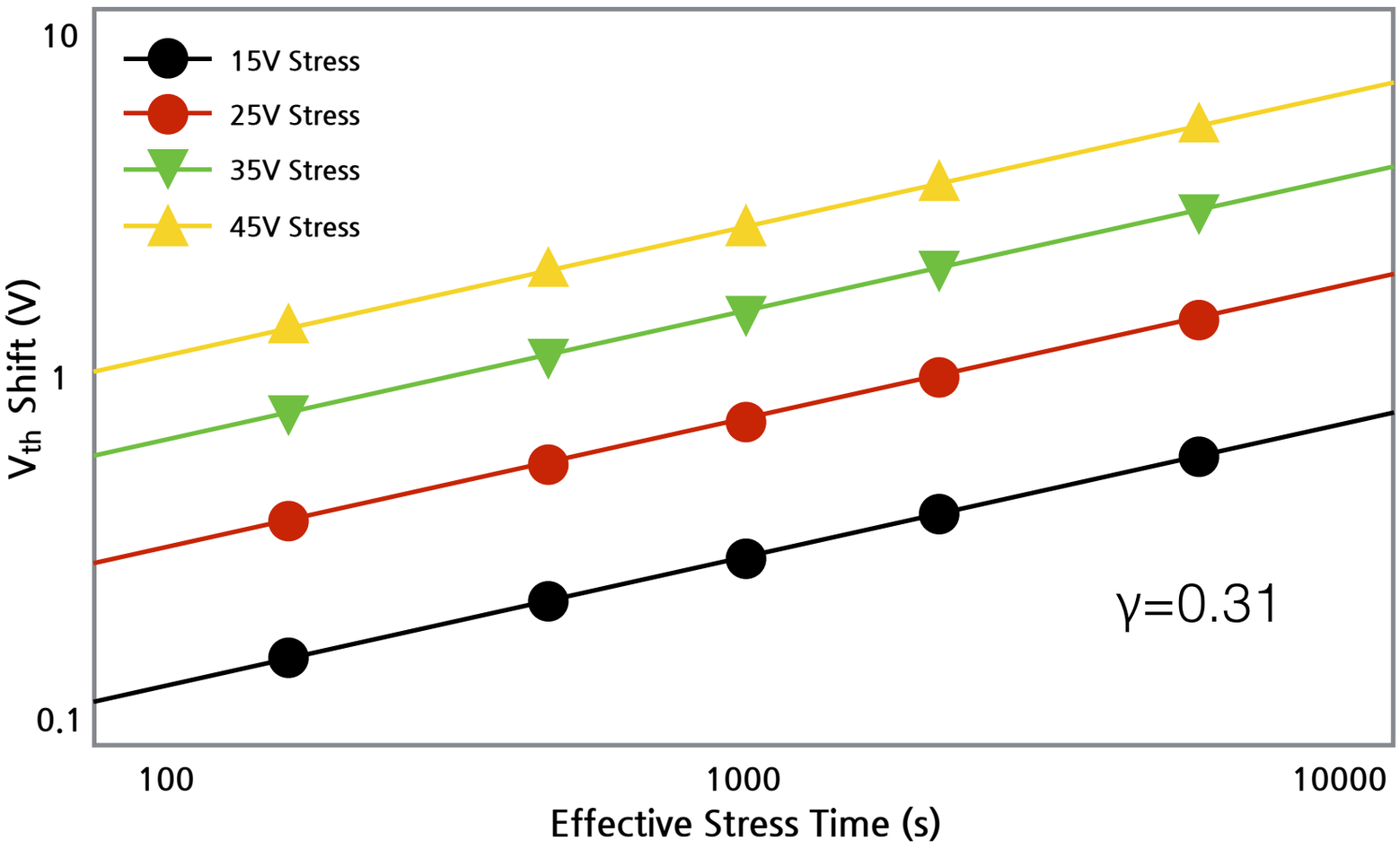
중소형 고정기기 : CRT → **TFT-LCD**

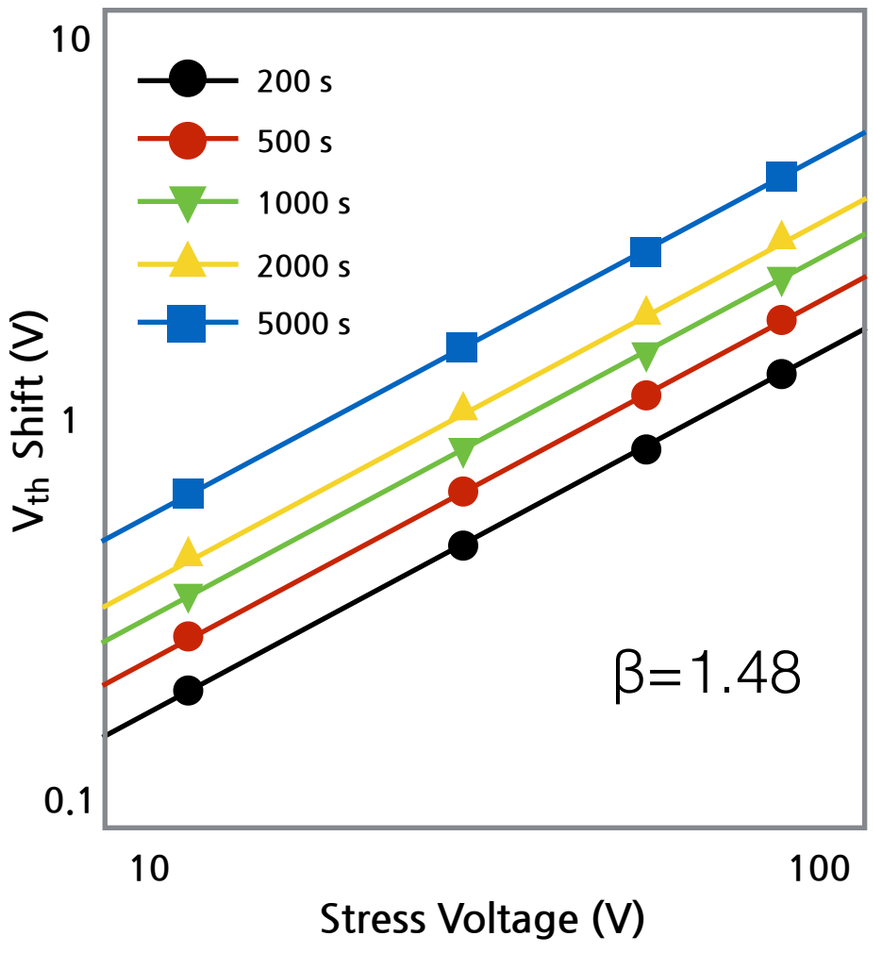
대형 고정기기 : Projection → PDP / TFT-LCD → **TFT-LCD**

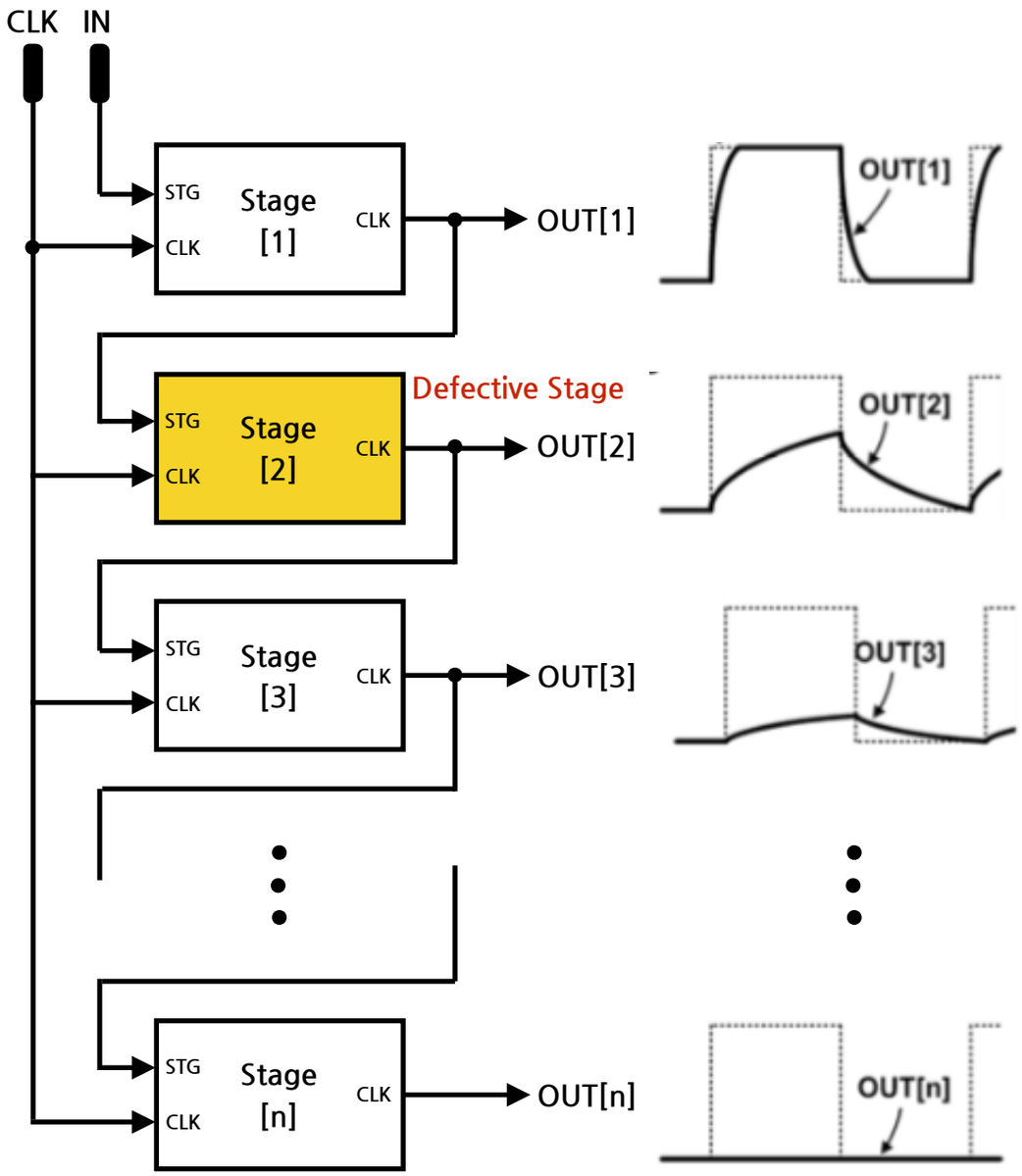
이동기기 : STN-LCD → TFT-LCD

PM-OLED → **AM-OLED** → Flexible, Foldable

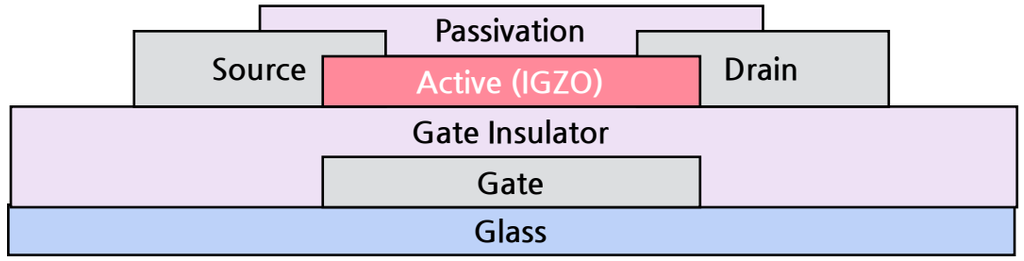


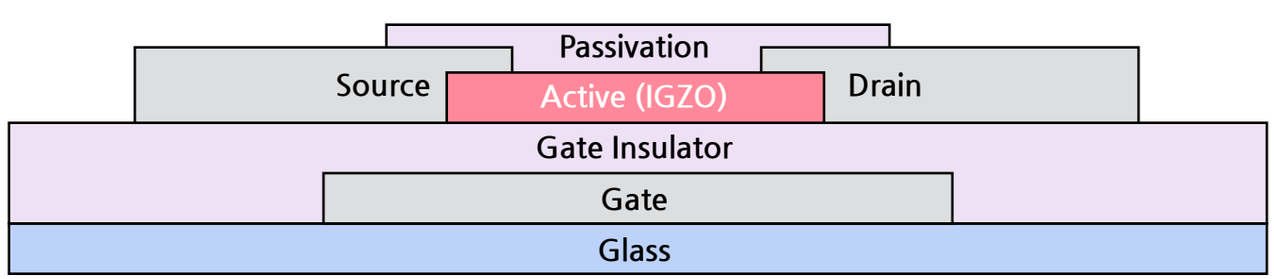

10
1
0.1
V_{th} Shift (V)
15V Stress
25V Stress
35V Stress
45V Stress
γ=0.31
100
1000
10000
Effective Stress Time (s)

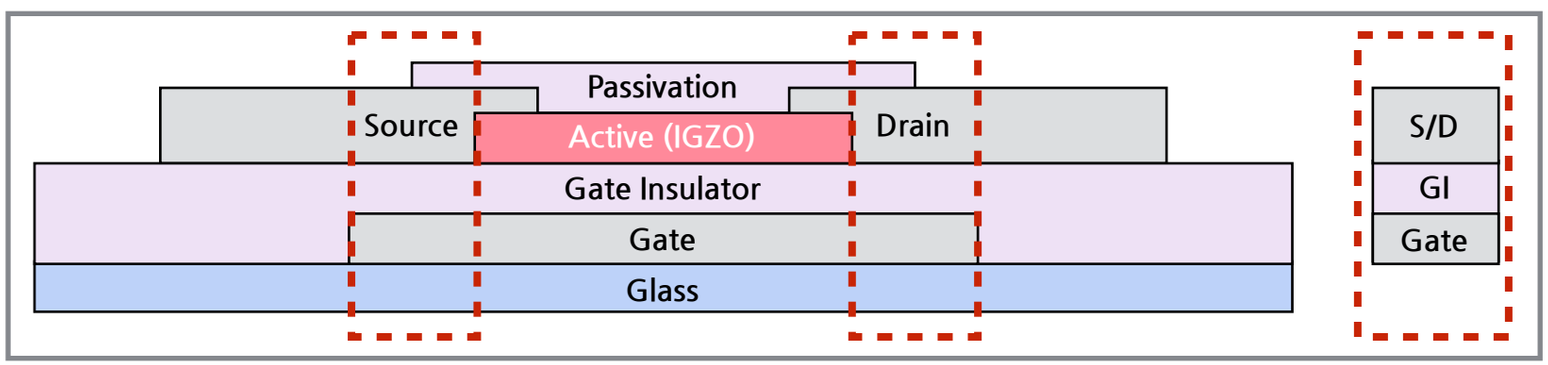

10
1
0.1
V_{th} Shift (V)
200 s
500 s
1000 s
2000 s
5000 s
β=1.48
10
100
Stress Voltage (V)


CLK
IN
STG
CLK
Stage
[1]
CLK
OUT[1]
OUT[1]
Defective Stage
STG
CLK
Stage
[2]
CLK
OUT[2]
OUT[2]
STG
CLK
Stage
[3]
CLK
OUT[3]
OUT[3]
STG
CLK
Stage
[n]
CLK
OUT[n]
OUT[n]

a-IGZO TFT

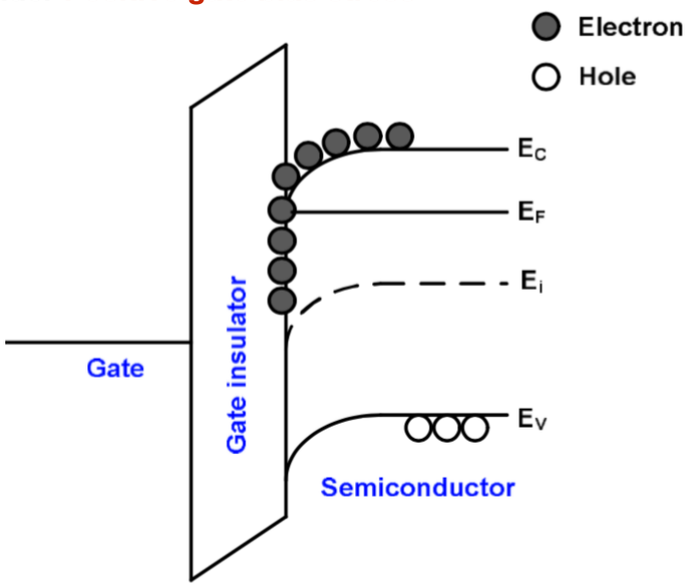

Passivation
Source
Active (IGZO)
Drain
Gate Insulator
Gate
Glass


Passivation
Source
Active (IGZO)
Drain
Gate Insulator
Gate
Glass

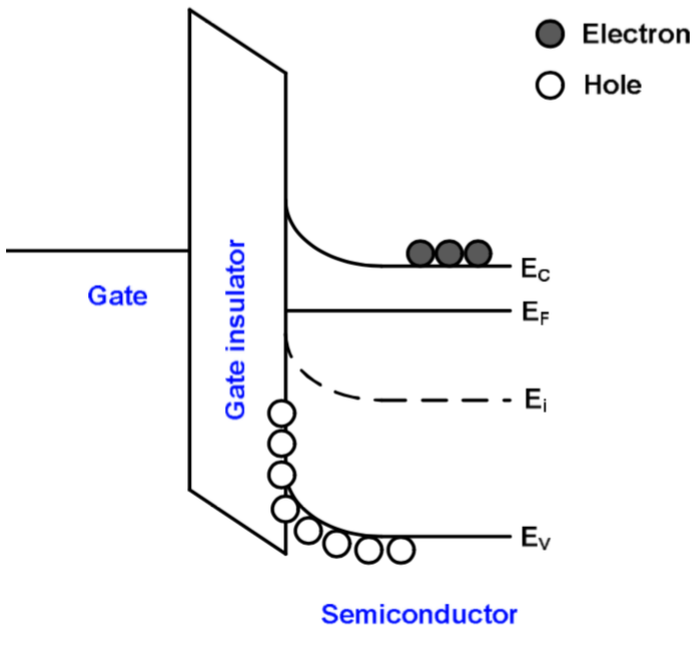

Passivation
Source
Active (IGZO)
Drain
Gate Insulator
Gate
Glass
S/D
GI
Gate

Gate Bias Stress of a-IGZO TFT

Energy band diagrams of a-IGZO TFTs under Positive gate bias stress



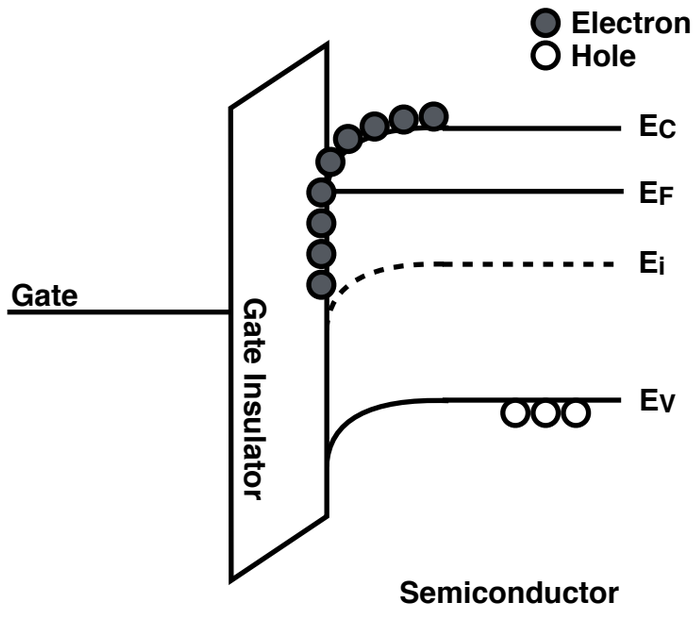
Energy band diagrams of a-IGZO TFTs under Negative gate bias stress



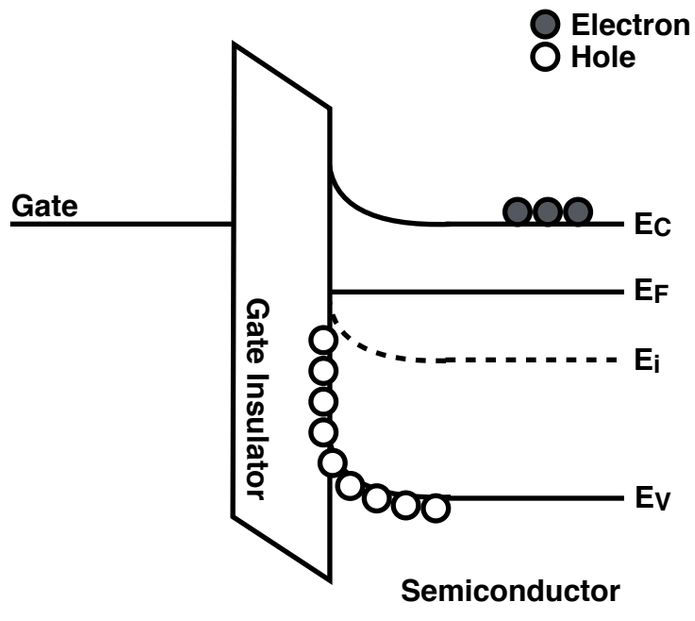
The stability of a-IGZO TFTs is an important factor to commercialize the device. However, a-IGZO TFTs exhibit instability characteristics in positive gate bias stress and negative gate bias stress. Figure shows the energy band diagrams of a-IGZO TFT when each positive and negative gate bias stress is applied to the gate terminal of TFT.

Under positive gate bias stress, V_{th} of a-IGZO TFTs is shifted in the positive direction due to electron trapping at the active-layer / gate-insulator interface [1]. Similarly, V_{th} is negatively shifted during the negative gate bias stress since the instability is attributed to hole trapping at the active-layer / gate-insulator interface [2].

The degree of threshold voltage shift depends on the stress time and the voltage level applied to the gate terminal. Although a post fabrication anneal improves the degree of carrier trapping, it does not completely prevent the instability characteristic caused by high gate bias stresses in display application. Therefore, the integrated circuits using a-IGZO TFTs is carefully designed to minimize the gate bias stress of TFTs.



Energy band diagrams of a-IGZO TFTs under Positive gate bias stress

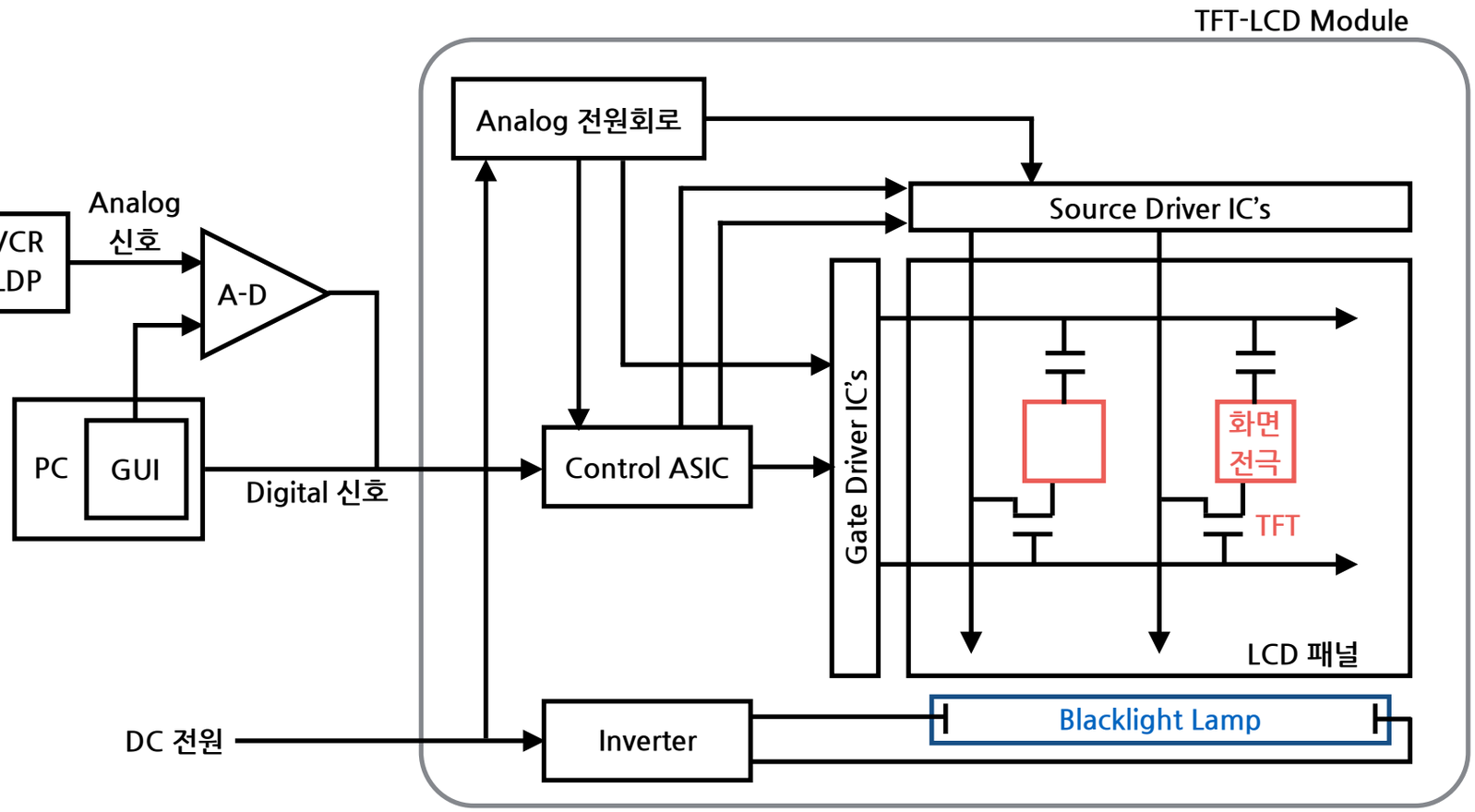


Energy band diagrams of a-IGZO TFTs under Negative gate bias stress

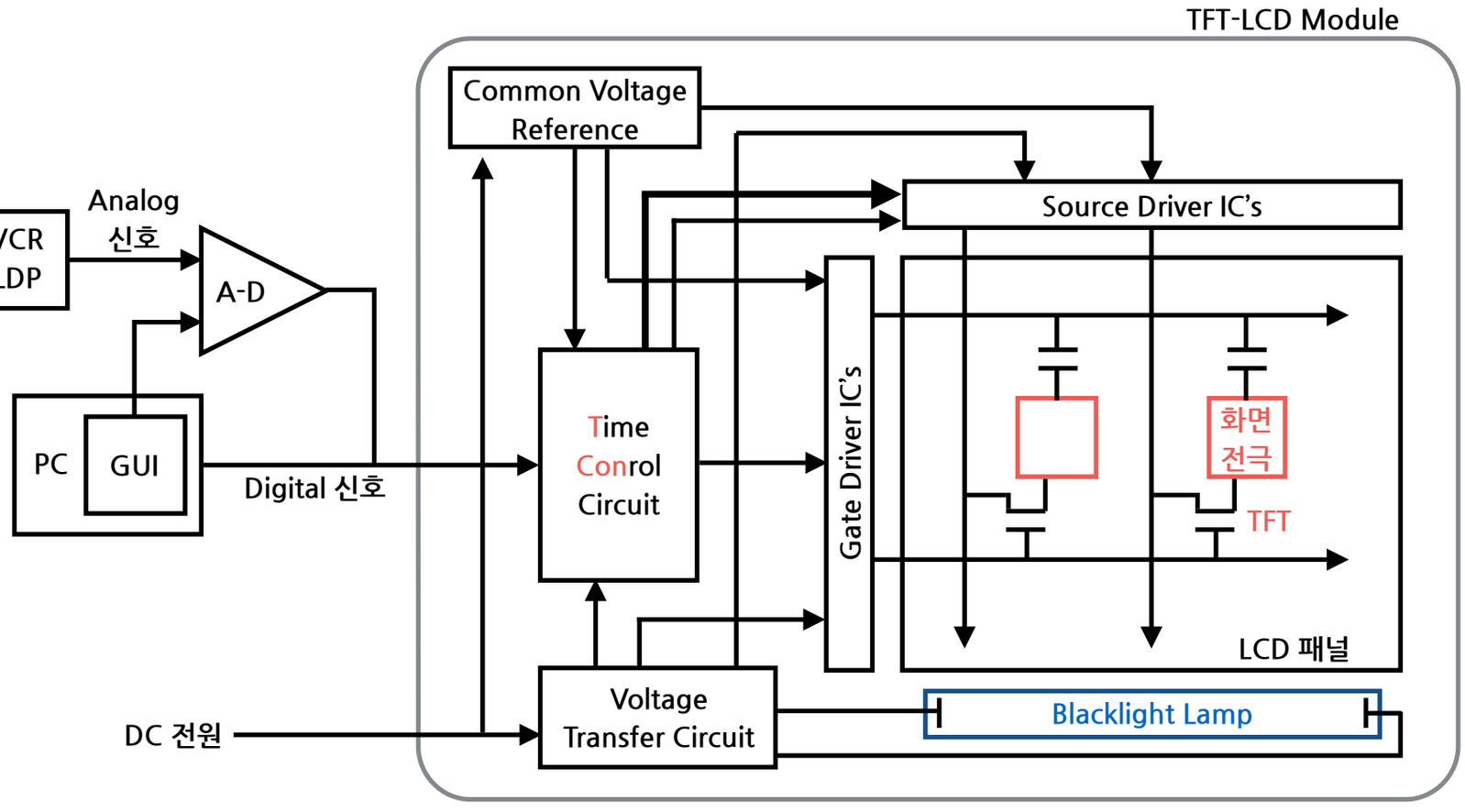
[1] M. E. Lopes, H. L. Gomes, M. C. R. Medeiros, P. Barquinha, and L. Pereira, "Gate-bias stress in amorphous oxide semiconductors thin-film transistors," Appl. Phys. Lett., vol. 95, no. 6, pp. 063502_1–063502_3. Aug. 2009.

[2] Y.S.Kim,S.C.Kim,W.J.Kim,M.Y.Bae,H.K.Jeong,D.Kong,S. Choi, D. M. Kim, and D. H. Kim, "Amorphous InGaZnO Thin-Film Transistor Part II: Modeling and Simulation of Negative Bias Illumination Stress-Induced Instability," IEEE Trans. Electron Dev., vol. 59, no. 10, pp. 2699–2706, Oct. 2012.

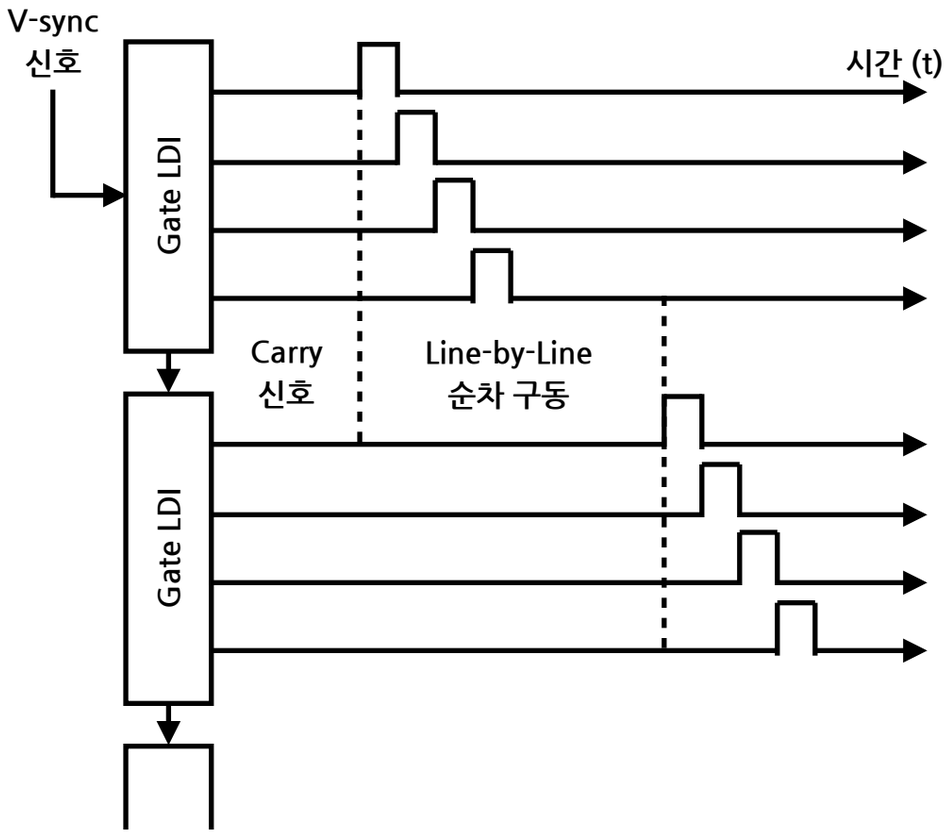
TFT-LCD System

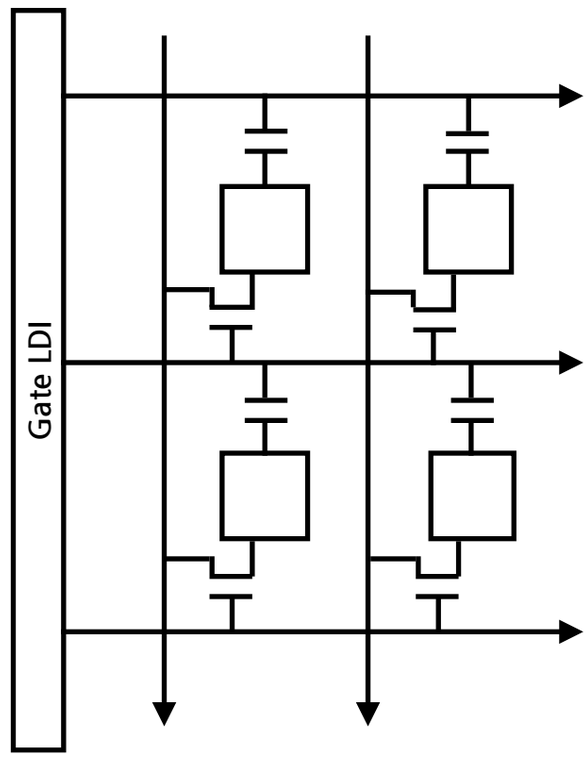


TFT-LCD System



Gate driver IC





Conventional a-Si integrated gate driver circuit

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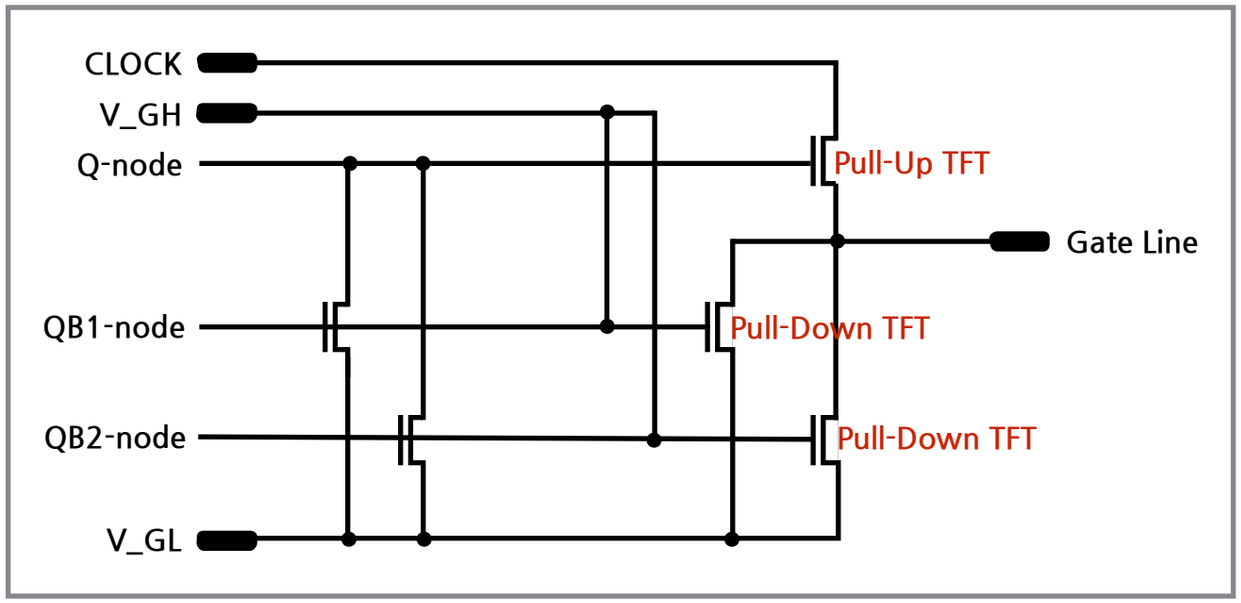
Figure shows a schematic of the conventional a-Si:H integrated gate driver circuit. The gate driver circuit consists of Q-node, QB-node, pull-up TFT, and pull-down TFT. The pull-up TFT provides high voltage to the gate line. When Q-node is high, the pull-up TFT is turned on. QB-node consistently receives high voltage to turn on the pull-down TFT that supplies low voltage to the gate line. As a result, the long-term operation of the pull-down TFT decreases, and this makes the voltage bias to the gate line insufficient. To overcome this problem, single QB-node is replaced by double QB-nodes (QB1-node and QB2-node). Using additional pull-down TFT is helpful for low less stress effect.

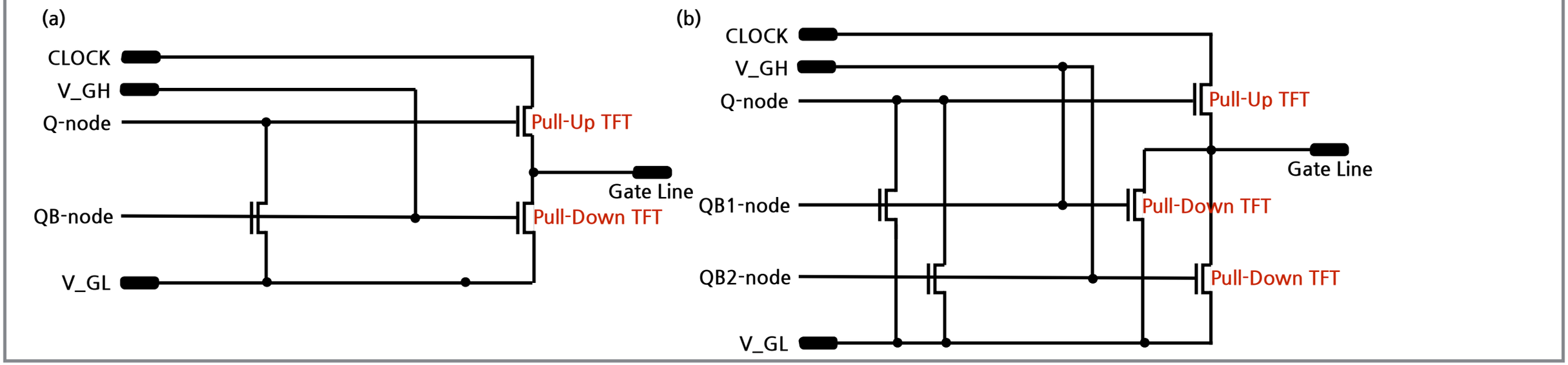


The pull-up TFT provides high voltage to the gate line.

The pull-down TFT supplies low voltage to the gate line.

When Q-node is high, the pull-up TFT is turned on.

QB-node consistently receives high voltage to turn on the pull-down TFT.


(a)
CLOCK
V_GH
Q-node
QB-node
V_GL
Pull-Up TFT
Gate Line
Pull-Down TFT
(b)
CLOCK
V_GH
Q-node
QB1-node
QB2-node
V_GL
Pull-Up TFT
Gate Line
Pull-Down TFT
Pull-Down TFT

Conventional a-Si integrated gate driver circuit

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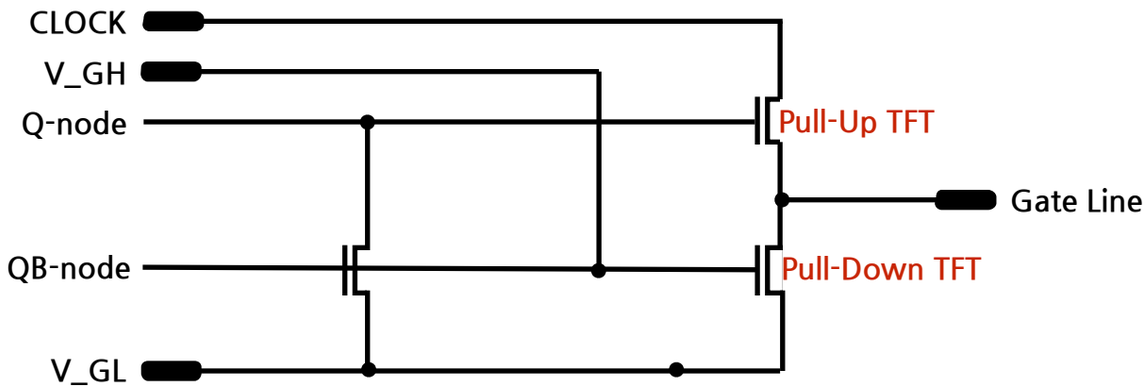

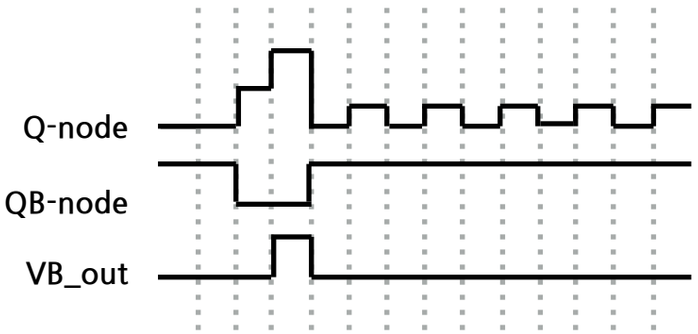

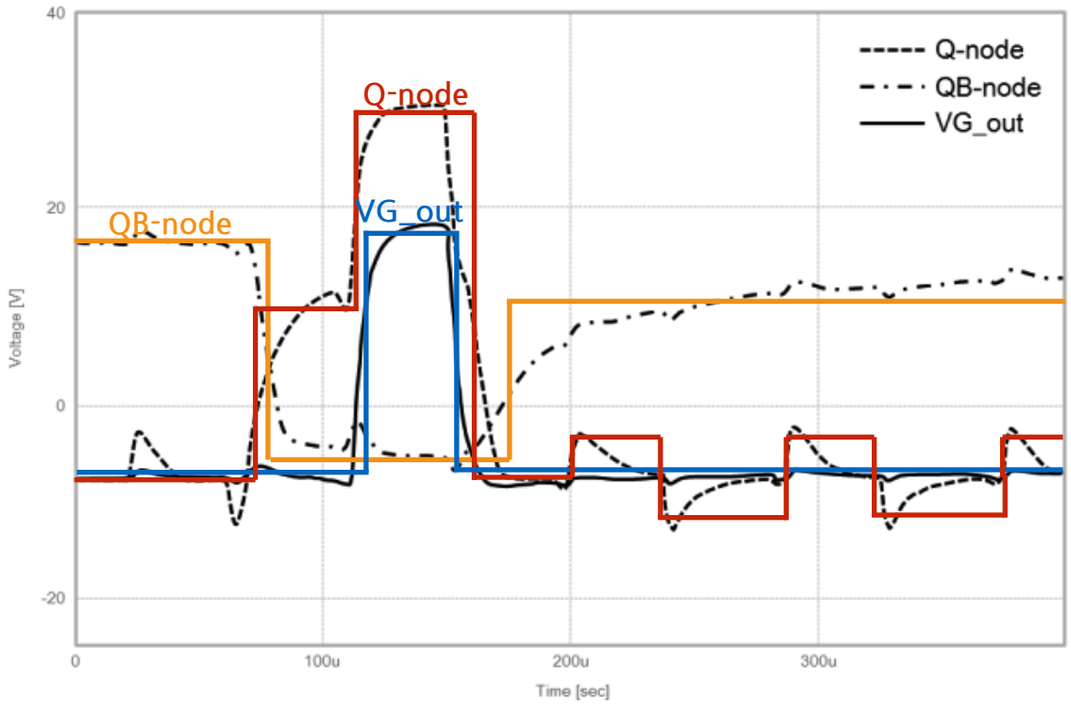

Figure illustrates simulation results of the conventional integrated circuit under the extreme condition. Figure shows the ideal gate output of t he initial state at -40’C. In compared with the simulation result of the initial state integrated circuit at -40’C, the non-ideal output of the conventional gate driver circuit at the extreme condition condition is shown in Figure. To minimize the stress of pull-down transistors, the conventional integrated circuit operating using AC driving method (double QB-nodes). However decreasing the on current of a-Si TFT by Vth shift and operating at low temperature causes the non-ideal gate output.

We fabricated 7.0 inch panel with conventional integrated circuit and evaluated the reliability of the conventional circuit under three different conditions. First, the panel operating at 95’C for 1000 hours is confirmed the normal operation. Second, the panel operating at -40’C for 1000 hours works normally. Finally, cold start test (after operating at 95’C for 1000 hours and stand-by at -40’C for 3 hours), the display panel consisting of the conventional driver circuit does not operate. Experimental results indicate the same as those in Figure.

Cont

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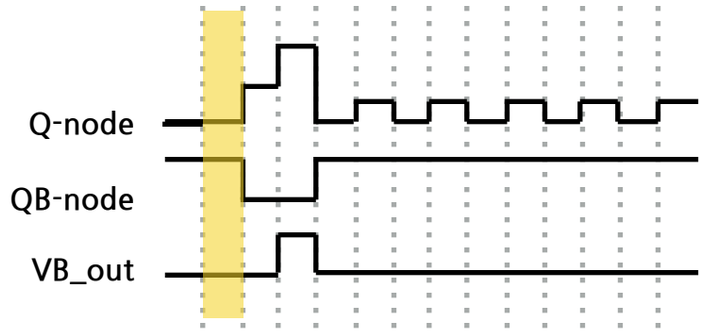

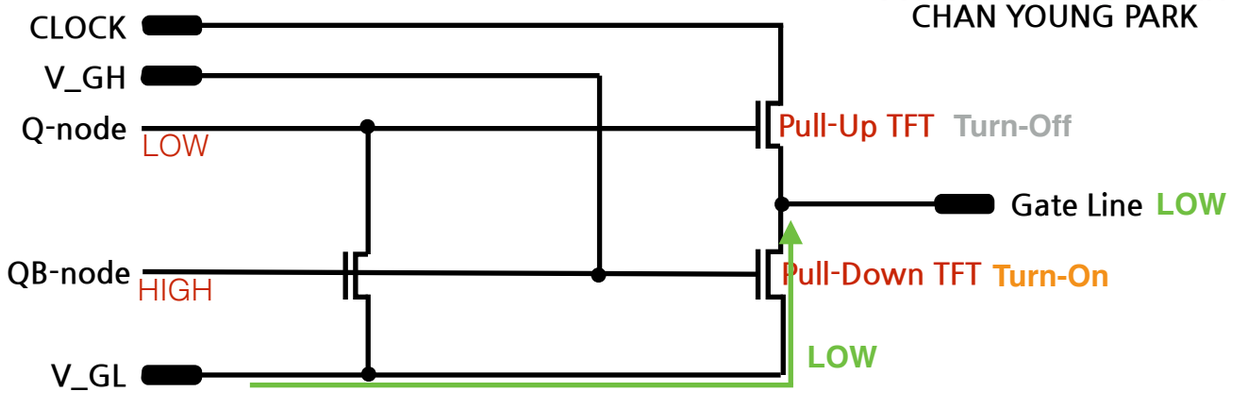

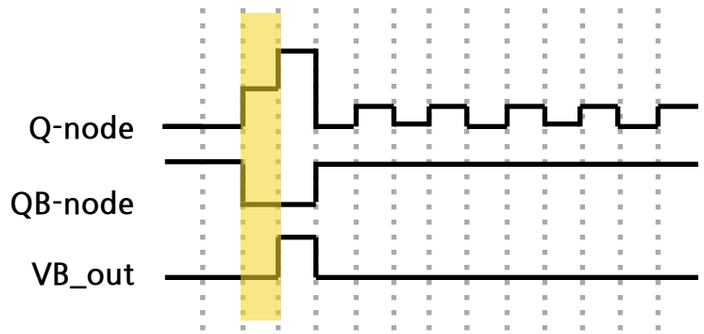

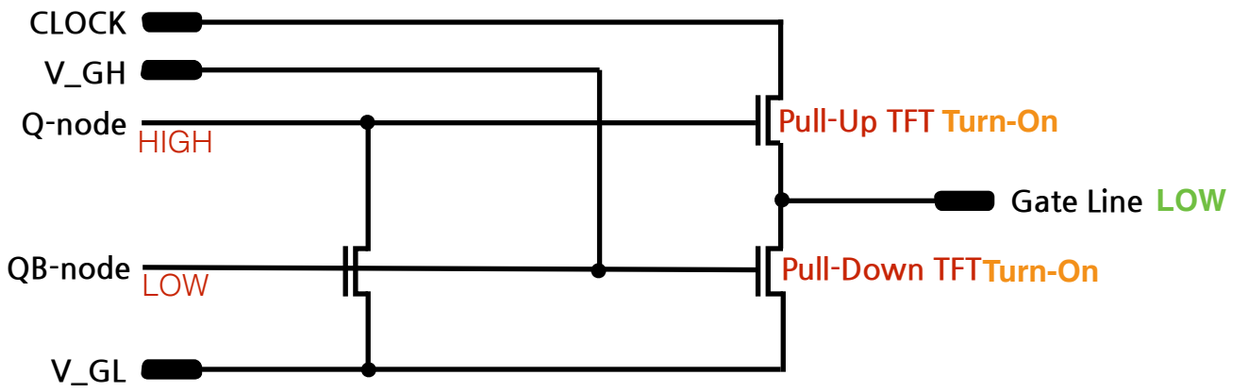

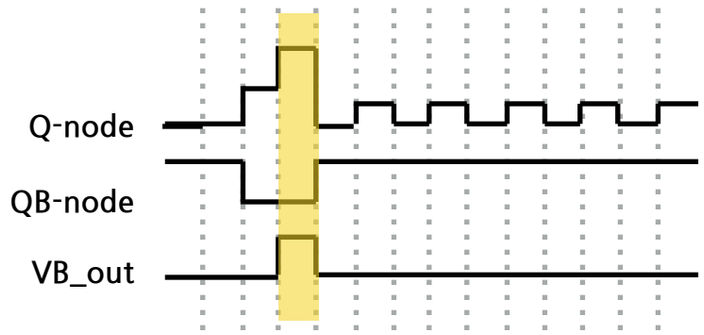

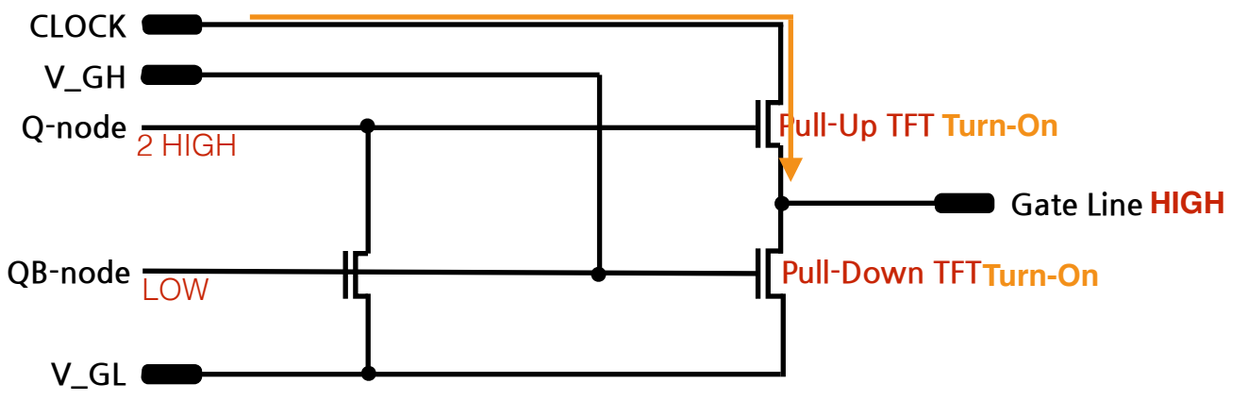

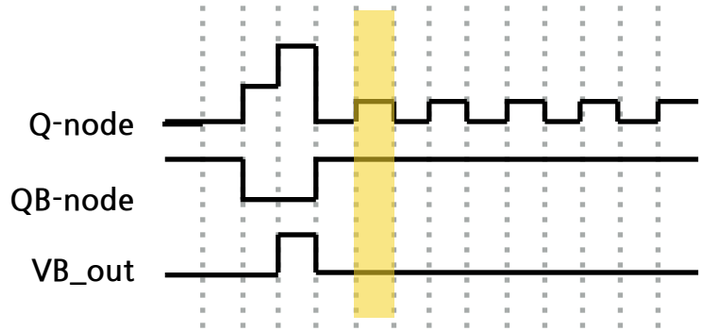

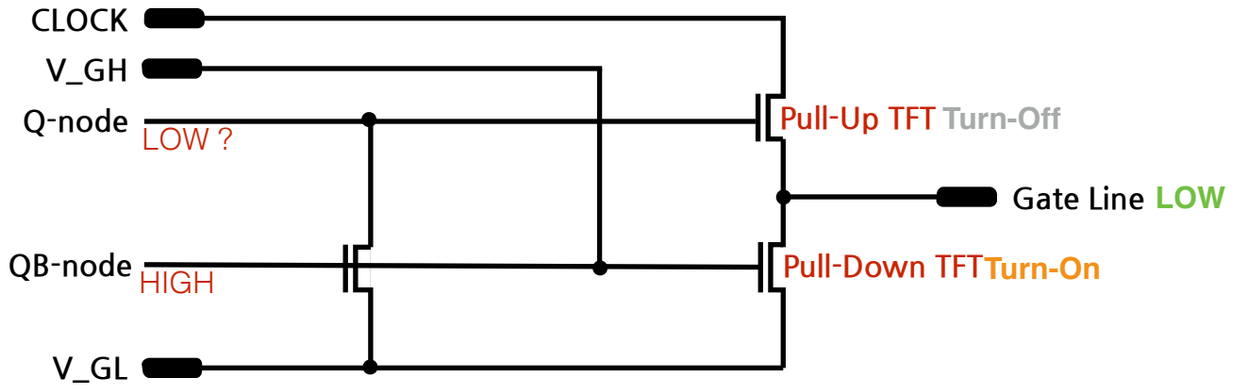

Proposed a-Si integrated gate driver circuit

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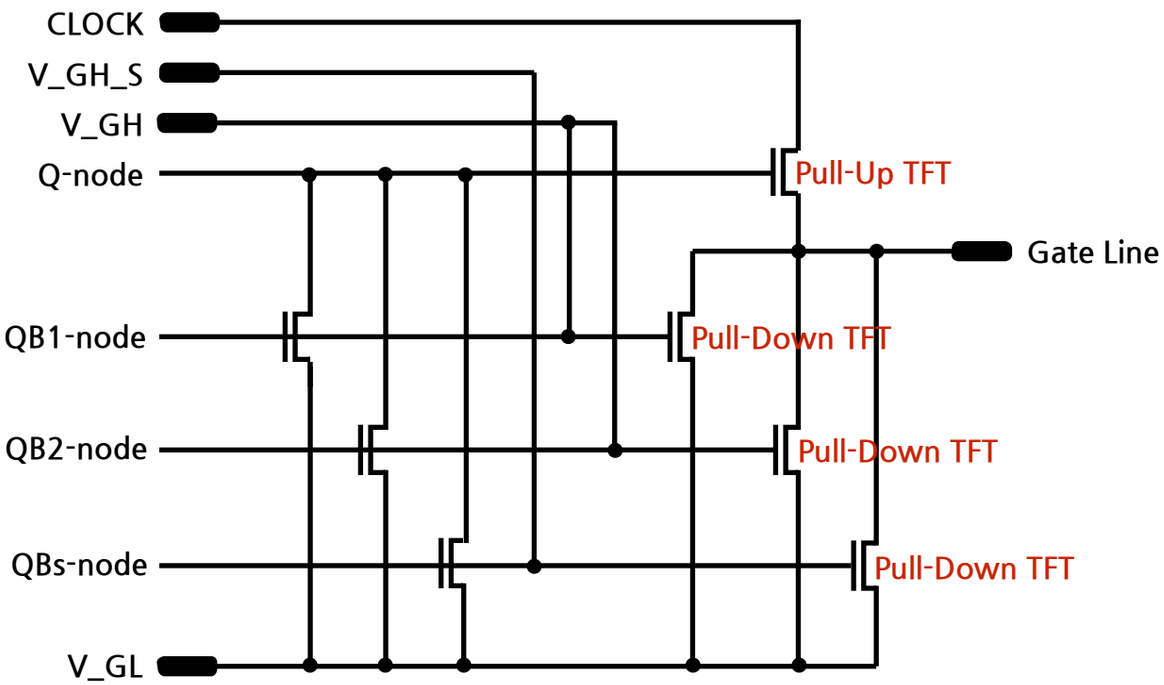
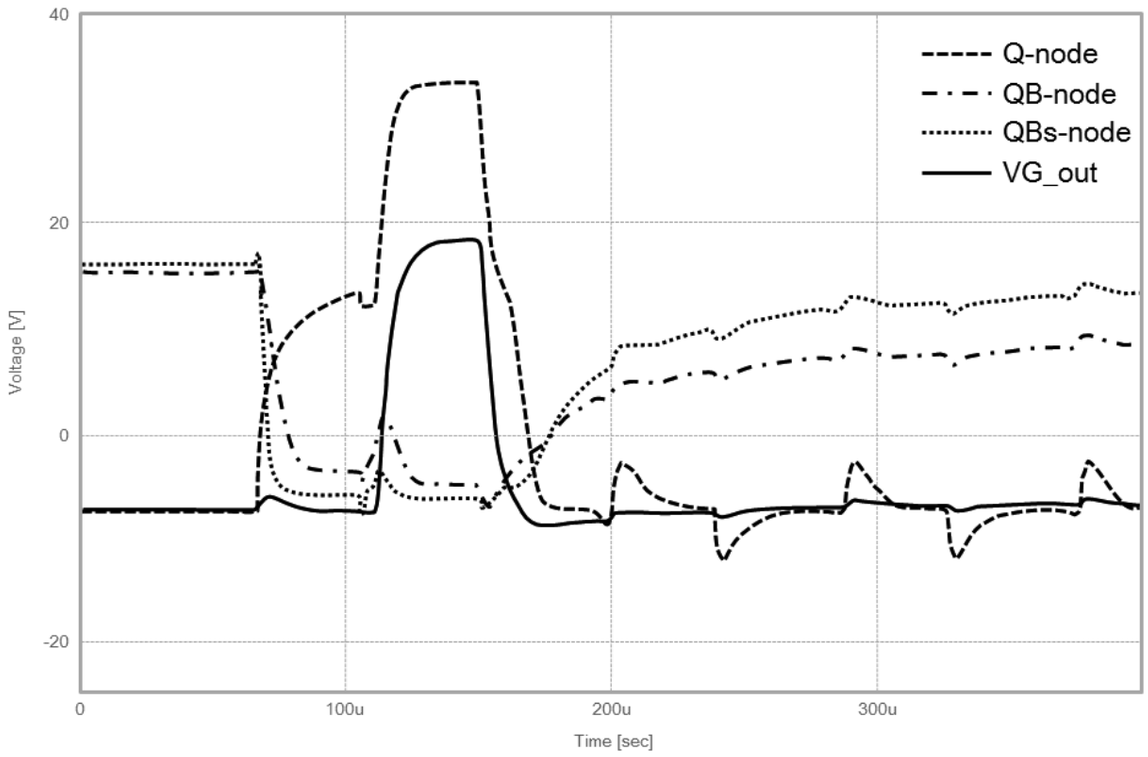
Figure is a schematic of the proposed a-Si:H integrated gate driver circuit in this study. The operation modes of QB1-node and QB2-node are identical to the conventional circuit, but QBs-node only operates at the extreme condition. The addition of the pull-down transistor connected to QBs-node is aided to compensate the bias condition under extreme environments in the entire circuit.





Conventional Gate Driver Circuit

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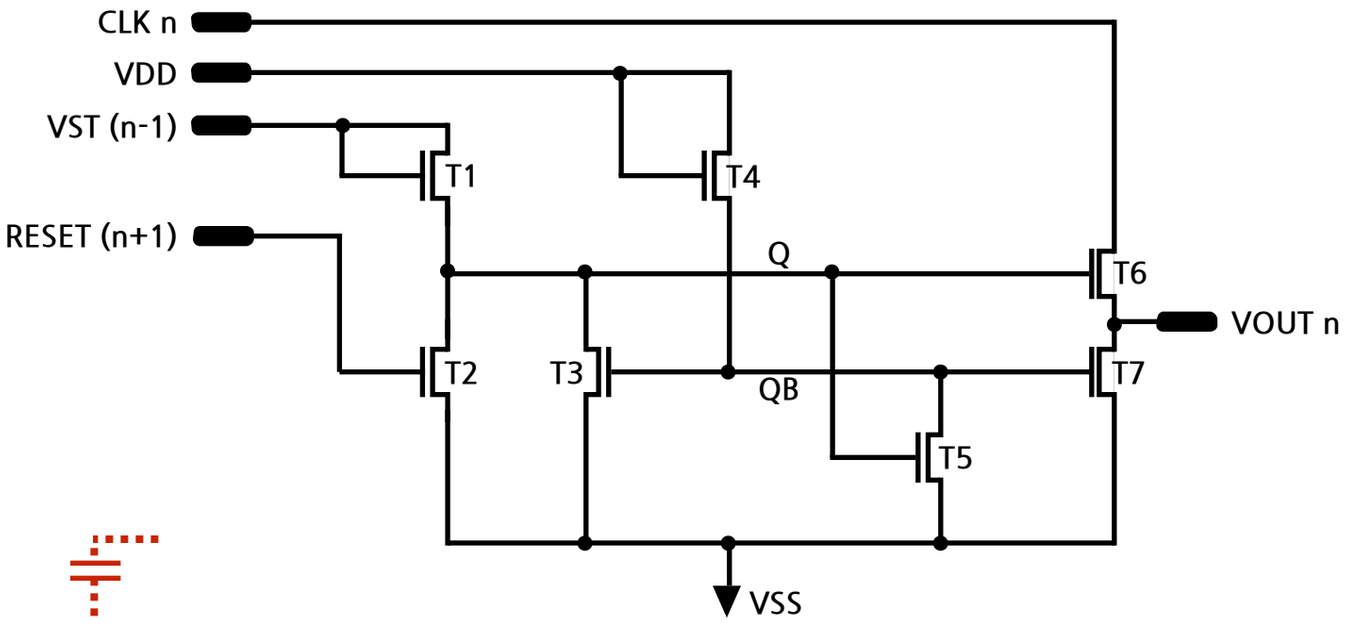

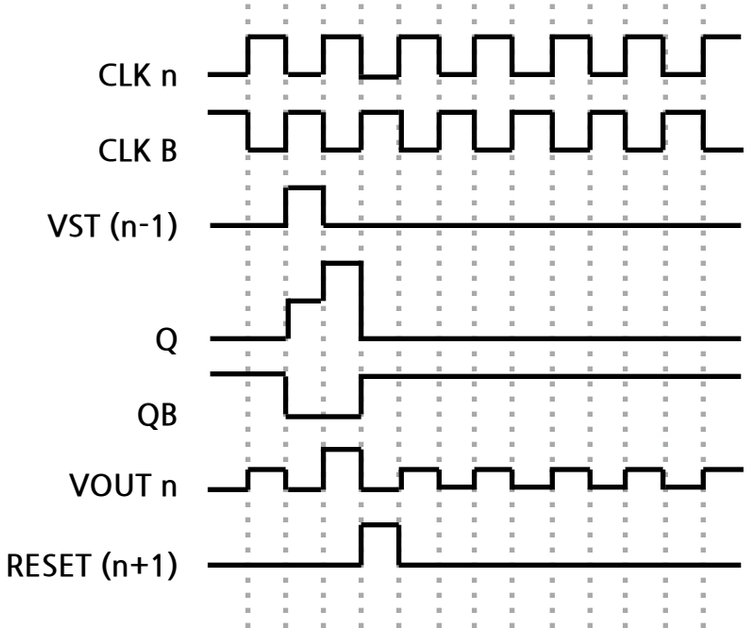

Conventional Gate Driver Circuit

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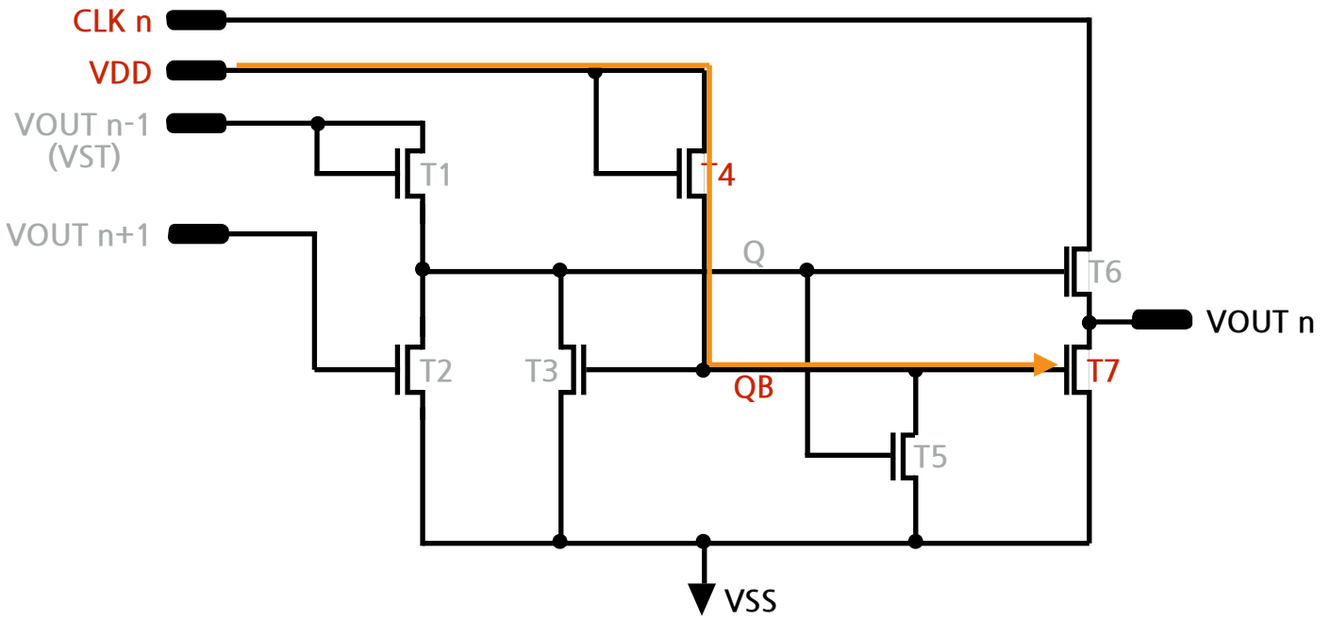

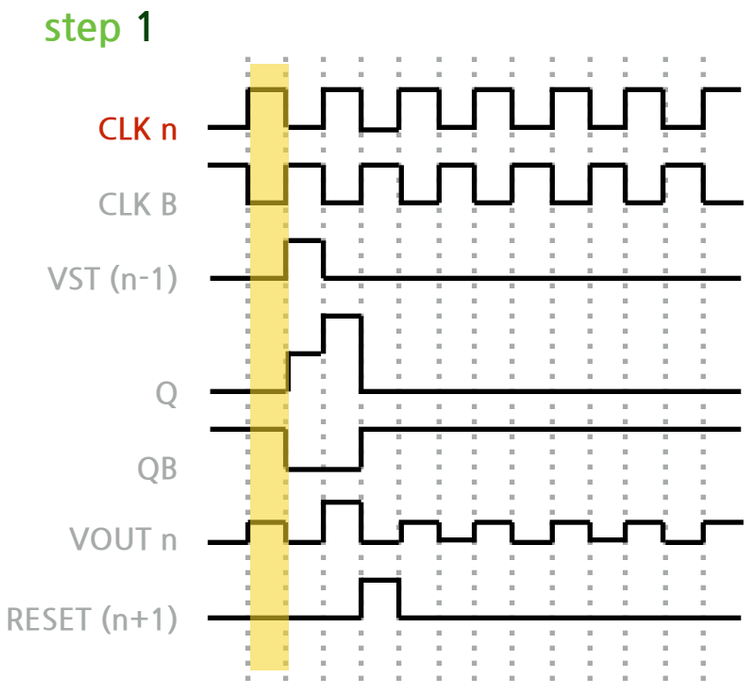

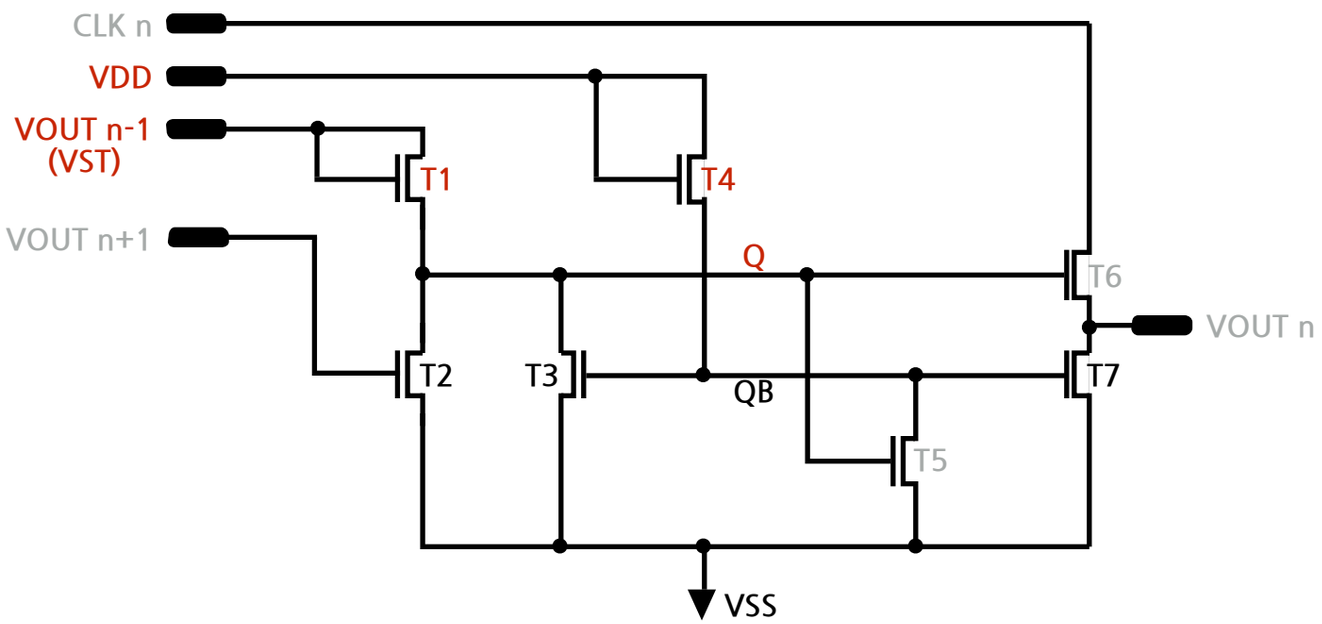

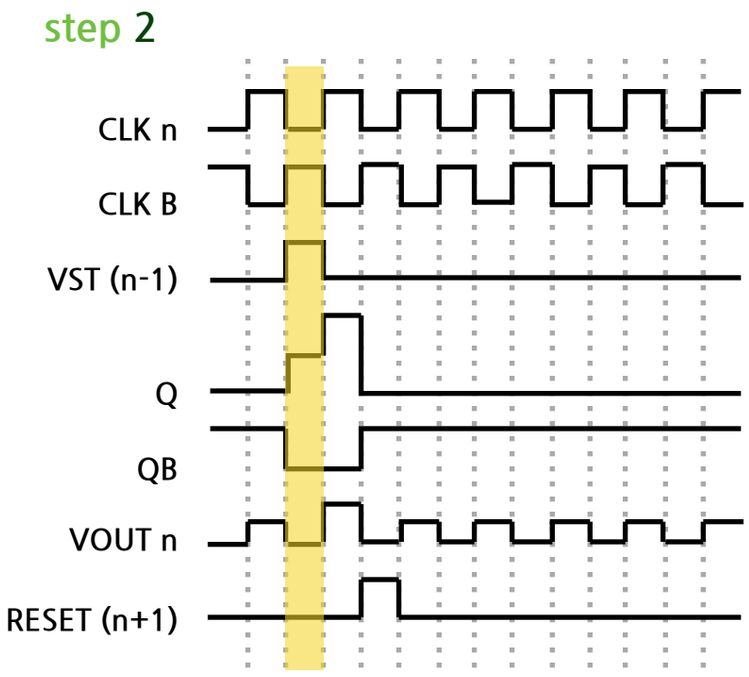

Conventional Gate Driver Circuit

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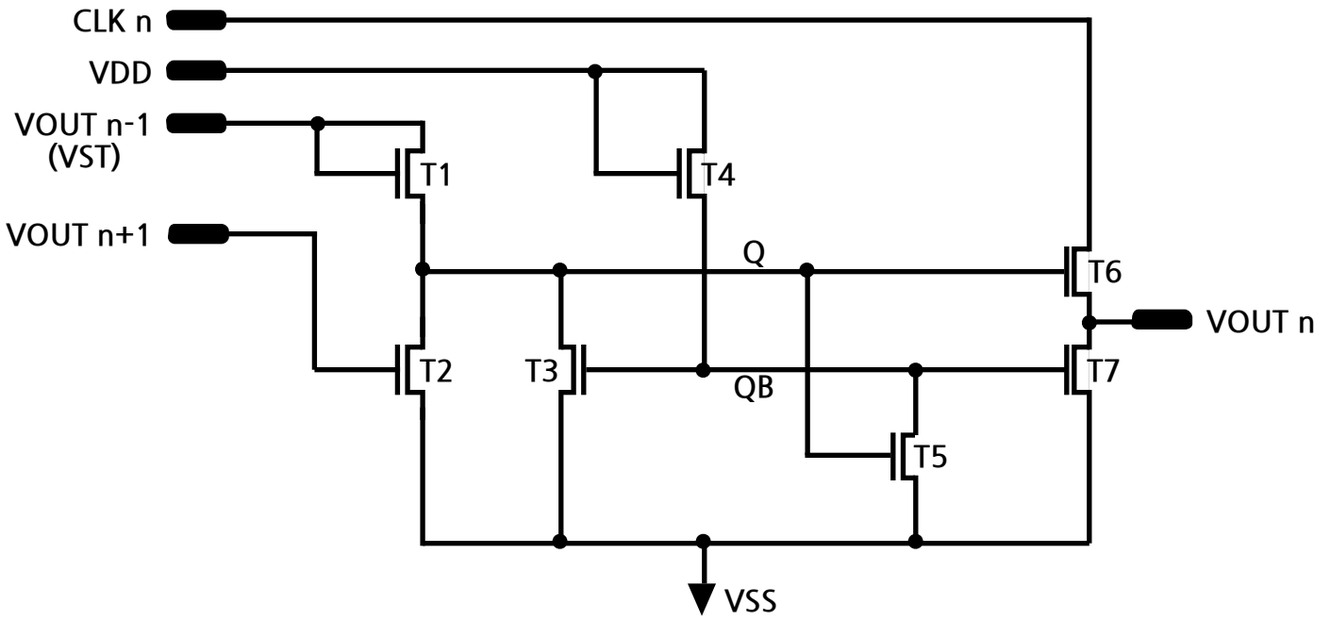
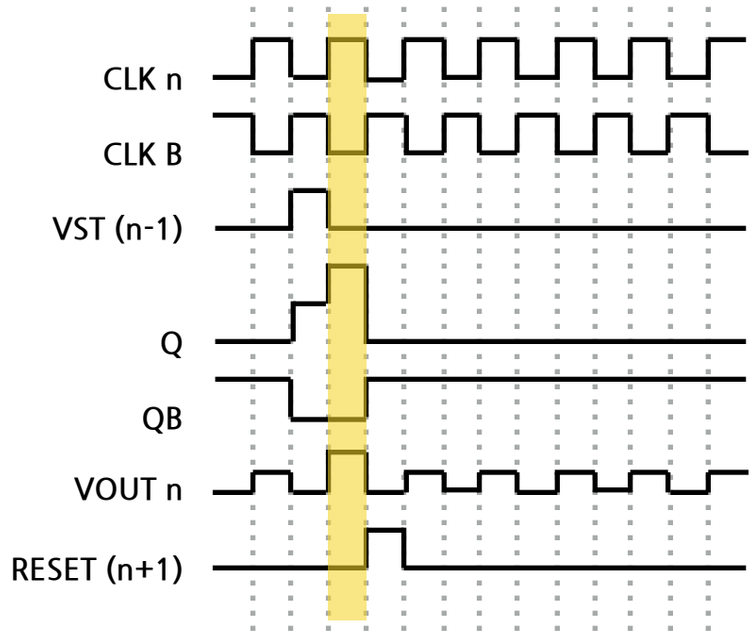
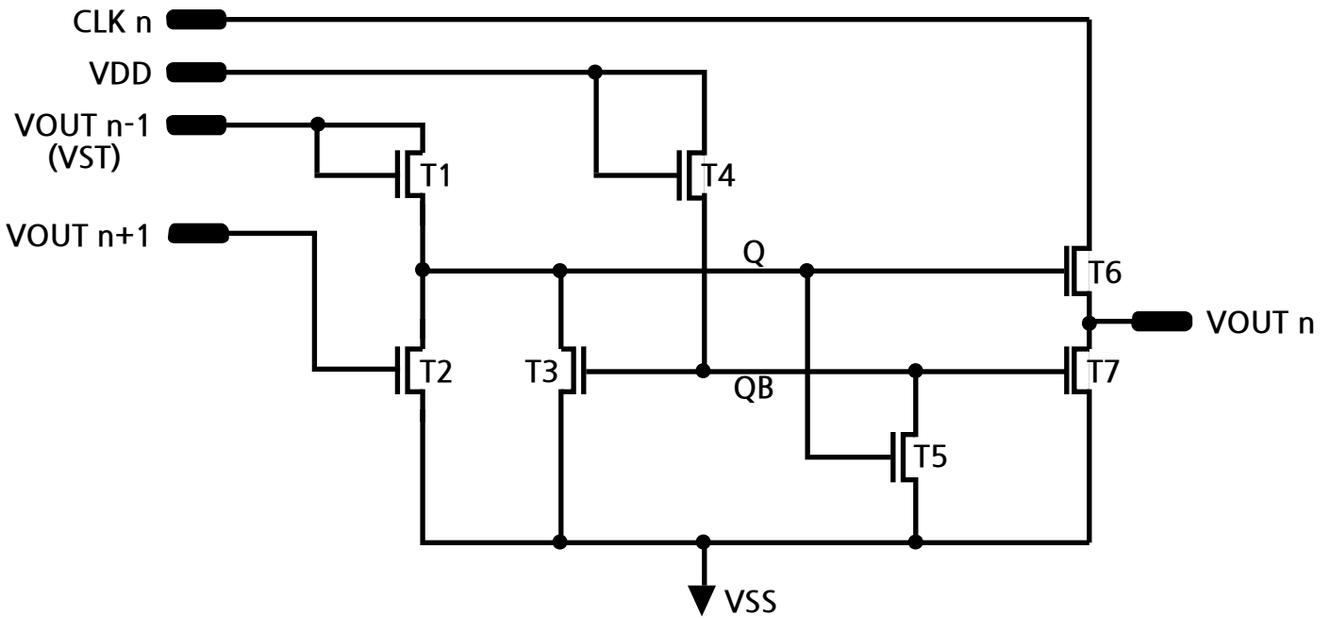
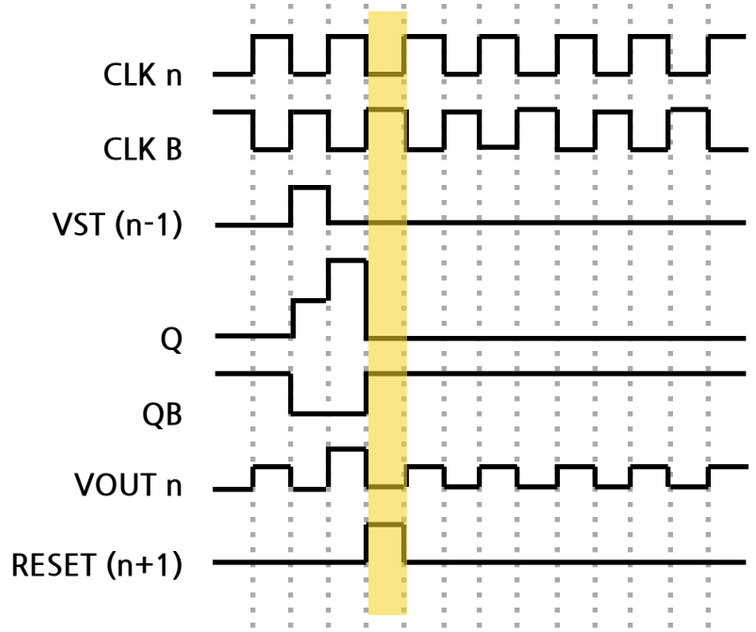


step 3





step 4



Conventional Gate Driver Circuit

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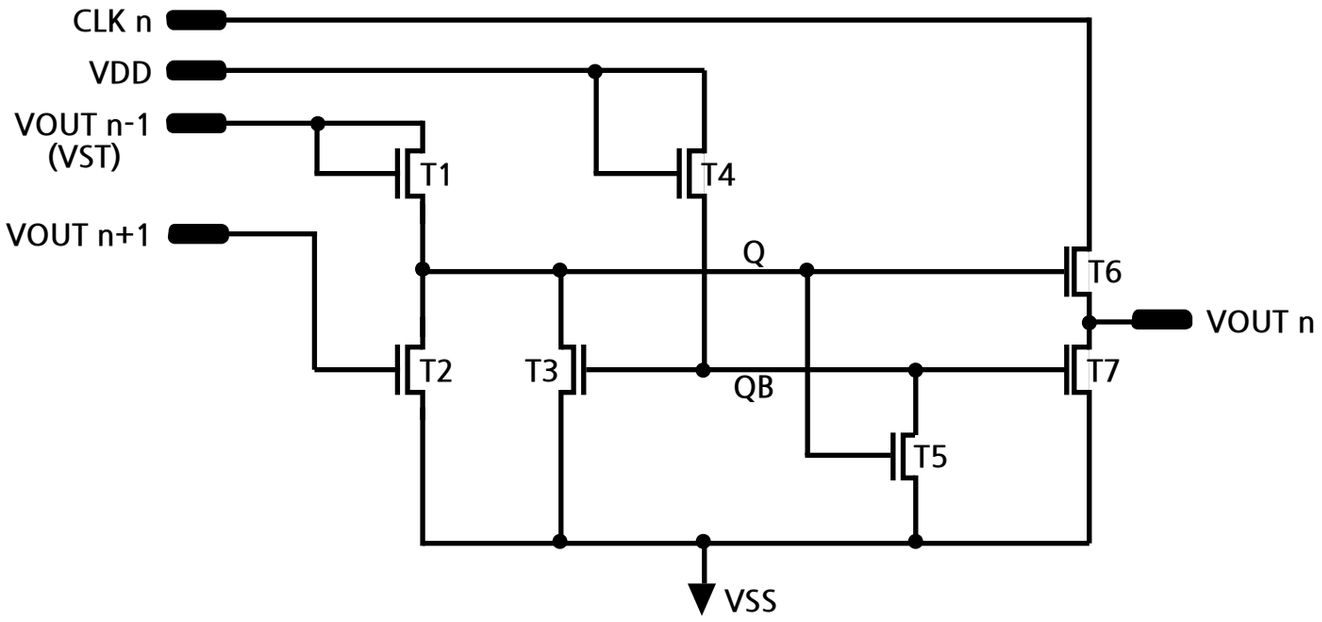

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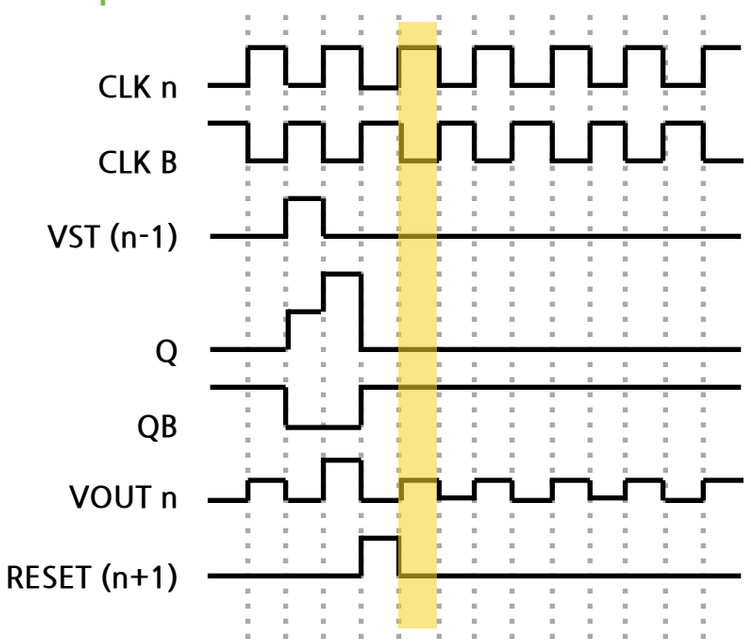
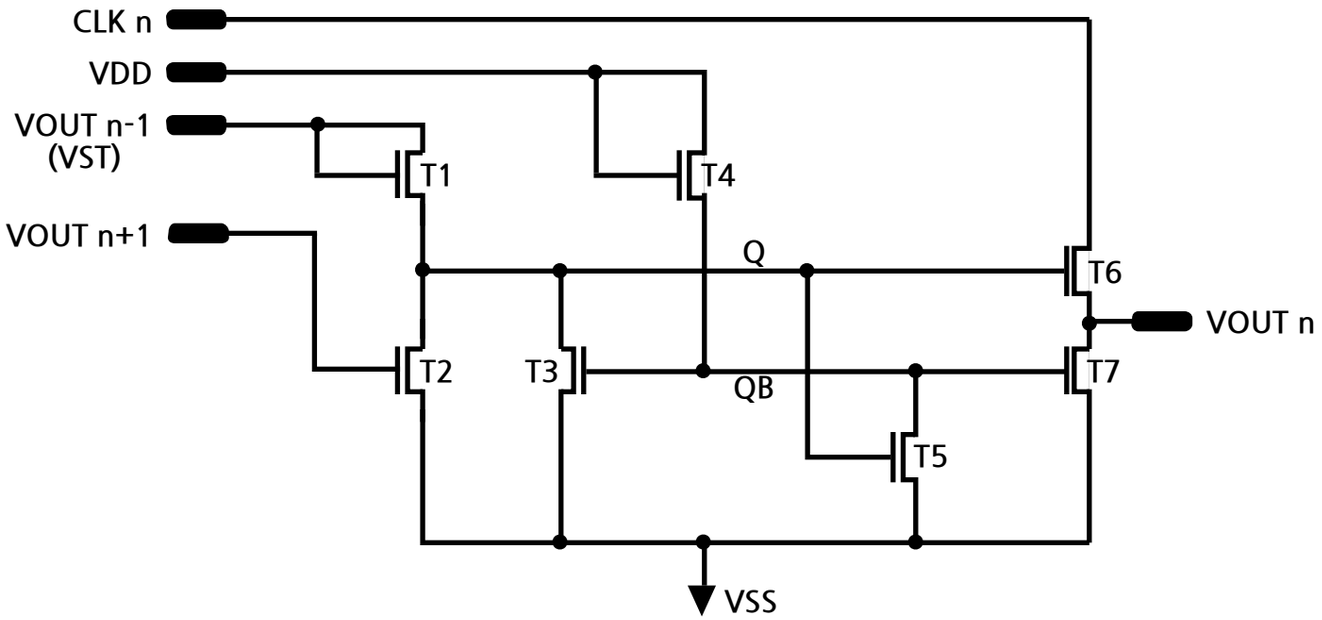
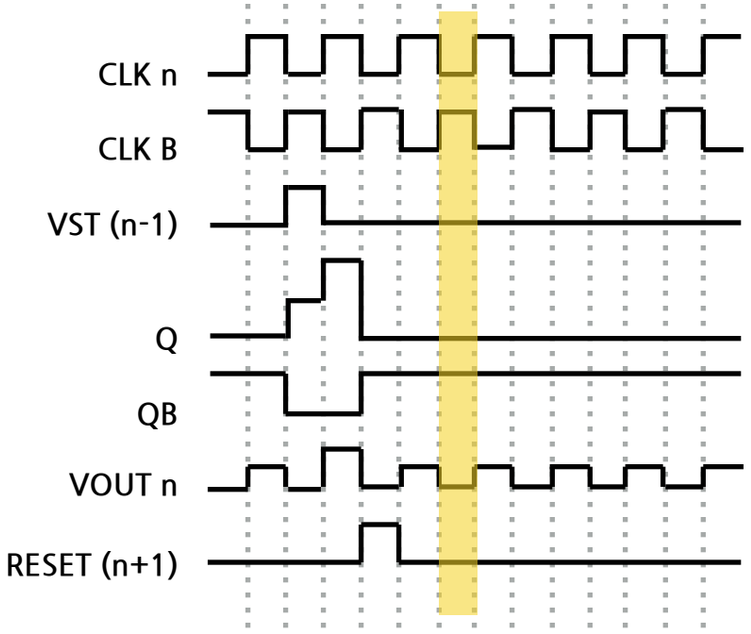




step 6



Proposed New Scan Driver Circuit Design

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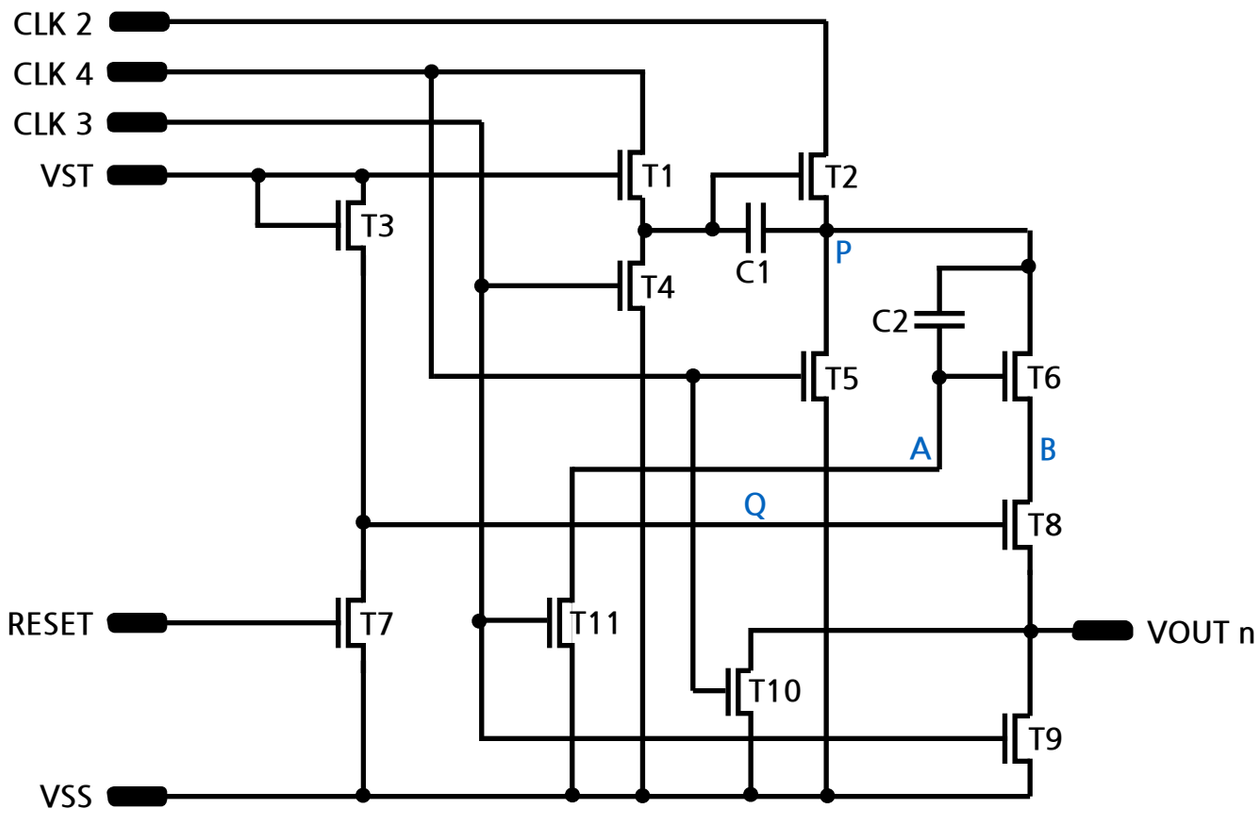
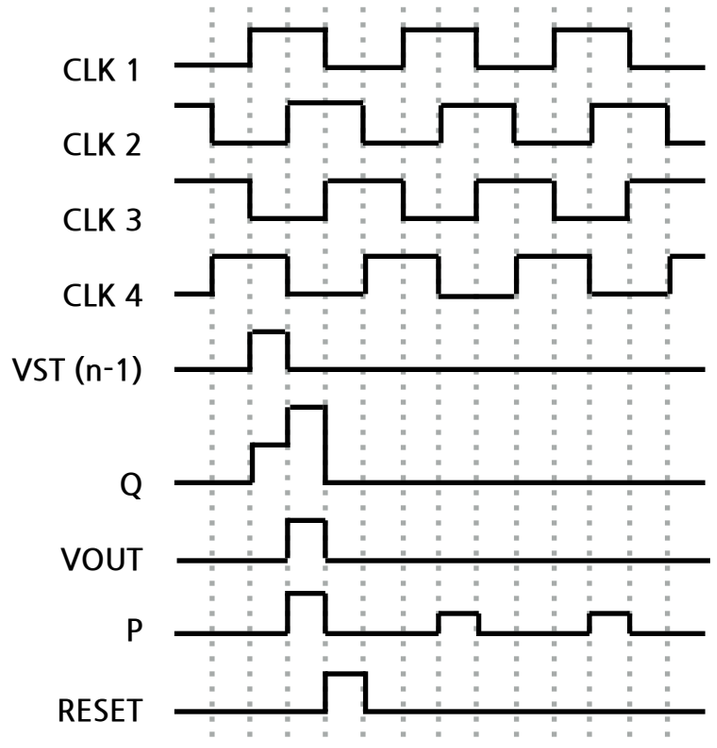
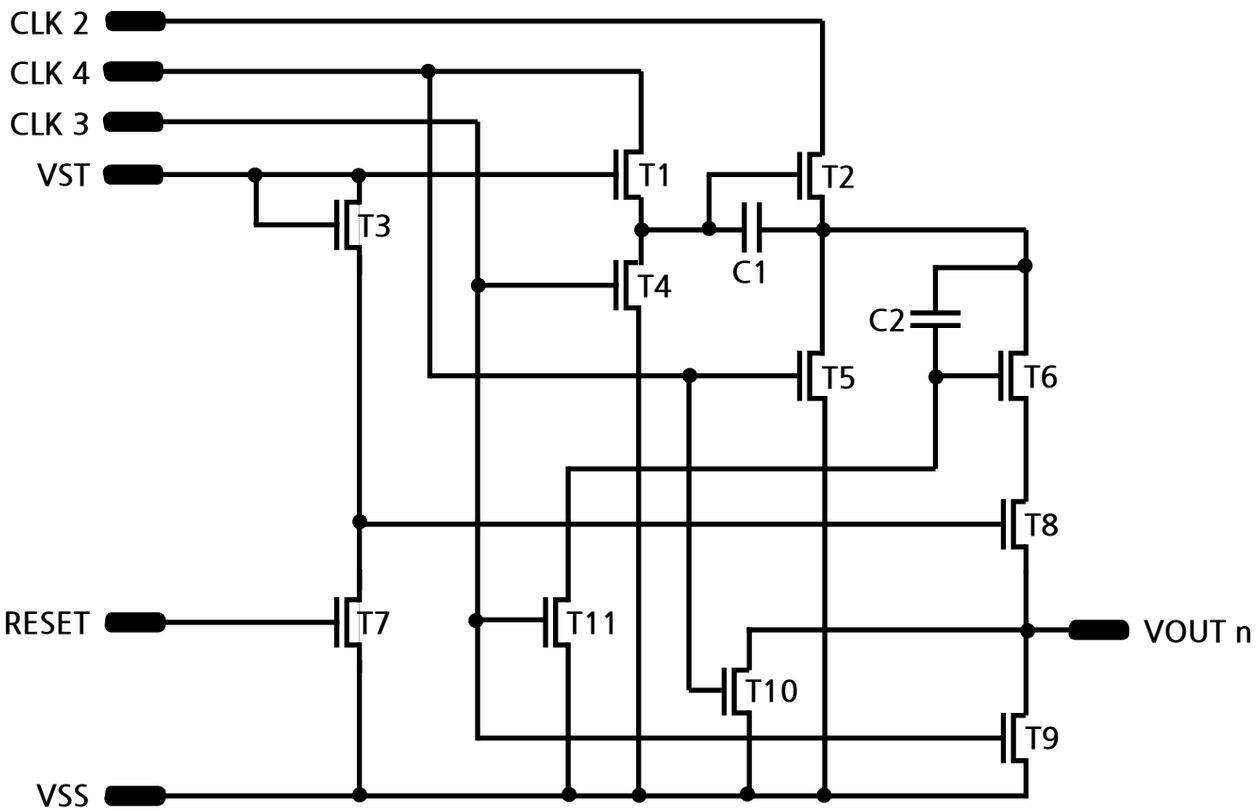
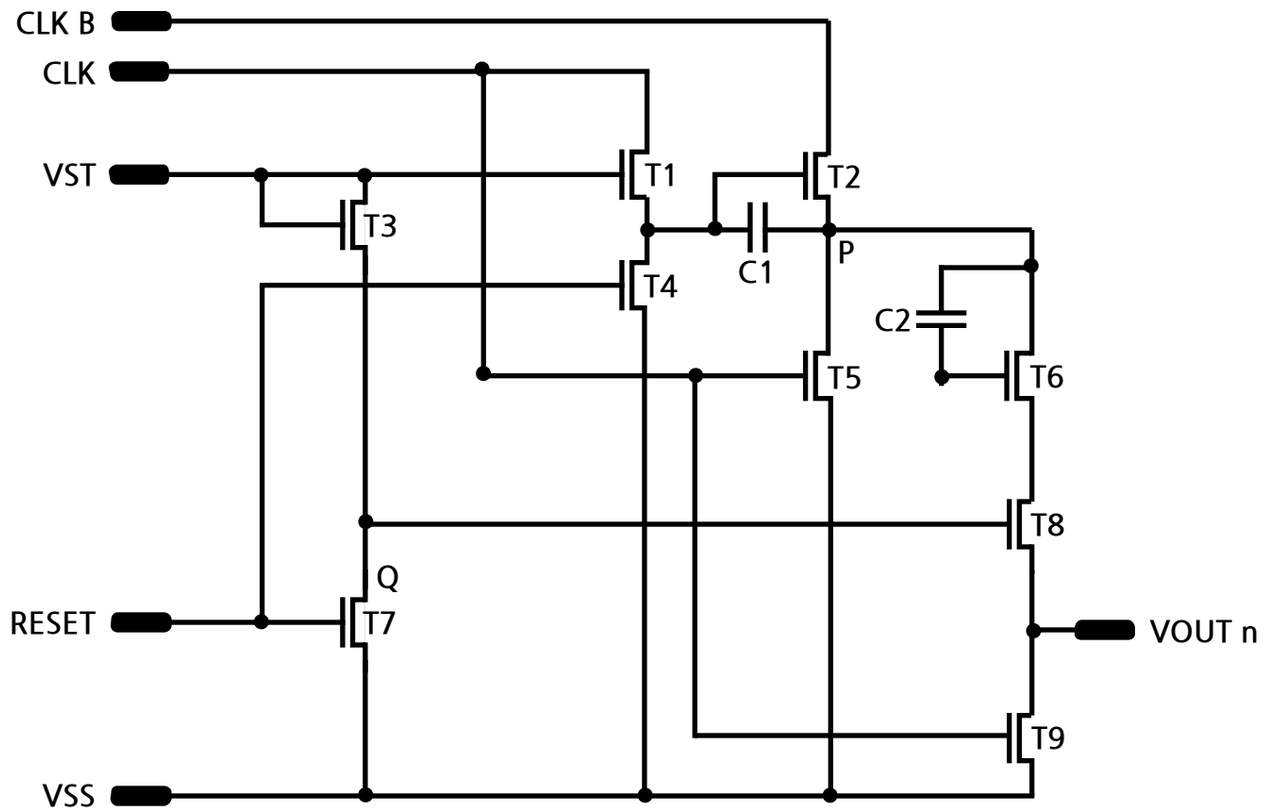


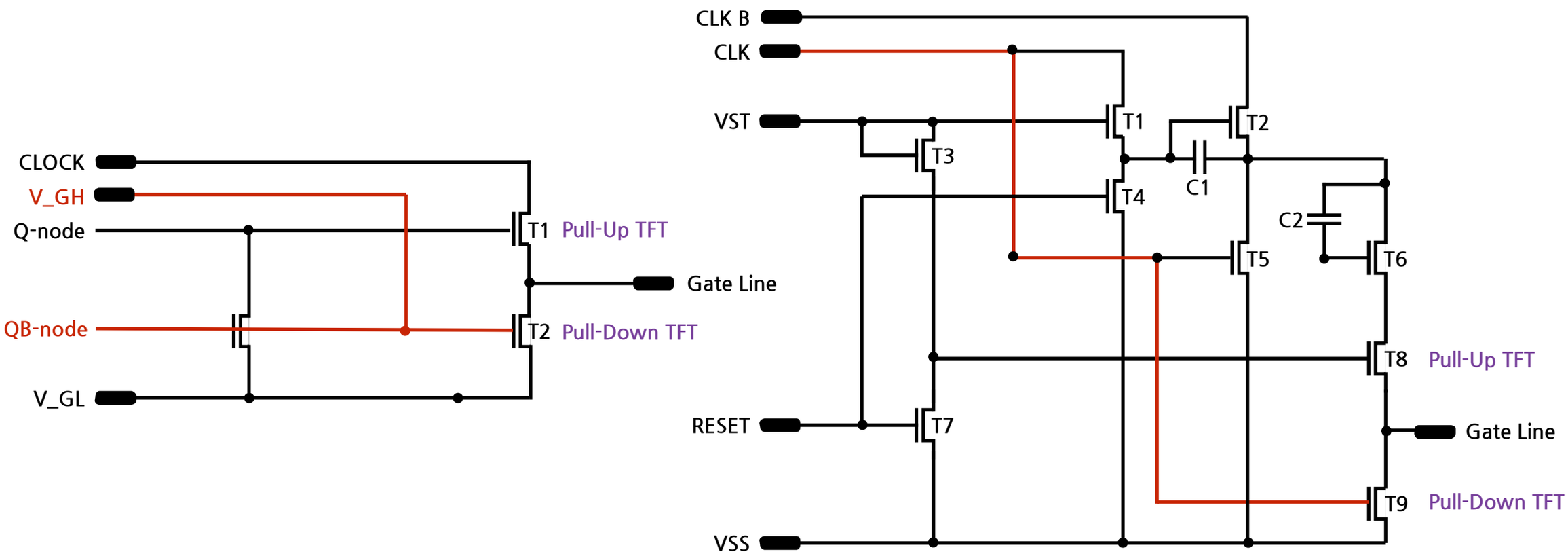




(a) Conventional



(b) Proposed



(a) Conventional

(b) Proposed

Proposed New Scan Driver Circuit Design

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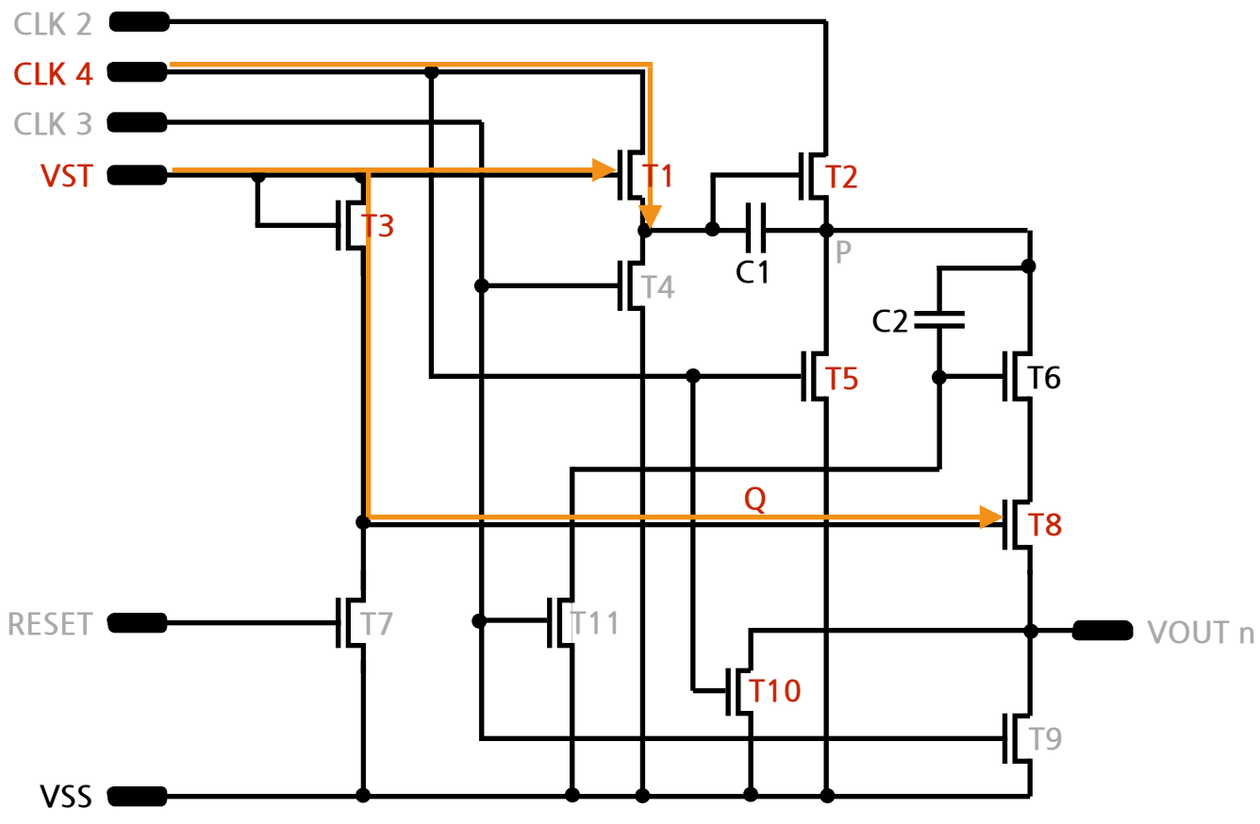

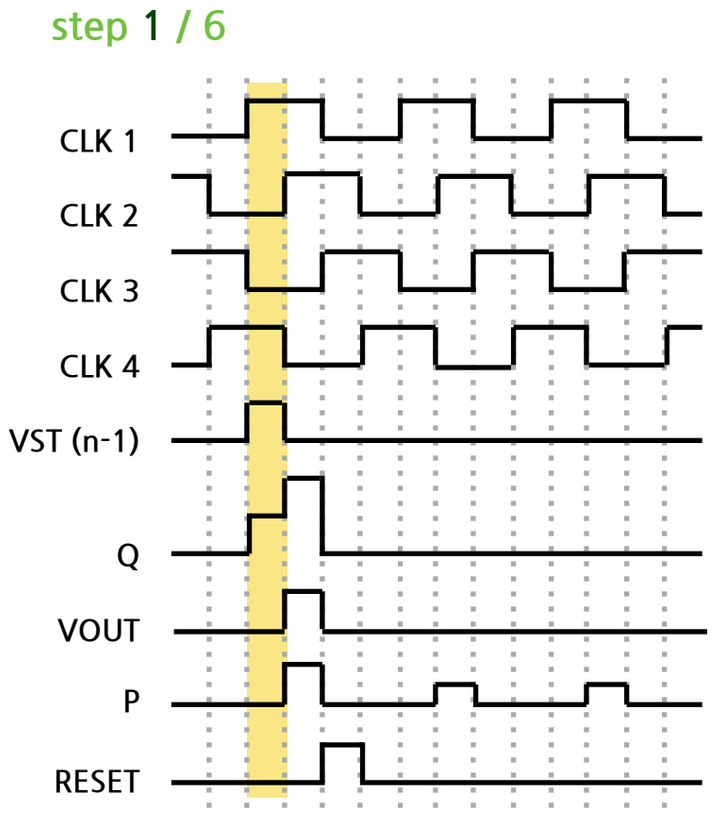

Proposed New Scan Driver Circuit Design

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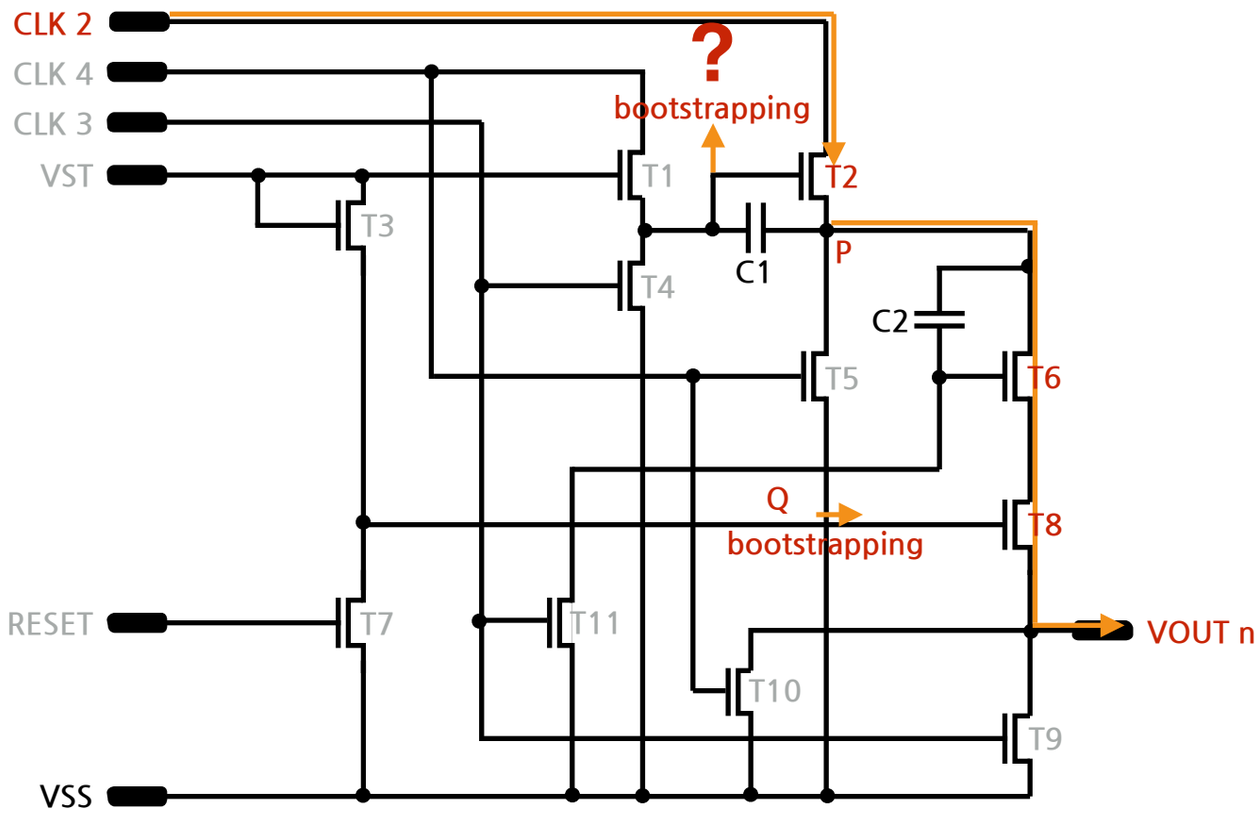
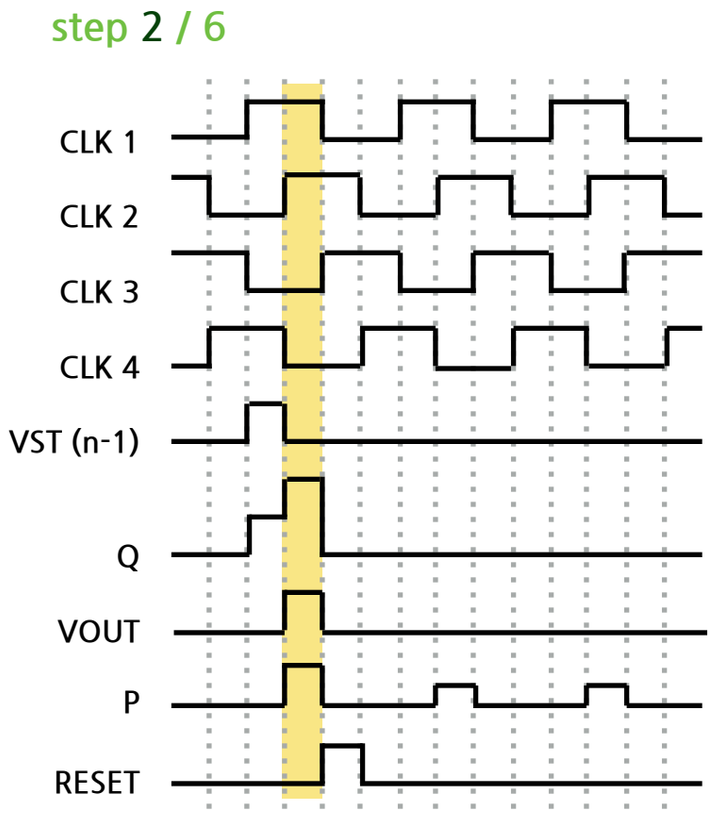
The term bootstrapping usually refers to "pulling up" the value of a physical parameter. In the present context, we will analyze a situation where the voltage on an isolated node is boosted to a value well above the power supply value of V_DD by means of dynamic switching.





Proposed New Scan Driver Circuit Design

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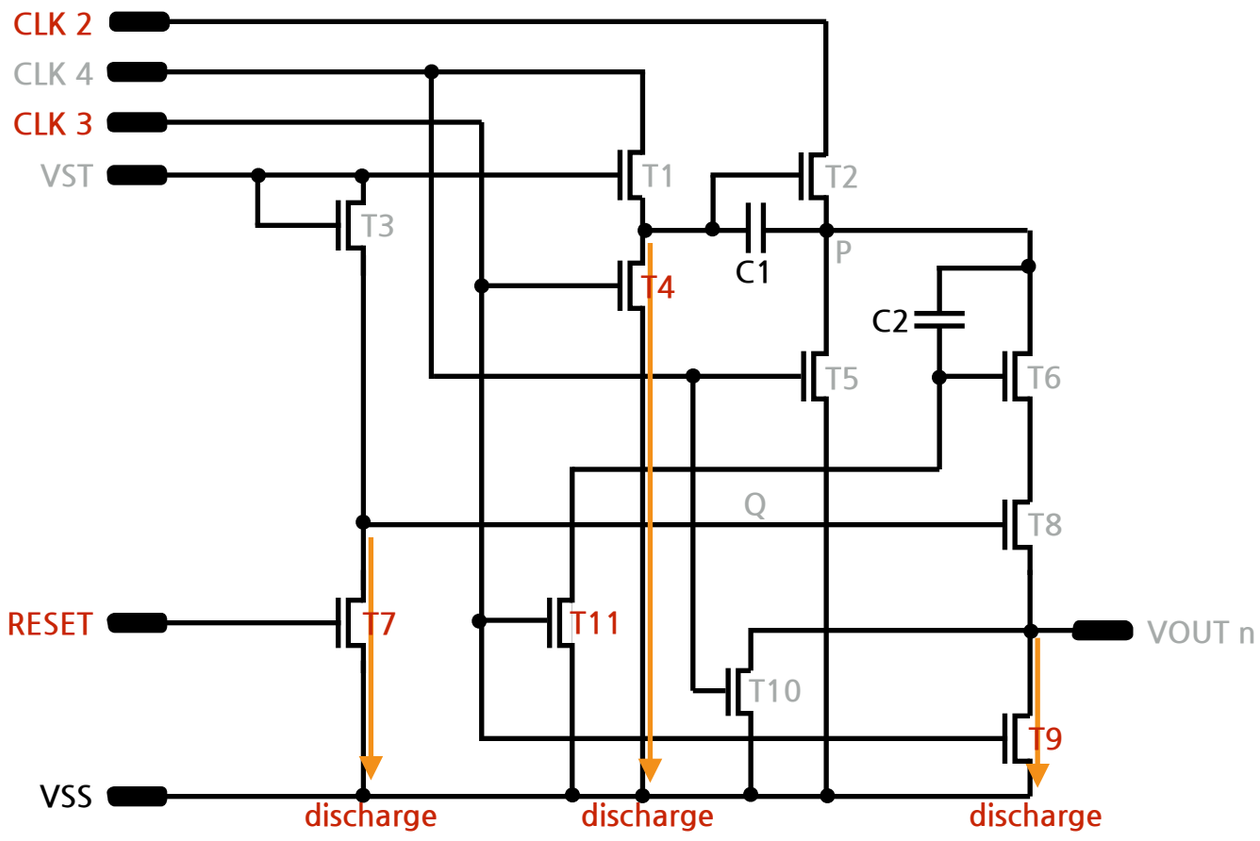
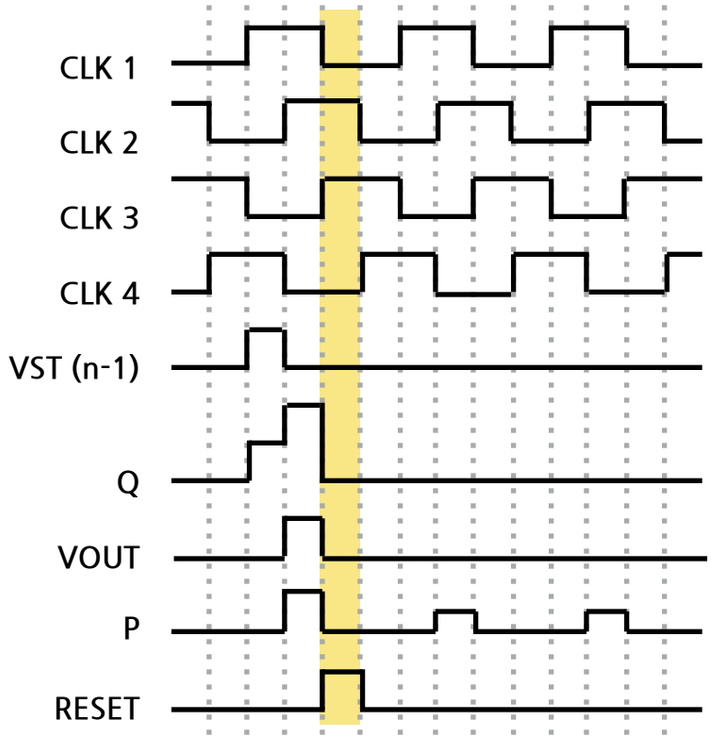


step 3 / 6



Proposed New Scan Driver Circuit Design

SUNG KYUN KWAN UNIV
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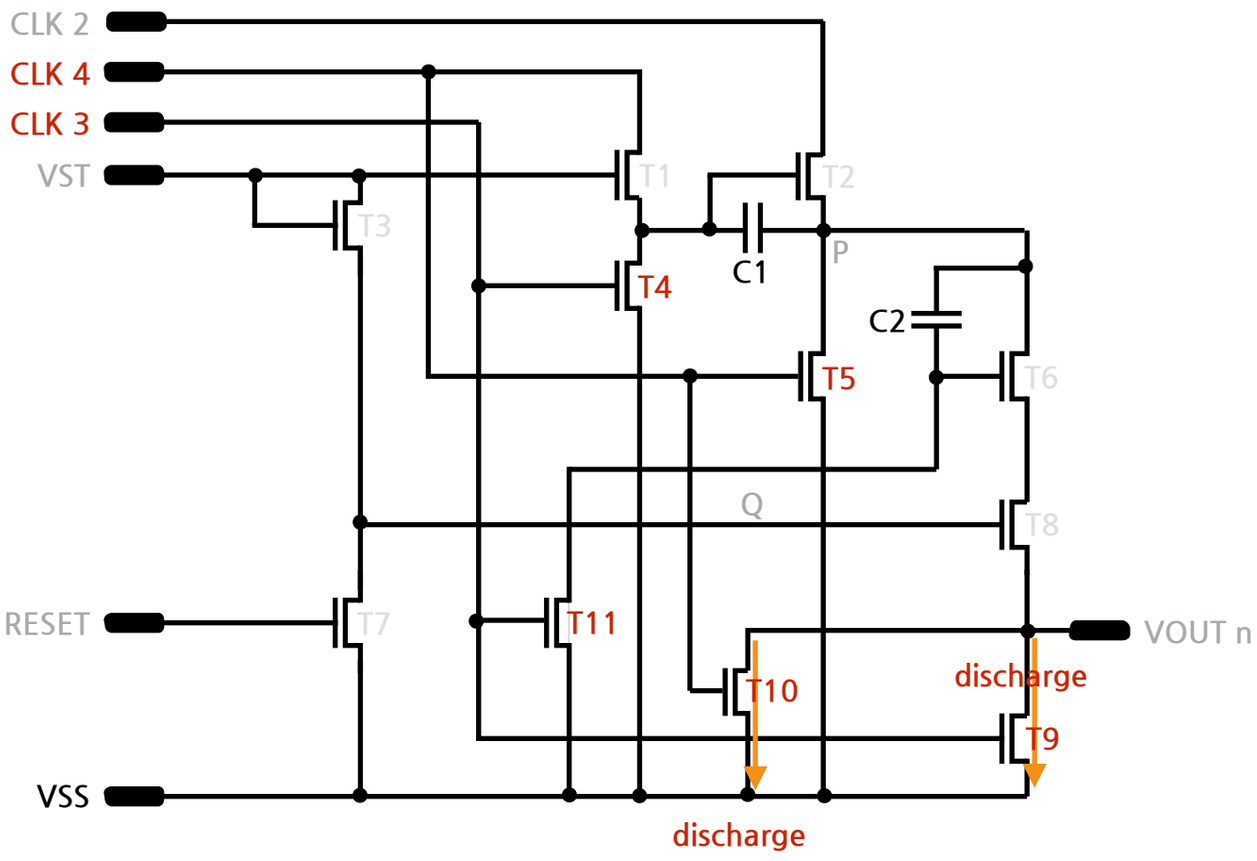
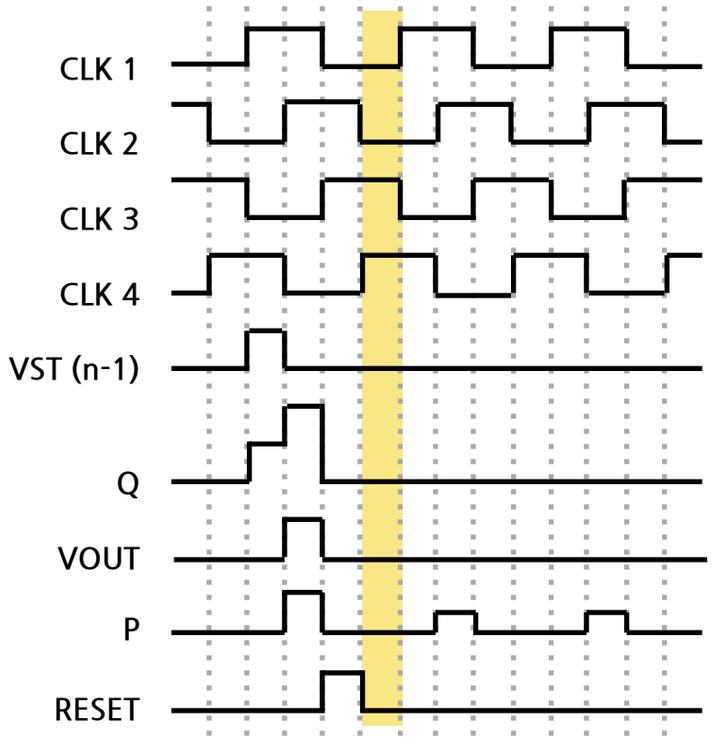
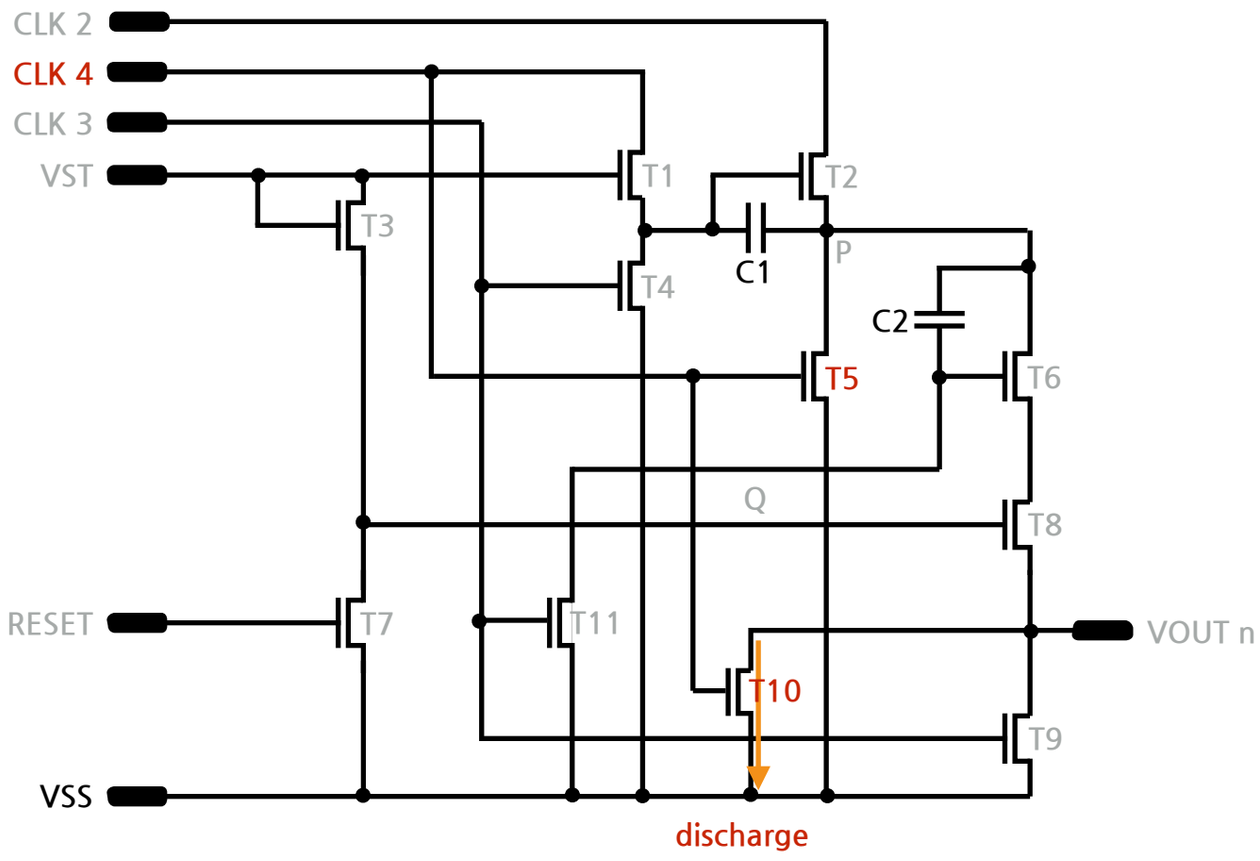


step 4 / 6

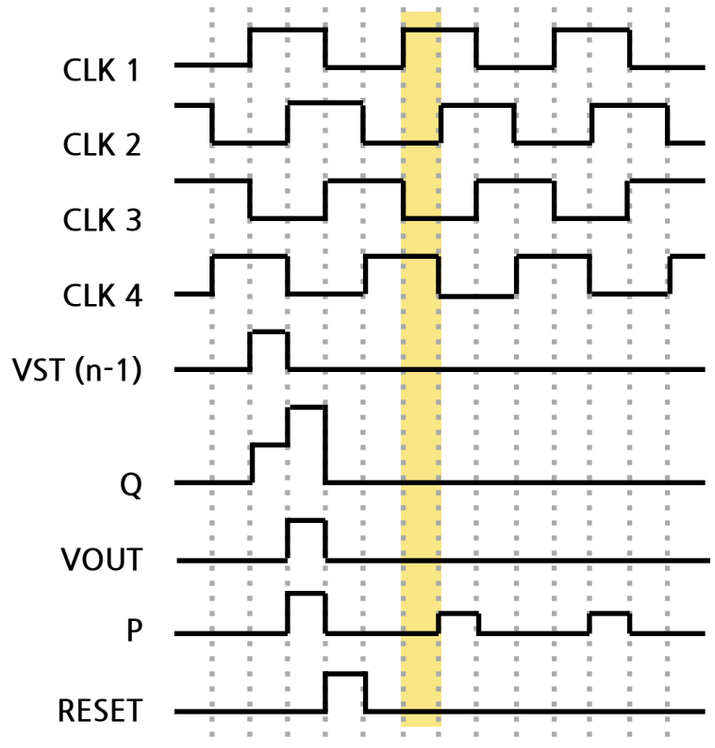


Proposed New Scan Driver Circuit Design

SUNG KYUN KWAN UNIV
CHAN YOUNG PARK

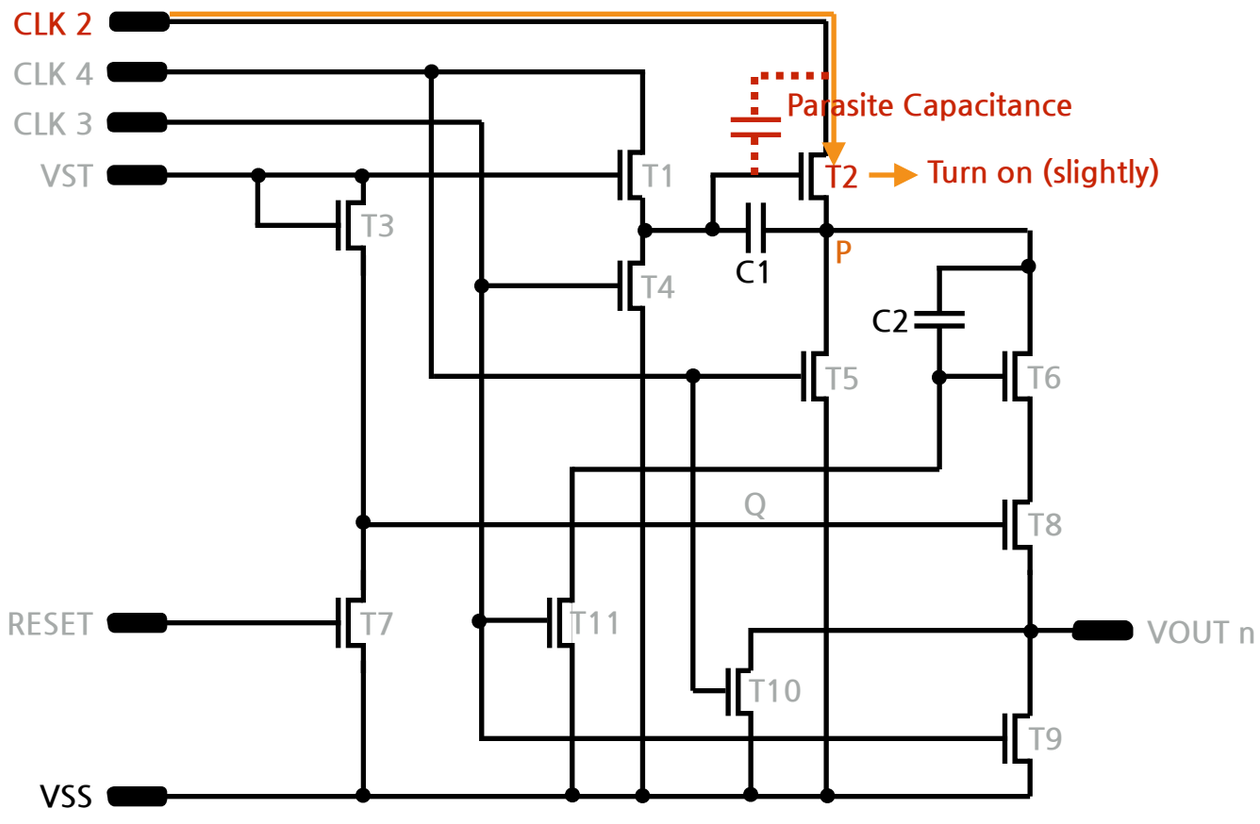


step 5 / 6

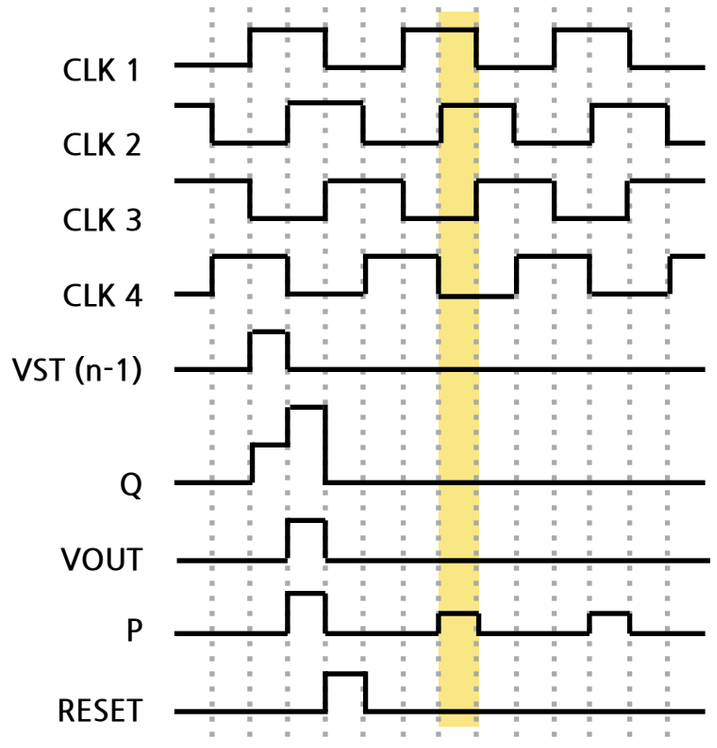


Proposed New Scan Driver Circuit Design

SUNG KYUN KWAN UNIV
CHAN YOUNG PARK

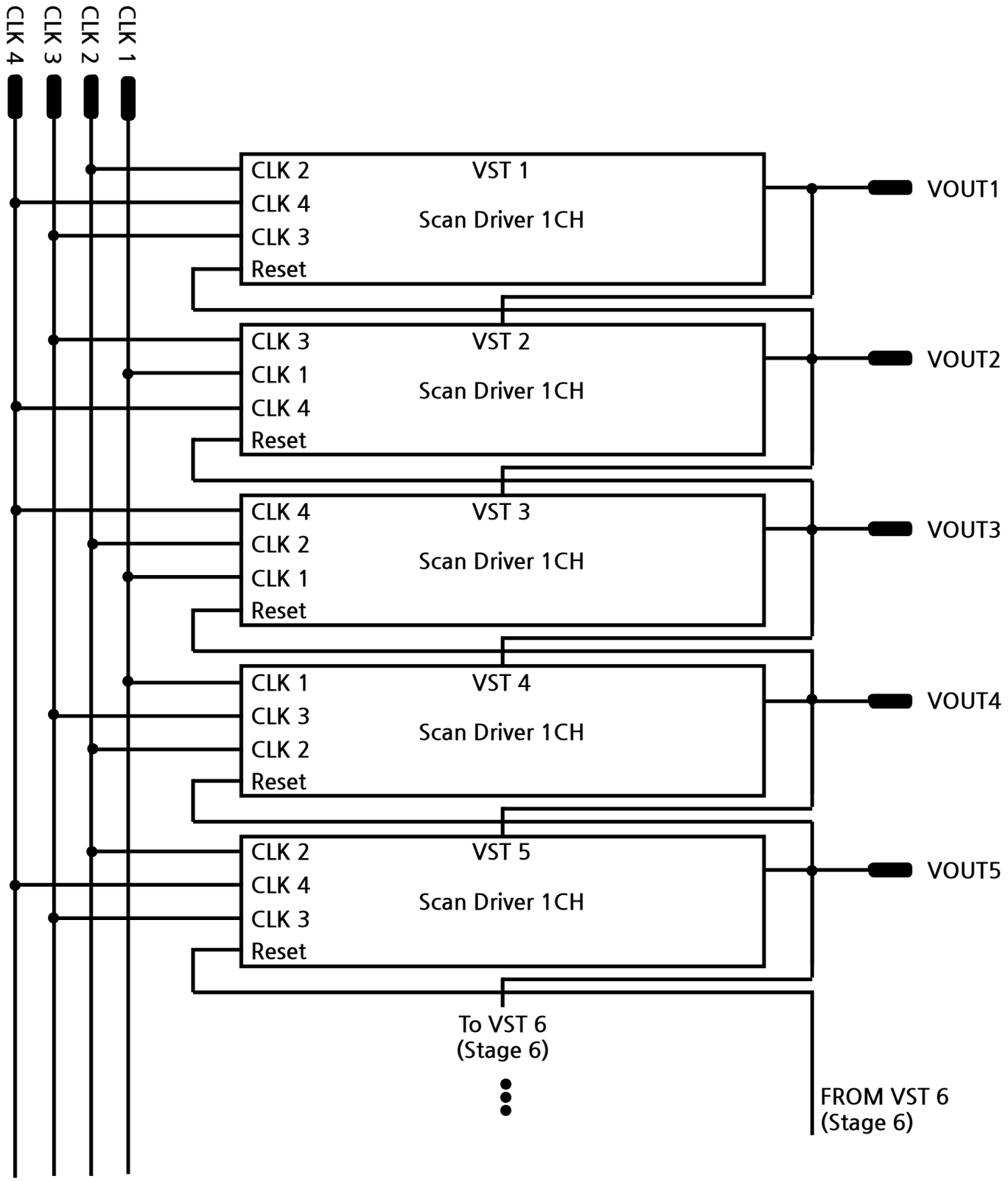


step 6 / 6



Proposed New Scan Driver Circuit Design

SUNG KYUN KWAN UNIV
CHAN YOUNG PARK



Oxide Gate Driver Circuit

NEW TYPE

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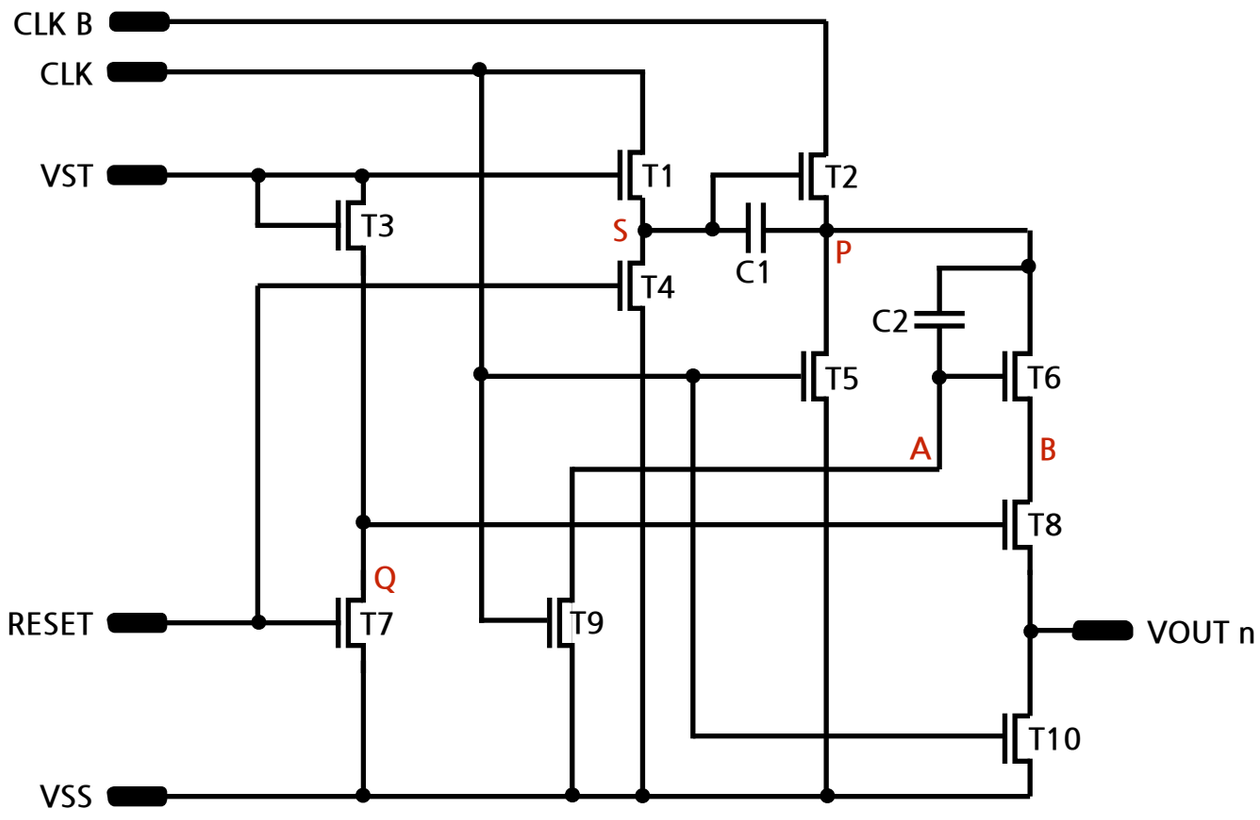
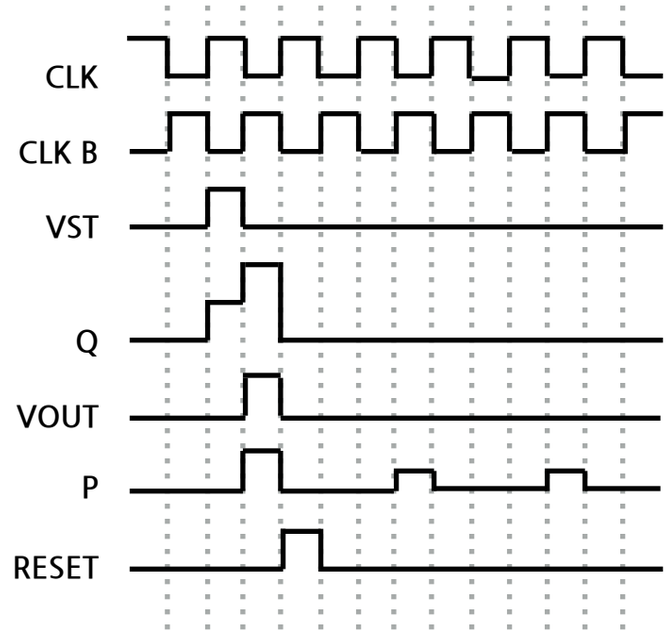
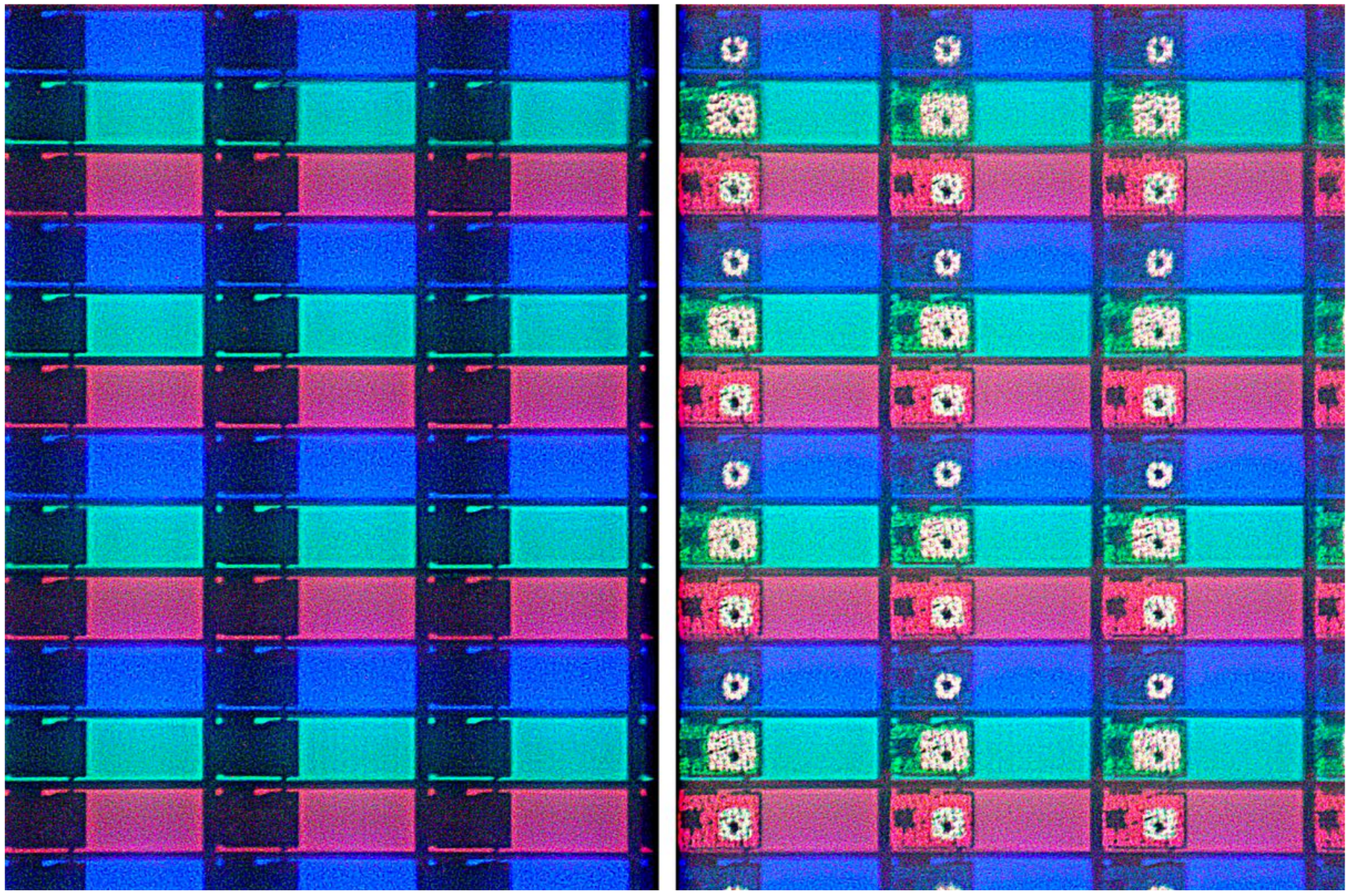




Appendix



https://en.wikipedia.org/wiki/Thin-film-transistor_liquid-crystal_display#mediaviewer/File:Dell_axim_LCD_under_microscope.jpg

Oxide Gate Driver Circuit

FINAL TYPE

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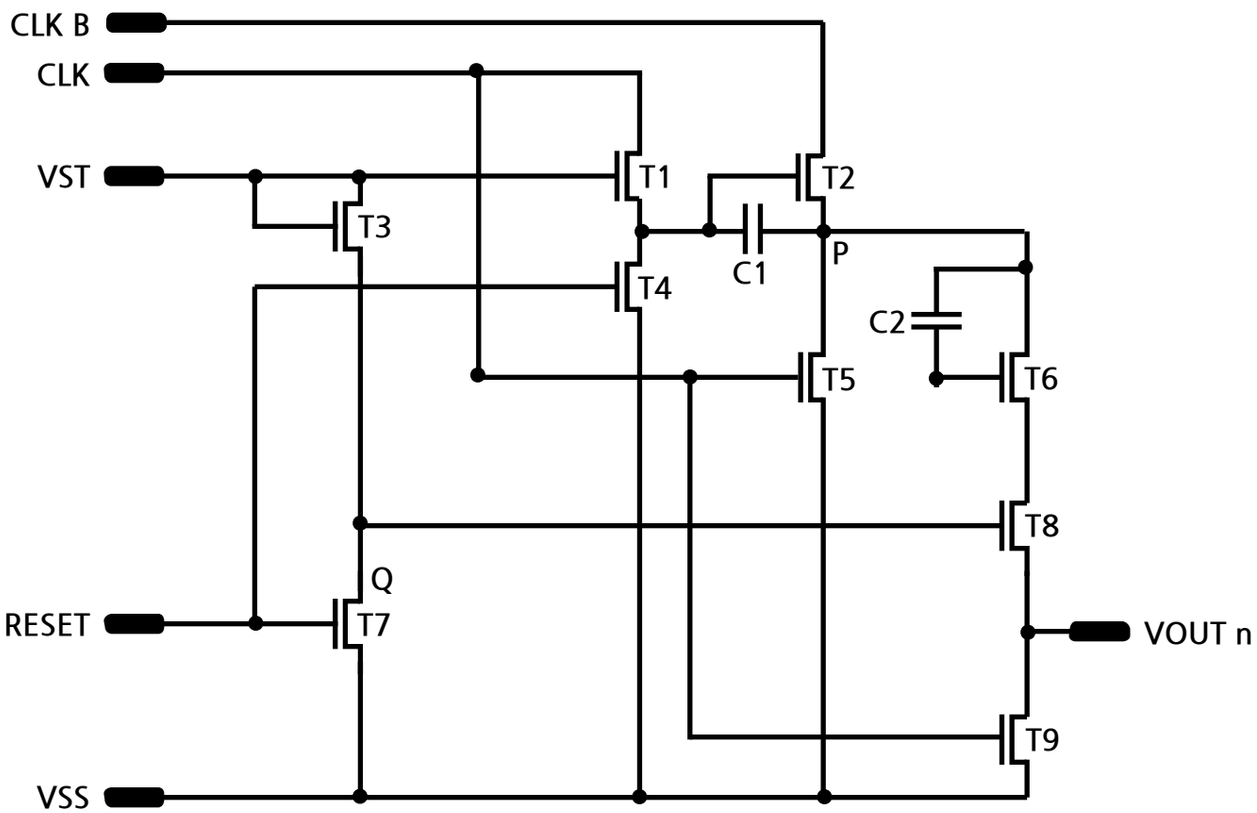

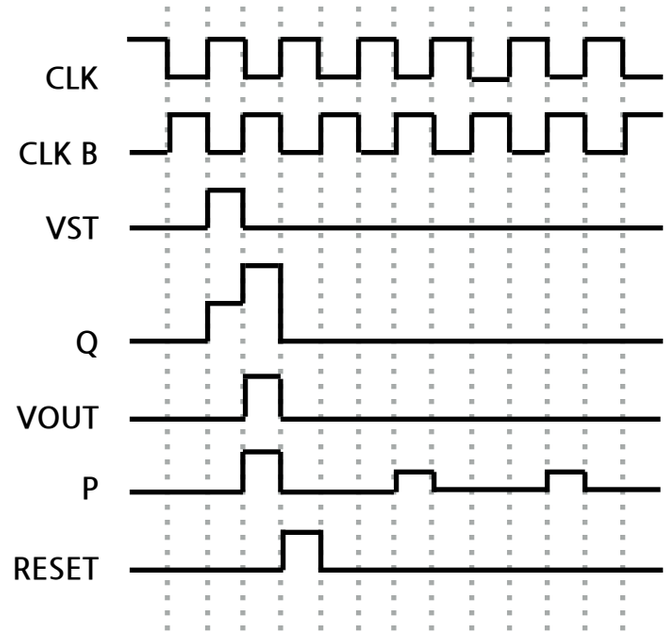

Oxide Gate Driver Circuit

FINAL TYPE

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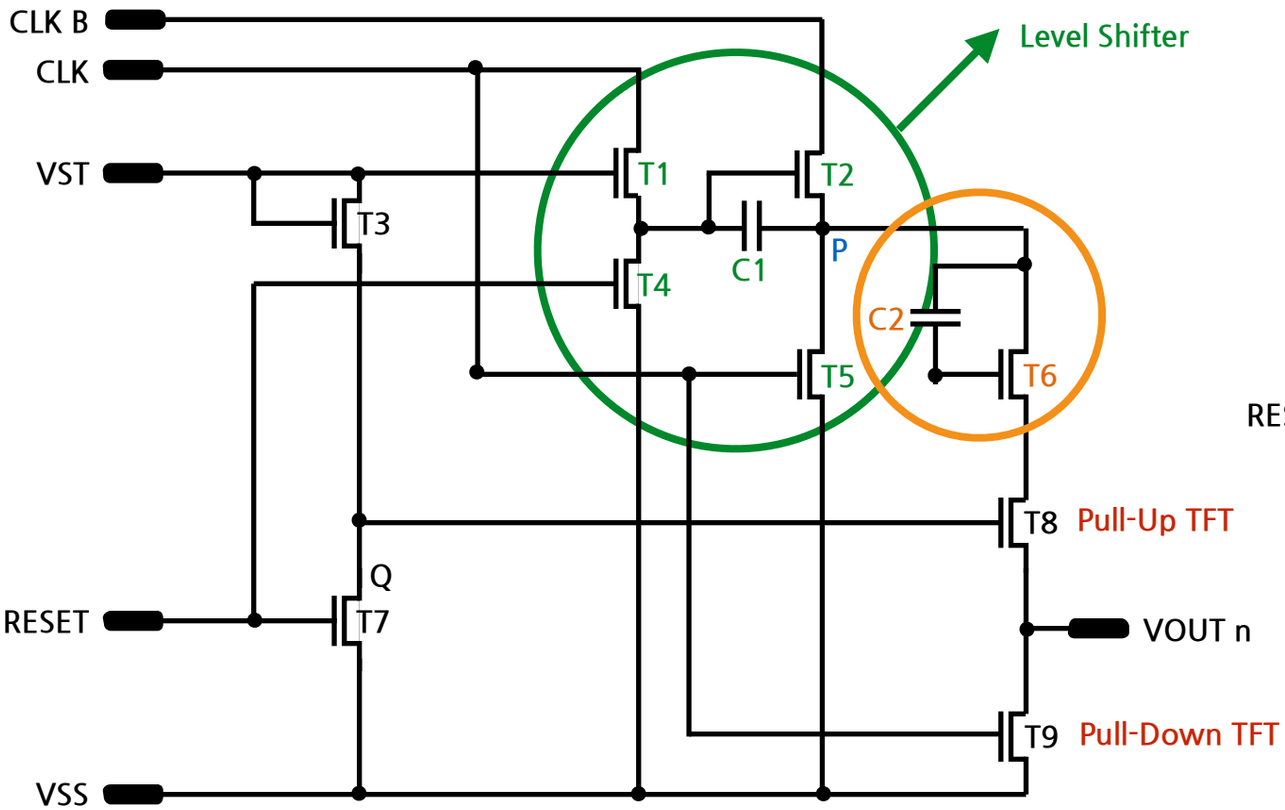
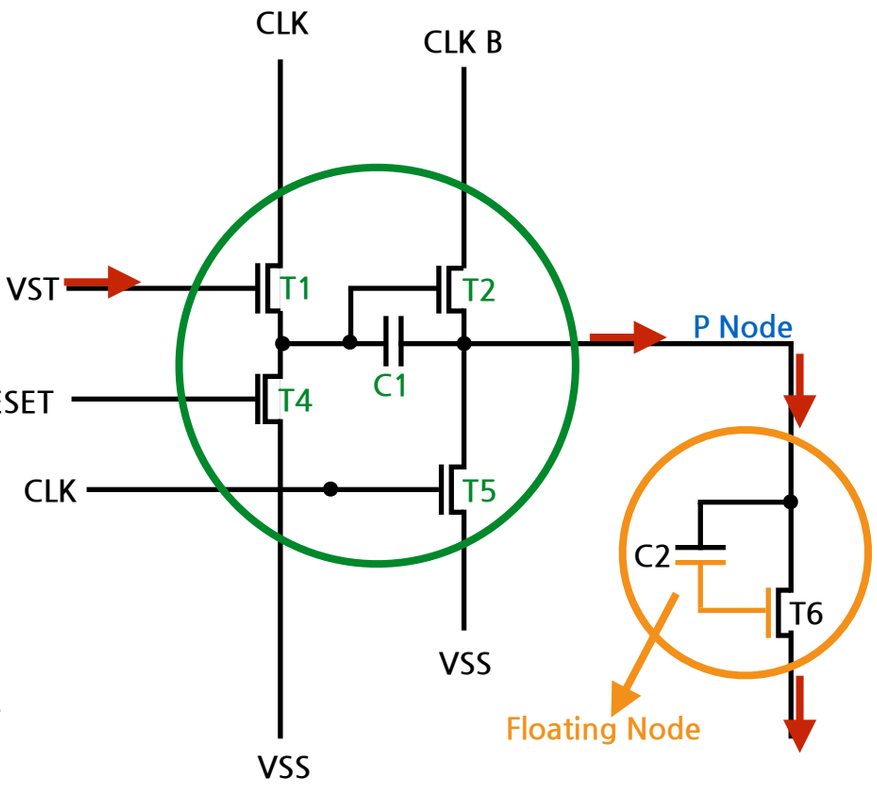
Level Shifter (or logic-level shifter) is a circuit used to translate signals from one logic level or voltage domain to another, allowing compatibility between ICs with different requirements, such as TTL and CMOS. Many modern full featured systems use level shifters to bridge domains between low-power application processors runing at 1.8V and other system functions like sensors or other analog intensive applications running at 3.3 or 5V.





Oxide Gate Driver Circuit

FINAL TYPE

SUNG KYUN KWAN UNIV
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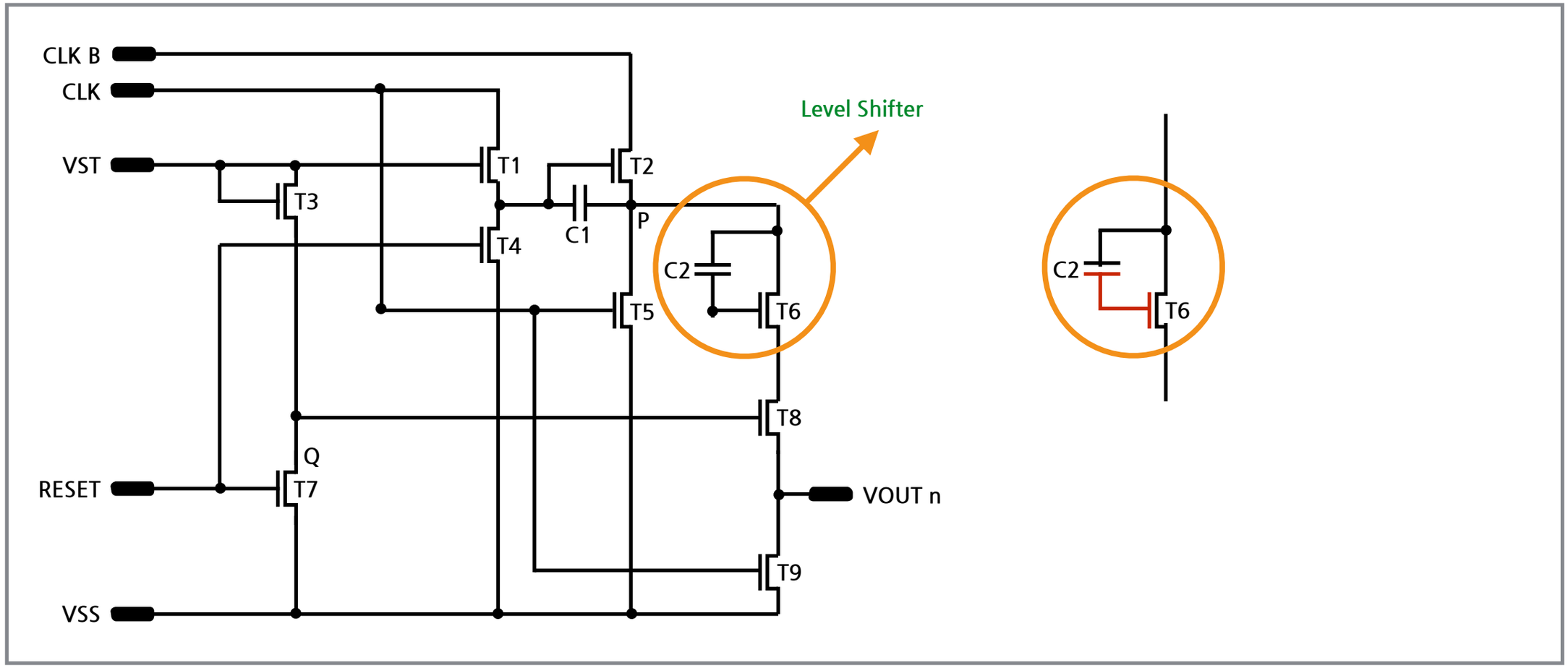
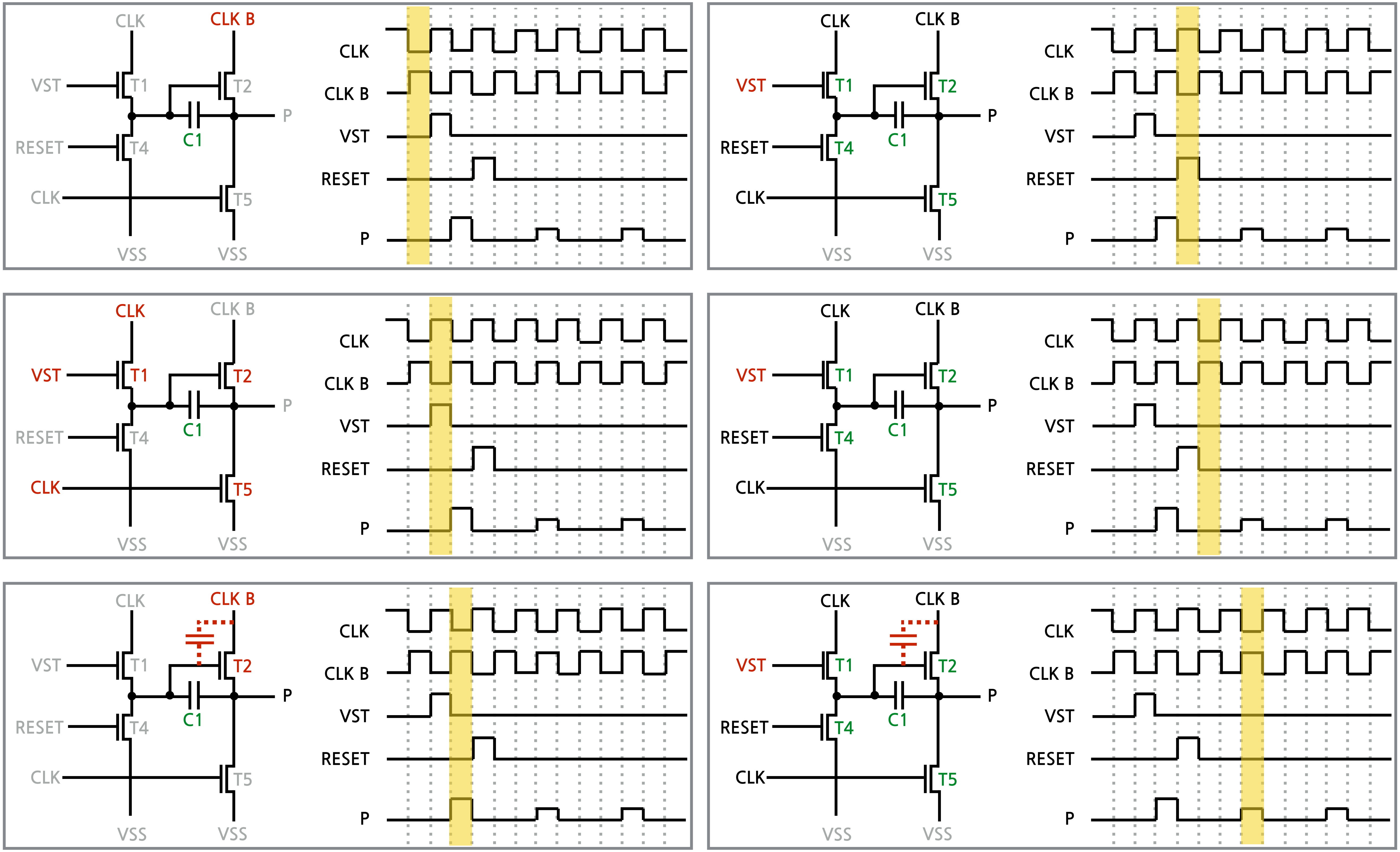


Oxide Gate Driver Circuit

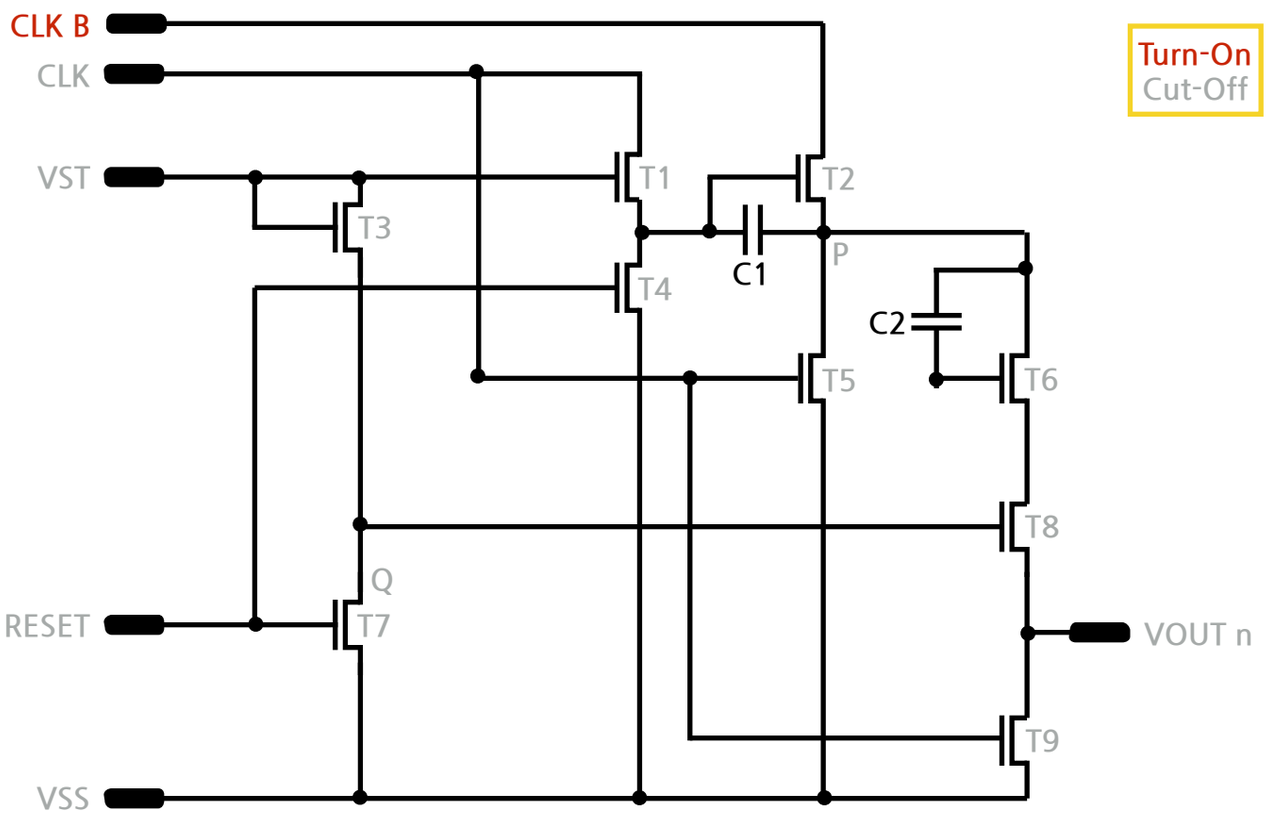
SUNG KYUN KWAN UNIV
CHAN YOUNG PARK



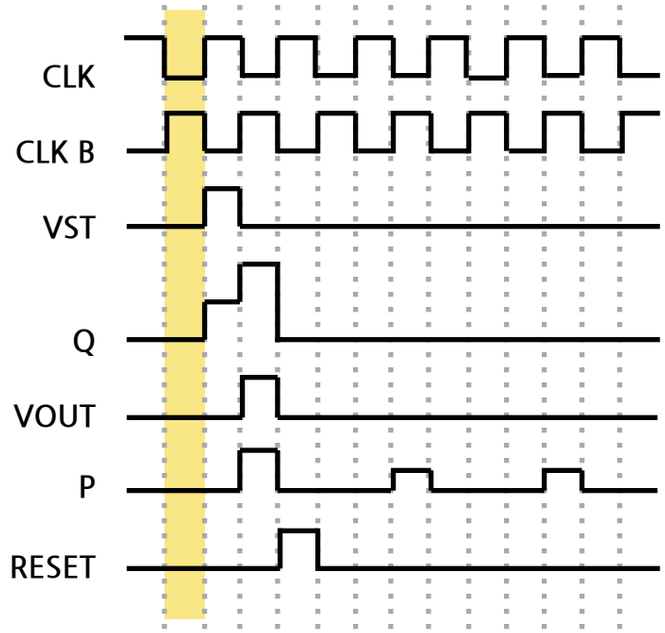
Oxide Gate Driver Circuit

Analyzing FINAL TYPE

SUNG KYUN KWAN UNIV
CHAN YOUNG PARK



Turn-On
Cut-Off



Oxide Gate Driver Circuit

Analyzing FINAL TYPE

SUNG KYUN KWAN UNIV
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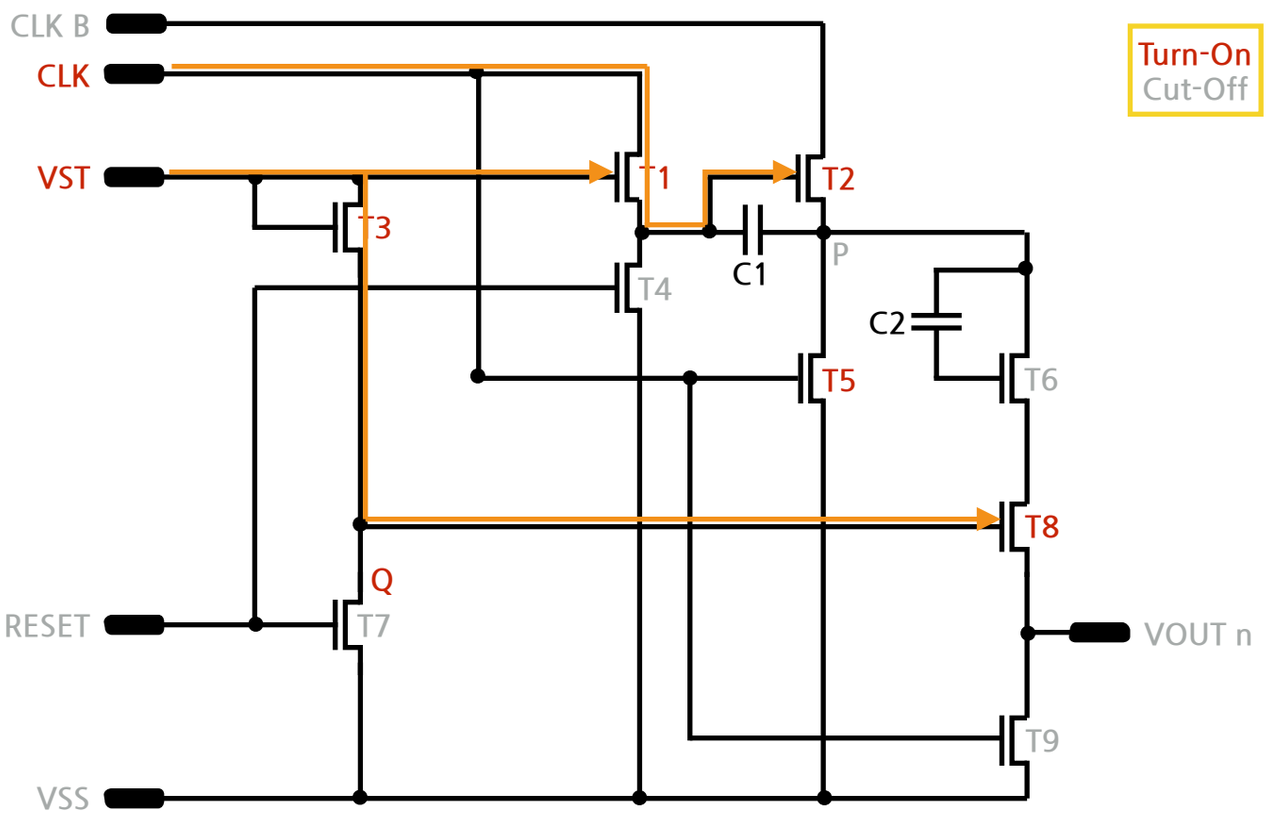
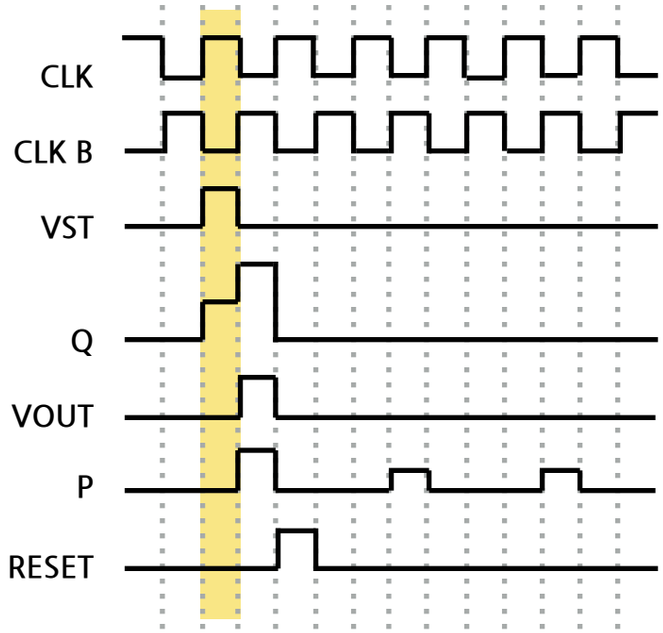


Turn-On
Cut-Off



Oxide Gate Driver Circuit

Analyzing FINAL TYPE

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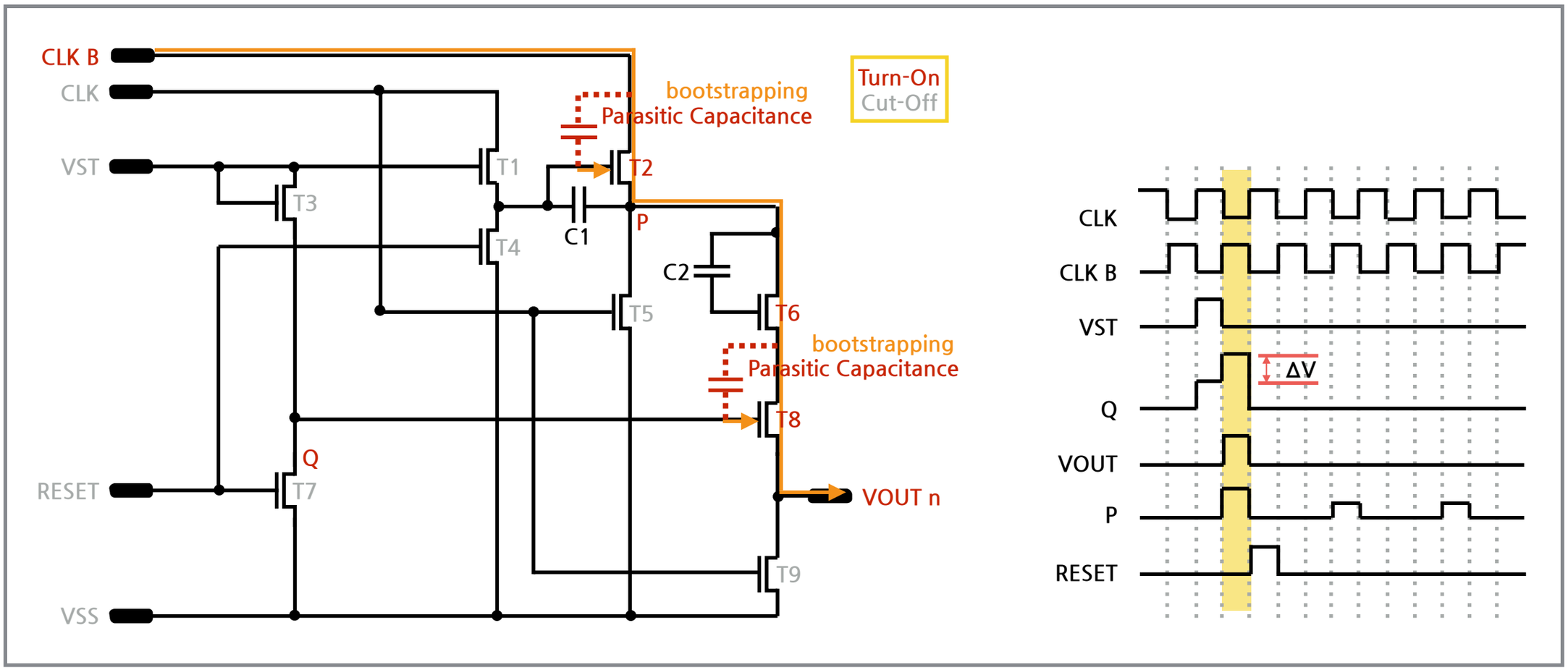
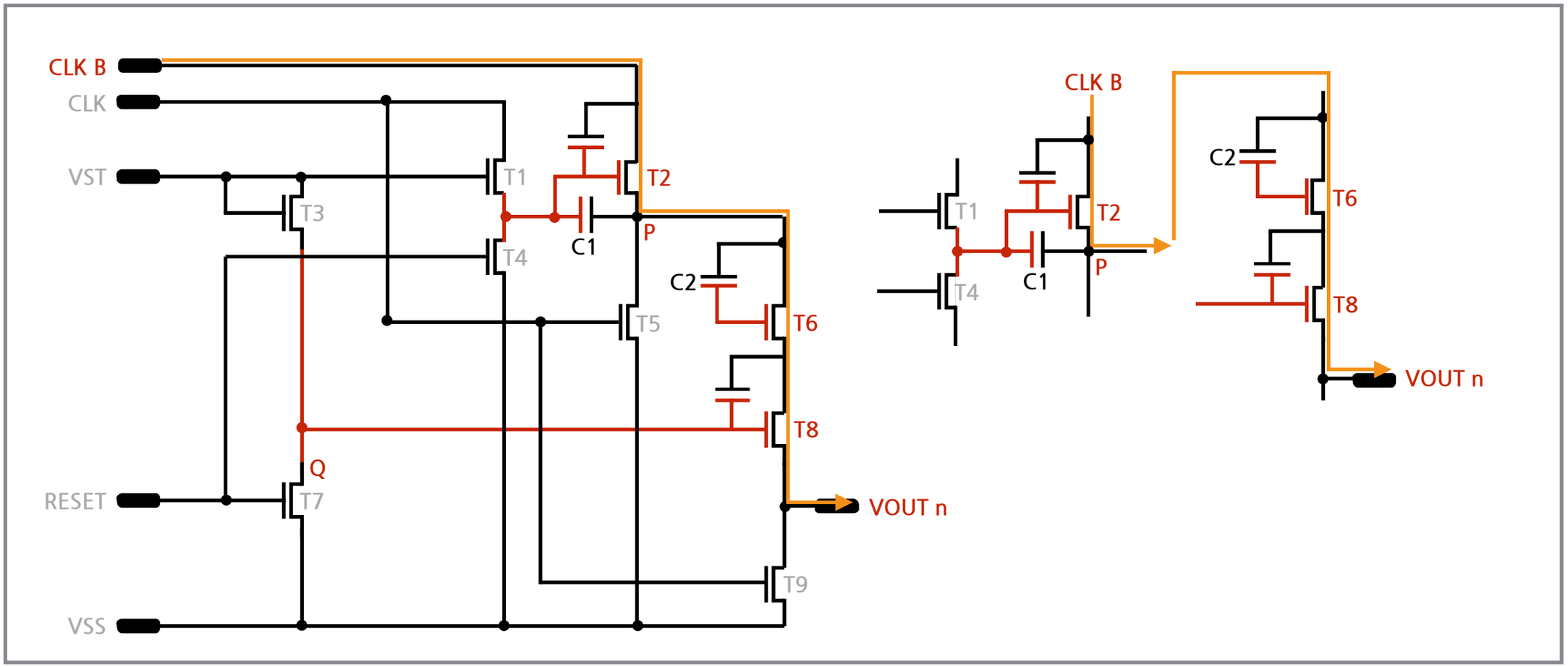


$$\Delta V = \frac{C1 + T2\text{의 } C_{GD}}{C1 + T2\text{의 } C_{GS} + T2\text{의 } C_{GD} + T2\text{의 } C_{GS} + T2\text{의 } C_{GD}} \times (V_{HIGH} - V_{LOW})$$

Oxide Gate Driver Circuit

Analyzing FINAL TYPE

SUNG KYUN KWAN UNIV
CHAN YOUNG PARK



$$\Delta V = \frac{C1 + T2\text{의 } C_{GD}}{C1 + T2\text{의 } C_{GS} + T2\text{의 } C_{GD} + T2\text{의 } C_{GS} + T2\text{의 } C_{GD}} \times (V_{HIGH} - V_{LOW})$$

Oxide Gate Driver Circuit

Analyzing FINAL TYPE

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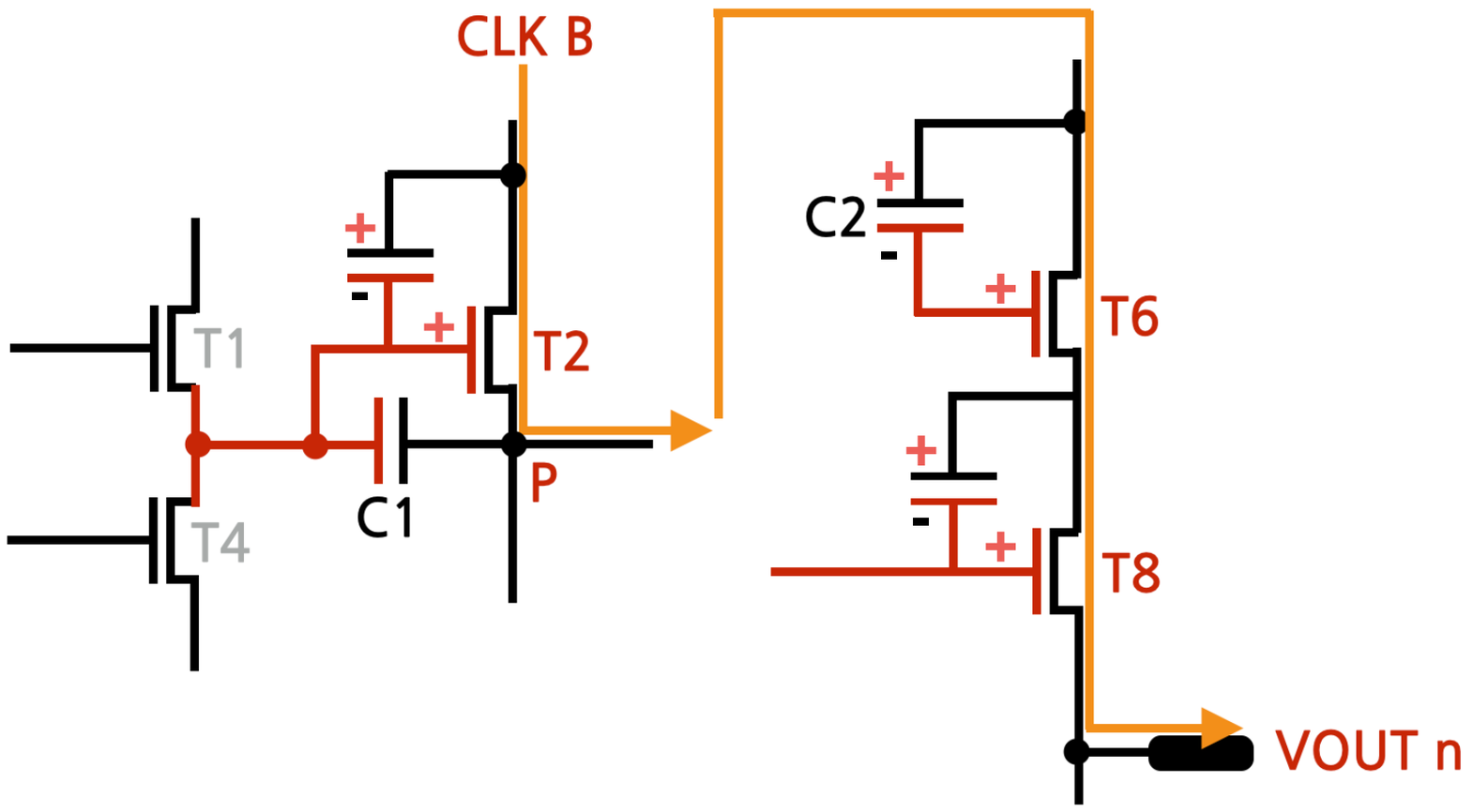

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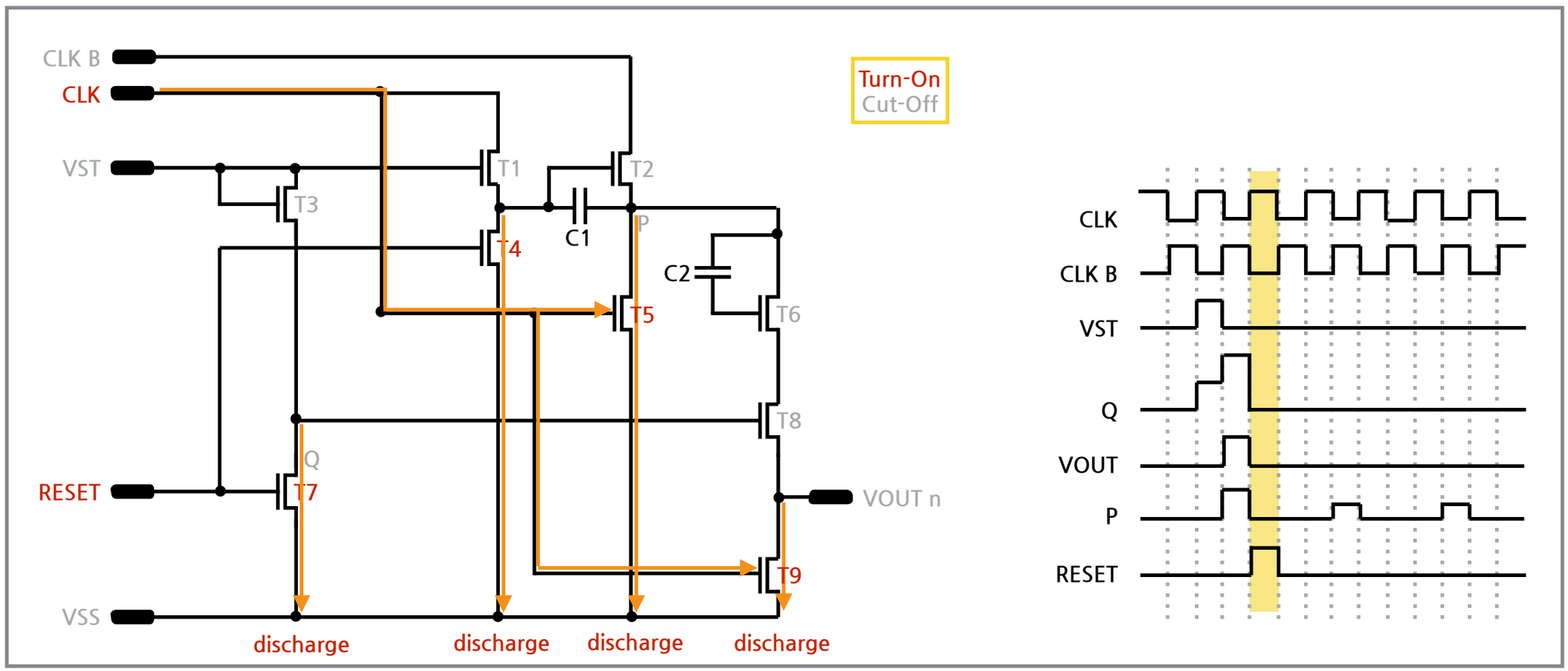
Oxide Gate Driver Circuit

Analyzing FINAL TYPE

SUNG KYUN KWAN UNIV
CHAN YOUNG PARK



Oxide Gate Driver Circuit

Analyzing FINAL TYPE

SUNG KYUN KWAN UNIV
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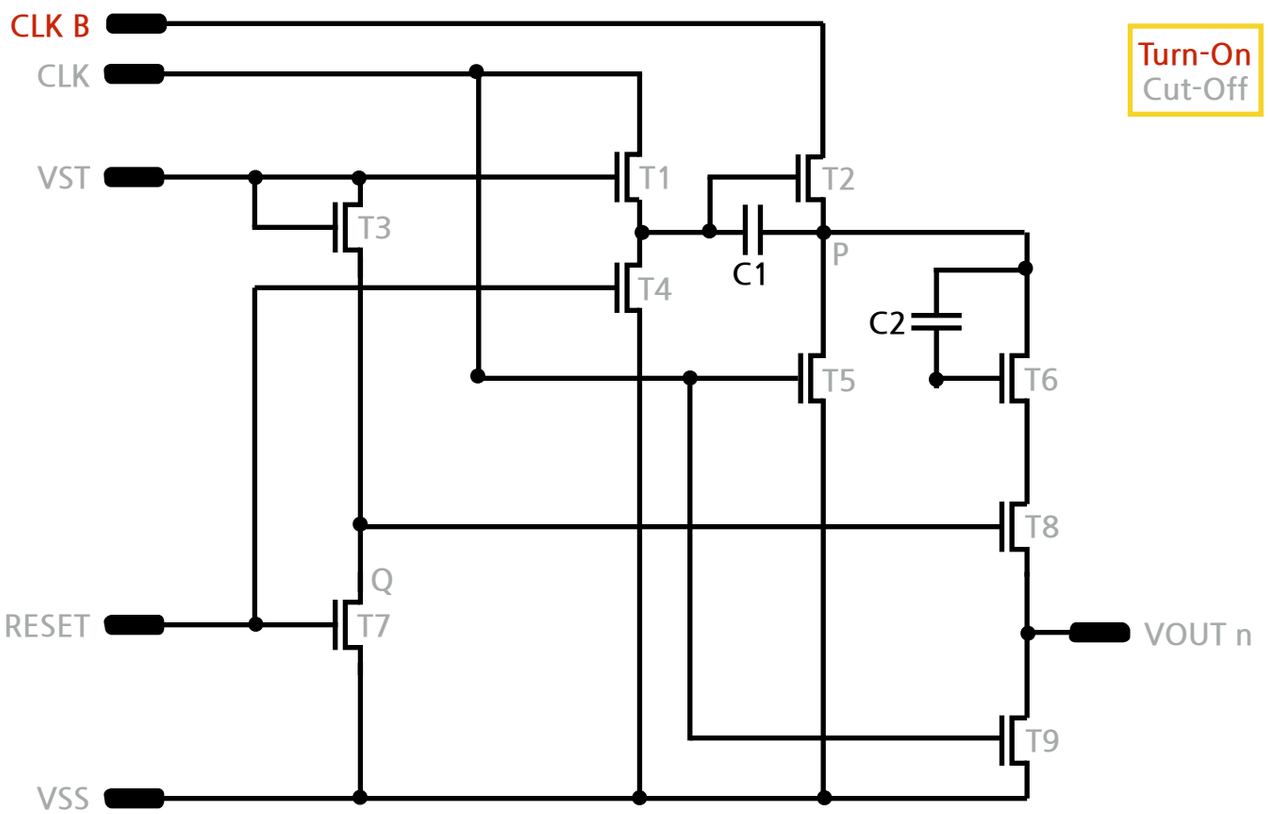
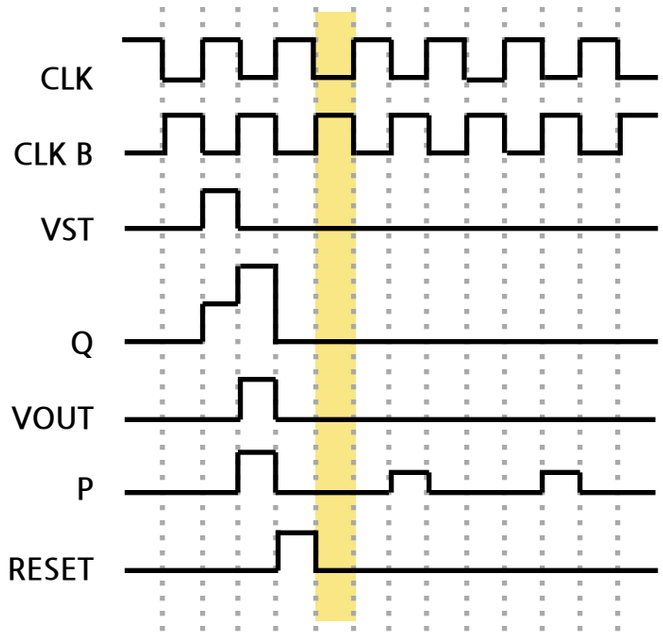


Turn-On
Cut-Off



Oxide Gate Driver Circuit

Analyzing FINAL TYPE

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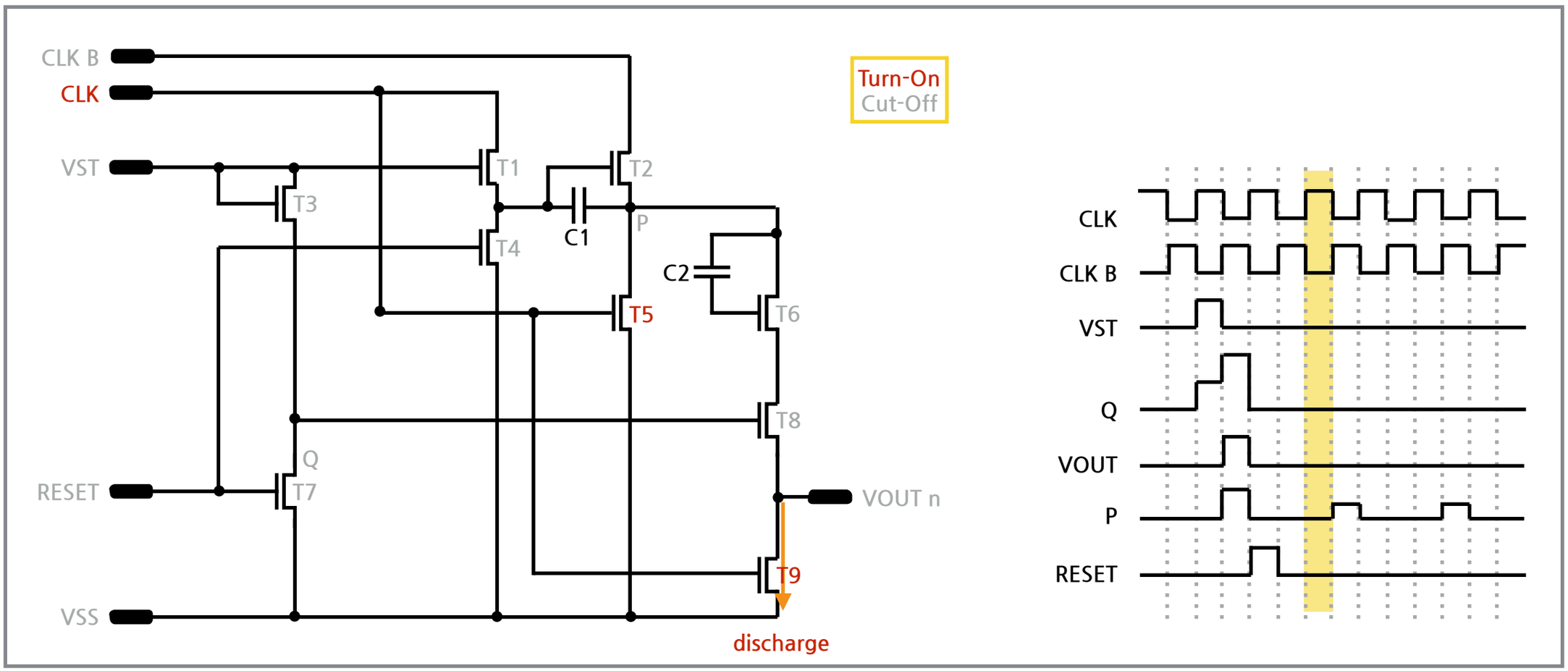

Oxide Gate Driver Circuit

Analyzing FINAL TYPE

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Parasitc Capacitance (or Stay Capacitance) is an unavidable and usually unwanted capacitance that exists between the parts of an electric component or circuit simply because of their proximity to each other. When two electrical conductors at different voltages are close together, the electric field between them causes electric charge to be stored on them; this effect is parasitic capacitance. All actual circuit elements such as inductors, diodes and transistors have internal capacitance, which can cause their behavior to depart from that of 'ideal' circuit elements. Additionally, there is always non-zero capacitance between any two conductors; this can be significant at higher frequencies with closely spaced conductors, such as wires or printed board traces. The parasitic capacitance between the turns of an inductor or other wound component is often described as self-capacitance. Howecer, self-capacitance of a conductive object is a different phenomenon, referring to the capacitance of the object without reference to another object.