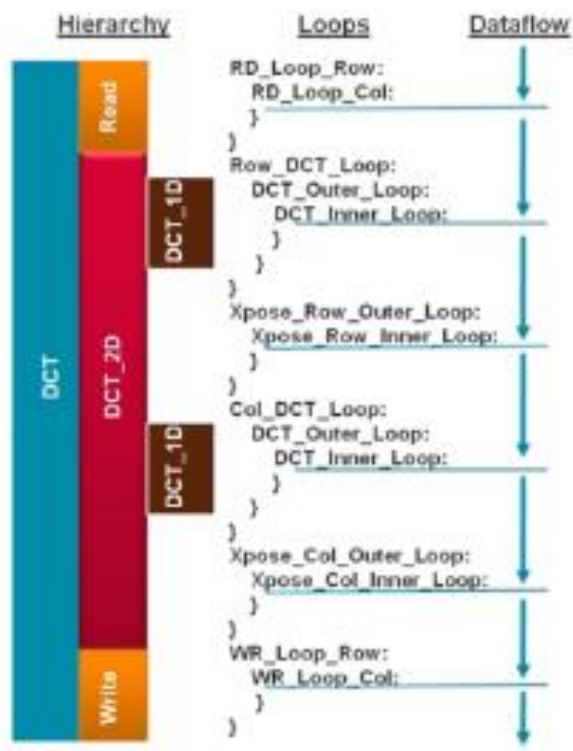


Github: [chaontuee/HLS Lab-A: This is for HLS Lab-A \(github.com\)](https://github.com/chaontuee/HLS_Lab-A)

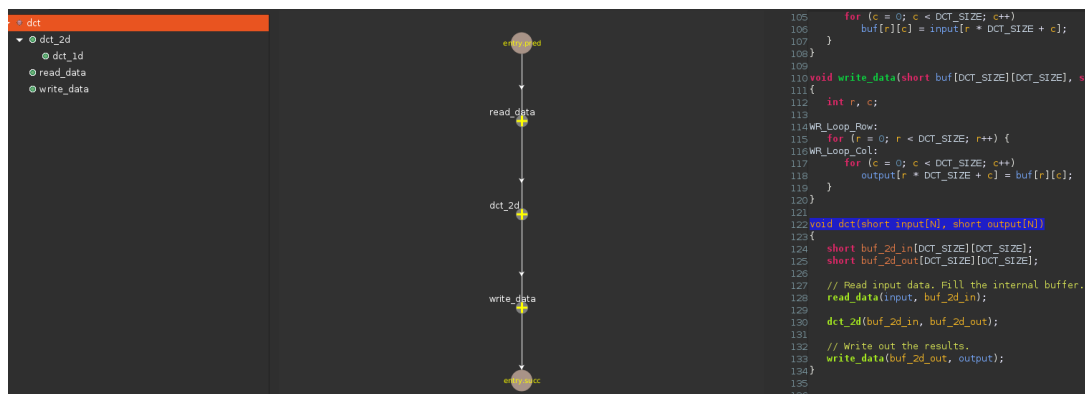
此次 Lab 參考步驟 [Vitis-Tutorials/Getting_Started/Vitis HLS at 2022.1 ·](https://www.xilinx.com/en/zh-CN/tutorials/vitis/vitis_hls_at_2022.1.html)

[Xilinx/Vitis-Tutorials \(github.com\)](https://www.xilinx.com/en/zh-CN/tutorials/vitis/vitis_hls_at_2022.1.html)，來了解如何分析資訊和 5 個幫助 optimize 的方式

DCT code structure, hierarchy:



dct



Dct_id

```

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39 subject only to applicable laws and regulations governing
40 liability.
41
42 THIS COPYRIGHT NOTICE AND DISCLAIMER MUST BE RETAINED
43 ALL TIMES.
44
45 *****
46 #include "dct.h"
47
48 void dct_id(dct_data_t src[DCT_SIZE], dct_data_t dst[DCT_SIZE])
49 {
50     unsigned int k, n;
51     int tmp;
52     const dct_data_t dct_coeff_table[DCT_SIZE][DCT_SIZE] = {
53         #include "dct_coeff_table.txt"
54     };
55
56 DCT_Outer_Loop:
57     for (k = 0; k < DCT_SIZE; k++) {
58 DCT_Inner_Loop:
59         for (n = 0; tmp = 0; n < DCT_SIZE; n++) {
60             int coeff = (int)dct_coeff_table[k][n];
61             tmp += src[n] * coeff;
62         }
63         dst[k] = DESCALE(tmp, CONST_BITS);
64     }
65 }
66
67 void dct_2d(dct_data_t in_block[DCT_SIZE][DCT_SIZE],
68            dct_data_t out_block[DCT_SIZE][DCT_SIZE])
69 {
70     dct_data_t row_outbuf[DCT_SIZE][DCT_SIZE];

```

Read/write

```

93 Xpose_Col_Inner_Loop:
94     for (i = 0; i < DCT_SIZE; i++)
95         out_block[i][i] = col_outbuf[i][i];
96 }
97
98 void read_data(short input[N], short buf[DCT_SIZE][DCT_SIZE])
99 {
100     int r, c;
101
102 RD_Loop_Row:
103     for (r = 0; r < DCT_SIZE; r++) {
104 RD_Loop_Col:
105         for (c = 0; c < DCT_SIZE; c++)
106             buf[r][c] = input[r * DCT_SIZE + c];
107     }
108 }
109
110 void write_data(short buf[DCT_SIZE][DCT_SIZE],
111                short output[N])
112 {
113     int r, c;
114 WR_Loop_Row:
115     for (r = 0; r < DCT_SIZE; r++) {
116 WR_Loop_Col:
117         for (c = 0; c < DCT_SIZE; c++)
118             output[r * DCT_SIZE + c] = buf[r][c];
119     }
120 }
121
122 void dct(short input[N], short output[N])
123 {
124     short buf_2d_in[DCT_SIZE][DCT_SIZE];
125     short buf_2d_out[DCT_SIZE][DCT_SIZE];

```

Latency:

Baseline:

Performance Estimates

* Timing:

Clock	Target	Estimated	Uncertainty
lap_clk	10.00 ns	4.159 ns	2.78 ns

* Latency:

Latency (cycles)	Latency (absolute)	Interval	Pipeline
min	max	min	max
415	415	4.150 us	4.150 us
416	416		

* Detail:

Instance	Module	Latency (cycles)	Latency (absolute)	Interval	Pipeline
		min	max	min	max
grp_dct_Pipeline_RD_Loop_Row_RD_Loop_Col_fu_70	dct_Pipeline_RD_Loop_Row_RD_Loop_Col	66	66	0.660 us	0.660 us
grp_dct_Pipeline_Row_DCT_Loop_DCT_Out_Loop_fu_78	dct_Pipeline_Row_DCT_Loop_DCT_Out_Loop	70	70	0.700 us	0.700 us
grp_dct_Pipeline_Xpose_Row_Out_Loop_Xpose_Row_Inner_Loop_fu_100	dct_Pipeline_Xpose_Row_Out_Loop_Xpose_Row_Inner_Loop	66	66	0.660 us	0.660 us
grp_dct_Pipeline_Col_DCT_Loop_DCT_Out_Loop_fu_106	dct_Pipeline_Col_DCT_Loop_DCT_Out_Loop	70	70	0.700 us	0.700 us
grp_dct_Pipeline_Xpose_Col_Out_Loop_Xpose_Col_Inner_Loop_fu_128	dct_Pipeline_Xpose_Col_Out_Loop_Xpose_Col_Inner_Loop	66	66	0.660 us	0.660 us
grp_dct_Pipeline_WR_Loop_Row_WR_Loop_Col_fu_134	dct_Pipeline_WR_Loop_Row_WR_Loop_Col	66	66	0.660 us	0.660 us

* Loop:
N/A

ConsoleErrorsWarningsGuidancePropertiesMan PagesGit RepositoriesModules/Loops

SynthesisCosimulation

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM	
dct	-	-	-	-	70	4.150E3	-	-	410	-	no	17	16	671	1992	0
dct_Pipeline_Row_DCT_Loop_DC	-	-	-	-	70	700.000	-	-	70	-	no	0	8	219	369	0
dct_Pipeline_Col_DCT_Loop_DCT	-	-	-	-	70	700.000	-	-	70	-	no	0	8	219	369	0
Row_DCT_Loop_DCT_Outer_Loop	-	-	-	-	70	680.000	-	-	6	64	yes	-	-	-	-	-
Col_DCT_Loop_DCT_Outer_Loop	-	-	-	-	68	680.000	-	-	6	64	yes	-	-	-	-	-
dct_Pipeline_RD_Loop_Row_RD	-	-	-	-	66	660.000	-	-	66	-	no	0	0	24	153	0
dct_Pipeline_Xpose_Row_Outer	-	-	-	-	66	660.000	-	-	66	-	no	0	0	24	166	0
dct_Pipeline_Xpose_Col_Outer_L	-	-	-	-	66	660.000	-	-	66	-	no	0	0	24	166	0
dct_Pipeline_WR_Loop_Row_WR	-	-	-	-	66	660.000	-	-	66	-	no	0	0	24	153	0
RD_Loop_Row_RD_Loop_Col	-	-	-	-	64	640.000	-	-	2	64	yes	-	-	-	-	-
Xpose_Row_Outer_Loop_Xpose_	-	-	-	-	64	640.000	-	-	2	64	yes	-	-	-	-	-
Xpose_Col_Outer_Loop_Xpose_C	-	-	-	-	64	640.000	-	-	2	64	yes	-	-	-	-	-
WR_Loop_Row_WR_Loop_Col	-	-	-	-	64	640.000	-	-	2	64	yes	-	-	-	-	-

Baseline with “#pragma HLS pipeline off”:

```

1228 void dct(short input[N], short output[N])
1229 {
1230     short buf_2d_in[DCT_SIZE][DCT_SIZE];
1231     short buf_2d_out[DCT_SIZE][DCT_SIZE];
1232     #pragma HLS pipeline off
1233     // Read input data. Fill the internal buffer.
1234     read_data(buf_2d_in, input);
1235     // Write out the results.
1236     write_data(buf_2d_out, output);
1237 }

```

Timing Estimate

Target	Estimated	Uncertainty
10.00 ns	2.564 ns	2.70 ns

Performance & Resource Estimates

</

synthesis log to list what steps the tool takes during synthesis:

```

27 INFO: [HLS 200-777] Using interface defaults for 'Vivado' flow target.
28 INFO: [HLS 214-198] Inlining function 'dct_2d(short (*) [8], short (*) [8])' into 'dct(short*, short*)' (dct.cpp:59:10)
29 INFO: [HLS 214-178] Inlining function 'read_data(short*, short (*) [8])' into 'dct(short*, short*)' (dct.cpp:123:0)
30 INFO: [HLS 214-178] Inlining function 'dct_2d(short (*) [8], short (*) [8])' into 'dct(short*, short*)' (dct.cpp:123:0)
31 INFO: [HLS 214-178] Inlining function 'write_data(short (*) [8], short*)' into 'dct(short*, short*)' (dct.cpp:123:0)
32 INFO: [HLS 200-111] Finished Compiling Optimization and Transform: CPU user time: 1.98 seconds, CPU system time: 0.16 seconds, Elapsed time: 2.6 seconds; current allocated memory: 212.883 MB.
33 INFO: [HLS 200-111] Finished Checking Pragmas: CPU user time: 0 seconds, CPU system time: 0 seconds, Elapsed time: 0 seconds; current allocated memory: 212.883 MB.

```

```

Implementing module 'dct_Pipeline_RD_Loop_Row_RD_Loop_Col'
Implementing module 'dct_Pipeline_Row_DCT_Loop_DCT_Outer_Loop'
Implementing module
'dct_Pipeline_Xpose_Row_Outer_Loop_Xpose_Row_Inner_Loop'
Implementing module 'dct_Pipeline_Col_DCT_Loop_DCT_Outer_Loop'

```

Implementing module

'dct_Pipeline_Xpose_Col_Outer_Loop_Xpose_Col_Inner_Loop'

Implementing module 'dct_Pipeline_WR_Loop_Row_WR_Loop_Col'

Implementing module 'dct'

Generating RTL for module 'dct_Pipeline_RD_Loop_Row_RD_Loop_Col'

Generating RTL for module 'dct_Pipeline_Row_DCT_Loop_DCT_Outer_Loop'

Pipelining result : Target II = NA, Final II = 1, Depth = 2, loop 'RD_Loop_Row_RD_Loop_Col'

Pipelining result : Target II = NA, Final II = 1, Depth = 6, loop 'Row_DCT_Loop_DCT_Outer_Loop'

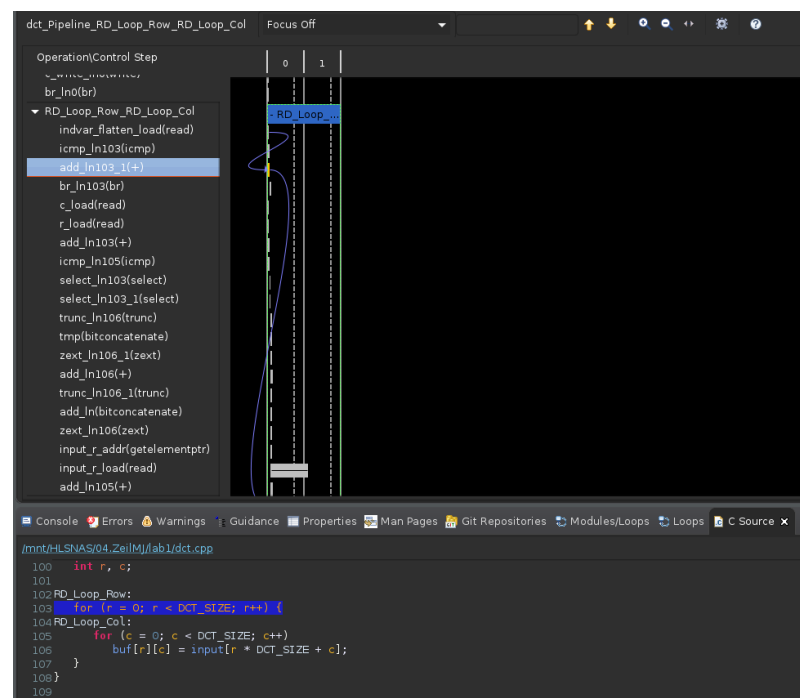
Pipelining result : Target II = NA, Final II = 1, Depth = 2, loop 'Xpose_Row_Outer_Loop_Xpose_Row_Inner_Loop'

Pipelining result : Target II = NA, Final II = 1, Depth = 6, loop 'Col_DCT_Loop_DCT_Outer_Loop'

Pipelining result : Target II = NA, Final II = 1, Depth = 2, loop 'Xpose_Col_Outer_Loop_Xpose_Col_Inner_Loop'

Pipelining result : Target II = NA, Final II = 1, Depth = 2, loop 'WR_Loop_Row_WR_Loop_Col'

Schedule Viewer baseline:



latency, iteration latency

Performance & Resource Estimates								
Modules & Loops								
	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval
dct				-	415	4.150E3	-	416
dct_Pipeline_RD_Loop_Row_RD_Loop_Col				-	66	660.000	-	66
dct_Pipeline_Row_DCT_Loop_DCT_Outer_Loop				-	70	700.000	-	70
dct_Pipeline_Xpose_Row_Outer_Loop_Xpose_Row_Inner_Loop				-	66	660.000	-	66
dct_Pipeline_Col_DCT_Loop_DCT_Outer_Loop				-	70	700.000	-	70
dct_Pipeline_Xpose_Col_Outer_Loop_Xpose_Col_Inner_Loop				-	66	660.000	-	66
dct_Pipeline_WR_Loop_Row_WR_Loop_Col				-	66	660.000	-	66

dct.cpp compare reports Co-simulation Report(solution6) x

Cosimulation Report for 'dct'

General Information

Date: Fri 14 Oct 2022 06:05:08 PM CST
Version: 2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022)
Project: dct_prj
Status: Pass

Solution: solution6 (Vivado IP Flow Target)
Product family: virtexuplus
Target device: xcvu9p-flgb2104-1-e

Cosim Options

Tool: Vivado XSIM RTL: Verilog
Dump Trace: all

Performance Estimates

Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency
dct				594	594	594
read_data				64	64	64
dct_2d				464	464	464
write_data				64	64	64

```

graph TD
    input_r --> read_data_U0
    read_data_U0 --> dct_2d_U0
    dct_2d_U0 --> write_data_U0
    write_data_U0 --> output_r
  
```

Console Errors Warnings Guidance Properties Man Pages Git Repositories Modules/Loops Dataflow x

Name	Cosim Category	Cosim Stalling Time	FIFO EMPTY	FIFO FULL	Cosim Stall No Start	Cosim Stall No Continue	Cosim AVG II	Cosim Max II	Cosim Min II	Cosim AVG Latency
read_data_U0	none	0.00%	0.00%	0.00%	0.00%	0.00%	N/A	N/A	N/A	64
dct_2d_U0	none	0.00%	0.00%	0.00%	0.00%	0.00%	N/A	N/A	N/A	464
write_data_U0	none	0.00%	0.00%	0.00%	0.00%	0.00%	N/A	N/A	N/A	64

The biggest problem is that I can't borrow board since they are rent by others...