ECEN620 HW2

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1. Phase Detector Characterization.

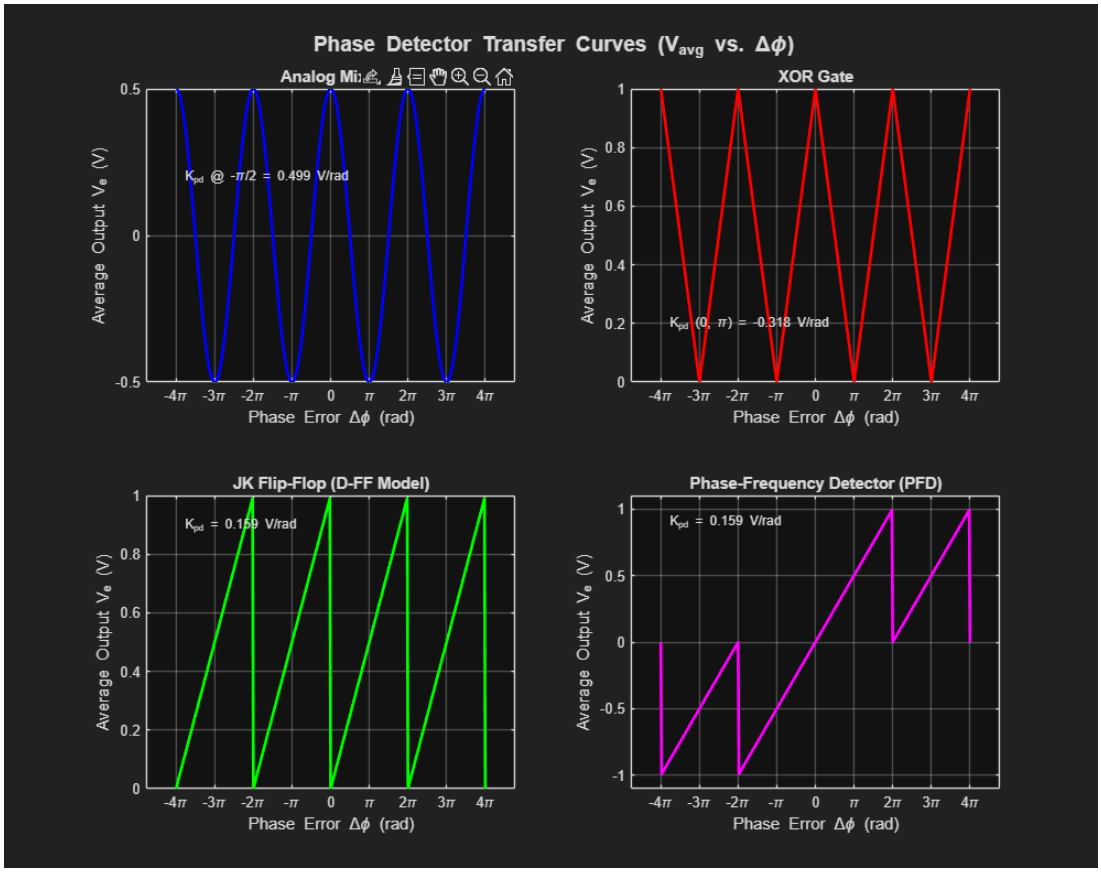

Figure 1. Transfer Curves (avg(Ve) vs Φe)

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--- Simulation Results: avg(ve) ---
Phase Detector          |  f_fb = 0.50x f_ref |  f_fb = 0.75x f_ref |  f_fb = 1.50x f_ref |  f_fb = 2.00x f_ref
-------------------------------------------------------------------------------------------
Analog Mixer            |      +0.0000 V      |      +0.0000 V      |      +0.0000 V      |      +0.0001 V
XOR Gate                |      +0.4994 V      |      +0.4995 V      |      +0.4991 V      |      +0.4989 V
JK Flip-Flop            |      +0.5000 V      |      +0.5000 V      |      +0.5000 V      |      +0.0000 V
PFD                     |      +0.5000 V      |      +0.5012 V      |      -0.4975 V      |      -0.5000 V
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Figure 2. average output with ffb=0.5, 0.75, 1.5, and 2fref

The simulation values reveal that only the Phase-Frequency Detector (PFD) is truly useful as a frequency detector. The other circuits are poor at this task because

they lack the ability to provide directional information.

2. Phase-Frequency Detector Design.

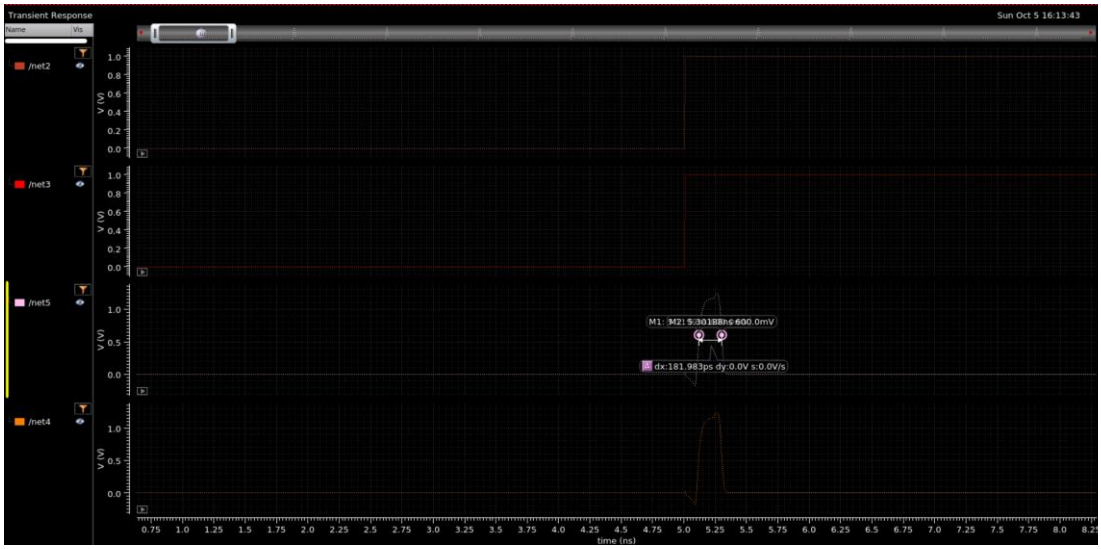

Figure 3. PFD output pulse=182ps>100ps

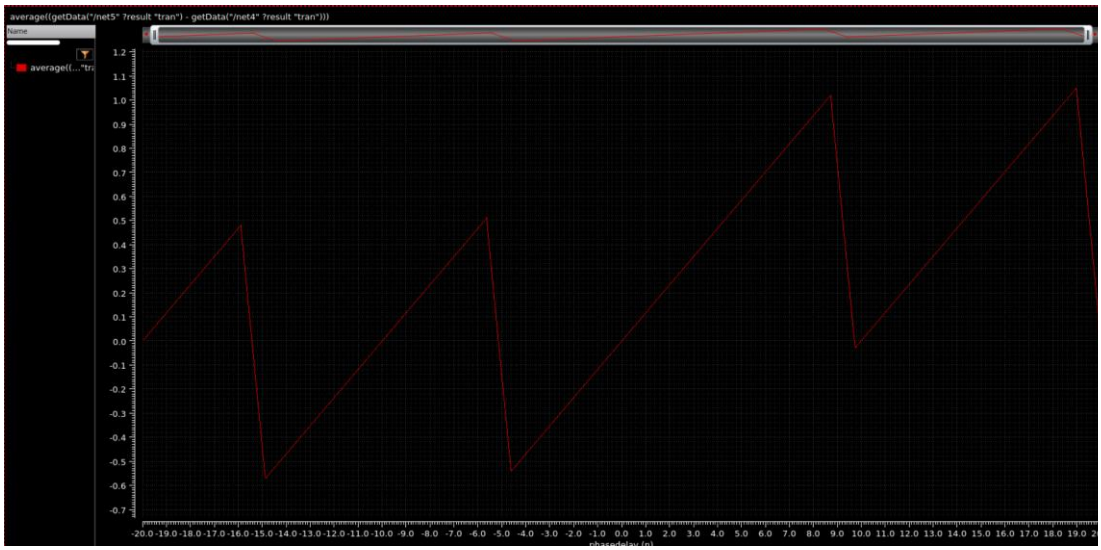

Figure 4. This simulation result with Reset Delay.

3. Charge Pump Design.

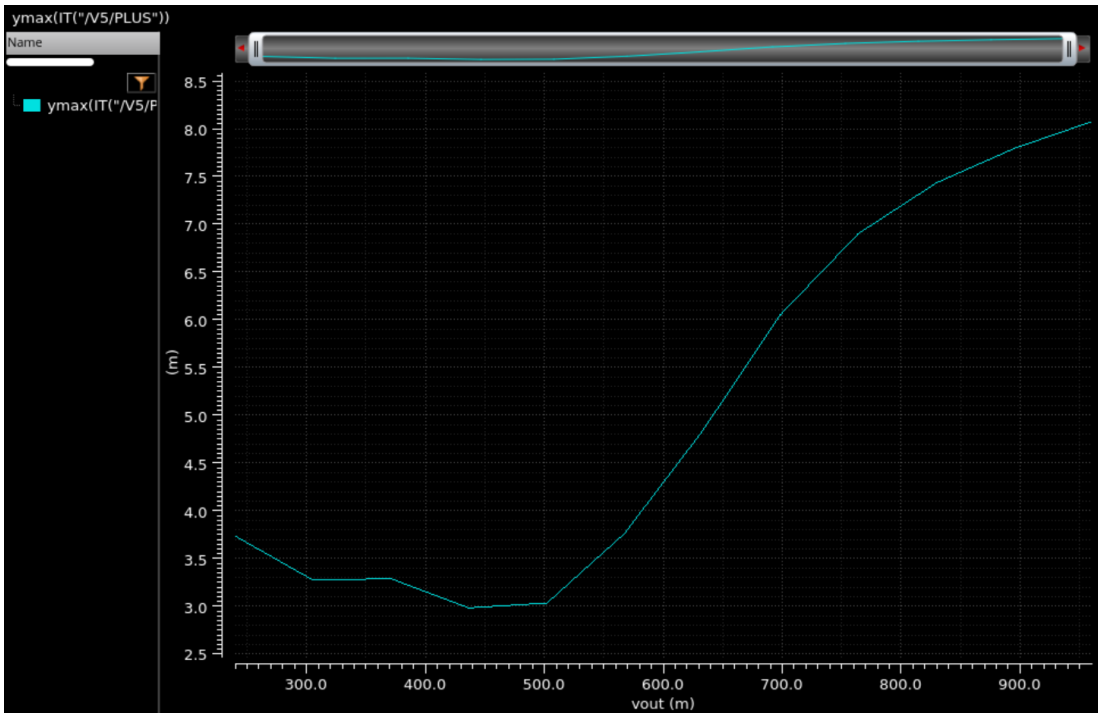

Figure 5. (3-a)Peak (absolute value) Transient Iout

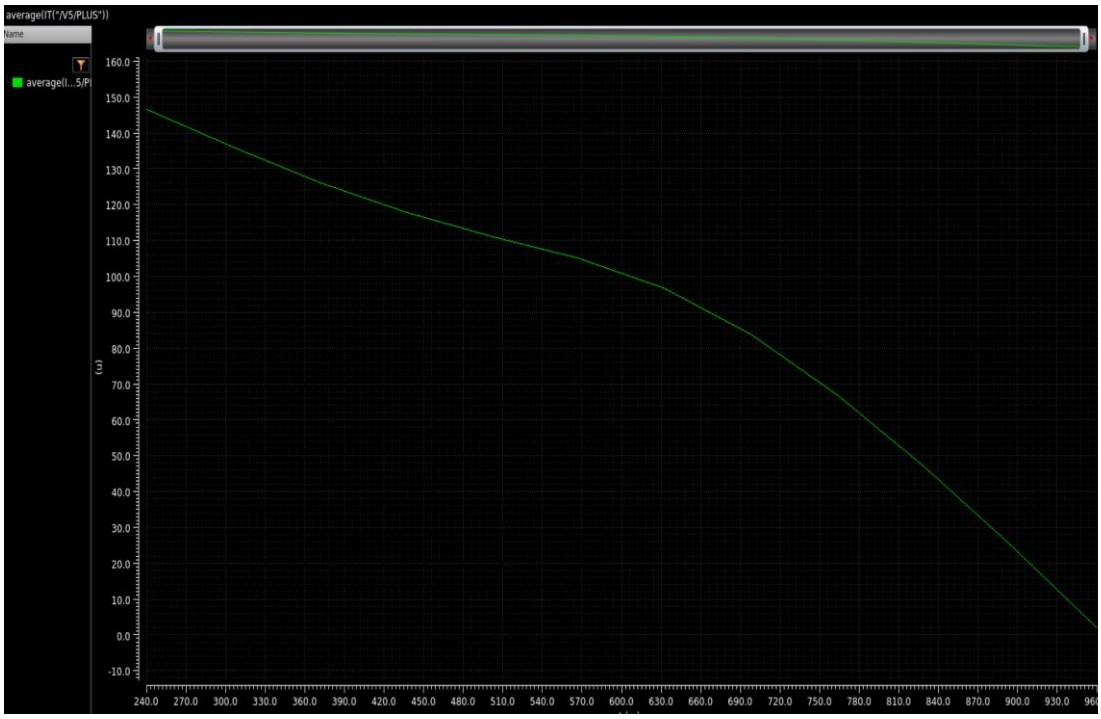

Figure 6. (3-a) Average Iout

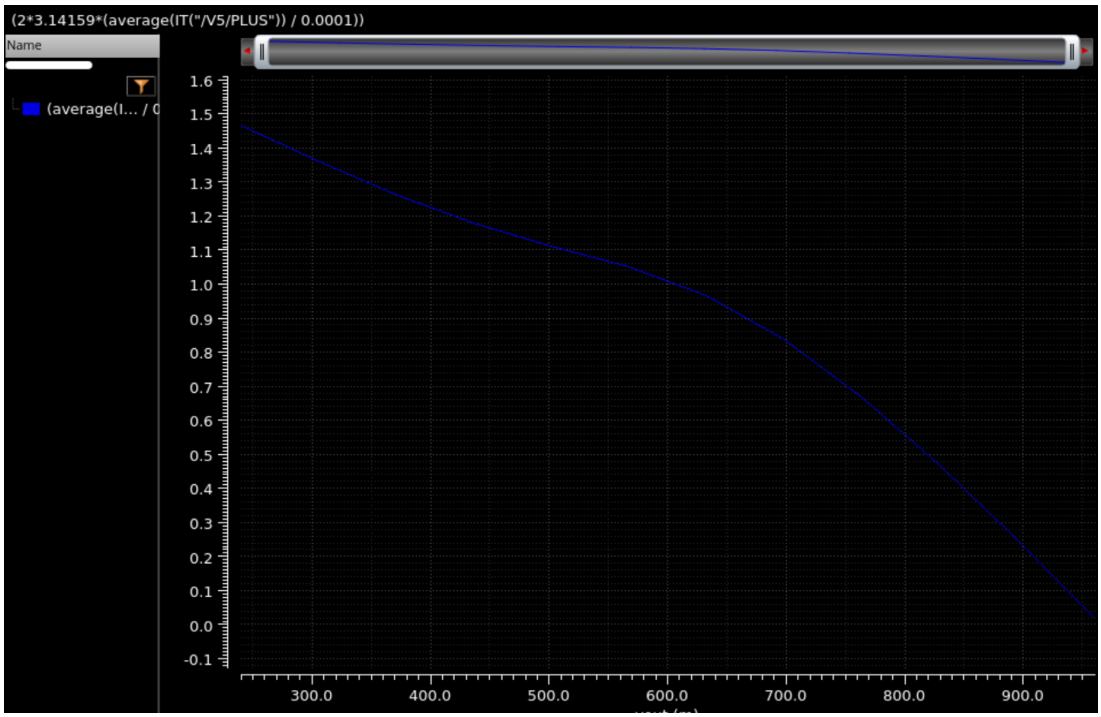

Figure 7. (3-a)Phase Error

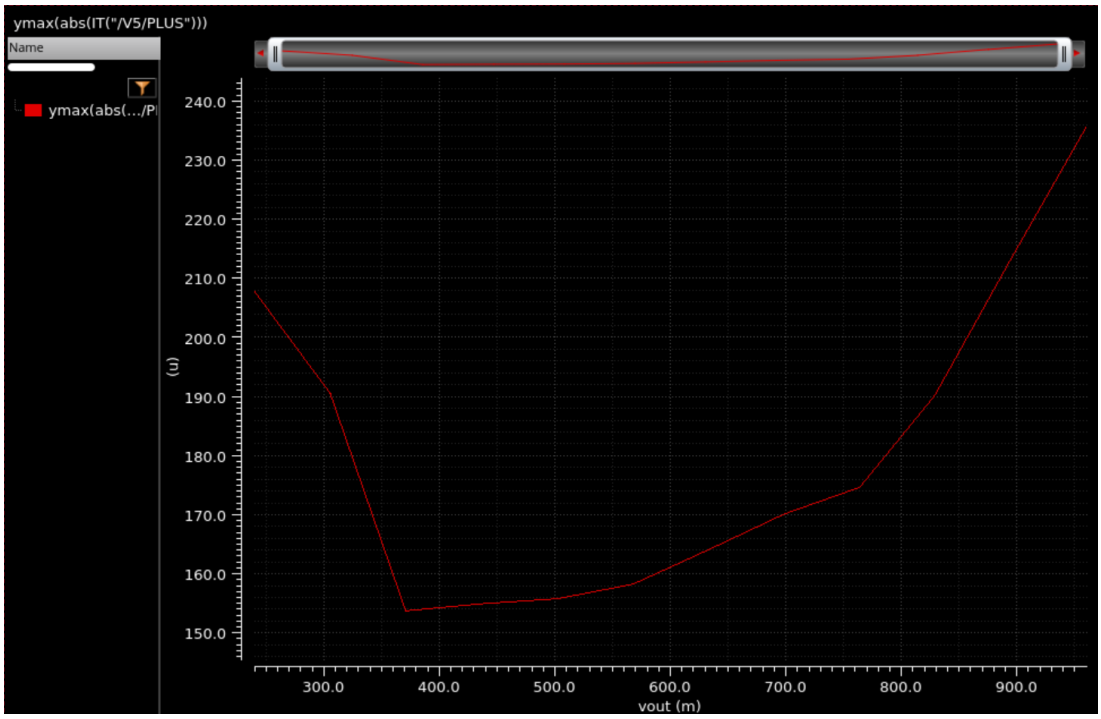

Figure 8. (3-b)Peak (absolute value) Transient Iout

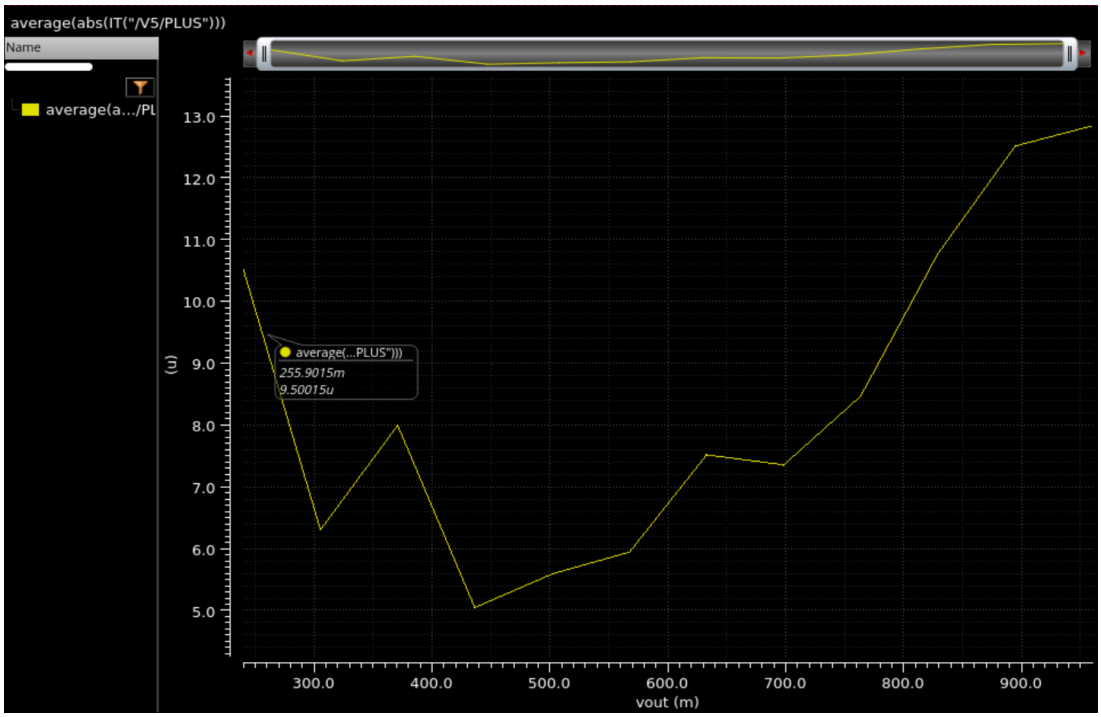

Figure 9. (3-b)Average Iout

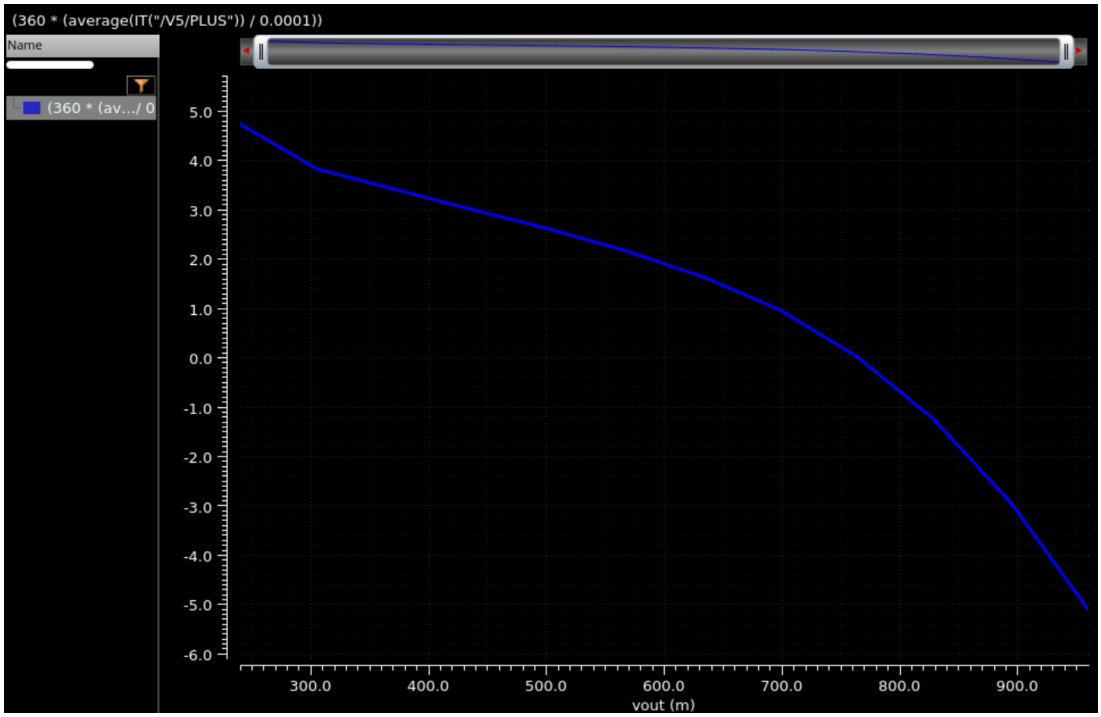

Figure 10. (3-b)Phase Error

3-c. Implementing feedback biasing in the PLL makes its performance stable and predictable against variations in

the manufacturing Process, supply Voltage, and operating Temperature (PVT). Feedback biasing uses a control loop (an op-amp) to create a self-correcting mechanism that maintains a constant, desired parameter despite PVT variations