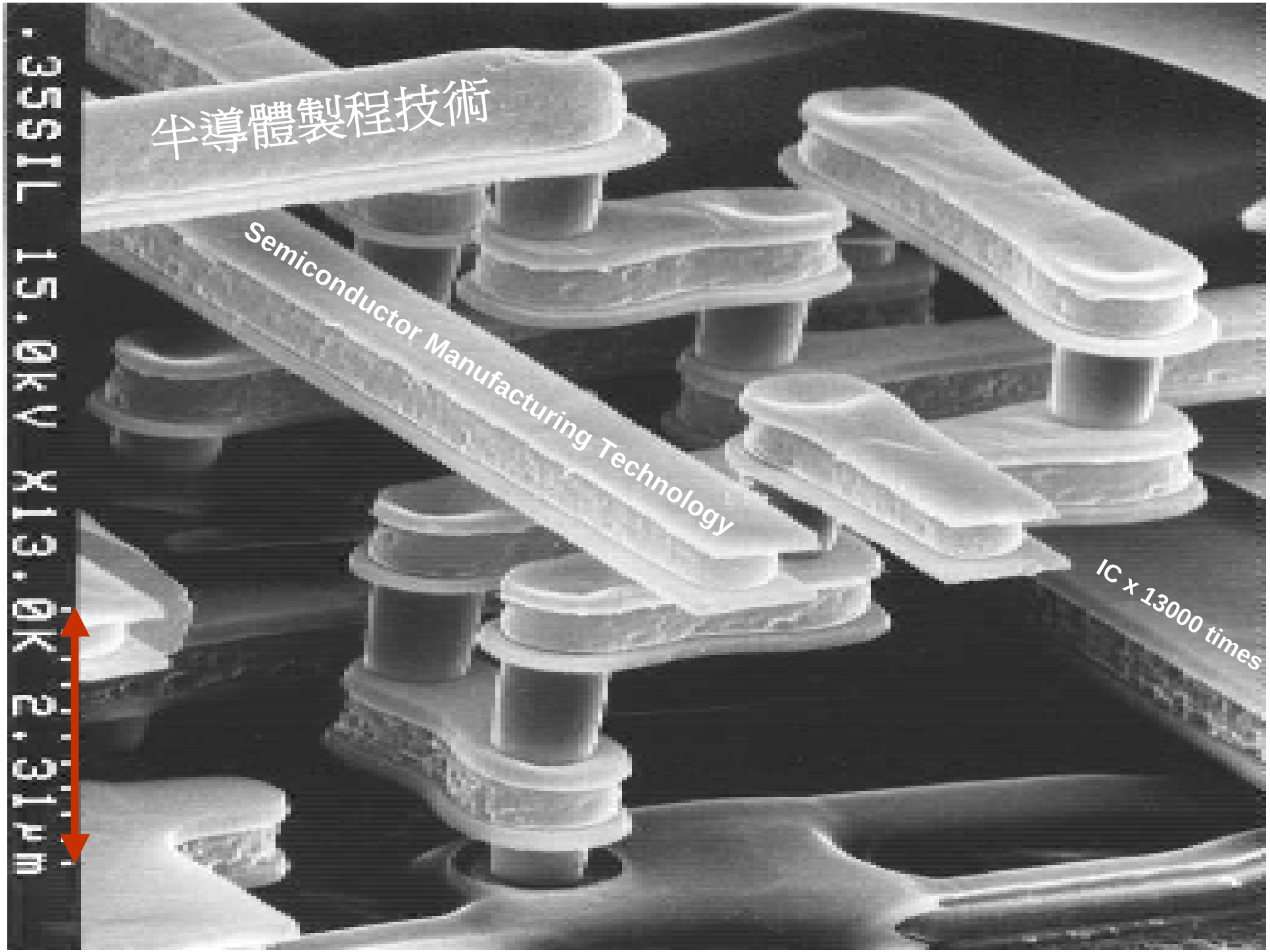
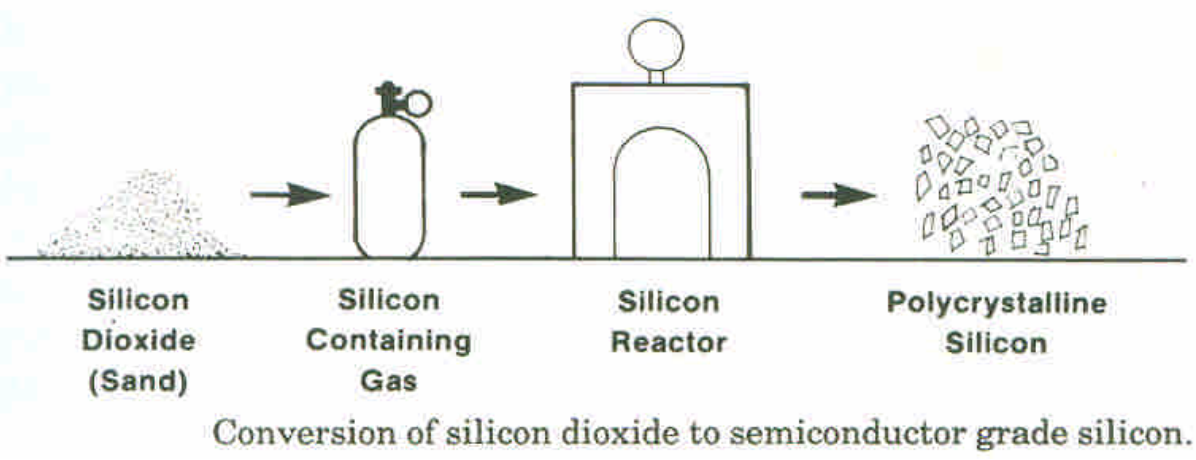
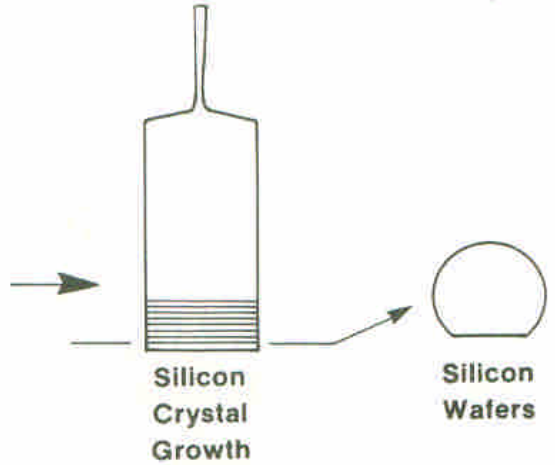

半導體製程技術
Semiconductor Manufacturing Technology
IC x 13000 times
3511 15.0kV X13,0K 2.31μm

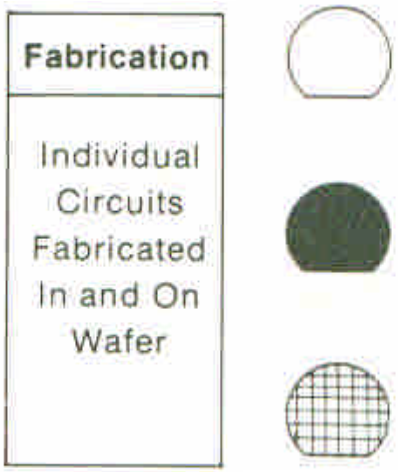
IC 製造基本流程

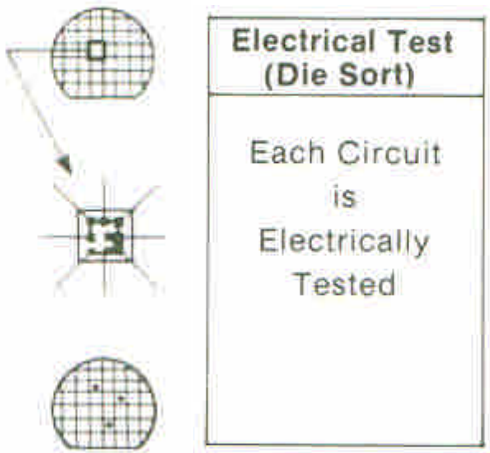


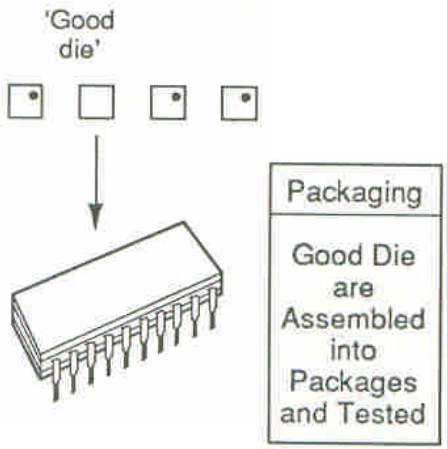
Conversion of silicon dioxide to semiconductor grade silicon.



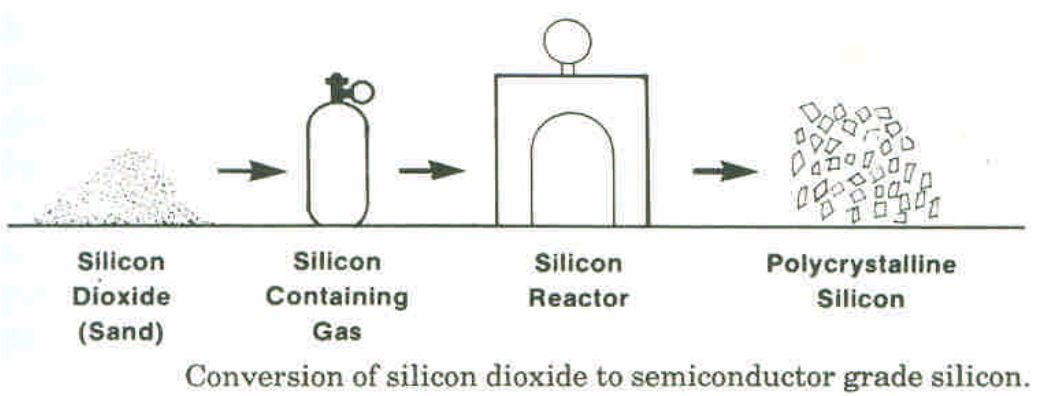
Crystal growth and wafer prep





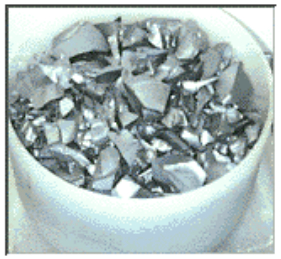


單晶塊材成長 (Bulk Crystal Growth)

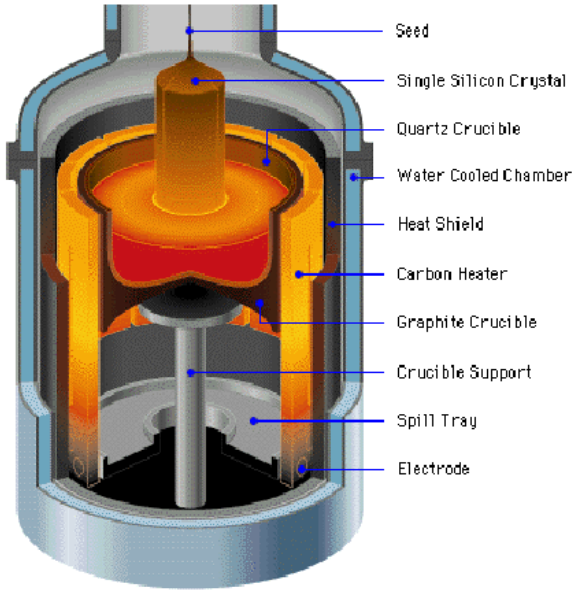


Conversion of silicon dioxide to semiconductor grade silicon.

Raw materials (polycystalline Si)



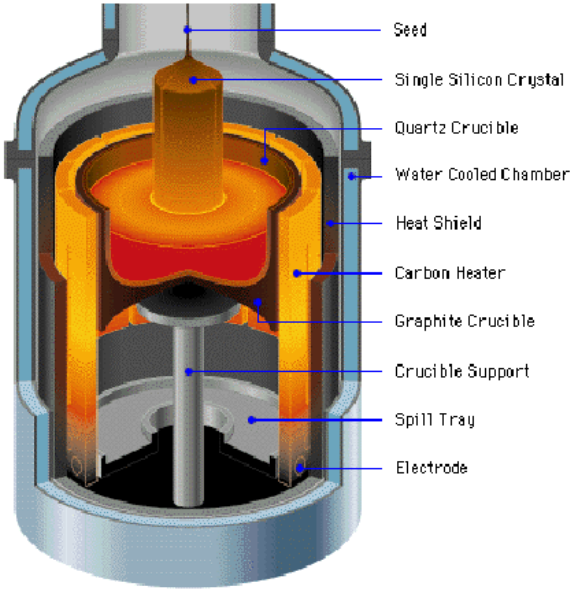
CZ-furnace

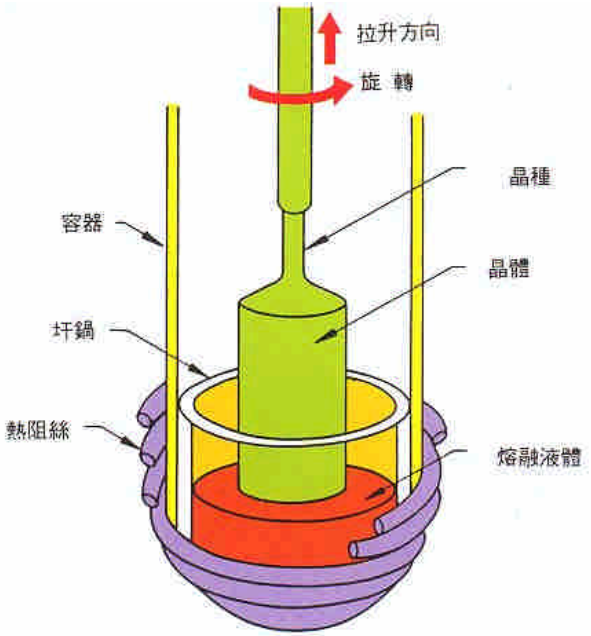


矽單晶通常以柴氏法或浮區法成長。圖爲柴氏法成長單晶示意圖。大致上是將矽鍋中，盛有高純度矽的熔融液(維持在矽熔點攝氏1414度以上的高溫)利用長條狀的晶種與熔液接觸，再緩緩升起。單晶在固體晶種與熔液界面成長。目前矽單晶成長技術已相當成熟，可長成一米長，直徑超過二十公分的龐大晶體。其純度可達到每十億矽原子中僅含一個雜質原子 (像一個外國人躋身於十億人口的中國大陸一樣，比例非常低) ，而晶體中幾乎全無缺陷。

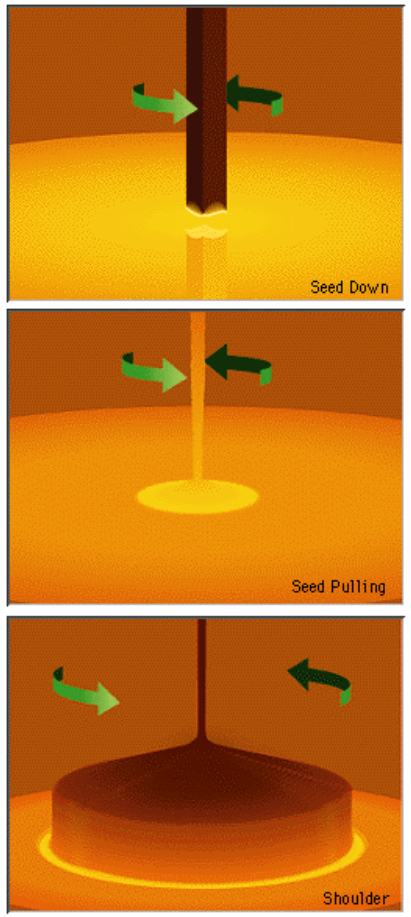
單晶塊材成長 (Bulk Crystal Growth)

CZ-furnace



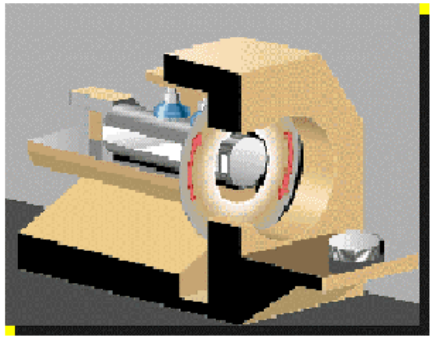


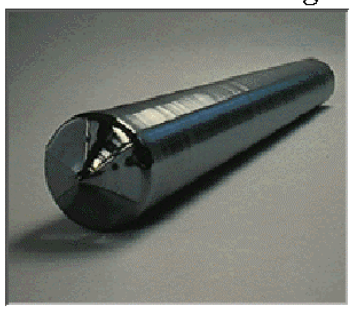
ingot is pulled from the melt



晶圓 (Wafer)

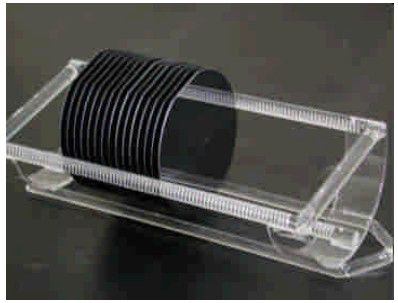
wafers are cut from the ingot using a rotating diamond saw



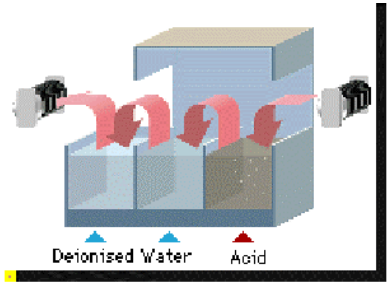


ingot

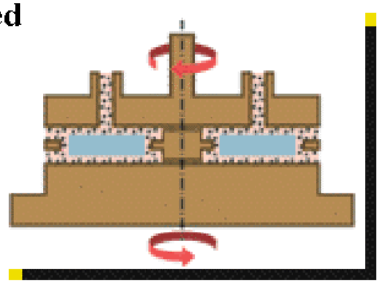
長成的圓柱形矽晶棒首先經切割成晶片。晶片的厚度選取隨其直徑增加而增加，一般約數百微米。切割好的晶片再經機械研磨及化學侵蝕，將表面磨光平滑如鏡，即成爲積體電路基底的晶圓。

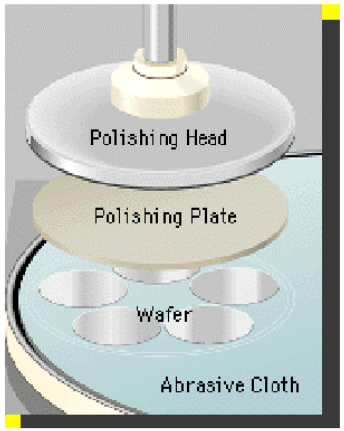


etching to remove damage



next the wafers are lapped to improve flatness and reduce roughness



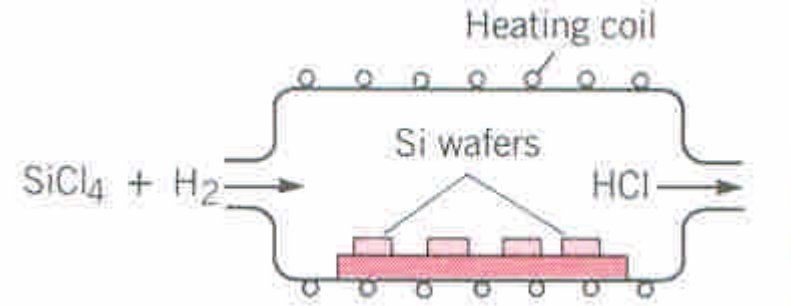


and then the edges are beveled

before the wafers are polished...

and ready for use!

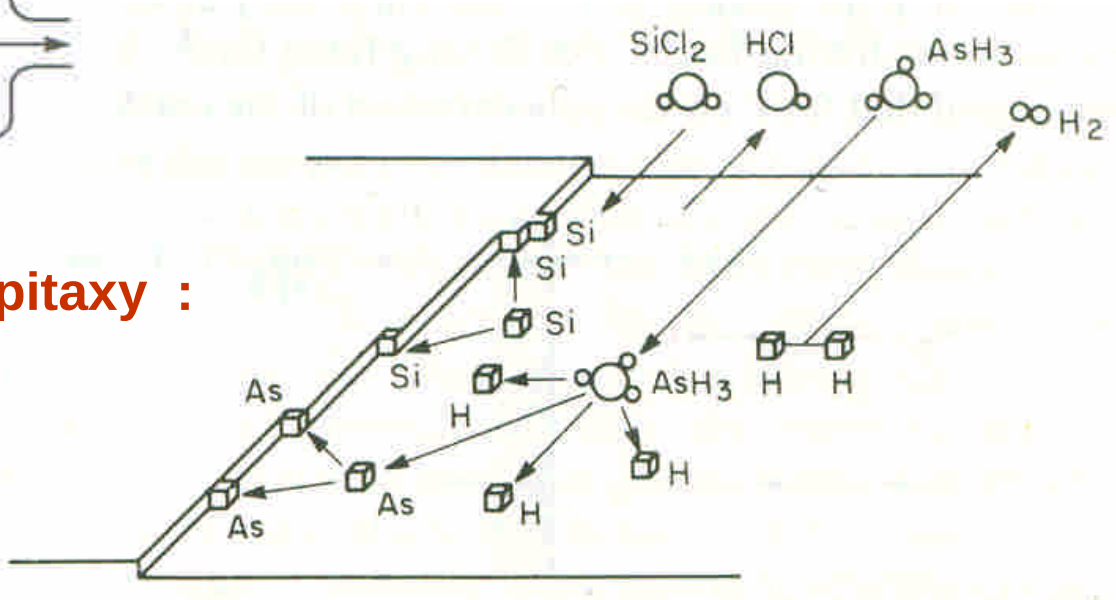
單晶成長 – 磊晶 (Epitaxy Layer Growth)



example of vapor phase epitaxy ：

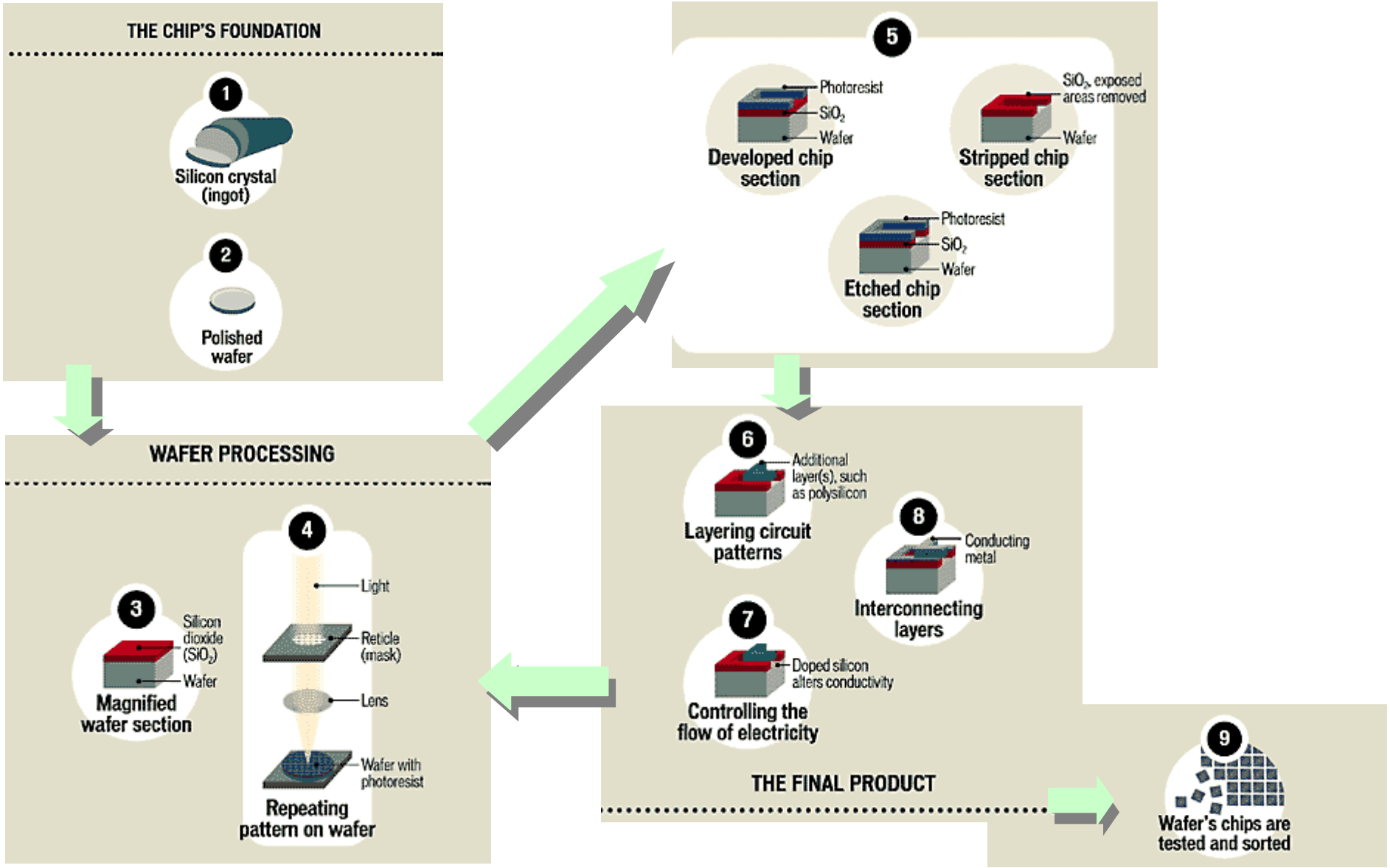
$SiCl_4 + 2H_2 \rightarrow Si + 4\ HCl$

(@ 1250 ^oC)



磊晶矽薄膜的純度高、缺陷少、性質佳，但其製程溫度最高、難度最高，因此在元件應用上有其限制，一般用在積體電路製程最前段。複晶矽薄膜則在積體電路中應用極廣，這要歸功於其製程溫度較低，耐高溫，與二氧化矽界面特性佳，可靠度好，而且能均勻覆蓋不平坦的結構。另一方面，更低溫複晶矽薄膜製程，則是用在以玻璃爲基材的液晶顯示器薄膜電晶體。

IC 晶圓製造流程 (IC Wafer Fabrication Process Flow)



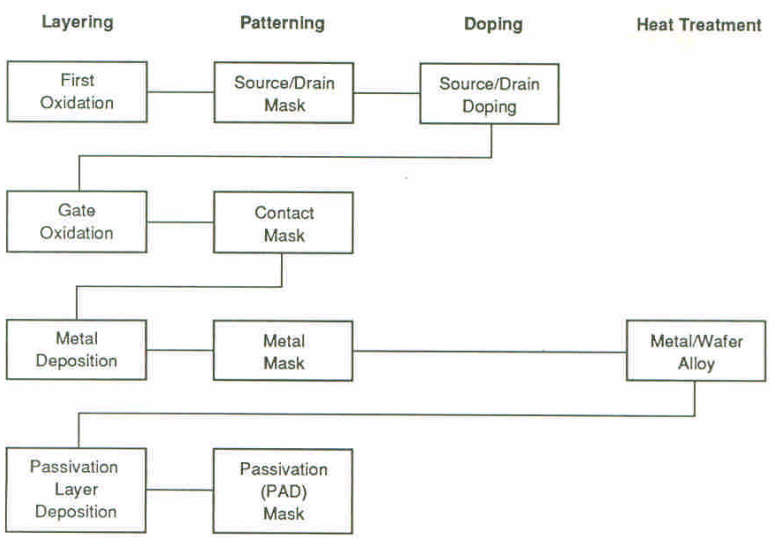
IC 晶圓製造技術 (IC Wafer Fabrication Techniques)

Operation	Purpose	Techniques
Layering	Grow or deposit a thin layer on the wafer surface.	Oxidation Atmospheric Pressure High Pressure CVD Epi Low Pressure Plasma Evaporation Metals Sputtering Metals Insulators
Patterning	Selective removal of the top LAYER(s) on the wafer.	Resist Positive Negative Exposure Contact Proximity Projection Direct Step E Beam X Ray Etch Wet Dry Lift-Off Ion Milling RIE

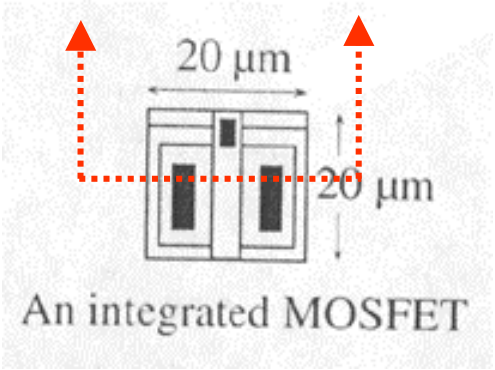
IC 晶圓製造技術 (IC Wafer Fabrication Techniques)

Operation	Purpose	Techniques
Doping	Change conductivity type and resistivity of selected portions of the wafer surface.	Thermal Diffusion Open Tube Closed Tube Doped Film Ion Implantation
Heat Treatments	Heat and/or cool the wafer for various effects.	Heat Hot Plate Convection IR Cool Freeze plate

Metal Gate MOS Process Flow



cross section view

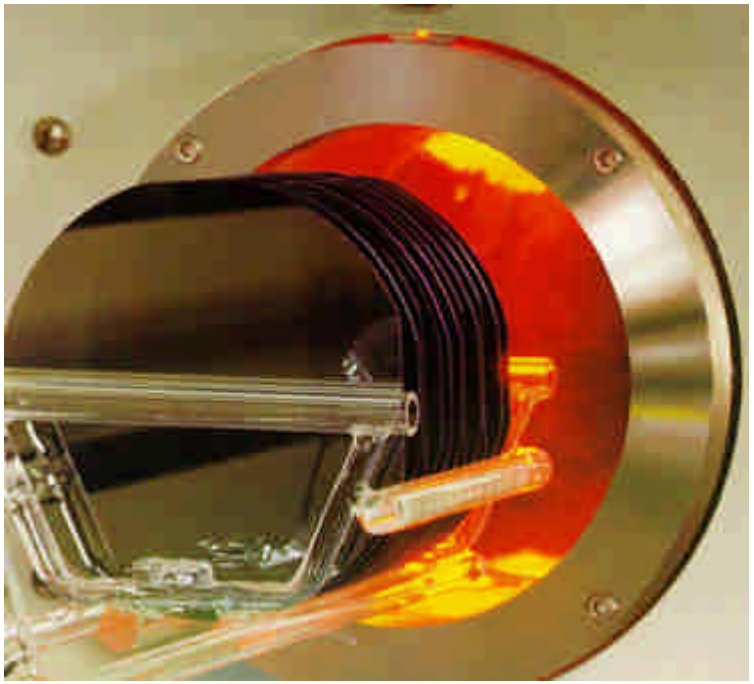


Cross Section	Step	Operation	Name/Purpose
		Starting wafer	
	1	Layering	Field Oxide
	2	Patterning	Source/drain holes
	3	Doping Layering	N-type doping and reoxidation of source/drain
	4	Patterning	Gate region is formed
	5	Layering	Gate oxide is grown
	6	Patterning	Contact holes are patterned into source/drain regions
	7	Layering	Conducting metal layer is deposited
	8	Patterning	Metal layer is patterned
	9	Heat Treatment	Metal is alloyed to layer
	10	Layering	Protective passivation layer is deposited
	11	Patterning	Passivation layer is removed over metal pads

絕緣層披覆 – 氧化 (Oxidation)

處理晶元的最先步驟，通常爲在矽晶上成長二氧化矽絕緣層。二氧化矽可由矽晶在氧化氣氛中加熱生成。依需要氧化氣氛可爲氧氣或水蒸氣。而加熱溫度則在攝氏900一1000度間。加熱時間則由所需氧化層厚度決定。

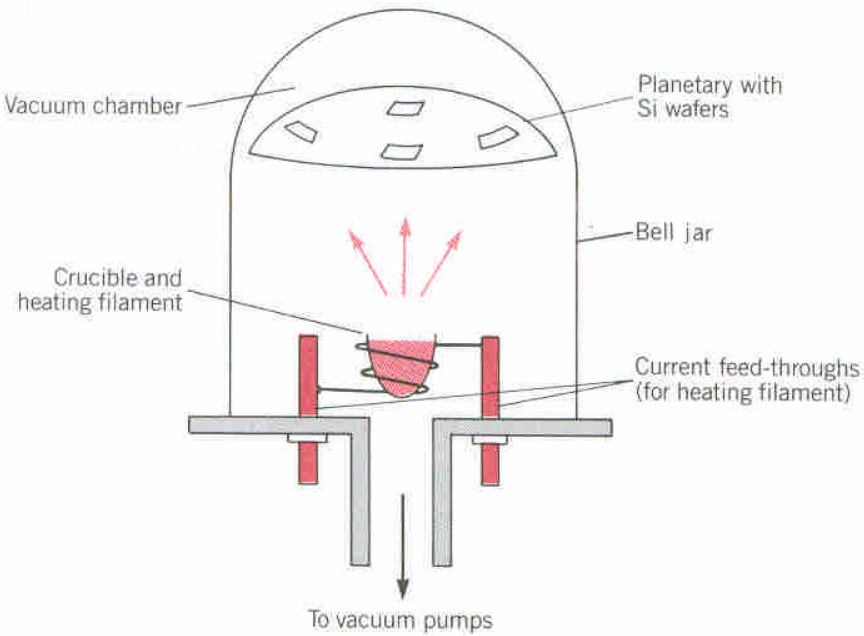
氧化層可用於製成積體電路圖形，摻入電活性雜質之障、保護層及閘極介電質等。在某些製程中亦用到氮化矽 (Si_3N_4)的絕緣層。氧化矽及氮化矽均可由化學氣相沉積法生成，所需溫度在攝氏250~450度間。



金屬披覆 (Metallization)

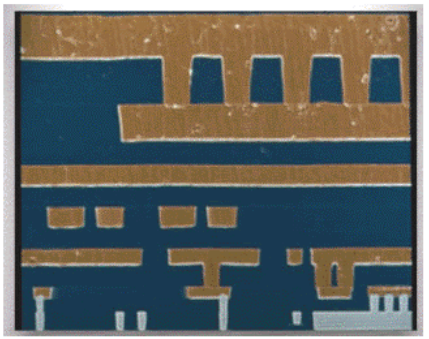
在積體電路中各電路元件，通常由導線連絡。這些導線除在接面地區外，通常與矽晶基底有一絕緣層間隔。 導電層也用於電晶體接觸及金氧半電晶體閘極之電極導體接觸及閘極電極，一般要求導電性好即電阻低。在元件尺寸較大時，均利用鋁膜，但鋁薄與矽晶反應過強，近年來閘極電極多改用低阻值的多晶矽或金屬與矽的化合物(金屬矽化物)，接觸則改用金屬矽化物。在大型積體電路中，金屬矽化物應用甚爲普遍。金屬矽化物常由在矽晶上沉積金屬或金屬-矽薄膜再經熱處理形成。

在元件連線特性方面，須與絕緣層黏著力好，但不易穿越絕緣層與矽晶接觸，在元件操作時不易斷線，電阻值低。以往均利用鋁或鋁合金膜，近年來有改用銅膜的趨勢。

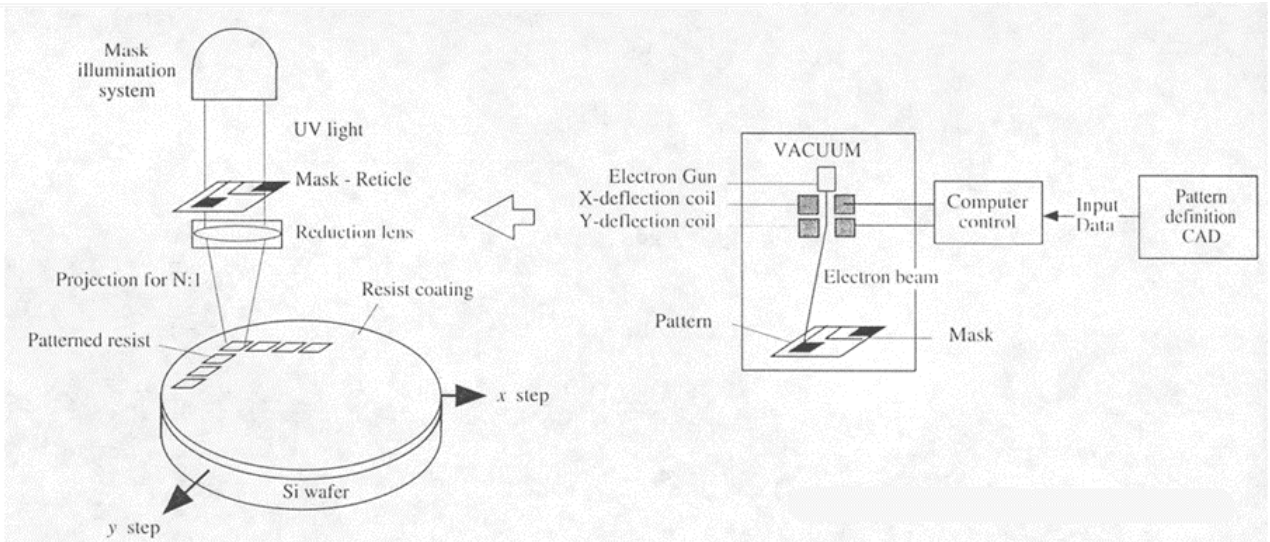


例：**thermal evaporation of metal in a vacuum chamber**

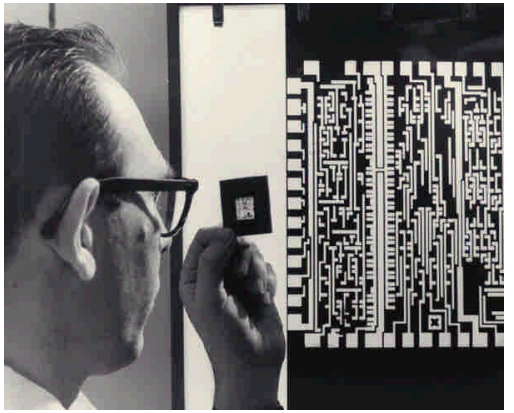
Copper metallization (materials issues)

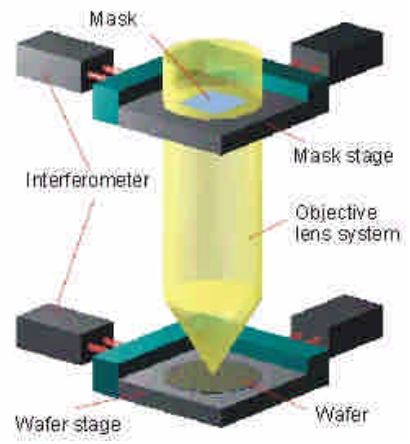


微影成形 (Lithography Patterning)

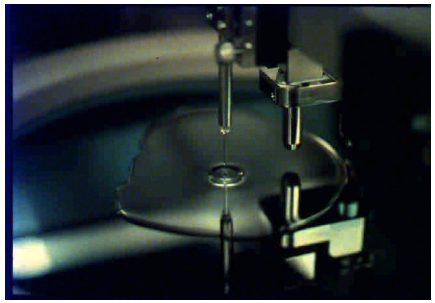


A UV illumination system is used to project the mask pattern onto the wafer surface. The projection demagnifies the mask image so that the pattern on the resist surface is *N* times smaller. The wafer is stepped and the exposure is repeated to pattern the neighboring chip on the wafer. The mask is generated (patterned) using an election beam whose scan is computer controlled.

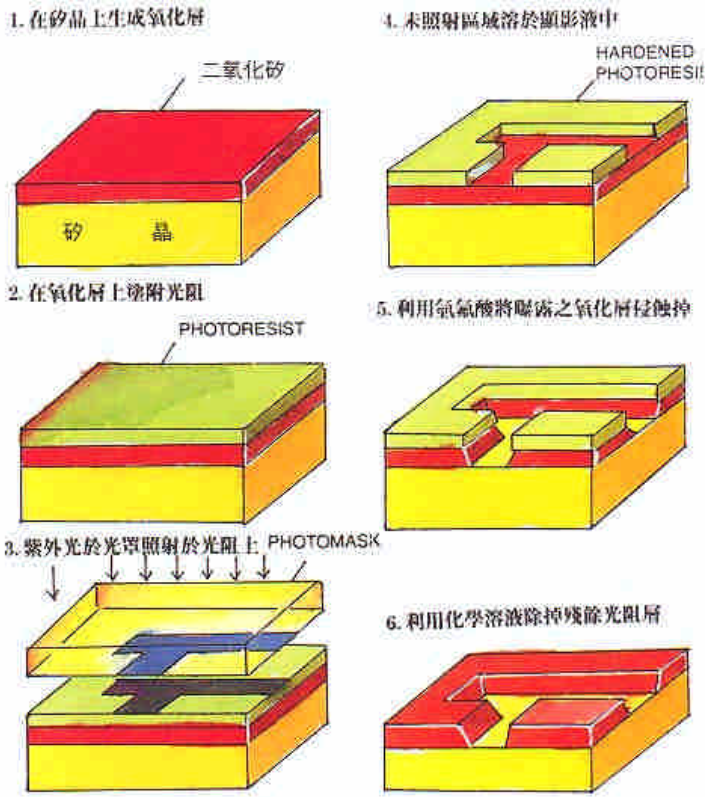




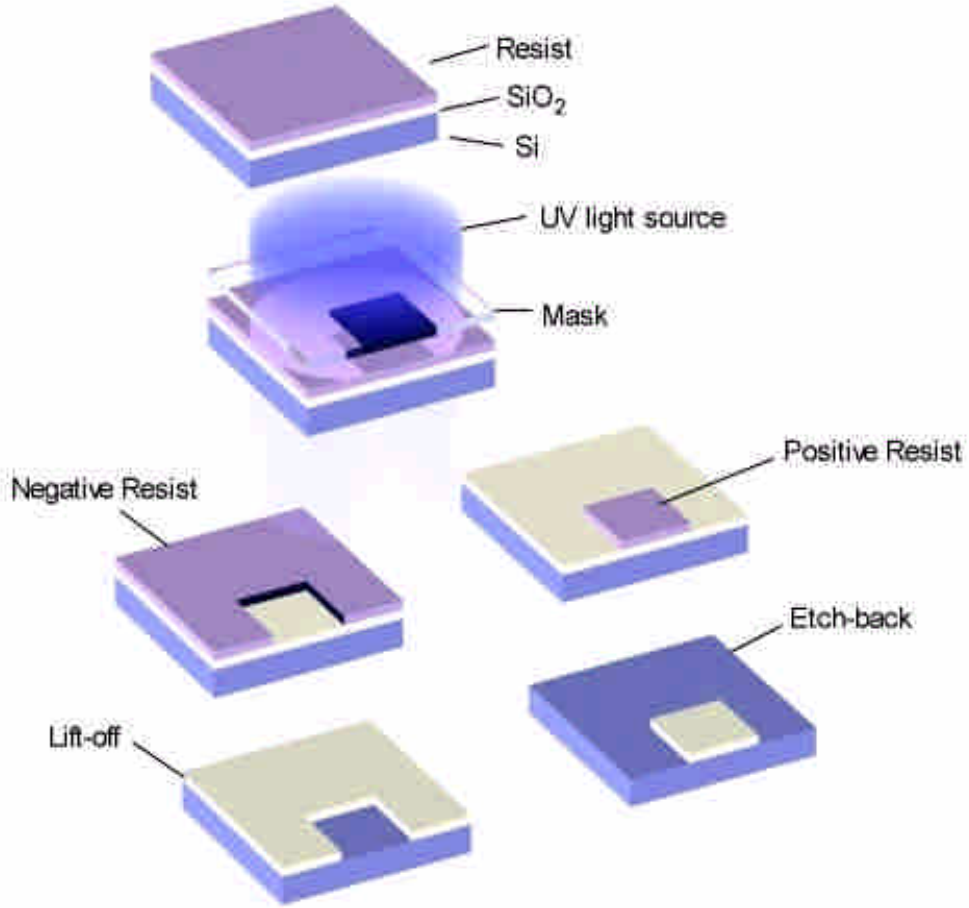
微影成形 (Lithography Patterning)



形成積體電路圖形的步驟如圖所示。首先在矽晶上以熱處理方法長一層氧化層，其次在氧化層上塗一有機光阻層。利用紫外光通過一光罩透光的部份。對某些光阻材料經紫外線照射其分子鏈被破壞，而可以有機溶劑清洗掉，再以氫氟酸除去曝露部份的氧化物，再將未反應光阻材料清除，最後在半導體表面得到與光罩圖形一樣的圖形。上例乃爲利用正光阻材料，如利用負光阻材料，經曝光後，負光阻材料分子結合在一起而較未曝光光阻難清除，如此得到的圖形與光罩透光部份互補。另外因開口尺寸微小化，曝光光源有利用更短波長電磁波一X光及電子束的趨勢。



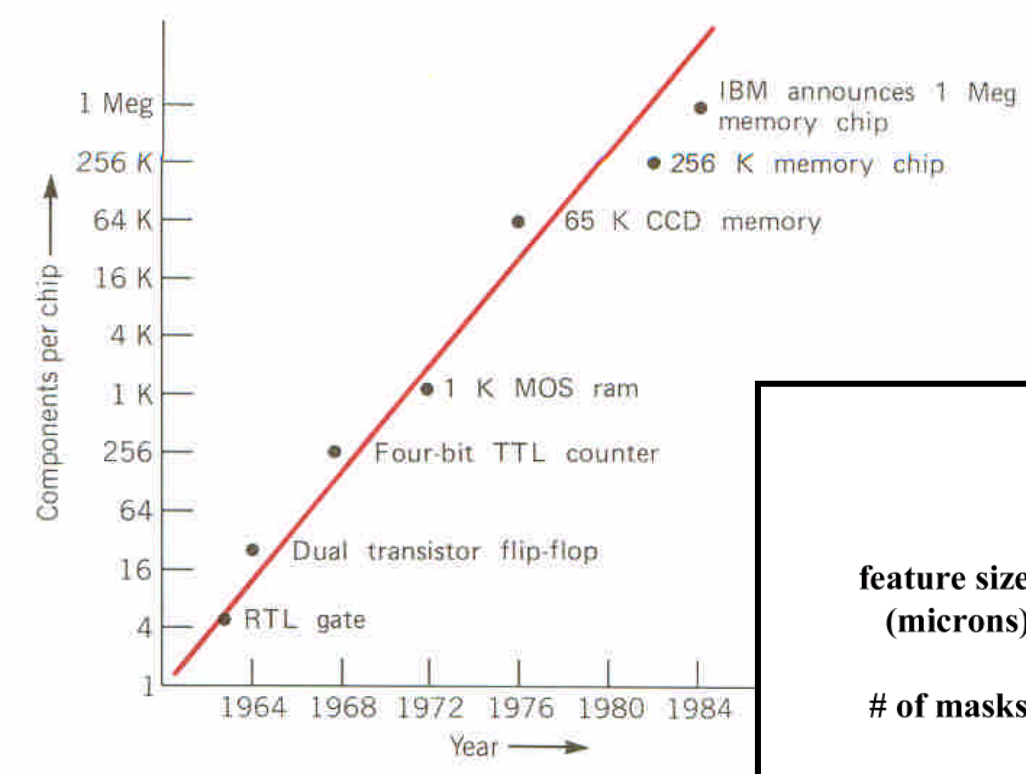
微影成形 (Lithography Patterning)



在半導體面形成積體電路所需的圖形，通常要用蝕刻方法；蝕刻方法分爲乾蝕刻法（dry etch)與濕蝕刻法（wet etch ）兩種。乾蝕刻法是利用離子束清除未受光阻保護區域的材料方法。其優點在不等向蝕刻性較高。

在積體電路製作步驟中，蝕刻形成圖形爲必經步驟，較複雜的積體電路，利用光罩形成圖形的次數達三十次以上。

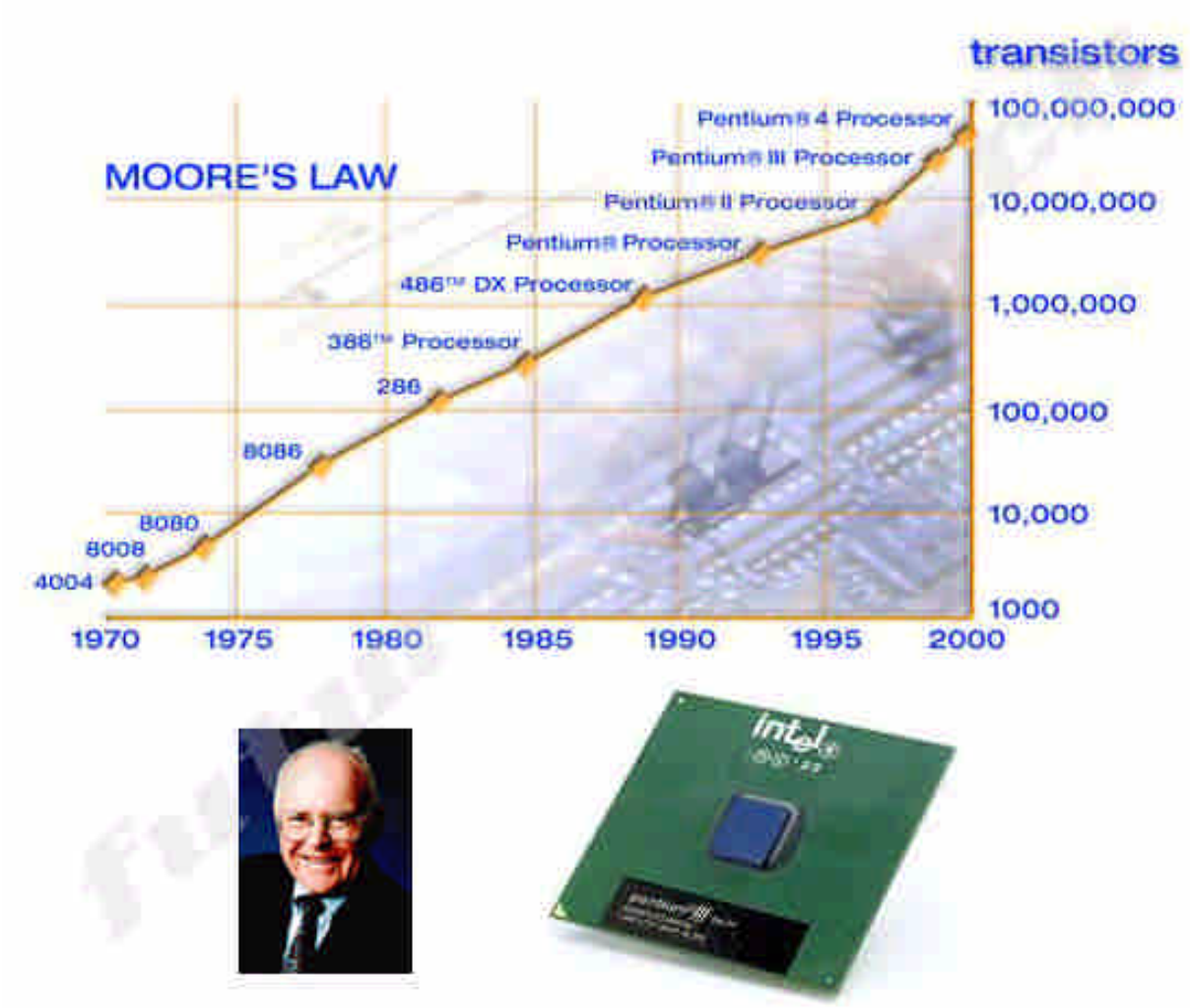
微影成形 (Lithography Patterning)

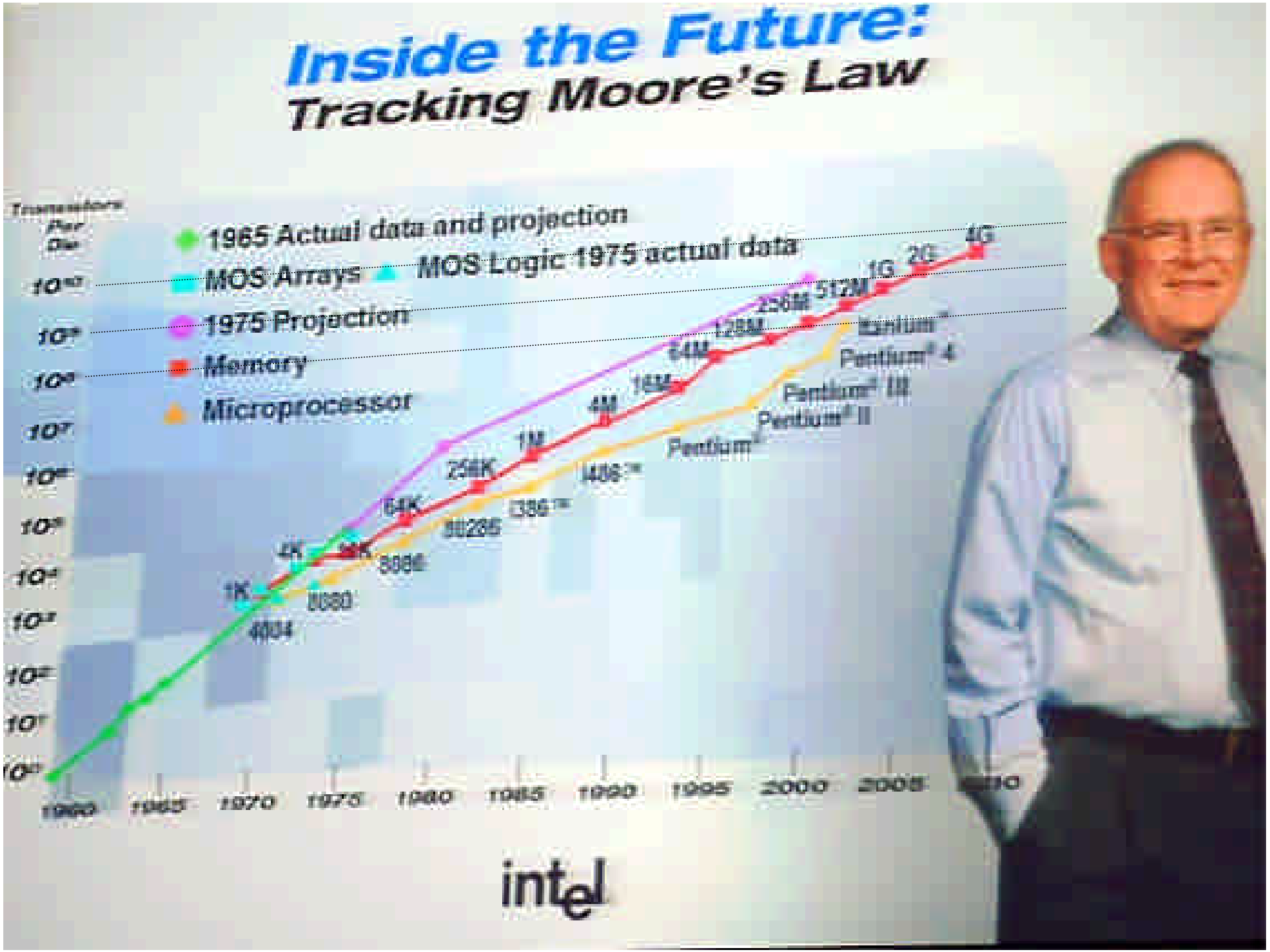


Level	Abbreviation	# Components per Chip
Small Scale Integration	SSI	2 - 50
Medium Scale Integration	MSI	50 - 5000
Large Scale Integration	LSI	5000 - 100,000
Very Large Scale Integration	VLSI	Over 100,000 - 1,000,000
Ultra Large Scale Integration	ULSI	> 1,000,000

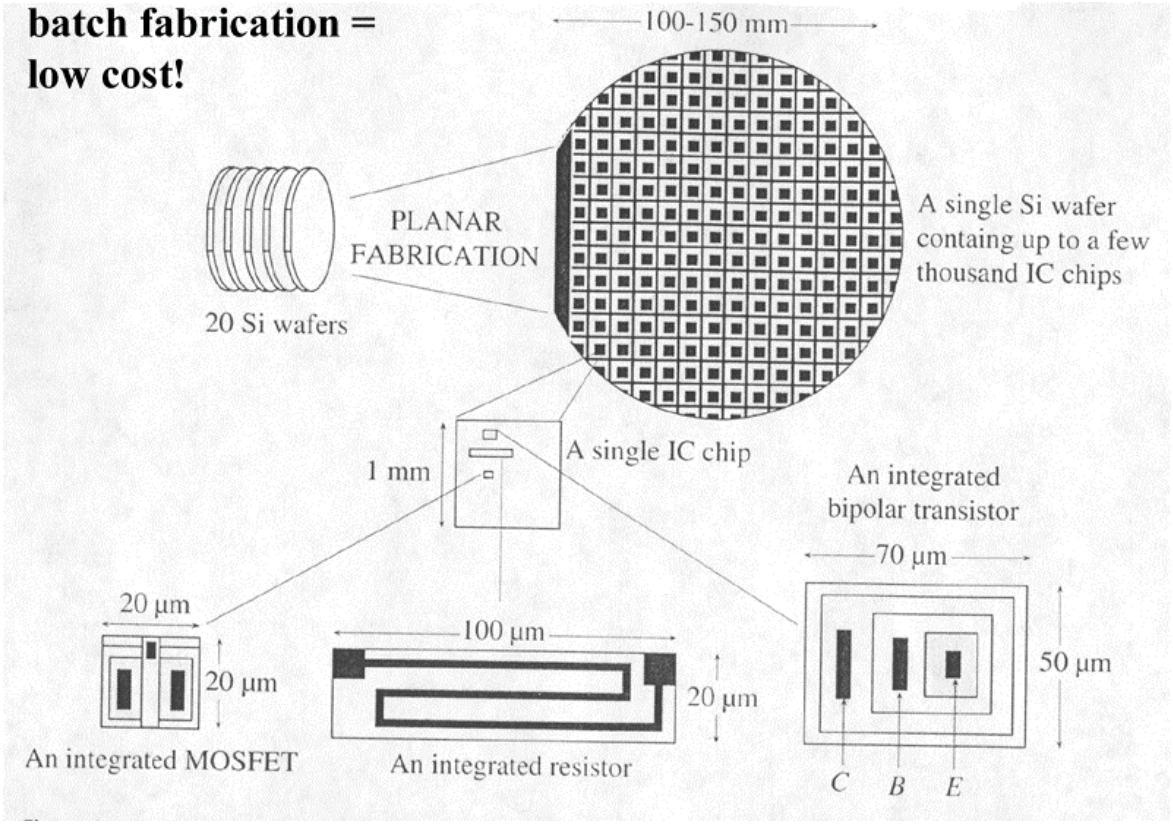
IC integration scale.

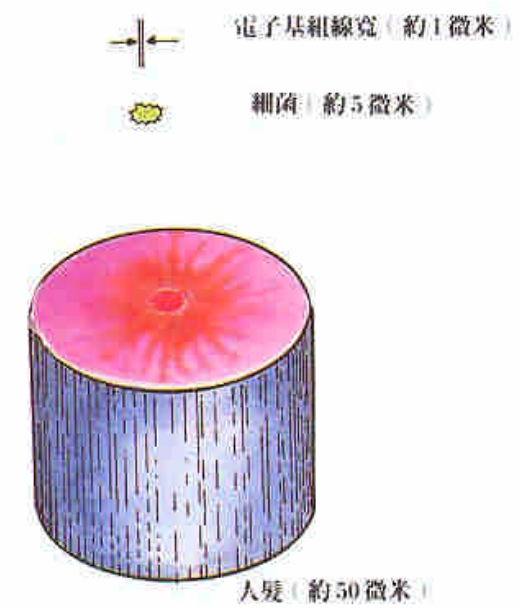
	15 years ago (1980)	5 years ago (1998)
feature size (microns)	5 - 1	0.3 to 0.1
# of masks	5	25
# of layers	3 - 5	50+
# of transistors per chip	1000's	millions


transistors
MOORE'S LAW
Pentium® 4 Processor
Pentium® III Processor
Pentium® II Processor
Pentium® Processor
486™ DX Processor
386™ Processor
286
8086
8080
8008
4004
100,000,000
10,000,000
1,000,000
100,000
10,000
1000
1970
1975
1980
1985
1990
1995
2000
intel


Inside the Future:
Tracking Moore's Law
1965 Actual data and projection
MOS Arrays
MOS Logic 1975 actual data
1975 Projection
Memory
Microprocessor
4004
8080
8086
80285
386™
486™
Pentium®
Pentium® II
Pentium® III
Pentium® 4
Itanium™
1K
4K
64K
256K
1M
4M
16M
64M
128M
256M
512M
1G
2G
4G
1970
1975
1980
1985
1990
1995
2000
2005
intel

無塵室環境 (Clean Room Environment)

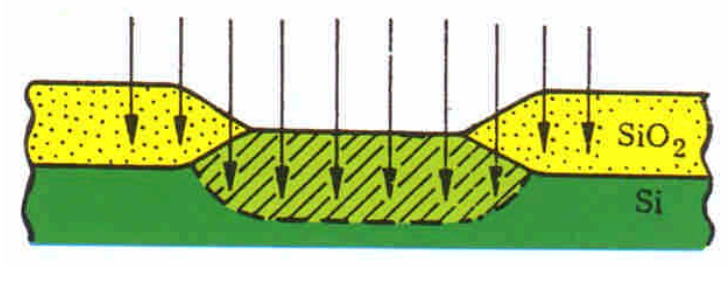


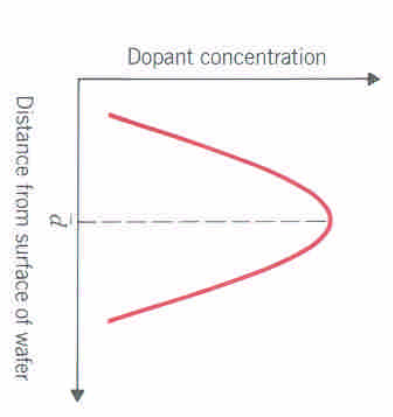


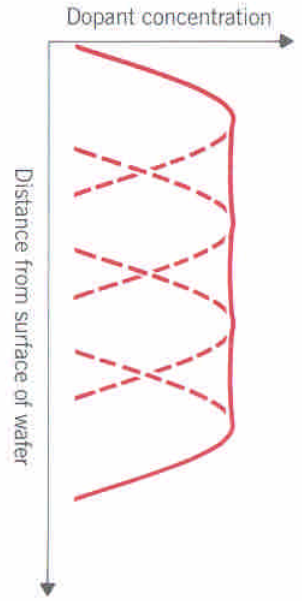
One hair will destroy thousands of devices on a chip.

摻雜 (Doping) – 離子植入 (Ion Implantation)

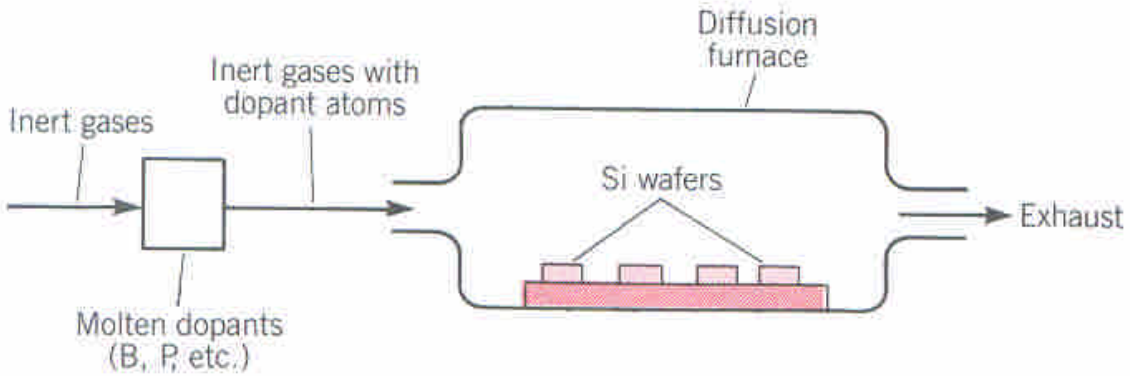
矽晶中一般均須加入電活性雜質原子(如三價的硼，五價的砷或磷) ，來控制半導體，形成 P、N 接面電晶體。摻入雜質的方法包括擴散法及離子佈植法。離子佈植法因在雜質濃度、縱深分佈及純度控制方面遠較擴散法優越，在大型積體電路製作上已被廣泛應用。其方法是利用加速器將高能量雜質離子植入矽晶表面中。因高能量離子常會破壞矽晶表面晶體結構，造成輻射損傷，生成各種缺陷。生成的缺陷對矽晶電性往往有不良的影響，因此在離子佈植後必須有一段熱處理的步驟，以去除晶體中的缺陷或減低其密度。







摻雜 (Doping) – 擴散 (Diffusion)



熱處理 (Heat Treatment)

在離子佈植後必須有一段熱處理的步驟，去除晶體中的缺陷或減低其密度。 熱處理通常在石英管惰性氣體中進行。熱處理溫度一般在攝氏1100度以下。時間則視消除缺陷及雜質分佈的需要而定。

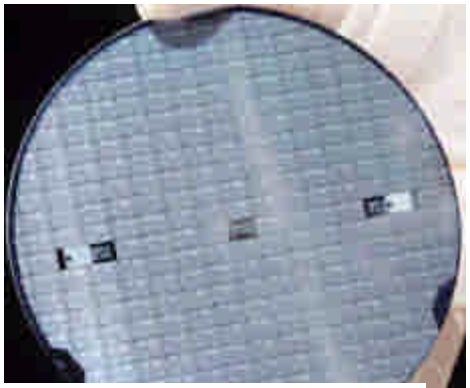
快速高溫處理

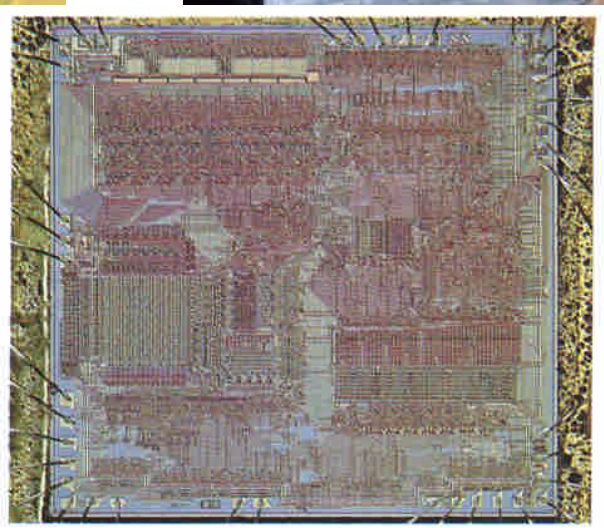
快速高溫處理（**RTP：Rapid Thermal Processing**）爲電晶體與電容成形過程中重要的步驟之一，可用來修正薄膜性質與製程結果。在此短暫且精確控制的高溫處理過程中，晶圓溫度可在短短**10**秒內自室溫快速升至**1000**℃高溫。快速高溫處理通常用於回火製程（**annealing**），負責控制元件內摻質原子之均勻度，也可用來進行矽化金屬，及透過高溫產生含矽化之化合物與矽化鈦等。

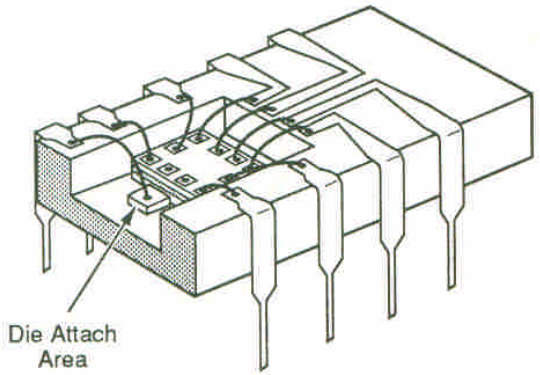
IC 封裝 (IC Package)

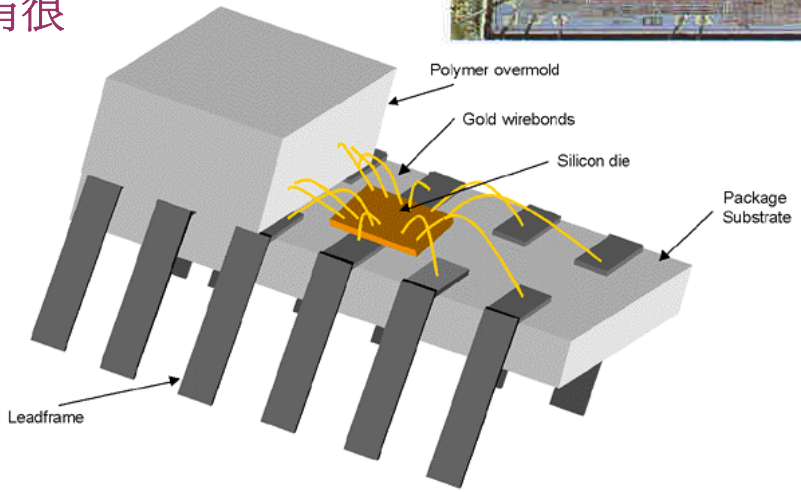
積體電路在製程中，均在一晶元上同時製作許多 5-10毫米大小長方形晶片 。各晶片含高達百萬個電路基組。經切割後，各晶片須焊黏於電路基板，再分別構裝才能應用。

構裝包括封裝及接線，封裝的日的在防止積體電路的受潮、受蝕、碰損，增加導熱能力，而可在較惡劣的情況下操作。接線則使積體電路得以對外輸入、輸出訊號，對微電子產品性能、價格和可靠性都有很大影響。

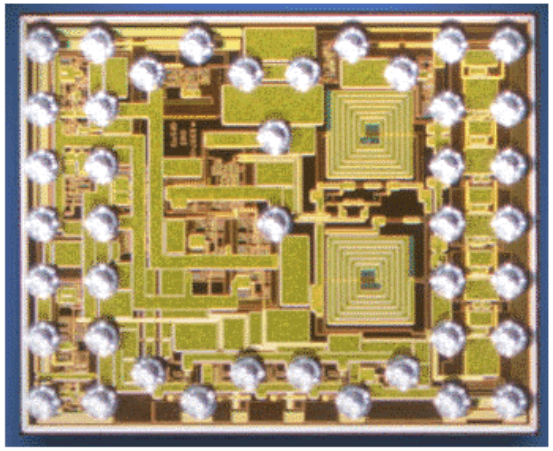


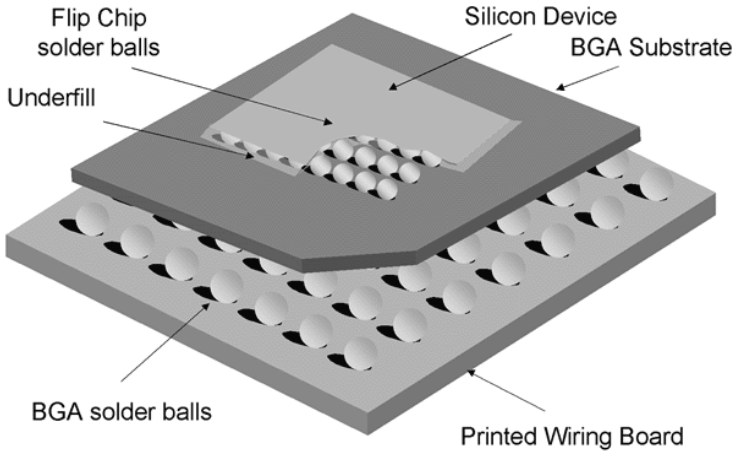






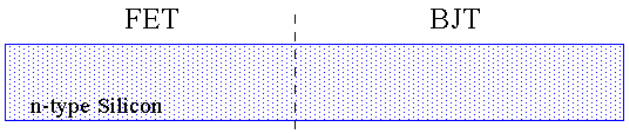
IC 封裝 (IC Package)





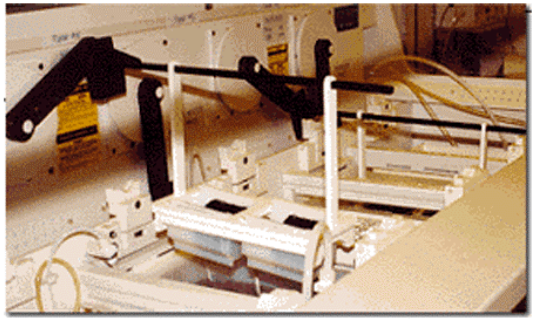
FET and BJT Process Flow

Field Effect Transistor **Bipolar Junction Transistor**

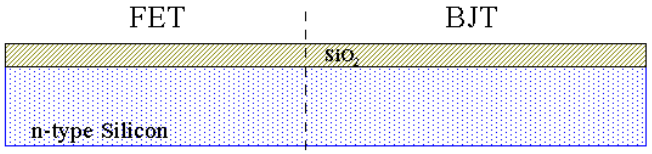


Step 1. RCA clean + HF dip

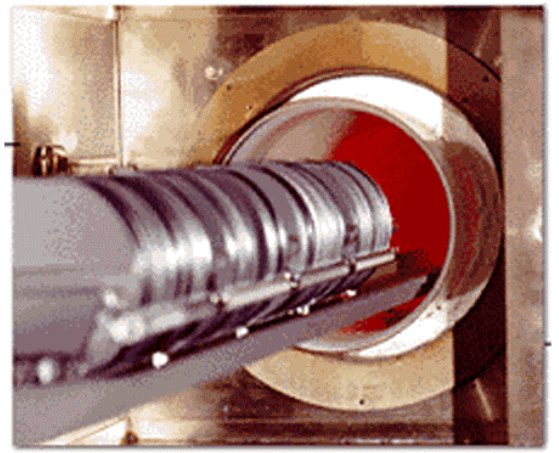
RCA Clean: To remove residual organics and certain metals
HF dip: To remove oxides



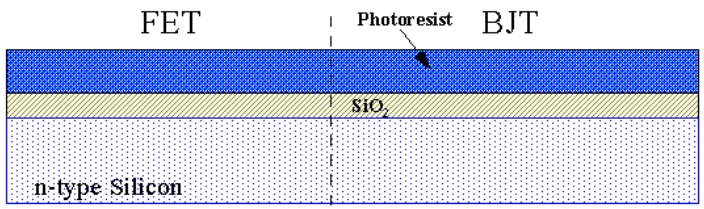
a picture of RCA baths courtesy of MCNC



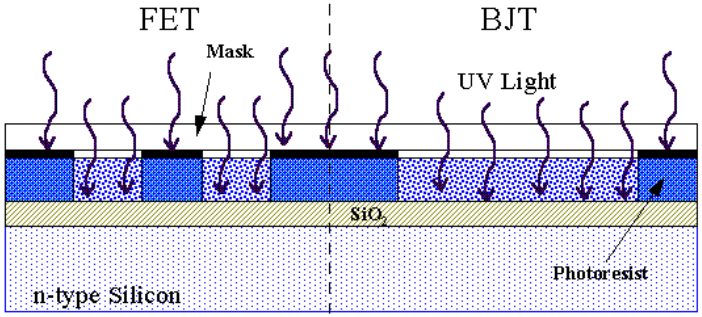
Step 2. Grow thermal oxide



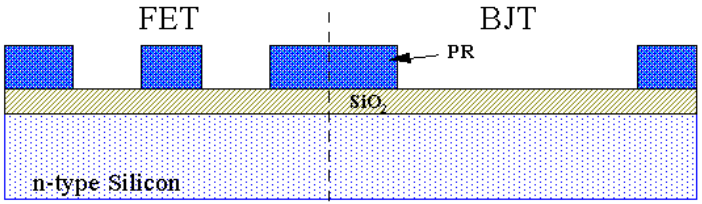
a picture of a wafer boat going into a furnace
courtesy of MCNC



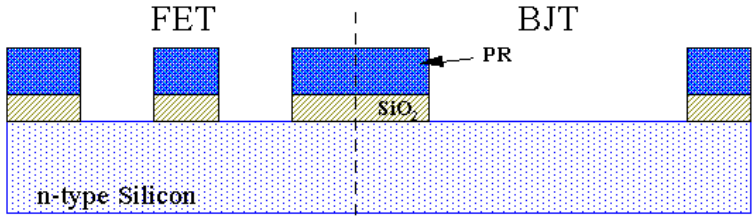
Step 3. Spin on photoresist



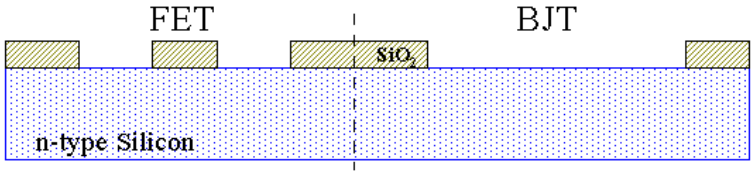
Step 4. Expose photoresist



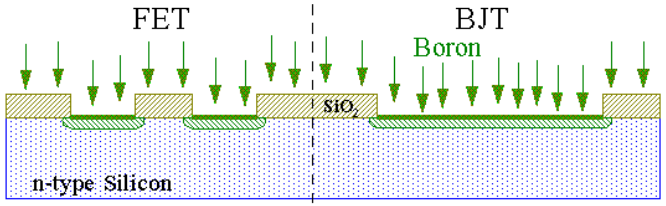
Step 5. Develop photoresist



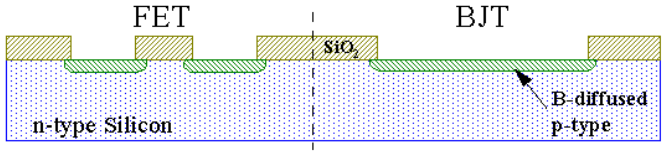
Step 6. HF etch to pattern the oxide



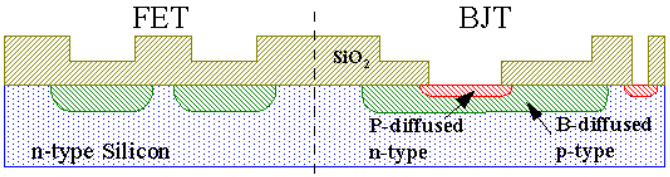
Step 7. Strip photoresist



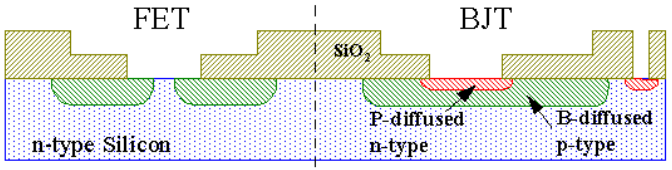
Step 8. Deposit BSG (Borosilicate Glass)



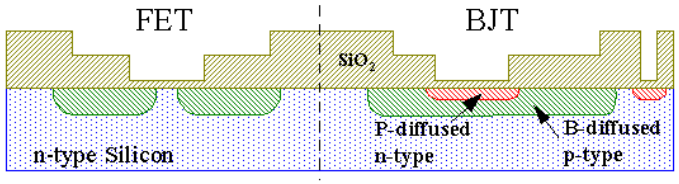
Step 9. Etch to remove BSG (HF, sulfuric + nitric



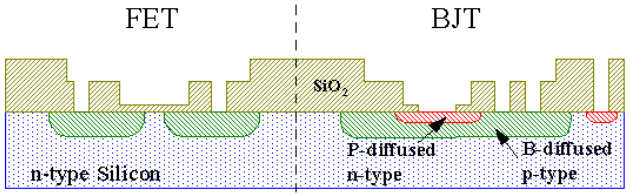
Step 12. Phosphorous doping using phosphosilicate glass



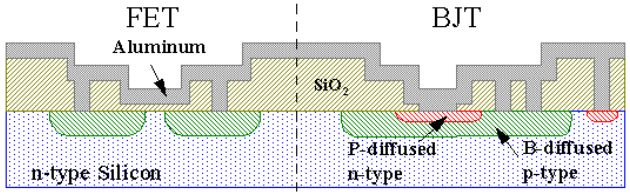
Step 13. FET: Pattern oxide using MASK#3 (lithography)



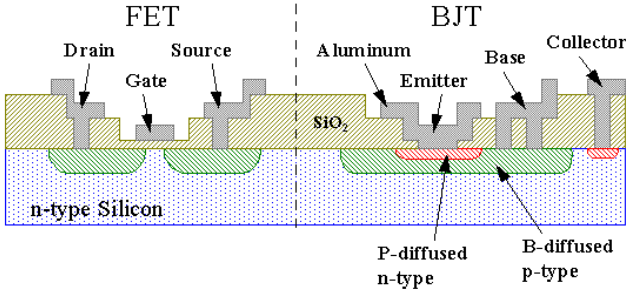
Step 14. Grow gate oxide (10-50nm thick)



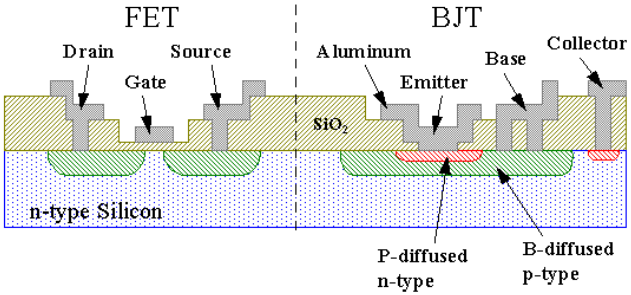
Step 15. Pattern oxide for contact to active areas



Step 16. Deposit (evaporation) a blanket Al film

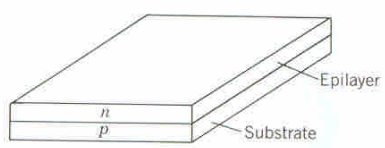


Step 17. Pattern Al film using MASK#5 (lithography)

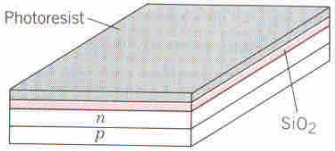


Step 18. Low temperature anneal (450C) for contacts

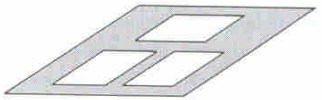
IC fabrication of a NOR gate

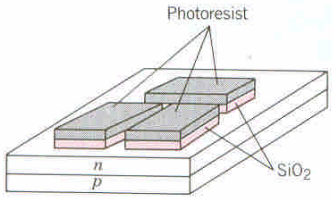


(a) n-type epitaxial layer grown on p-type wafer

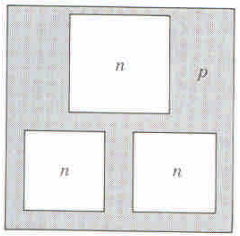


(b) Oxidation of n-type layer followed by photoresist coating

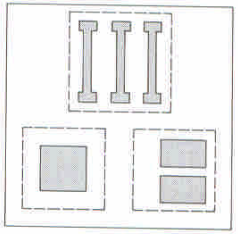

(c) Mask for n-type island formation

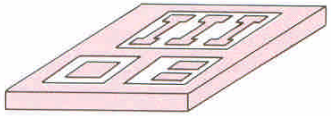


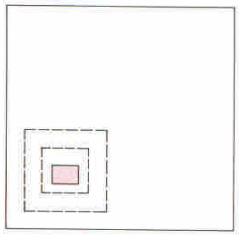
(d) Formation of oxide island with exposed photoresist on top

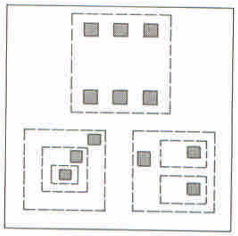


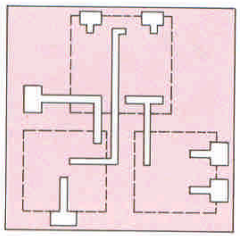
(e) Top view of wafer after n-type island formation

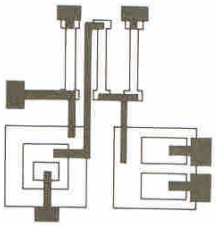

(f) Mask for p dopant diffusion

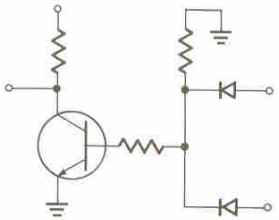

(g) State of the chip after p-type diffusion; shaded areas are p-type, white areas are n-type


(h) Mask for emitter diffusion


(i) Mask for electrical contact window-opening


(j) Mask for aluminum evaporation


(k) Complete and interconnected circuit


(l) Gate using conventional electronic symbols