Supporting Information: Side gate tunable Josephson junctions at the LaAlO$_3$/SrTiO$_3$ interface

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Fabrication

The steps for the fabrication of the nanoscale constrictions and side gate electrodes are illustrated in Figure S1a. As discussed in the main text, a template with the desired pattern is realized on the SrTiO$_3$ (STO) substrates by depositing a thin AlOx layer before the epitaxial growth of the LaAlO$_3$ (LAO) thin film. To this purpose, we use a single-step electron beam lithography procedure optimized for insulating materials.

The process starts off with single crystal TiO$_2$-terminated STO(001) substrates, purchased from CrysTec GmbH. A double-layer layer of positive resist (PMMA 495K/950K) is spun on the surface of the as-received substrates and subsequently covered by a conductive protective coating for e-beam resist (Elektra 92). This layer acts as a charge dissipation layer, thus reducing accumulation of surface charges on the STO insulating substrate. The pattern resolution and the exposure dose required due to the added Elektra layer have been

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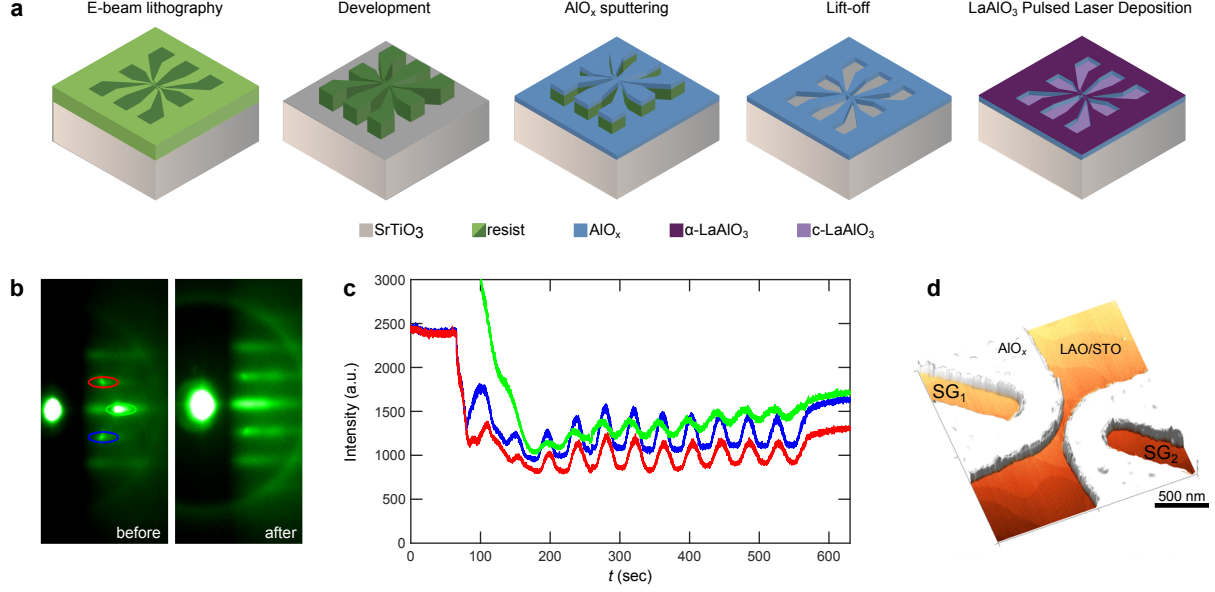[*]To whom correspondence should be addressed

Figure S1: (a) Schematic representation of the fabrication process steps. (b) Reflection high energy electron diffraction (RHEED) patterns before (left) and after (right) LaAlO$_3$ deposition. (c) RHEED oscillations obtained during the deposition. (d) Atomic force microscopy image of a side gated device.

studied and optimized. The optimal dose for a beam-spot size of 3 nm was $850 \, \mu$C/cm^2. After exposure, the Elektra layer layer is removed by dipping in DI-water, after which the PMMA is developed using a diluted methyl isobutyl ketone (MIBK) solution, revealing the pattern. After development, we sputter a thin (~ 13 nm) AlOx layer, before removing the resist with a lift-off procedure. With the described procedure, we obtain an insulating hard-mask with the desired pattern on the STO substrate. Finally, crystalline LAO (c-LAO) is grown via pulsed laser deposition (PLD), monitored in-situ by reflection high energy electron diffraction (RHEED) to confirm layer-by-layer growth (Figure S1c). The RHEED diffraction pattern corroborates the two-dimensional nature of the growth (Figure S1b). The LAO films are grown at an oxygen pressure of 6×10^{-5} mbar and two different temperatures: 770°C and 840°C. Lower growth temperature results in samples with lower carrier densities, whereas samples grown at higher temperature exhibit higher carrier density and superconductivity. A KrF excimer laser with a fluency of $1 \, $J/cm^2 and a repetition rate of $1 \, $Hz is used. Immediately after deposition, the samples are annealed in oxygen: the deposition chamber is filled

with 300 mbar of oxygen and the sample temperature is kept at 600° for 1 hour. The sample is then slowly cooled down to room temperature in the same oxygen atmosphere. After growth, a metallic back gate is established with silver conductive epoxy on the back of the STO substrate. Ultrasonic wedge bonding with Al wire is used to make electrical contact to the conducting regions. An atomic force microscope image of a side gated nano-constriction realized with this technique is shown in Figure S1d.

Finite Elements Analysis

The finite element simulations of the side gated constrictions have been carried out in Comsol®5.3. The physical modeling was based on the electric currents (ec) module under stationary conditions. Electric insulation was imposed at all the external boundaries and current conservation was imposed in bulk. 'Dielectric permittivity' was used as constitutive relationship for the electric field. The STO substrate was modeled as a rectangular parallelepiped with a thickness of 500 nm and lateral size of $1.5\,\mu$m, as shown in Figure S2a. The dependence of the DC dielectric constant of STO on the electric field intensity was modeled as a first approximation by using the Landau-Ginzburg-Devonshire theory [1,2]

$$\varepsilon_{\mathrm{STO}}(E) = 1 + \frac{B}{[1 + (E/E_0)^2]^{1/3}} \tag{1}$$

where $B = 23,500$ and $E_0 = 82,000\,\mathrm{V/m}$, according to previous reports.[3] The LAO thin film is modeled as a 2 nm-thick layer having a fixed dielectric constant [4] of 24.
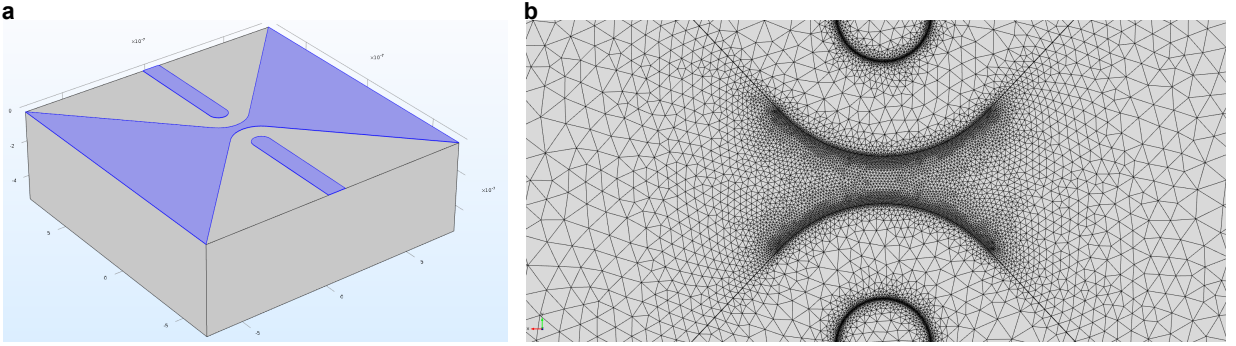
Figure S2: (a) Geometry of the simulated device showing the STO substrate (grey) and the LAO layer (blue). (b) Mesh grid in the constriction region.

At the interface between the LAO layer and the substrate we imposed a fixed voltage condition. The most central region comprising the constriction was grounded, while the interface below the side gates was polarized at negative voltage values.

The mesh was created by using a stepped sequence of decreasing density, starting from the centre of the constriction towards the outer edges of the substrate (see Figure S2b). The

mesh started with a free triangular mapping on the surface having minimum element size of $1 \cdot 10^{-11} m$. The volume was filled with a swept mesh of prisms made out of 10 elements with an element ratio of 20. The complete mesh consists of 250656 domain elements, 60214 boundary elements, and 2300 edge elements. The solution was computed using a fully coupled iterative solver based on the conjugate gradients, and an algebraic multigrid as preconditioner.

Estimation of the lithographic length of the constriction

The length of the constriction was estimated from the AFM images, as shown in Figure S3. The edges of the narrow region are defined by 2 large circles, which then open up in a linear fashion, at a 45° angle. The length was estimated by extrapolating the lines tangent to the circles and taking their intersection at both ends of the channel. This yields $L \approx 500 \, \text{nm}$.
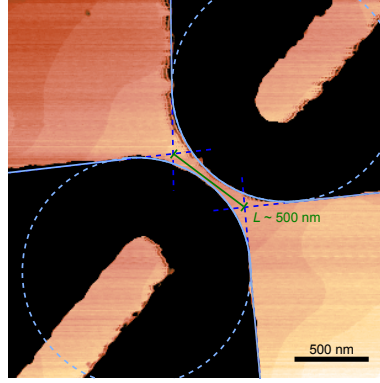

Figure S3: Schematic representation of the estimation of the lithographic length of the constriction.

Determination of G, I_c, δG^{rms} and δI_c^{rms}

The values of I_c and G were both determined from the differential resistance dV/dI curves, from the position of the maximum and the value of the normal state resistance at $I_{bias} = 10\,nA$, respectively, as shown in Figure S4a and b.

To extract the values of quadratic mean of the fluctuations in G and I_c, we first remove the monotonically decreasing background component that arises from the decrease in carrier density induced by the application of negative voltages in the side gate electrodes. In both cases, this is done by subtracting a second degree polynomial fitted to the data. The fits to G and I_c as a function of side gate voltage are shown in Figure S4a and b, respectively. The resulting fluctuations after subtraction of the background modulation, which are used to determine δG^{rms} and δI_c^{rms}, are shown in Figure S4c.
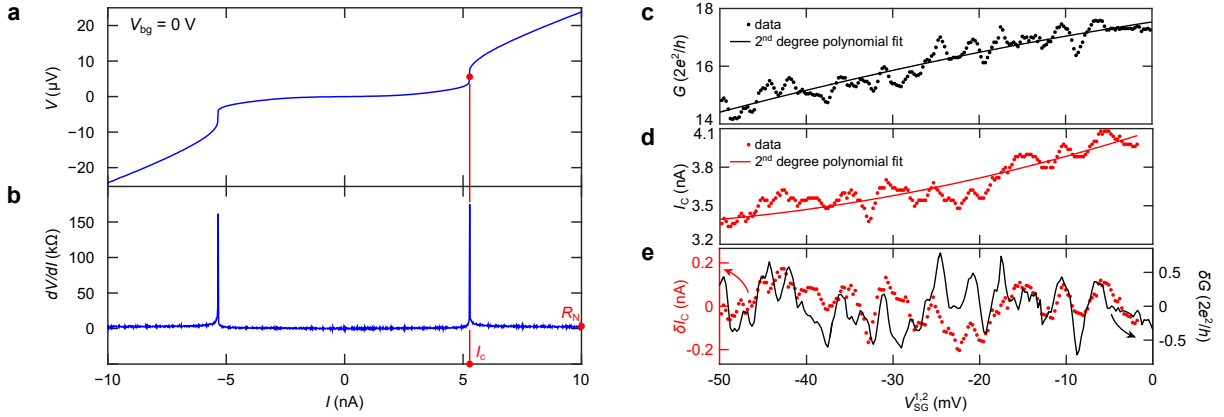

Figure S4: (a) VI characteristic and (b) corresponding differential resistance dV/dI curve, recorded at $V_{bg} = 0\,V$. (c) Conductance G and (d) critical current I_c as a function of applied side gate voltage and respective second degree polynomial fits. (e) Fluctuations δG^{rms} and δI_c^{rms} as a function of applied side gate voltage after subtraction of the background modulation.

Reproducibility of the mesoscopic fluctuations

In order to confirm that the observed fluctuations are time-independent and reproducible, we have compared the fluctuation patterns of two different sweeps. Figure S5 shows the variations in G and I_c as a function of side gate voltage, where a good agreement is observed between both measurements.
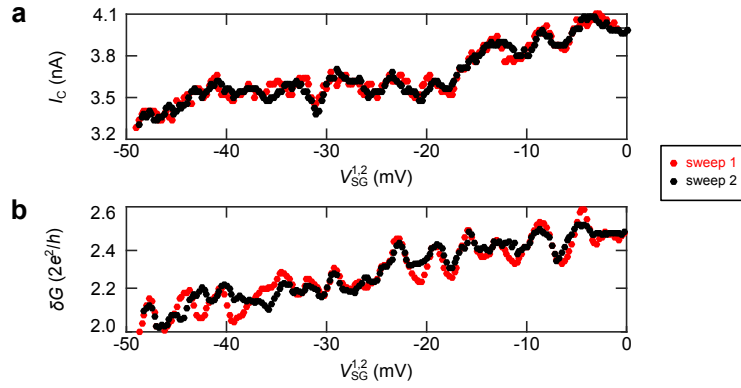

Figure S5: (a) Critical current I_c and (b) conductance G oscillation patterns for two different measurements.

Fluctuations of R_N and I_c as a function of the individual side gate voltages
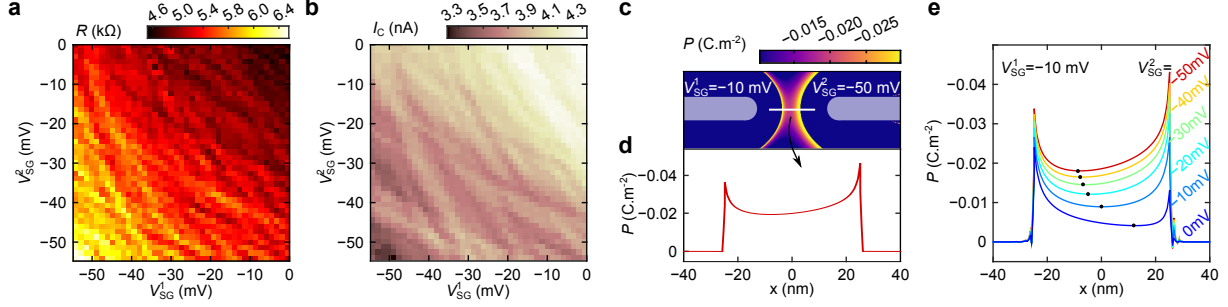
Figure S6: (a) 2D map of resistance (R) and (b) critical current I_c as a function of side gate voltages V_SG^1 and V_SG^2, measured at $V_\mathrm{BG} = -11\,\mathrm{V}$ and $T = 50\,\mathrm{mK}$. (c) Spatial map of the out-of-plane electric polarization P from FEA under asymmetric bias of the side gates ($V_\mathrm{SG}^1 = -10\,\mathrm{mV}$ and $V_\mathrm{SG}^2 = -50\,\mathrm{mV}$) and corresponding cut-line at the constriction center showing the polarization profile. (d) Electric polarization P across the channel (along the white line in panel c) for V_SG^2 ranging from 0 to $-50\,\mathrm{mV}$ while V_SG^1 is fixed at $-10\,\mathrm{mV}$. The black dots indicate the minimum magnitude of P for each profile.

The independent control of the side gates enables the investigation of the fluctuations in R_N and I_c as a function of the independent side gate voltages V_SG^1 and V_SG^2, as shown in Figure S6a and b, respectively. In both cases, a similar pattern of fluctuations is revealed which is not symmetric across the diagonal. As mentioned before, these fluctuations appear at sufficiently low temperatures, stemming from phase coherent effects determined by the local disorder potential. Figure S6c shows a spatial map of the calculated out-of-plane electric polarization in a configuration of asymmetric biasing of the side gates. One can immediately observe that the charge depletion is strongest at the constriction edge near SG_2. A closer look at the polarization profile for this configuration (Figure S6d) indeed shows that the minimum of the magnitude of P is not located in the middle of the constriction, but shifted towards SG_1. Moreover, when V_SG^1 is kept fixed at $10\,\mathrm{mV}$ and V_SG^2 assumes progressively lower values, the minimum of P continuously shifts towards SG_2. Thus, asymmetric biasing of the side gates results in probing different regions of the channel. Since the impurities responsible for the scattering of the itinerant electrons are randomly distributed across the constriction,

switching V_{SG}^1 and V_{SG}^2 effectively results in probing a different disorder landscape, hence the lack of symmetry across the diagonal in the maps of R_{N} and I_c.

SQUID asymmetry

By independently tuning the critical current of each c-JJ via the side gates, we demonstrate the control of the (a)symmetry in the SQUID response. To highlight the shifts of the interference pattern, we plot the variation of $\Delta\Phi$ with $I_{\mathrm{c,max}}$ in Figure S7. The blue (green) points correspond to measurements performed by varying $\mathrm{SG_L}$ ($\mathrm{SG_R}$) while the other gate is fixed at $0\,\mathrm{mV}$.
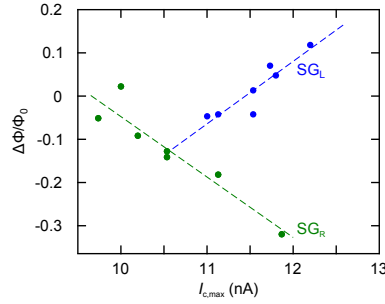

Figure S7: Variation of $\Delta\Phi/\Phi_0$ with $I_{\mathrm{c,max}}$. Dashed lines: linear fits.

References

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