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We report on the fabrication and electrical characteristics of the first $SrTiO_3/GdTiO_3$ (STO/GTO) heterostructure field-effect transistors (HFETs). The high two-dimensional electron gas (2DEG) density of $3 \times 10^{14}\,cm^{-2}$ formed due to the polar discontinuity at the STO/GTO interface was used as a channel to create inverted HFETs. Plasma O_2 treatment was found to reduce current leakage by 3 orders of magnitude at reverse bias, leading to rectifying Schottky behavior. A charge modulation of $0.6 \times 10^{14}\,cm^{-2}$ is reported here, which represents the highest sheet charge modulated in any planar field effect transistor to date. © *2013 AIP Publishing LLC*.
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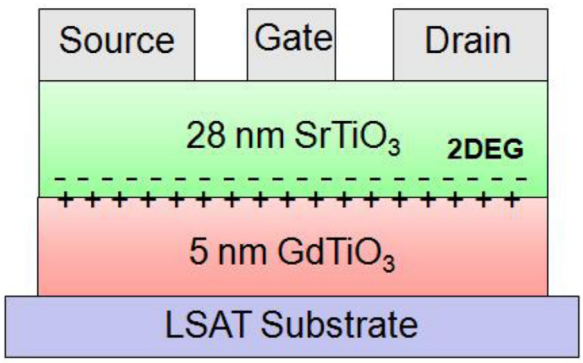
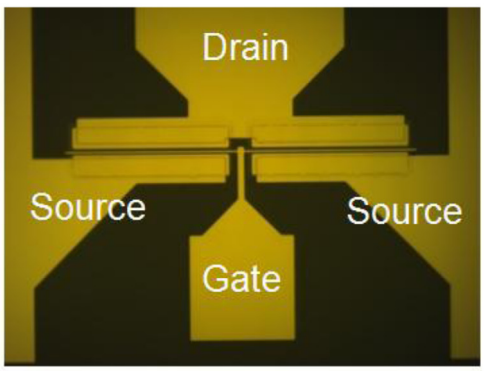
Since the pioneering discovery of a two dimensional electron gas (2DEG) at the interface between the two insulating oxides $LaTiO_3/SrTiO_3$,[1] several oxide interfaces combinations including $LaAlO_3/SrTiO_3$,[2,3] $LaVO_3/SrTiO_3$,[4] $SrTiO_3/GdTiO_3$,[5] $PrTiO_3/SrTiO_3$, and $NdTiO_3/SrTiO_3$[6] have been investigated. In addition to exhibiting unique electronic[7,8] and magnetic properties,[9–11] oxide heterostructures have attracted considerable attention because the 2DEG sheet carrier density achieved in these materials is at least an order of magnitude greater than in any other semiconductor system, such as the III-nitride system (maximum sheet charge of $3 \times 10^{13}\,cm^{-2}$).[8,12,13] The $SrTiO_3/GdTiO_3$ (STO/GTO) interface investigated in this work was shown to have an extremely high sheet charge density of $3 \times 10^{14}\,cm^{-2}$, equivalent to the 1/2 electron per interface unit cell required to compensate the polar discontinuity at the interface.[5] Such interfacial electron gases can be used to design innovative oxide electronic devices, analogous to heterostructure field effect transistors (HFETs)[14–16] based on conventional semiconductors such as GaAs and GaN, but with an order of magnitude higher charge density. The modulation of such high charge density could have applications in high current density electronics, or in plasmonics, where high density electron gases could enable tunable optical properties in the technologically important infrared wavelength range. Field-effect transistors (FETs)[17,18] can also be a useful tool to investigate the physics of correlated electron systems, allowing for controlled and reversible changes of the carrier concentration without altering the disorder.

Oxide materials also provide the advantage of higher breakdown strength due to the higher dielectric constant. The maximum sheet charge density that can be modulated, based on the relationship $qn_s = \varepsilon_r\varepsilon_0 F_{BR}$ (where n_s is the sheet carrier density, $\varepsilon_r\varepsilon_0$ is the relative permittivity, and F_{BR} is the breakdown field), is an order of magnitude higher in STO than other traditional semiconductors such as Si, GaAs, or GaN, due to the higher dielectric constant (~300) of STO. In this paper, we report on an STO/GTO HFET, with the first results of direct current modulation in the $SrTiO_3/GdTiO_3$ system and the highest recorded charge modulation of up to 6×10^{13} electrons/cm^2 (or 0.096 C/cm^2) for any semiconductor material system.

Recent work has shown that STO/GTO has a staggered band line-up,[19] causing the 2DEG to reside in the wider bandgap material, STO. In this work, we take advantage of this by employing an inverted HFET structure as shown in Fig. 1(a). The energy band diagram and the carrier concentration profiles (Fig. 2) were obtained using a self-consistent



(a)



(b)

FIG. 1. (a) Epitaxial structure of the STO/GTO heterostructure field effect transistor. (b) Optical micrograph of the transistor.

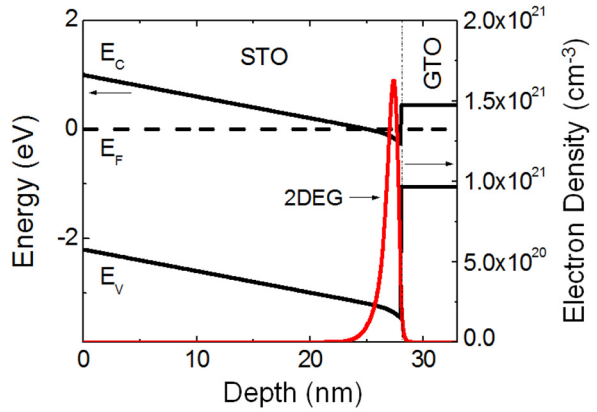


FIG. 2. Equilibrium energy band diagram and carrier density for a STO/28 nm, GTO/5 nm, and LSAT heterostructure field effect transistor. A fixed charge of $3 \times 10^{14}\,cm^{-2}$ was assumed at the STO/GTO interface. The surface is to the left, and a Schottky barrier of 1 eV was assumed for this calculation.

Schrödinger-Poisson solver. In the inverted structure, the electric field applied by the gate is sustained in the STO layer material, which also has high breakdown strength due to its large band gap and dielectric constant, thus enabling a higher density of electrons to be modulated. In addition, as for AlGaN/GaN high-electron-mobility transistors (HEMTs), inverted structures have additional advantages for high-frequency devices.[20] In vertically scaled devices, the inverted topology *reduces* the gate-channel distance and therefore increases the intrinsic gate-source capacitance and transconductance relative to the parasitic capacitances, thus boosting small-signal gain. This is evident from the energy band diagram for the inverted structure (Fig. 2), where the gate-channel distance is reduced by the wavefunction spread of the 2DEG.[21] The built-in back-barrier in inverted HEMTs can also reduce short-channel effects by mitigating electron overflow into the buffer. Finally, since there is no conduction band barrier layer between the surface and the 2DEG, it is easier to make low resistance contacts to the 2DEG, as demonstrated in N-polar HEMT structures in the III-nitride system that were shown to have very low contact resistance ($<0.05\ \Omega$ mm).[22]

The HFET structure (Fig. 1(a)) was grown on (001) $(LaAlO_3)_{0.3}(Sr_2AlTaO_6)_{0.7}$ (LSAT) single crystals by molecular beam epitaxy using a metal organic precursor (titanium isopropoxide) as both the Ti and oxygen source. Details of growth, structural characteristics, and electrical properties were reported in detail earlier.[19,23] These growth conditions likely cause oxygen deficiency and residual carriers in the STO layer, which could have impact on the transport properties of these structures.[5] The heterostructure consists of a 5 nm GTO layer and a 28 nm STO layer. Device fabrication involved i-line stepper lithography, with e-beam deposition of Ohmic contacts Al/Ni/Au (20/400/200 nm), inductively coupled plasma reactive ion etching Cl_2/BCl_3 (50/5 sccm, 5 mTorr, 100 W RIE, 0 W ICP), and Ag/Au (20/200 nm) gate metal (Fig. 1(b)). In order to improve the rectifying behavior of the Schottky contacts, O_2 plasma exposure (25sccm, 1.5 mbar, 45 W, 30 min) was used prior to the gate deposition, as discussed in further detail below. The contact resistance R_C and sheet resistance R_{sh} were determined using transmission line model (TLM) structures. The Al/Ni/Au contacts were found to be Ohmic with contact resistance of 3.6 Ω mm and sheet resistance of 2.75 kΩ/□, in agreement with Hall measurements.[19] The measurements reported below were carried out at room temperature on transistors (Fig. 1(b)) with gate width, gate length, gate-source spacing, and gate-drain spacing of 75 μm, 1 μm, 0.5 μm, and 3.5 μm, respectively.

To obtain rectifying Schottky contacts on oxide materials,[24,25] we used oxygen plasma exposure. Fig. 3 shows the effect of O_2 plasma exposure on the I-V characteristics of gate Schottky diodes. The diodes exposed to O_2 plasma diodes were found to have 3 orders of magnitude lower gate leakage currents. The reduction in leakage using oxygen treatment could be attributed to removal of surface carbon contamination.[26,27] From the forward characteristics of the Ag Schottky, the ideality factor was found to be high (ranging from 3 to 5), which indicates non-ideal thermionic emission transport, and an effective Schottky barrier height could not be extracted for this measurement from the conventional thermionic emission theory. Interfacial layers,[28] non-homogenous interfaces,[29] or some other transport mechanism such as tunneling could be the reason for the non-ideal behavior. More detailed measurements would help to clarify the transport mechanisms for the heterostructure Schottky junctions in this study.

Capacitance-voltage (C-V) measurements (Fig. 4) of the gate Schottky diode as a function of bias were done using a B1500 parameter analyzer (signal amplitude 30 mV, frequency 1 MHz). The loss tangent ($1/RC\omega$) was found to be relatively high (>0.2) above a reverse bias of −5 V, which limited the measurement range. For an applied bias of $V_G = -5$ V, $2.5 \times 10^{13}\,cm^{-2}$ carriers (approximately 8.3% of the total sheet charge) was modulated. From the capacitance value at equilibrium and the epitaxial thickness of the film (28 nm), the dielectric constant of STO film was found to be 45, which is much lower than the dielectric constant of bulk STO at room temperature (300). As suggested by a recent publication,[25] the oxygen deficiency related to the growth conditions of the STO film could be responsible for the lower dielectric constant in the films investigated here. Local electric fields in some region of the heterostructure (for example,

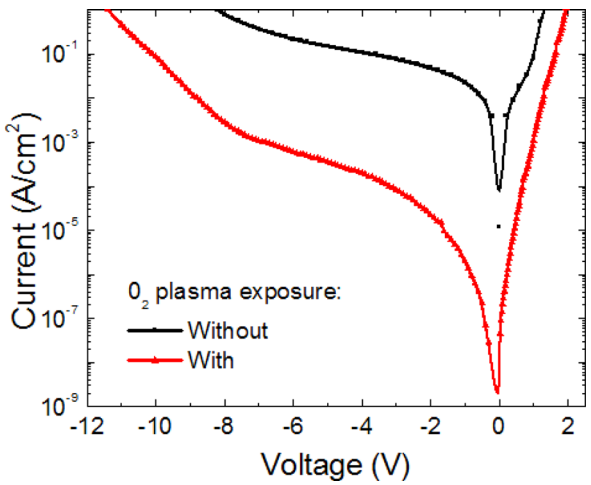


FIG. 3. I-V characteristics of Schottky contacts with and without 30 min of O_2 plasma exposure, respectively.

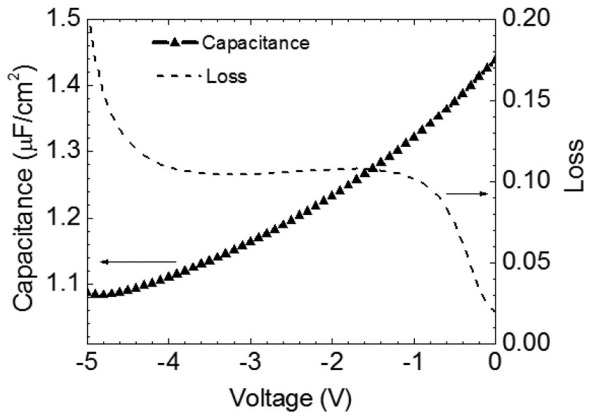


FIG. 4. Capacitance voltage characteristics (1 MHz, 30 mV) of the STO/GTO structure. Based on the epitaxial structure, dielectric constant of STO was estimated to be 45.

close to the 2DEG) could also account for a lowering of the dielectric constant since the dielectric constant of STO decreases at higher electric field values.[30,31] The decrease of capacitance with respect to the reverse gate bias voltage may also be attributed to the field dependence of the dielectric constant.

Three terminal measurements were carried out on the fabricated transistors. The measured output characteristics of the device are shown in Fig. 5(a). For the available gate voltage range (up to −12 V), 20.3% of total current was modulated. The measured transconductance g_m at a drain bias $V_D = 5$ V is shown in Fig. 5(b). As expected from the C-V measurements and the relatively low mobility, a flat transconductance profile was obtained with an average $g_m \sim 1.75$ mS/mm. The gate leakage was lower than 1 mA/mm for the bias range described here and therefore much lower than the drain current. While the channel could not be completely pinched-off, based on the equilibrium charge density of 3×10^{14} cm^{-2}, the modulated charge density is estimated to be 6×10^{13} cm^{-2}, which is the highest carrier density modulated in any material system.

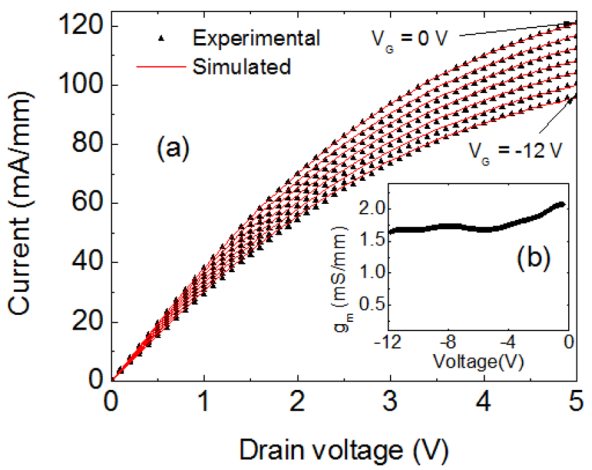


FIG. 5. (a) Measured and calculated output characteristics for the STO/GTO HFET. The gate voltage V_G was swept from 0 V to −12 V in steps of −2 V. A field effect mobility of 5 cm^2 V^{-1} s^{-1} was extracted. (b) Transconductance profile of the HFET at a drain voltage of $V_D = 5$ V.

The current-voltage characteristics of FET transistor were modeled using gradual channel model where the drain current is given by

$$I_D = \mu C_{STO}[(V_G - V_T)V_D - {V_D}^2/2]W/L, \quad (1)$$

where μ is the carrier mobility, C_{STO} is the capacitance per unit area of the STO layer, V_D is the applied drain voltage, V_T is the pinch-off voltage, L and W are the length and the width of the channel, respectively. The capacitance C_{STO} was extracted from the experimental C-V characteristics at $V_G = 0$ V. The experimental and the theoretical results were found to match for pinch-off voltage $V_T = -60$ V and a field effect mobility μ of approximately 5 cm^2 V^{-1} s^{-1}, which matches well with the measured mobility for 2DEG at the GTO/STO interface at room temperature.

The maximum negative gate voltage applied was limited by the gate leakage, presumably caused by electric breakdown of the STO barrier layer, since the electric field in the STO approaches the breakdown field (3 MV/cm) at the highest gate biases applied. The channel was not pinched off because the effective dielectric constant was found to be 45, which is much lower than the expected value (300). Increasing this dielectric constant through improvements in growth, optimization of the STO thickness, or post-growth treatment could help to increase the dielectric constant and thereby the maximum charge modulation possible.

In conclusion, we demonstrated the feasibility of STO/GTO heterostructure field effect transistors. An STO/GTO heterostructure was designed to exploit the advantages an inverted HFET topology. Oxygen plasma treatment was found to be critical in achieving low-leakage Schottky contacts on STO. The heterostructure field effect transistors presented here show modulation of up to 6×10^{13} electrons/cm^2, which represents the highest charge density modulated in a planar field effect transistor in any material system. The results presented here represent the first oxide field effect transistor with high sheet charge modulation and could have applications in various fields including plasmonics, electronics, and the physics of correlated systems.

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