A 0.54 THz Signal Generator in 40 nm Bulk CMOS With 22 GHz Tuning Range and Integrated Planar Antenna

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***Abstract*—This work presents the design and measurements of a 0.54 THz signal generator implemented in a 40 nm bulk CMOS technology. An *LC*-VCO operating at 180 GHz is connected to a nonlinear buffer, which is designed to generate the wanted third harmonic at 540 GHz. The third harmonic is coupled via a transformer to the output. The developed techniques are implemented on two different chips: one with a probe pad for on-wafer measurements and one with an on-chip planar dipole. The measured peak output power using a WR-1.5 probe is −31 dBm at 543 GHz, for 16.8 mW of dc power consumption. By changing value of the parasitic I-MOS varactors of the *LC*-VCO ("parasitic tuning"), the output frequency can be tuned from 561.5 to 539.6 GHz, resulting in a 21.9 GHz tuning range, which is the highest reported so far for CMOS THz oscillators. The 3-dB output bandwidth is 5.5 GHz. The 540 GHz signal generator with on-chip antenna is used for THz imaging without the use of substrate or focusing lenses, demonstrating some of the capabilities of CMOS for low-cost, mass-produced THz imagers.**

***Index Terms*—CMOS, dielectric contrast, harmonic, imaging, on-chip antenna, signal generator, sub-mm wave, terahertz (THz), VCO.**

I. Introduction

With the continuing scaling of CMOS nodes and increases in operation frequency of RF integrated circuits, there is more interest in the terahertz (THz) spectrum than ever before [1]–[33]. Ranging from 300 GHz to 3 THz, the THz or sub-mm wave spectrum lies between the domains of optics and electronics on the frequency scale. The reason for the current interest is the wide range of possible applications of THz electronics [1]–[6]. The presence of large chunks of available bandwidth in the THz spectrum would allow Gbit/s communications, meeting the steady demand for higher (wireless) data rates. Another reason for the THz interest is its imaging capabilities: THz waves can penetrate through clothing and detect concealed items, proving useful in stand-off personnel screening for security reasons. Nondestructive quality control of packaged goods, as well as 3-D imaging and accurate distance, speed and acceleration measurements are also among the potential uses of the sub-mm wave waves. Due to the interaction of THz waves with different chemical components, these circuits can be used for spectroscopy applications such as cancer detection, cavity detection for dentistry, or detecting the water contents (and ripeness) of fruits and vegetables.

While the possible applications look promising, building THz circuit blocks has proven to be difficult. Most commercially available THz products are based on III-V technologies, where the $f_{\max}$ has reached the 1 THz mark [7], [8]. While III-V technologies are acceptable for low-volume niche markets, the preferred technology for mass-produced THz chips would be CMOS. The main roadblock preventing CMOS THz circuit blocks is the $f_{\max}$, which is around 300 GHz for a 40 nm bulk CMOS technology and preventing fundamental oscillators and power amplification above this frequency. However, it is still possible to generate power above $f_{\max}$ in the form of harmonics of sub-$f_{\max}$ signals. By using high-frequency harmonics, CMOS signal generators operating near and in the THz spectrum have been demonstrated. A major drawback of these harmonic generators is the limited output power generated at these high frequencies. Several techniques have been proposed to improve the output power by combining harmonic signals, including N-push VCOs [21]–[23], linear superposition [24], and (magnetically) coupled oscillators [25], [26]. Additionally, harmonics-based signal generators have a low power efficiency, as the majority is wasted at the fundamental frequency and other unwanted harmonics. Furthermore, the tuning range of sub-mm wave transmitters is limited as well.

In recent years, progress has been made at the high end of the mm-wave spectrum to reach output powers near and over 0 dBm [27], [28] and raising the fundamental frequency of VCOs and amplifiers [29]–[32], but these performances have yet to be achieved in sub-mm wave CMOS transmitters. On top of all of these drawbacks, the design of THz circuits is further complicated by the limited accuracy of transistor simulation models, the increasingly dominant impact of the parasitic components, and the modeling of passives and interconnect structures at (sub)-mm wave frequencies.

This work will present the design and measurement of a sub-mm wave THz signal generator with large tuning range, fabricated in a 40 nm bulk CMOS technology. The wanted third harmonic is coupled through a transformer to the output, which is a probe pad or an on-chip planar antenna. Preliminary results of the version with probe pads are discussed in [33]. Section II

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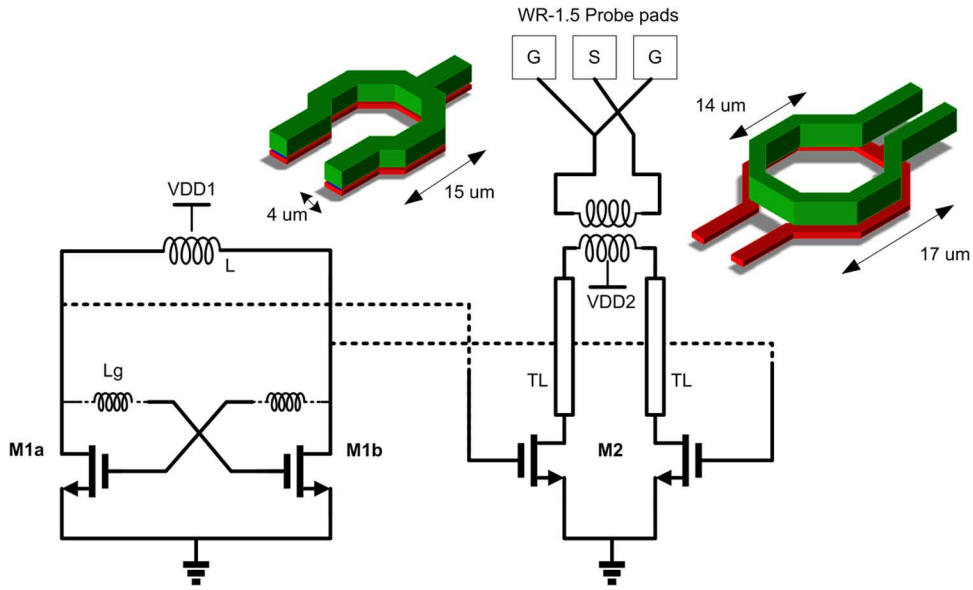


Fig. 1. Overview of the signal generator, consisting of a 180 GHz VCO, a nonlinear amplifier/buffer to generate the third harmonics, and the transformer to couple the third harmonic to the output.

will describe the design choices and difficulties of the different blocks of the signal generator. Section III contains the measurement results for the fabricated circuits, as well as some THz imaging examples that were realized using the transmitter with integrated antenna presented in this work. The measurement results are compared with current state-of-the-art THz CMOS signal generators. Conclusions are given in Section IV.

II. Third-Harmonic Generation and Extraction From VCO to Load

The objective of this work was to design a signal generator operating above 500 GHz using harmonics. The circuit topology is shown in Fig. 1. The THz signal generation starts with an *LC*-VCO with cross-coupled transistors to generate the fundamental frequency at 180 GHz. The VCO is connected to a differential amplifier, which generates the third harmonic while also acting as a buffer between the output and the VCO core. This third harmonic is then coupled through a transformer to the output probe pad or antenna. This section will discuss the building blocks of the signal generator.

A. VCO Core

The starting point is the fundamental frequency (below $f_{\max}$) from which the harmonics (above $f_{\max}$) will be derived. A low fundamental frequency is easier to generate but requires a higher order harmonic to reach the THz spectrum, which quickly degrades the output power. On the other hand, a high fundamental frequency makes generating THz signals possible with a lower harmonics, but increases the design difficulty of the VCO as the fundamental oscillation nears the $f_{\max}$. This work chooses the latter approach and uses the third harmonic of a 180 GHz VCO.

The fundamental oscillator is an *LC*-VCO with cross-coupled transistors, shown in Fig. 1. As the oscillation frequency f_0 of the VCO is determined by the L and C components of the tank

$$f_0 = \frac{1}{2.\pi.L_{\text{tank}}.C_{\text{tank}}} = \frac{1}{2.\pi.(L_{\text{ind}}+L_{\text{par}}).(C_{CC}+C_{\text{buffer}}+C_{\text{IMOS}}+C_{\text{par}})} \quad (1)$$

then these components become very small for near-$f_{\max}$ oscillation.

The L of the LC tank is provided by a small, single-turn symmetrical inductor with a center tap for the VCO supply voltage, VDD1. In many *LC*-VCOs, a varactor is placed in parallel with the tank inductor, between the drains of the cross-coupled transistors M1a and M1b. This varactor allows tuning the oscillation frequency by varying the capacitive part of the resonance tank [34], [35]. To effectively control the oscillation frequency, this varactor should be sufficiently large compared with the other (parasitic) capacitances. However, a large tuning varactor would add too much capacitance to the tank whose LC values should be very small for resonance at the target frequency. In addition, the quality factor of varactors decreases with frequency, reducing the overall quality of the LC tank. For these reasons, the tuning varactor was omitted from the *LC*-tank. The resulting tank capacitance comprises the capacitances of the cross-coupled pair M1 ($\mathrm{C_{cc}}$), buffer transistors M2 ($\mathrm{C_{buff}}$) and the parasitic capacitance of the inductor and interconnect ($\mathrm{C_{par}}$). Even though no tuning element was added to keep the tank components small, the frequency can still be controlled: the gate–source capacitance $\mathrm{C_{gs}}$ of the cross-coupled transistors, which contains a parasitic inversion-MOS varactor, can be varied by changing the biasing voltage ($=$ supply voltage VDD1), as shown in Fig. 2.

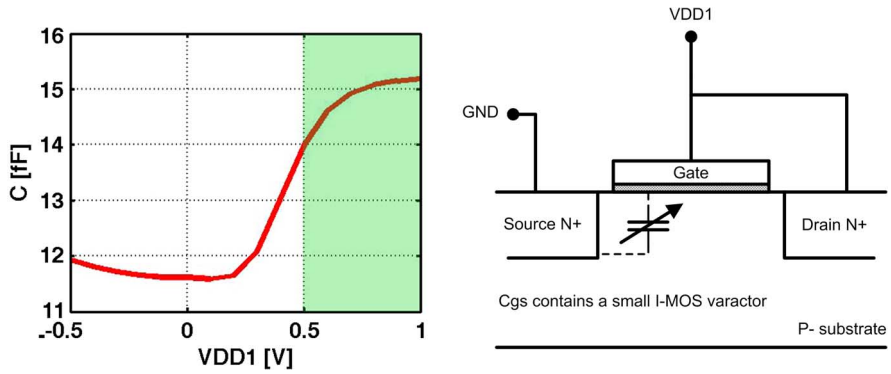


Fig. 2. Capacitance variation of the parasitic I-MOS varactors in one of the cross-coupled transistors. By changing the supply voltage VDD1, the capacitance of the tank can be changed.

This variation in capacitance is only a few femto-Farads and is usually negligible compared with the fixed capacitance or tuning varactor. However, since no tuning varactor is added and the fixed capacitance is kept small, the impact of this parasitic I-MOS varactor on the tank capacitance becomes sufficiently large to allow "parasitic tuning."

In addition to capacitance for the tank, the cross-coupled pair also provides a negative resistance to compensate the resistive losses in the *LC* tank. As the generated negative resistance diminishes with increasing frequency, the size of the M1 transistors has to be increased to adequately compensate the inductor losses. Unfortunately, larger transistors also increase parasitic capacitances, lowering the *LC* tank's resonance frequency. By implementing series inductors in the cross-coupling connections, the performance of the M1 transistors is improved: this allows smaller transistor sizes for the same negative resistance at high frequencies, resulting in a smaller tank capacitance [36], [37].

Due to the small values of *L* and *C*, parasitic effects that are otherwise non-dominant can have a critical impact when designing sub-mm wave circuits. It is therefore important that the transistor models include this high-frequency behavior. While the $f_{\max}$ of a minimal 40 nm transistor is above 300 GHz, the practical limit on a transistor's speed will be lower due to the transistor size, layout and wiring. To maximize the $f_{\max}$ of M1 and M2, all transistors have double-contact gates to reduce the gate resistance $\mathrm{R_g}$ and narrow, 1 μm fingers (Fig. 3). $\mathrm{C_g}$ and $\mathrm{C_d}$ of M1 form the majority of the capacitive part of the *LC*-tank. To reduce $\mathrm{C_g}$, metals 3–6 were used in parallel for the cross-coupling connection of the M1 transistors, as lower metal layers would result in a larger $\mathrm{C_{gb}}$. Fig. 4 shows the layout of the VCO core. One important detail is the connection between the drain of the M1 transistors in the bottom metal layer and the leads of the inductor, in the top two metal layers. Using a small via stack straight to the top metals would keep $\mathrm{C_{db}}$ small, but would introduce a larger series resistance. As this resistance would add to the resistive losses of the inductor, a larger negative resistance has to be generated to allow the oscillator to start up. A big via stack, on the other hand, would have a low series resistance but a large overlap of lower-layer metal and substrate, creating a large $\mathrm{C_{db}}$ and reduce the $\mathrm{f_0}$ of the VCO. To optimize this interconnect, the via stack was given a tapered

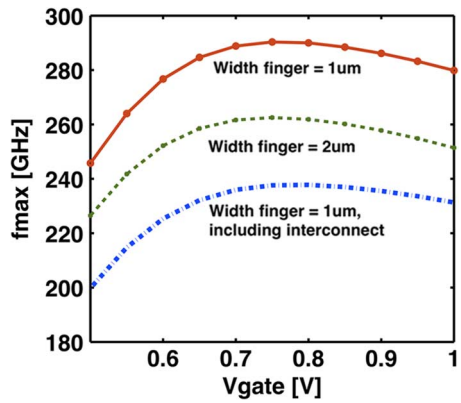


Fig. 3. Simulated $f_{\max}$ of transistors with the same W/L ratio (20/0.04 μm) but different width and number of fingers configuration. This also shows the difference in $f_{\max}$ for a stand-alone transistor, and one including interconnecting metals.

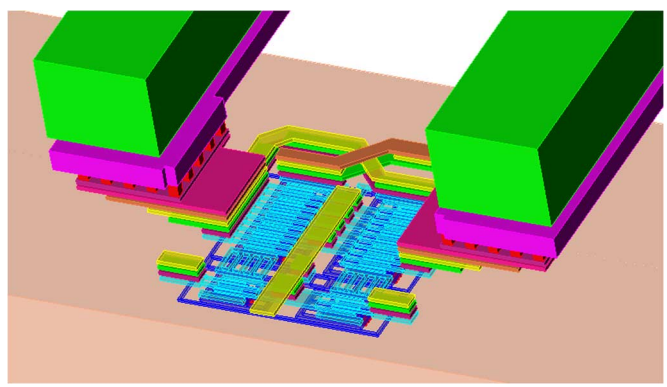


Fig. 4. Layout of the VCO core. The inductor leads in the top metal layers are connected to the transistors through a tapered via stack. All transistors have double gate contacts and 1 μm finger widths.

shape (visible in Fig. 4): narrower at the bottom, to minimize the metal-substrate capacitance, and getting wider to allow for more via's at higher metal layers, where the substrate coupling is less. To accurately model all layout-dependent parasitics of the interconnecting metals as well as passive components (inductor, transformers, transmission lines. . .), a EM-simulator (ADS Momentum/Integrand EMX) is used.

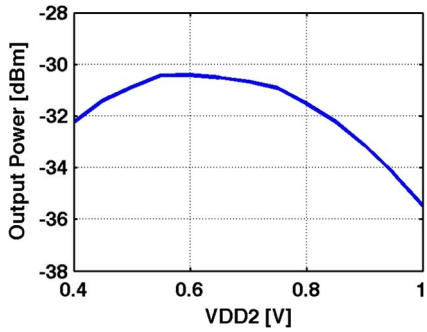


Fig. 5. Simulated output power versus buffer supply voltage VDD2. A value of 600 mV increases the nonlinear behavior of the buffer, resulting in more third-harmonic generation.

The single-turn inductor L used in the oscillator determines not only the inductance of the *LC*-tank, but also the resistive loss that the cross-coupled transistors have to compensate. By using the top two metal layers in parallel instead of only one metal layer, the series resistance of the inductor is reduced, as well as a small reduction in inductance. The inductor has an inner diameter of 15 μm and width of 4 μm, resulting in an inductance of 24.3 pH and a Q-factor of 22.9 at 180 GHz.

B. Buffer and Double-Frequency Transformer

Transistors M2 create the nonlinear buffer that isolates the *LC*-tank from the load. The transistor size is kept small to reduce the capacitive loading of the *LC*-tank. This buffer also generates the third harmonic of the 180 GHz oscillation signal. To improve the generation of the third harmonic, the voltage swing of the VCO signal, which is applied at the gates of the buffer, should be large. To maximize the VCO swing, the traditional current-biasing transistor between M1 and VDD1 is removed, increasing the voltage headroom. Additionally, the supply voltage of the buffer (VDD2) is chosen differently from the VCO core to improve non-linear operation. The gate bias of the buffer is VDD1, the supply of the VCO core. For VDD1 higher than 800 mV, the simulated output power saturates. Simulations showed that a VDD2 of 600 mV resulted in the highest amount of output power at the third harmonic (Fig. 5).

After generation, the third harmonic is coupled to the output using a transformer. The buffer transistors still have to operate at the fundamental frequency, as the third harmonic's power is related to the fundamental signal. The transformer (Fig. 6) thus has two purposes: 1) biasing and output matching of the buffer at the fundamental frequency on one side of the transformer and 2) transferring the third harmonic to the output while suppressing other unwanted harmonics.

To achieve this double functionality, the transformer was designed to have a good coupling of the third harmonic from the buffer to the output, and is matched with the probe pads at 540 GHz. At the same time, the resulting transformer is conjugate matched with the output of the buffer at the f_0 of 180 GHz using high Z_0 (130 Ω) differential transmission lines. Simulations show that the whole coupling structure, which starts at the drains of the M2 transistors, favors the transfer of the third harmonic to the output over the fundamental frequency (Fig. 7).

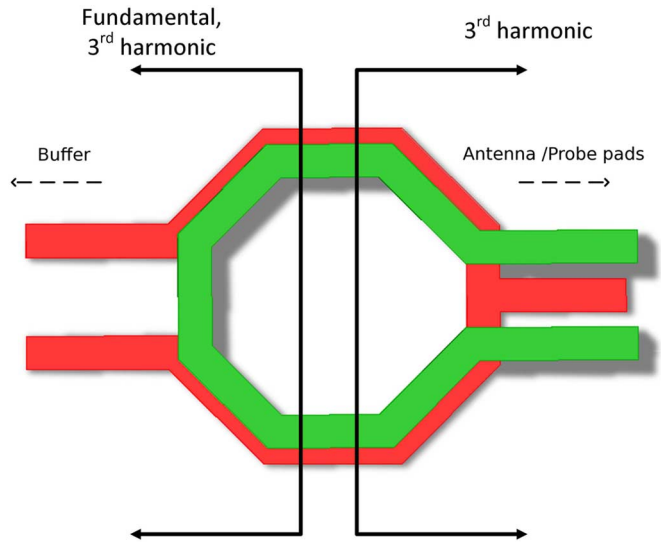


Fig. 6. Transformer has a different purpose and target operation frequency at each side. Transformer windings have an inner diameter of 17 and 14 μm, respectively.

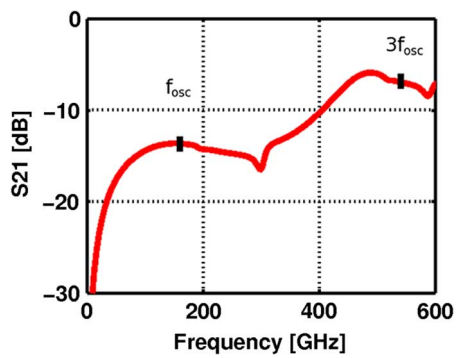


Fig. 7. Simulated S_{21} for the coupling of fundamental and third harmonic from the buffer drain node to the output.

The transformer used in the buffer is implemented as two coupled single-turn inductors in the top two metal layers. To keep the self-resonance frequency (SRF) of the transformer windings above the third harmonic, small inductor diameters and narrow trace widths are used. The primary (17 μm) and secondary winding (14 μm) have different diameters, as this is a trade-off between the higher SRF of a planar transformer and the better coupling of a stacked topology. The inductor on the buffer side includes a center tap for the biasing of the M2 transistors through the differential transmission lines. Each probe pad is 25 μm $\times$ 40 μm. While larger and longer probe pads make it easier for landing the probe tips, this will negatively impact the transfer of high-frequency signals as the probe pads form a parallel-plate capacitor with the substrate and between the pads themselves.

C. Antenna Design

For imaging applications, an antenna is necessary to radiate the THz waves. While an in-depth explanation of high-frequency antennas lies beyond the scope of this work, a short overview of several options is given.

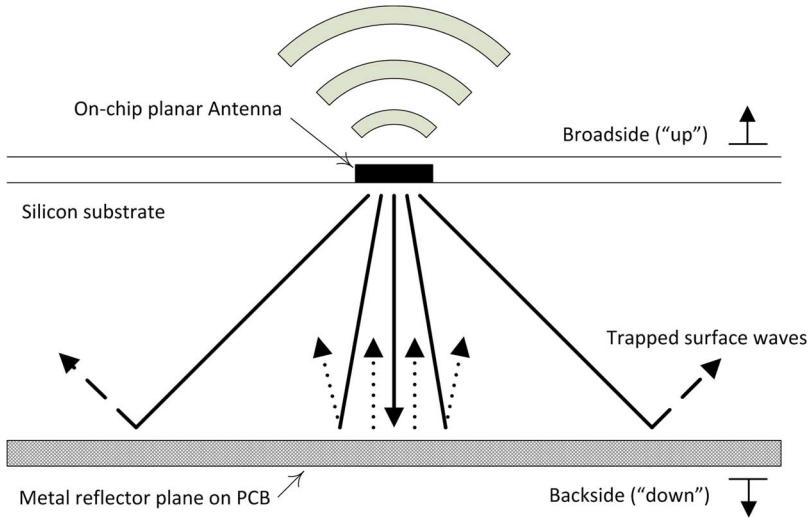


Fig. 8. Diagram of on-chip antenna and substrate radiation, which significantly reduces antenna efficiency. By using a metal reflector at the bottom of the Si substrate, part of the substrate waves can be recovered.

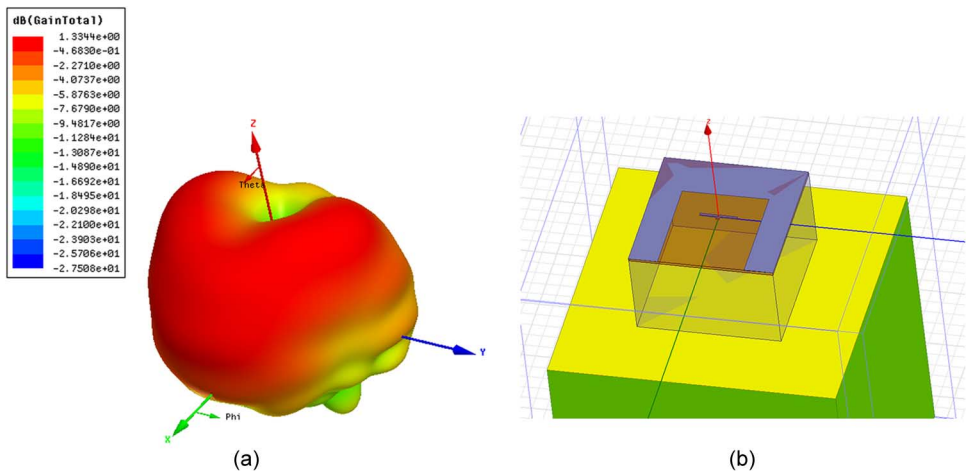


Fig. 9. (a) Simulated antenna gain and (b) HFSS simulation model, which includes dummy metals surrounding the dipole antenna for metal density purposes.

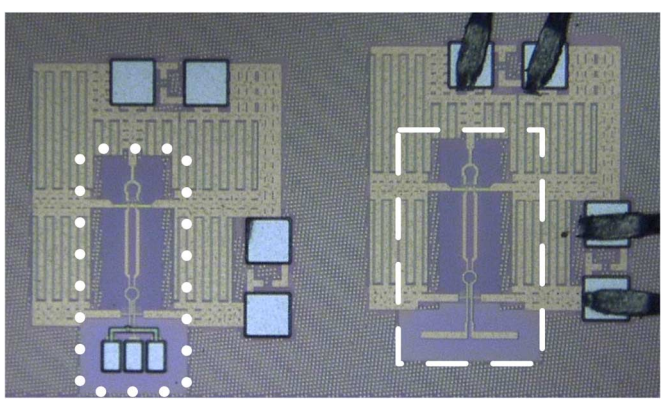


Fig. 10. Die photograph of the fabricated signal generators, with probe pads for on-wafer measurements (left dotted area) and on-chip planar antenna for imaging (right, dashed area).

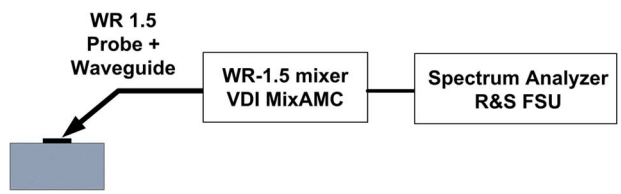


Fig. 11. Measurement setup for on-wafer measurements using WR-1.5 probe.

Using a high-performance off-chip antenna is very difficult due to the large attenuation of the inter-chip connections (bond wire or flip-chip). With the wavelength lambda being smaller than 1 mm for THz signals, antennas can be fabricated on-chip without immense area penalties. Unfortunately, on-chip antennas tend to have low radiating efficiency because of the low-resistive silicon substrate. The majority of the transmitted power is radiated in the dielectric Silicon substrate, resulting in power loss due to trapped waves and substrate modes, and these losses increase with the thickness of the dielectric substrate.

While the use of thinner substrates (0.01 λ for dipole antenna [38]) might provide a solution at lower frequencies, at sub-mm wave frequencies this would result in very thin and delicate wafers of only a couple of microns thick. Bondwire antennas [39] show good results at mm-wave frequencies, but the very

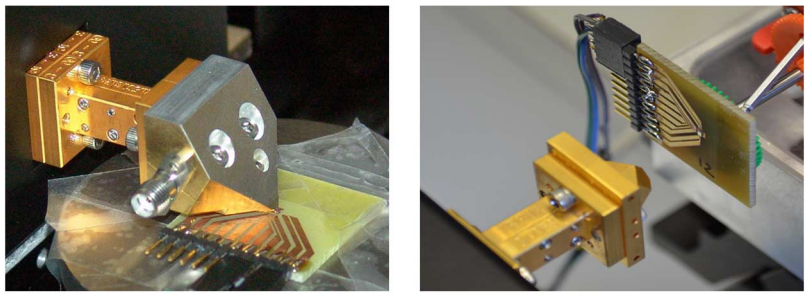


Fig. 12. Closeup of the two measurement setups: (a) probe and (b) diagonal horn antenna.

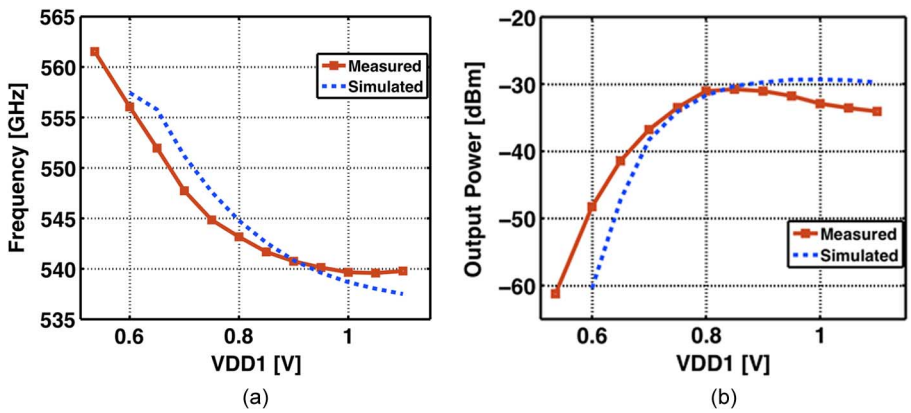


Fig. 13. Measured (on-wafer) and simulated (a) frequency and (b) output power for varying VDD1 from 540 mV to 1.1 V. VDD2 remains fixed at 650 mV. Good correlation between measurements and simulations is observed. Peak output power is −31 dBm at 543 GHz.

short wires necessary in the THz spectrum increase the packaging and bonding requirements. Another approach in recent works [25], [27] places the chip on a (hyper-) hemispherical Silicon lens [40], which refocuses the substrate-radiated power. This results in the main radiation lobe being on the substrate side (backside) instead of the top side (broadside). The directivity and radiation efficiency is greatly improved by these substrate lenses, but a more complicated packaging process is required. Additionally, silicon substrate lenses are expensive and would thus negate the cost benefits of using CMOS.

To explore the possibility of a low-cost CMOS THz imaging system, the on-chip planar dipole antenna is not augmented with a Silicon lens. Instead, the chip was mounted on a regular FR4 PCB with a metal plane on top. The metal will act as a reflector for the substrate waves, which will travel back through the substrate and combine with the broadside-radiated waves for constructive interference (Fig. 8).

As the reflector introduces a 180° phase shift, the distance between antenna and reflector should be $\lambda/4$ (total path length of reflected signal is $\lambda/2$) to result in optimal constructive interference between the reflected backside and radiated broadside waves [41]. Varying the substrate thickness can set this antenna-reflector distance. While a distance of $\lambda/4$ would also result in impractically thin wafers, the same constructive interference will be present for uneven multiples of $\lambda/4$, albeit with increasing substrate losses. This results in a trade-off between mechanical strength of the thinned wafer and antenna efficiency. In this work, the foundry's default 12 mil ($\sim$ 300 μm) thickness was used. Simulations in Ansoft HFSS show a radiation efficiency of 28% at 540 GHz. The simulated gain is shown in Fig. 9, showing a peak gain of 1.33 dB. The simulation model includes a large metal plane surrounding the dipole to emulate dummy metals. These surrounding (dummy) metals will skew the ideal radiation pattern. Using a large, uniform metal surface instead of the actual dummies is an overestimation of this effect, but necessary to maintain a reasonable simulation time.

III. Measurement Results

Using the above-mentioned techniques, two chips were implemented in 40 nm CMOS were measured: one with a probe pad and one with an on-chip antenna. Die photographs of both chips are shown in Fig. 10. The active area is 110 μm $\times$ 300 μm for the probe pad version (dotted line) and 170 μm $\times$ 300 μm for the implementation with antenna (dashed line). The total chip area including bond pads and decoupling is 350 μm $\times$ 430 μm for each version.

Measuring sub-mm wave signals is a challenging endeavor, as the high losses of the measurement equipment at these frequencies make it hard to detect the THz output signals. Other works at these frequencies use a quasi-optic measurement approach [22], [23] where an on-chip antenna radiates the signal into a Fourier-transform infrared spectroscopy (FTIR) system with sensitive, liquid nitrogen cooled bolometers to be able to detect the THz signals. Measurements in the presented work

were done using a VDI MixAMC with sub-harmonic mixer for the 500–750 GHz band. The output of the mixer is connected to a R&S FSU Spectrum Analyzer. The spectrum analyzer was calibrated using a Erickson PM4 power meter and a VDI AMC source module.

A. Probe Measurements

For the on-wafer measurements, this work uses a high-frequency probe and downconverter to accurately determine output frequency and power of the 540 GHz signal generator. The measurement setup is shown in Fig. 11. It consists of a WR-1.5 DMProbe [42] attached to the VDI MixAMC downconverter.

The measurement results and comparison with simulations are displayed in Fig. 13. Measurements show good agreement with simulation results, indicating correct modeling of the passives and RF transistor's behavior at frequencies above f_{max}. When the supply voltage of the buffer, VDD2, is fixed at 650 mV, the VCO starts oscillating at 561.5 GHz for VDD1 = 540 mV. By changing the supply voltage of the VCO core, a 21.9 GHz tuning range is measured (539.6 to 561.5 GHz). After accounting for the losses of the probe and mixer, the peak output power is −31 dBm at 543 GHz, with a DC power consumption of 16.8 mW for a VDD1 of 800 mV. If the tuning range is limited to frequencies with an output power within 3 dB of the 31 dBm peak, the tuning range becomes 5.5 GHz, stretching from 539.6 to 545.1 GHz. Thanks to the fully differential approach, even harmonics are suppressed in favor of the uneven harmonics: the fourth harmonic at 730 GHz did not rise above the noise floor, meaning that it's output power is at least 30 dB lower than the wanted third harmonic. Fundamental and second harmonic could not be measured in the on-wafer version because of the small bond pad pitch required for the WR-1.5 probe. The simulated phase noise at 543 GHz is 69.6 dBc/Hz at 1 MHz offset.

B. Antenna and THz Imaging Results

To measure the oscillator chip with on-chip antenna, the probe was replaced with a diagonal horn antenna. The distance between the transmitter and the receiving antenna was 20 mm to fulfill the radiating far-field region criterion [43]. An example of the measured output spectrum is shown in Fig. 14. Simulated and measured radiation patterns are shown in Fig. 15. Using Friis formula [44], the equivalent isotropically radiated power (EIRP) was calculated to be −31.8 dBm for one chip. This EIRP can be improved by using antenna arrays or (substrate) lenses to increase the radiated power and directivity. These devices were not used in this work, as this would increase cost and packaging requirements of the transmitter. Assuming the simulated antenna gain of 1.33 dB is correct, the estimated radiated power of the transmitter is −33.13 dBm ($\mathrm{EIRP_{dBm}} - \mathrm{Antenna\ Gain_{dB}}$). The radiated 180 GHz fundamental signal was measured using a pyramidal horn antenna and a RPG WR-05 sub-harmonic mixer for the 140 GHz–220 GHz band. The resulting fundamental EIRP is −22.8 dBm. Additional matching/filter networks between the transformer and antenna could further reduce the transmission

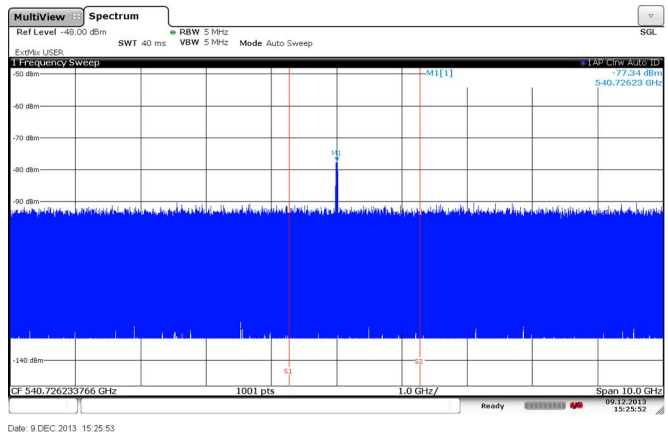
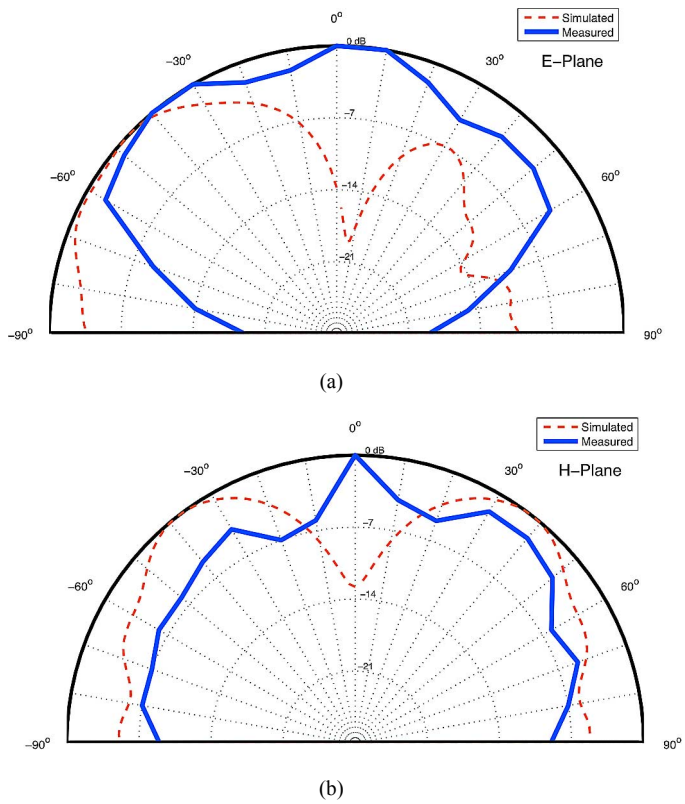


Fig. 14. Measured output spectrum of the chip with planar antenna, before accounting for losses.



(a)

(b)

Fig. 15. Simulated (dashed line) and measured (full line) radiation pattern of the transmitter with antenna.

of the fundamental signal, but will also attenuate the desired third harmonic power.

The peak received radiated signal at 540 GHz is 14 dB above the receiver's noise floor, which is −45 dBm in the wireless setup. To demonstrate the capabilities of lens-free THz CMOS imaging, the setup of Fig. 16 is used as a 1-pixel THz scanner for various objects. A mechanical stepper moves the object in the XZ plane (step size: 0.5 mm). The received power depends on the reflection, absorption and scattering of THz waves by the object. Fig. 17 shows the imaging result of an envelope containing a coin and vitamin tablet. Due to differences in material interaction with THz waves, the dielectric contrast allows the

TABLE I
COMPARISON WITH STATE-OF-THE-ART SIGNAL GENERATORS IN BULK CMOS

Ref.	Harmonic	Frequency (GHz)	Tuning Range (GHz)	Output Power (dBm)	Measurement	DC power (mW)	Area (mm^2)	Process Technology
This work	**3rd**	**543**	**21.9**	**-31**	**Probe**	**16.8**	**0.15**	**40 nm bulk CMOS**
	3rd	**540**	**11.3***	**-33.1**	**Antenna**	**18.9**	**0.15**	**40 nm bulk CMOS**
[22]	2nd	410	2	-47**	Antenna	16.5	0.25	45 nm bulk CMOS
[23]	4th	553	< 1	-36.6**	Antenna	64	0.29	45 nm bulk CMOS
[9]	3rd	482	NA	-7.9	Probe	61	0.02***	65 nm bulk CMOS
[18]	Fund.	573	< 1	-19.2	Probe	115	0.41	0.25 μm InP HBT
[25]	3rd	288	4	-1.5/-4.1	Probe/Antenna + Si lens	280	0.29	65 nm bulk CMOS
[27]	2nd	260	3.7	0.5	Antenna array + Si lens	800	2.3	65 nm bulk CMOS

* Limited by equipment noise floor.
** Measured using FTIR and bolometer.
*** Without bond pads.

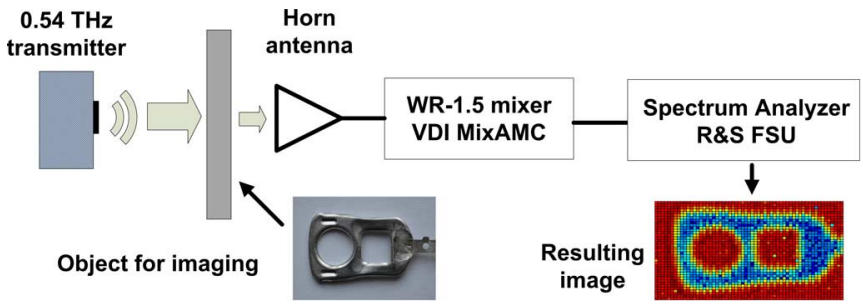


Fig. 16. Setup used for lens-free THz imaging using the 0.54 THz signal generator with antenna. The object under test (the lid of a can from a Belgian beer company) is moved in the XZ plane with a step size of 0.5 mm.

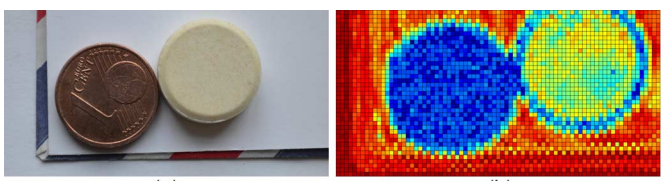


Fig. 17. (a) Lens-free THz imaging: a coin, vitamin tablet and name card are placed inside an envelope. (b) Using the setup shown in Fig. 16, a dielectric contrast image is created.

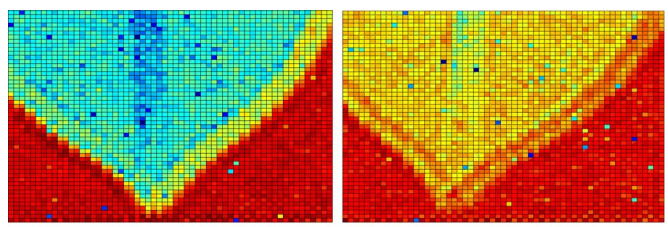


Fig. 18. Measured difference in water concentration of (a) a freshly cut and (b) dried for 48 h orange tree leaf. The remaining water content of the dried leaf is concentrated in the stem.

distinction between the two objects of the same size and geometry. Industrial production lines could use this type of dielectric contrast information for nondestructive quality control.

Since THz waves are greatly attenuated by water, THz imaging systems can also be used to determine the water concentration of products, such as food or plants. In Fig. 18, the drying process of a leaf is shown as seen through the THz imaging setup of this work. The freshly cut leaf has a high water concentration, resulting in a low power transmission through the leaf. As the leaf dries and the water concentration lowers, the absorption of THz waves diminishes, resulting in higher received power levels.

C. Comparison

Table I compares the results with current state-of-the-art THz oscillators. As the number of THz CMOS signal generators (300 GHz–3 THz) is quite limited, some signal generators operating at the high end of the mm-wave spectrum (100–300 GHz) have been included. The total tuning range and 3-dB output bandwidth of the presented chips are the largest reported for bulk CMOS oscillators above 400 GHz. The output power and EIRP of >500 GHz CMOS signal generators is low compared to recent advancements in the 250–300 GHz range. This work shows that despite this power gap, small and cheap CMOS transmitters for lens-free THz imaging are possible and can be used for a variety of (industrial) applications. Fully integrated systems containing transmitters, receivers and signal processing blocks will allow THz applications to be available for consumer products and unleash the full potential of the THz spectrum.

IV. Conclusion

In this work, a 0.54 THz signal generator fabricated in 40 nm bulk CMOS is presented which generates and extracts the third harmonic from a 180 GHz *LC*-VCO using respectively a buffer and transformer. Frequency tuning is realized by parasitic I-MOS varactors present in the VCO transistors. Two version of this signal generator are presented en discussed: one with probe pads, and one with an on-chip planar antenna. On-wafer measurements show a 21.9 GHz tuning range (539.6 to 561.5 GHz) and 3-dB output bandwidth of 5.5 GHz (539.6 to 545.1 GHz), which are the widest ranges for CMOS signal generators above 400 GHz. The measured peak output power is −31 dBm at 543 GHz, for a dc power consumption of 16.8 mW. The same signal generator was also fabricated with an on-chip planar dipole antenna. A metal plane on the substrate bottom is used to improve the radiation efficiency by reflecting substrate waves to create constructive interference at broadside. The transmitter with antenna is used in a lens-free THz imaging setup, resulting in the dielectric contrast images shown. This work demonstrates the feasibility of a low-cost CMOS THz imaging transmitters without bulky and expensive substrate or beam-focusing lenses.

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