SiFive Public Errata Notice
Errata_FU740-C000_20241112

Proprietary Notice

Information in this document is provided “as is,” with all faults.

SiFive expressly disclaims all warranties, representations, and conditions of any kind, whether express or implied, including, but not limited to, the implied warranties or conditions of merchantability, fitness for a particular purpose and non-infringement.

SiFive does not assume any liability rising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation indirect, incidental, special, exemplary, or consequential damages.

SiFive reserves the right to make changes without further notice to any products herein.

Errata_FU740-C000_20241112

This document lists all known issues impacting the SiFive FU740-C000 as of November 12, 2024.

The following table describes each errata category severity level (i.e. "CAT" level):

CAT-A	A **critical** error with **high probability** & the **absence of an effective workaround**. For an affected configuration, the error is likely to manifest in many systems and applications.
CAT-B	A **significant** error with **high/medium probability** and an acceptable workaround, or a **minor error** with a **high** probability (regardless of workaround), or a **critical** error with **medium/low probability**. For an affected configuration, the error is likely to manifest in many systems and applications.
CAT-C	A **minor** error with **high/medium probability** or **significant** error with **low probability** and an **acceptable workaround**.

Table 1-1. Errata Category Severity

The errata category classification is derived from the following impact/probability relationship:

Probability of an errata to manifest with the affected configuration	Impact		
	Critical	Significant	Minor (feature limiting)
High	CAT-A	CAT-B	CAT-B
Medium	CAT-B	CAT-B	CAT-C
Low	CAT-B	CAT-C	CAT-C

Table 1-2. Errata Category Classifications

Impact	
Critical	Functional
Significant	Functional, workaround available
Minor	Feature limiting
Probability	
Low	SiFive believes that it is very unlikely that a customer would encounter this behavior in real use of the IP. Examples of reasons for this would be: • Manifestation requires a specific instruction sequence that is not sensible for normal code to use and that a compiler would never emit. • Manifestation requires software to do something that we would not expect normal software to do, like writing to reserved regions/registers.
Medium	SiFive believes that it is possible, but not likely, that a customer would encounter this behavior in real use of the IP. For instance, we are only able to manifest the behavior by subjecting a block to targeted high-stress stimulus in a unit-level testbench and believe it to be unlikely that surrounding subsystem or system level logic could cause that level of stress.
High	SiFive believes that it is possible for a customer to encounter this behavior in real use of the IP in “normal” use cases.

Table 1-3. Errata Terminology

If you have any questions as to whether an erratum affects your configuration, please submit a customer support ticket or contact support@sifive.com.

CIP-286

Title

Debug Module/ROM Accessible in M-Mode

Implication

It is possible to access Debug Module memory region in M-Mode, whereas the Debug Specification indicates that region should only be accessible in Debug Mode.

Workaround

Do not access Debug Module memory region from M-Mode.

Impact

Minor

Probability

Low

Category

CAT-C

CIP-312

Title

MMIO access on ITIMs causes false correctable error

Implication

When accessing ITIM over MMIO (i.e., for ITIM accesses other than fetches), the ITIM might report a correctable error when there was no error.

Workaround

Ignore the error

Impact

Minor

Probability

Medium

Category

CAT-C

CIP-453

Title

stval/mtval CSRs are not sign-extended for instruction access/page fault exceptions

Implication

UPDATE 2021-03-27: (Errata reclassified to CAT-B from previous CAT-C classification) Instruction access exceptions and instruction page-fault exceptions corresponding to negative addresses will incorrectly report bits 63:39 of the address in the `stval` or `mtval` CSR. Operating system page-fault handlers are likely to be confused by the error, causing resumable page faults to be reported as fatal errors. When running Linux, this erratum can manifest when loading kernel modules.

PREVIOUS: In normal use, negative addresses are used by the kernel, and the kernel doesn't page out its code pages. Therefore, an instruction page fault manifesting this bug is not expected to occur; and if it does occur, the kernel should treat it as a fatal error anyway. If the kernel tried to use `stval` to handle the page fault, then it would incorrectly see an invalid address rather than a valid one.

Workaround

UPDATE 2021-03-27: When the `mcause` register indicates an instruction page fault or instruction access exception, do not rely on `mtval` directly. Instead, use the expression (`mepc` + `mepc` ^ `mtval`) & 2 in place of `mtval`. Note that this expression only holds for instruction page faults and access exceptions. For other exceptions, use the value from `mtval` directly.

The same workaround applies to `stval`, replacing `mepc` and `mcause` with `sepc` and `scause`.

PREVIOUS: If instruction page faults with negative addresses do not need to be resumable, as is the case for Linux, no workaround is necessary.

In other cases, the correct value for `mtval` can be computed with the expression (`mepc` + `mepc` ^ `mtval`) & 2. This expression only holds for instruction page faults and access exceptions. For other exceptions, use the value from `mtval` directly.

The same workarounds apply to `stval`, replacing `mepc` with `sepc`.

Impact

Minor

Probability

High

Category

CAT-B

CIP-546

Title

When performance counters are set to count exceptions, they do not count other retirement events

Implication

It is not possible to use the same performance counter to count both exceptions and other retirement events (including instructions retired of specific type). Doing so will lead to incorrect counts for the other events.

Workaround

Use two separate counters: one for exception events and one for other instructions of interest.

Impact

Minor

Probability

Medium

Category

CAT-B

CIP-575

Title

L2 Sideband can report ECC error even after it was overwritten

Implication

The L2 Sideband includes a path to bypass data from older writes to newer hazardous requests, but still uses the corrected/uncorrected ECC result from the over-written entry for several cycles.

Workaround

Delay subsequent reads until the write has finished, such as by writing multiple times (3 times is sufficient).

Impact

Medium

Probability

Low

Category

CAT-C

CIP-576

Title

L2 response can report ECC error even after being overwritten

Implication

The L2 D-Channel response includes a path to bypass data from older writes to newer hazardous requests, but still uses the result of the ECC check (ie, ECC_correct/corrected_ECC_error/uncorrected_ECC_error) from the over-written entry for several cycles. This means that there is a short window of time during which an ECC error may be reported even once it has been overwritten.

Workaround

Tolerate multiple ECC errors reported for a single cache entry.

Impact

Minor

Probability

Low

Category

CAT-C

CIP-737

Title

mcause values does not reset to 0 after reset

Implication

mcause cannot be used to determine the cause of reset in SiFive Core IP.

Workaround

Do not rely on the mcause value to determine reset condition; however, always assume that SiFive implementations do not distinguish different reset conditions.

Impact

Minor

Probability

High

Category

CAT-B

CIP-899

Title

ECC error in D$ can cause store to be dropped

Implication

In a situation consisting of a store to address A, load from some address, store to address A, then load, the second store can be dropped if there is a correctable/uncorrectable ECC error detected.

The second store to address A does not take effect, but the error is still reported to the Bus Error Unit.

Since the bug can only manifest with two nearby stores to the same word, the first not detecting an error and the second detecting an error, this bug is not likely to occur in practice. In particular, if the error formed before the sequence began, the bug would not manifest.

Workaround

None at this time

Impact

Medium

Probability

Low

Category

CAT-B

CIP-930

Title

Race condition between write to *status.FS and floating point load that changes *status.FS.

Implication

This errata occurs when a floating-point load is issued, then software clears mstatus.FS (setting it to 0x0, OFF), then the load writeback occurs. The load writeback can erroneously set the mstatus.FS to DIRTY, resulting in mstatus.FS being DIRTY instead of OFF at the completion of the instruction sequence.

This sequence of events can only occur for MMIO floating point loads.

Workaround

Execute a fence before setting mstatus.FS = OFF (0x0).

Impact

Minor

Probability

Low

Category

CAT-C

CIP-993

Title

MTVAL/STVAL CSR set to incorrect value following EBREAK instruction

Implication

MTVAL/STVAL should be 0 following an EBREAK instruction; instead, it is set to an arbitrary value.

Workaround

Do not rely on the value of MTVAL/STVAL following an EBREAK instruction. EBREAK being the cause of an exception can be identified by examining MCAUSE (for M-mode) or SCAUSE (for S-mode)

Impact

Minor

Probability

Medium

Category

CAT-C

CIP-1293

Title

An L2TLB write will almost always block the next L2TLB search, even many cycles later.

Implication

Performance impact only. In almost all cases, the Core would behave as if it doesn’t have an L2 TLB.

Workaround

Set bit 0 ("Disable data cache clock gating") of the Feature Disable CSR (0x7C1) to disable D-Cache clock gating

Impact

Medium

Probability

High

Category

CAT-B

CIP-1464

Title

Chained triggers with both instruction and data never fire

Implication

Hardware allows 2 triggers to be chained, meaning both conditions must be satisfied at the same time for the trigger to fire. When a chain includes both instruction trigger and data address trigger, the breakpoint does not fire.

Workaround

Set a data trigger on any access to the data item, then in the GDB breakpoint command script, check whether the PC is the one you want and restart if not. This has been identified & documented as the final fix for this errata, this will be ceased to be tracked as an errata, in releases post 21G2.01.00

Impact

Minor

Probability

High

Category

CAT-B

CIP-1756

Title

Debug Module does not fully conform to the version of debug spec reported in its version register

Implication

The Debug Module reports that it conforms to Debug Spec 0.13. However, it halted state may not be maintained through system reset. If a core is halted and undergoes a reset, it does not necessarily stay halted. The RISC-V Debug Spec 0.13 states that a core should maintain its halted state through a system reset. SiFive cores emerge from reset to either halted or running state dependent on the resethaltreq setting rather than previous halted state.

Workaround

Use the setresethaltreq and clrresethaltreq bits in dmcontrol to configure whether the core should run or be halted following reset.

Impact

Medium

Probability

Low

Category

CAT-C

CIP-3005

Title

Some Floating Point instructions are not counted by Performance Monitors

Implication

Due to an error in the instruction decode used for Performance Monitor counting; fdiv, fsqrt, fadd, fsub, fmul, and fma instructions are never counted.

Workaround

None

Impact

Minor

Probability

High

Category

CAT-C

CIP-3025

Title

MMU fault prioritization - access over permission fault

Implication

When both final access and permission faults will be reported, the core will report in `mcause` the access fault ahead of the permission fault.

Workaround

Software could in the ISR analyze the PTE in memory & determine whether the correct fault was raised.

Impact

Minor

Probability

Low

Category

CAT-C

CIP-3046

Title

Load/Store Misaligned Fault prioritized between page faults during/after translation

Implication

When both final page and misaligned faults will be reported, the core will report in `mcause` the misaligned fault ahead of the page fault.

Workaround

Software could in the ISR analyze the PTE in memory & determine whether the correct fault was raised.

Impact

Minor

Probability

Low

Category

CAT-C

