In the provided code in our report appendix II, two separate digital systems, the air conditioning (AC) and garage door functions, are integrated into a single design. This integration introduces complexities related to logic standard compatibility, timing compatibility, power consumption, and resource utilization. Let's discuss these challenges and potential mitigation strategies using the provided code as a reference.

Logic standard compatibility: In the integrated design, the AC and garage door functions communicate through shared wires, such as 'doorOpen'. Ensuring that these signals have the same logic levels is crucial to maintain correct data transfer and prevent component damage.

Mitigation:
- Both AC_FSM_top and garage_FSM_top are part of the same FPGA design, so they should share the same logic standard. If different logic standards are required, voltage level translators or level shifters can be used, or an FPGA supporting multiple I/O standards can be chosen.

Timing compatibility:
The design uses a single 'clk' input, ensuring that both AC and garage door functions share the same clock signal. However, different clock domains within the modules or timing constraints for data synchronization may still introduce timing challenges.

Mitigation:
- Implementing a common clock for both functions maintain timing compatibility. However, different clock domains or timing constraints exist, we generate many different heart beats for different condition's usage.

Power consumption: Integrating multiple digital systems in a single FPGA design can lead to increased power consumption, which may impact the overall system performance and reliability.

Mitigation:
- Optimize the design by reducing unnecessary logic or employing clock gating techniques to minimize power usage when certain functions are not needed.
- In our design, we use the FSM to ensure each time there is only exactly one state for each module. Also, instead of continusly checking the transition of the state, we divide the state into many mini states in our garage door design to ensure no waste of resource.

In conclusion, integrating separate digital systems in a single FPGA design introduces various challenges related to logic standard compatibility, timing

compatibility, power consumption, and resource utilization. By employing appropriate design choices and optimization techniques, these challenges can be mitigated, resulting in a more efficient and robust integrated system.