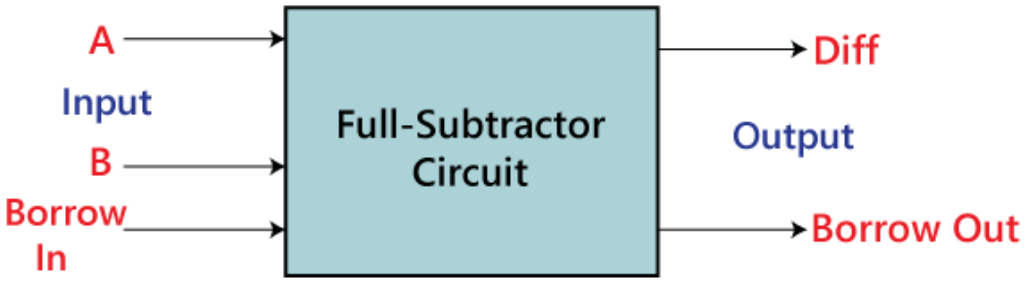
# FULL SUBTRACTOR

## EXPLANATION:

The Half Subtractor is used to subtract only two numbers. To overcome this problem, a full subtractor was designed. The full subtractor is used to subtract three 1-bit numbers A, B, and C, which are minuend, subtrahend, and borrow, respectively. The full subtractor has three input states and two output states i.e., diff and borrow.




**DIFF: (A XOR B) XOR Bin**

**BORROW OUT: A'Bin + A'B + BBin**

## RTL CODE:

## DATAFLOW METHOD:

```
module Full_subtractor(A,B,C,diff,brw);
  input A,B,C;
  output diff,brw;
  assign diff=A^B^C;
  assign brw=!A&B|(C&~(A^B));
endmodule
```

## BEHAVIOURAL METHOD:

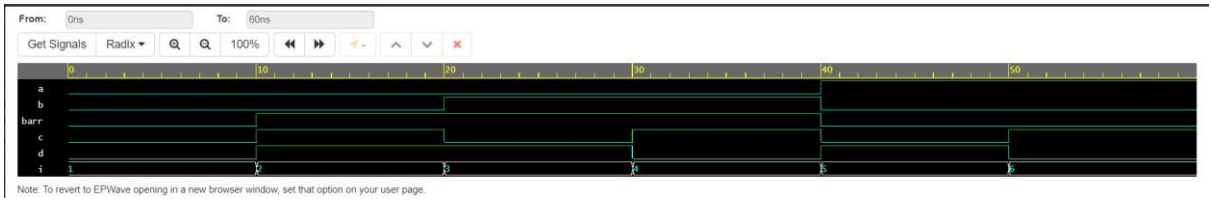
```
module
Full_subtractor(A
,B,C,diff,brw);
  input A,B,C;
  output diff,brw;
```

```
  always@(*);
  begin
   diff=A^B^C;
   brw=!A&B|(C&~(A^B));
  end
endmodule
```

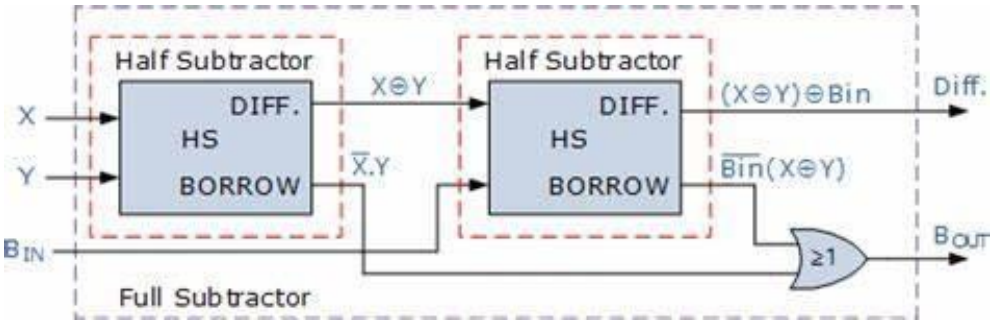
**TEST BENCH:**

```
module testbench;
  reg A,B,C;
  wire diff,brw;
  integer i;
  Full_subtractor a1(A,B,C,diff,brw);
  initial
    begin
      $dumpfile("dump.vcd");
      $dumpvars(1);
    end
  initial
    begin
      A=0;B=0;C=0;
    end
  initial
    begin
      for(i=1;i<8;i=i+1)
        begin
          #10{A,B,C}=i;
        end
    end
  initial
    begin
```

```
    #60$finish();
   end
endmodule
```




## FULLSUBRACTOR USING HALF SUBRACTOR




## RTL CODE:

```
module  full_subtractor(d,barr,a,b,c);

input a,b,c; output d,barr;

wire p, q, r; half_subtractor

u4(p,q,a,b);

half_subtractor u5(d,p,c);

or_gate u6(barr, p,q);

endmodule
```

## TEST BENCH:

```
module testbench;

  reg  a,b,c;      wire  d,barr;

integer    i;            full_sub
```

```
a1(d,barr,a,b,c);        initial
begin
     $dumpfile("dump.vcd");
$dumpvars(1);     end
initial     begin
a=0;b=0;c=0;     end   initial
begin       for(i=1;i<8;i=i+1)
begin
         #10 {a,b,c}=i;
end     end   initial
begin       #60
$finish();     end
endmodule
```