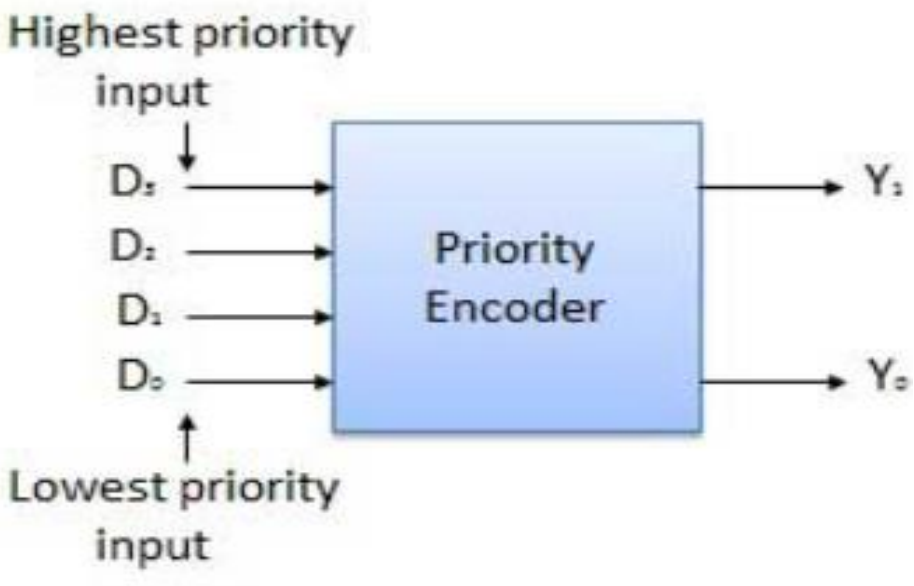
PRIORITY ENCODER:

4:2 ENCODER:

The priority encoder is a combinational logic circuit that contains 2^n input lines and n output lines and represents the highest priority input among all the input lines. When multiple input lines are active high at the same time, then the input that has the highest priority is considered first to generate the output.

It is used to solve the issues in binary encoders, which generate wrong output when more than one input line is active high. If more than one input line is active high(1) at the same time, then this encoder prioritizes every input level and allocates the priority level to each input.



RTL CODE:

```
module priority_encoder(input [3:0] D, output reg [1:0] Y);
```

```
always @(*)
begin
    case(D)
        4'b0001: Y = 2'b00;
        4'b001?: Y = 2'b01;
        4'b01??: Y = 2'b10;
        4'b1???: Y = 2'b11;
    endcase
end
endmodule
```

TESTBENCH:

```
module testbench;
  reg [3:0]D;
  wire [1:0]Y;
  priority_encoder a1 (D,Y);

  initial
    begin
      $dumpfile(".vcd");
      $dumpvars(1);
    end
  initial
    begin
```

```
      D=4'b0001;
      #10 D=4'b001?;
      #10 D=4'b01??;
      #10 D=4'b1???;
    end
  initial
    begin
      #60 $finish();
    end
endmodule
```