Day 23

D FLIPFLOP:

D flip flop is an electronic devices that is known as “delay flip flop” or “data flip flop” which is used to store single bit of data.D flip flops are synchronous or asynchronous. The clock single required for the synchronous version of D flip flops but not for the asynchronous one.The D flip flop has two inputs, data and clock input which controls the flip flop. when clock input is high, the data is transferred to the output of the flip flop and when the clock input is low, the output of the flip flop is held in its previous state.

Working of D Flip Flop

D flip flop consist of a single input D and two outputs (Q and Q’). The basic working of D Flip Flop is as follows:

When the clock signal is low, the flip flop holds its current state and ignores the D input.

When the clock signal is high, the flip flop samples and stores D input.

The value that was previously fed into the D input is reflected at the flip flop's Q output.

If **D = 0** then **Q will be 0.**

If **D = 1** then **Q will be 1**.

RTL CODE:

```
module D_flipflop(input D,clk, output reg q,qb);
  always@(posedge clk)
    begin
      q <= D;
    end
endmodule
```

TEST BENCH:

```
module testbench;
  reg D,clk;
  wire q,qb;
  D_flipflop d1 (D,clk,q);
  initial
    begin
      $dumpfile(".vcd");
```

```
    $dumpvars(1);
  end
 always
  begin
    clk = 0;
    #5 clk=1;
    #5 clk=0;
  end
 initial
  begin
    D=1'b0;
    D=1'b1;
  end
 initial
  begin
    #60 $finish();
  end
endmodule
```