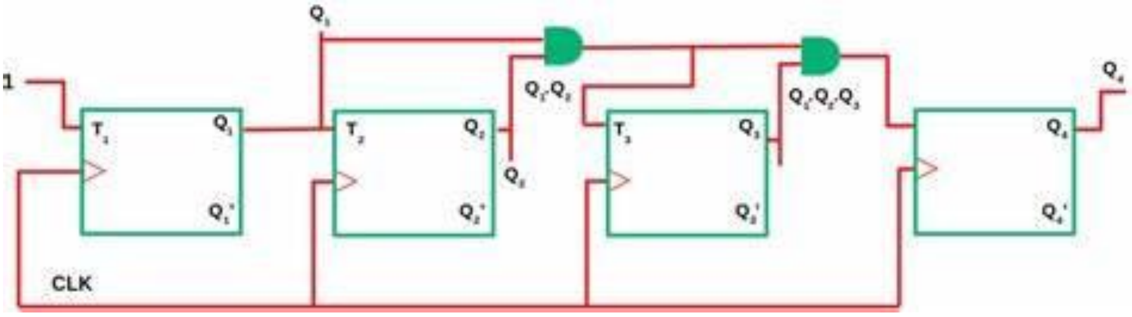
4 -BIT SYNCHRONOUS UP COUNTER

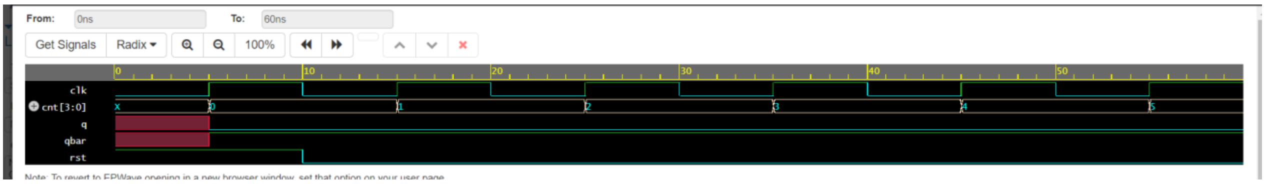


RTL CODE:

```
module test(input clk,rst,t,output reg q,output reg qbar);
  always@(posedge clk)begin
    if(rst)
      q<=0;
    else begin
      q<=t?~q:q;
    end
    assign qbar=~q;
  end
endmodule
module syn(input clk,rst,output q,qbar,output [3:0]cnt);
  wire [3:0]t;
  wire q0,q0bar,q1,q1bar,q2,q2bar;
  test a1(clk,rst,t[0],q0,q0bar);
  test a2(clk,rst,t[1],q1,q1bar);
  test a3(clk,rst,t[2],q2,q2bar);
  test a4(clk,rst,t[3],q,qbar);
  assign t[0]=1;
  assign t[1]=q0;
  assign t[2]=q1&q0;
  assign t[3]=q1&q2&q0;
  assign cnt={q,q2,q1,q0};
endmodule
```

TESTBENCH:

```
module tls;
  reg clk,rst;
  wire q,qbar;
  wire [3:0]cnt;
  syn h1(clk,rst,q,qbar,cnt);
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end
  initial begin
    forever #5 clk=~clk;
  end
  initial begin
    rst=1;clk=0;
    #10 rst=0;
  end
  initial begin
    #60 $finish();
  end
endmodule
```



From: 0ns To: 60ns

Note: To revert to EPWave opening in a new browser window, set that option on your user page.