ERROR DETECTOR

ODD/ EVEN PARITY

What is Parity Bit?

The parity generating technique is one of the most widely used error detection techniques for the data transmission. In digital systems, when binary data is transmitted and processed, data may be subjected to noise so that such noise can alter 0s (of data bits) to 1s and 1s to 0s.

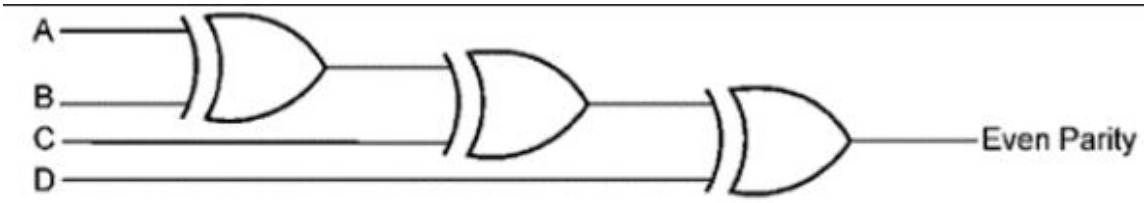
Hence, a Parity Bit is added to the word containing data in order to make number of 1s either even or odd. The message containing the data bits along with parity bit is transmitted from transmitter to the receiver.

At the receiving end, the number of 1s in the message is counted and if it doesn't match with the transmitted one, it means there is an error in the data. Thus, the Parity Bit it is used to detect errors, during the transmission of binary data.

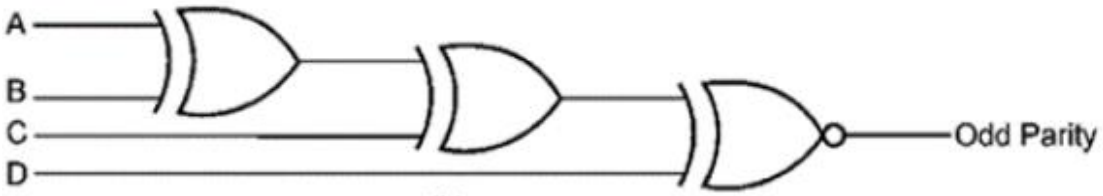
Even Parity and Odd Parity

The sum of the data bits and parity bits can be even or odd. In even parity, the added parity bit will make the total number of 1s an even number, whereas in odd parity, the added parity bit will make the total number of 1s an odd number.

The basic principle involved in the implementation of parity circuits is that sum of odd number of 1s is always 1 and sum of even number of 1s is always 0. Such error detecting and correction can be implemented by using Ex-OR gates (since Ex-OR gate produce zero output when there are even number of inputs).



(a)



(b)

RTL CODE:

```
module parity_checker(input A,B,C, output Podd,Peven);
  assign Peven = (A^B^C);
  assign Podd = ~(A^B^C);
endmodule
```

TEST BENCH:

```
module testbench;
  reg A,B,C;
  wire Podd,Peven;
  parity_checker p1 (A,B,C, Podd,Peven);
  initial
    begin
      $dumpfile(".vcd");
```

```
    $dumpvars(1);
  end
 initial
  begin
    A=0;B=0;C=0;
    #10 A=0;B=0;C=1;
    #10 A=0;B=1;C=0;
    #10 A=0;B=1;C=1;
    #10 A=1;B=0;C=0;
    #10 A=1;B=0;C=1;
    #10 A=1;B=1;C=0;
    #10 A=1;B=1;C=1;
  end
 initial
  begin
    #50 $finish();
  end
endmodule
```