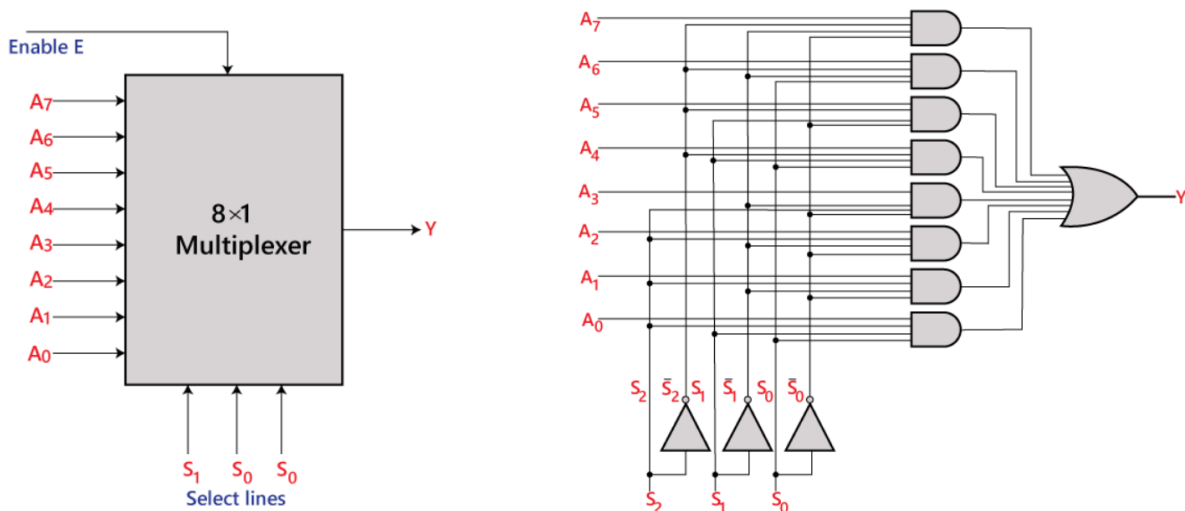


## 8:1 MUX

A multiplexer is a combinational circuit that has  $2^n$  input lines and a single output line. Simply, the multiplexer is a multi-input and single-output combinational circuit. The binary information is received from the input lines and directed to the output line. On the basis of the values of the selection lines, one of these data inputs will be connected to the output.

Unlike encoder and decoder, there are  $n$  selection lines and  $2^n$  input lines. So, there is a total of  $2^N$  possible combinations of inputs. A multiplexer is also treated as **Mux**.



In the 8 to 1 multiplexer, there are total eight inputs, i.e., A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>, A<sub>3</sub>, A<sub>4</sub>, A<sub>5</sub>, A<sub>6</sub>, and A<sub>7</sub>, 3 selection lines, i.e., S<sub>0</sub>, S<sub>1</sub> and S<sub>2</sub> and single output, i.e., Y. On the basis of the combination of inputs that are present at the selection lines S<sub>0</sub>, S<sub>1</sub>, and S<sub>2</sub>, one of these 8 inputs are connected to the output. T

## RTL CODE:

```
module MUX(input [7:0] I, input [2:0] s, output reg Y);
    always @(*)
    begin
        case(s)
            3'b000: Y = I[0];
            3'b001: Y = I[1];
            3'b010: Y = I[2];
            3'b011: Y = I[3];
            3'b100: Y = I[4];
            3'b101: Y = I[5];
            3'b110: Y = I[6];
            3'b111: Y = I[7];
        endcase
    end
endmodule
```

## TEST BENCH:

```
module testbench;
    wire Y;
    reg [7:0]I;
    reg [2:0]s;
    MUX a1(I,s,Y);
    initial
        begin
```

```

    $dumpfile(".vcd");
    $dumpvars(1);
end
initial
begin
    s[2]=0;s[1]=0;s[0]=0;I[0]=1;I[1]=0;I[2]=0;I[3]=0;I[4]=0;I[5]=0;I[6]=0;
    #20 s[2]=0;s[1]=0;s[0]=1;I[0]=0;I[1]=1;I[2]=0;I[3]=0;I[4]=0;I[5]=0;I[6]=0;
    #20 s[2]=0;s[1]=0;s[0]=0;I[0]=1;I[1]=0;I[2]=0;I[3]=0;I[4]=0;I[5]=0;I[6]=0;
end
initial
begin
    #20 $finish();
end
endmodule

```

