

BASIC GATES

EXPLANATION:

- **AND GATE** : whose output goes HIGH to a logic level 1 only when all of its inputs are HIGH
- **OR GATE** : whose output goes HIGH to a logic level 1 only when one or more of its inputs are HIGH
- **NOT GATE** : It is the most basic of all the logical gates and is often referred to as an Inverting Buffer or simply an Inverter
- **NAND GATE**: The output of the NAND gate is always at logic 1 and only goes to logic 0 when all the inputs to the NAND gate are at logic 1
- **NOR GATE** : Any one of the input is low ,output is high
- **XOR GATE**: odd number of inputs is high output is high
- **XNOR GATE**: Even number of inputs is high output is high

RTL CODE:

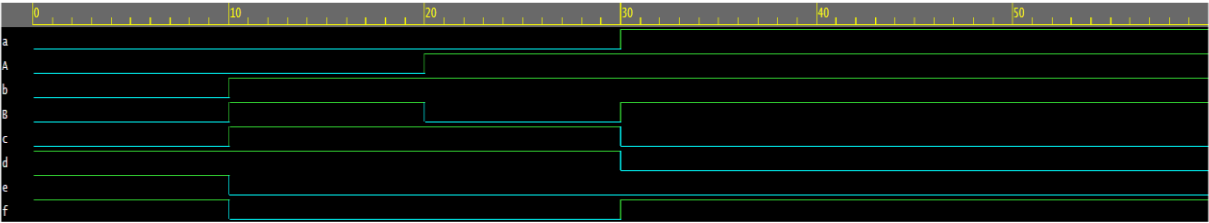
```
module gates(a,b,c,d,e,f,A,B);  
    output a,b,c,d,e,f;  
    input A,B;  
    assign a=A&B;  
    assign b=A|B;  
    assign c=A^B;  
    assign d=~(A&B);  
    assign e=~(A|B);  
    assign f=~(A^B);  
endmodule
```

TEST BENCH:

```
module test_best;
    reg A,B;
    wire a,b,c,d,e,f;
    gates a1(a,b,c,d,e,f,A,B);
    initial
        begin
            $dumpfile("dump.vcd");
            $dumpvars(1);
        end
    initial
        begin
            A=0;B=0;
        end
    initial
        begin
            #10 A=0;B=1;
            #10 A=1;B=0;
            #10 A=1;B=1;
        end
    initial
        begin
            #60 $finish();
        end
endmodule
```

From: 0nsTo: 60ns

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