***1 point***

Pick out the Analog device

 Speakers



 Pager



 Personal Computer



 PDA



***1 point***

Pick out the Digital device

 Speakers



 Microphones



 light pen



 PDA



***1 point***

Boolean algebra is defined as a set of

 Three values



 Two values



 Four values



 Five values



***1 point***

Arithmetic and Logic Unit is an example of

 Sequential Circuit



 Combinational Circuit



***1 point***

Binary Number System represented as

 Base 2. Digits used: 0, 1



 Base 8. Digits used: 0 to 7



 Base 2. Digits used: 0, 16



 Base 16. Digits used: 0 to 9, Letters used: A-F



***1 point***

Octal Number System represented as

 Base 2. Digits used: 0, 1



 Base 8. Digits used: 0 to 7



 Base 16. Digits used: 0, 16



 Base 16. Digits used: 0 to 9, Letters used: A- F



***1 point***

Hexa Decimal Number System represented as

 Base 2. Digits used: 0, 1



 Base 8. Digits used: 0 to 7



 Base 16. Digits used: 0, 16



 Base 16. Digits used: 0 to 9, Letters used: A- F



***1 point***

The digit at the extreme left has the highest positional value and is generally called

 Least Significant Digit



 Most Significant Digit



 Most Value Digit



 Least Value Digit



***1 point***

Convert (A4F)16 to decimal equivalent

 (2239)10



 (2187)10



 (2635)10



 (2132)10



***1 point***

Convert (1502)8 to hexa-decimal equivalent

 (342)16



 (322)16



 (37B)16



 (B3B)16



***1 point***

Representation of -41 in 8-bit sign magnitude

 00101001



 10101001



 11010110



 11011001



***1 point***

Representation of -41 in 8-bit 1's Complement

 00101001



 10101001



 11010110



 11011001



***1 point***

Representation of -41 in 8-bit 2's Complement

 00101001



 10101001



 11010110



 11011001



***1 point***

The widely used signed binary representations in computer systems are:

 Sign magnitude



 1's Complement



 2's Complement



***1 point***

Equivalent Gray code for the Binary (11011101)2

 00101001



 10101001



 10110011



 11011001



***1 point***

The output of an AND gate with three inputs, A, B, and C, is HIGH when \_\_\_\_\_\_\_\_.

 A is equal to 1, B is equal to 1, C is equal to 0



 A is equal to 0, B is equal to 0, C is equal to 0



 A is equal to 1, B is equal to 1, C is equal to 1



 A is equal to 1, B is equal to 0, C is equal to 1



***1 point***

The output of an AND gate with three inputs, A, B, and C, is HIGH when \_\_\_\_\_\_\_\_.

 A is equal to 1, B is equal to 1, C is equal to 0



 A is equal to 0, B is equal to 0, C is equal to 0



 A is equal to 1, B is equal to 1, C is equal to 1



 A is equal to 1, B is equal to 0, C is equal to 1



How many gates would be required to implement the Boolean expression AB + A(A + C) + B(A + C)  after simplification?

 1



 2



 4



 5



***1 point***

The output of an OR gate with three inputs, A, B, and C, is LOW when \_\_\_\_\_\_\_\_.

 A = 0, B = 0, C = 0



 A = 0, B = 0, C = 1



 A = 0, B = 1, C = 1



 all of the above



***1 point***

To implement the logic expressions AB+BC+A'BC+A'B'C' how many gates are needed? (assume all available gates are 3 input Gates)

 4 AND Gates,2 OR gates and 3 NOT Gate



 2 AND Gates,4 OR gates and 3 NOT Gate



 3 AND Gates,2 OR gates and 4 NOT Gate



 4 AND Gates,3 OR gates and 3 NOT Gate



***1 point***

How many gates would be required to implement the Boolean expression AB + A(A + C) + B(A + C)  before simplification? (assume all available gates are 2 input Gates)

 1



 2



 4



 5



***1 point***

XZ + XYZ = XZ

 True



 False



***1 point***

If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output?

 1



 2



 7



 8



***1 point***

How many inputs of a four-input AND gate must be HIGH in order for the output of the logic gate to go HIGH?

 any one of the inputs



 any two of the inputs



 any three of the inputs



 all four inputs



***1 point***

Logically, the output of a NOR gate would have the same Boolean expression as a(n):

 NAND gate immediately followed by an inverter



 OR gate immediately followed by an inverter



 AND gate immediately followed by an inverter



 NOR gate immediately followed by an inverter



***1 point***

If a 3-input OR gate has eight input possibilities, how many of those possibilities will result in a HIGH output?

 1



 2



 7



 8



***1 point***

To implement the logic expressions AB+BC+A'BC how many gates are needed? (assume all available gates are 2 input Gates)

 3 AND Gates,2 OR gates and 1 NOT Gate



 2 AND Gates,3 OR gates and 1 NOT Gate



 2 AND Gates,4 OR gates and 1 NOT Gate



 4 AND Gates,2 OR gates and 1 NOT Gate



***1 point***

Applying DeMorgan's theorem to the expression (A+B+C+D+E)' , we get \_\_\_\_\_\_\_\_.

 A'B'C'D'E'



 A'+B'+C'+D'+E'



 A+B'+C'+D+E'



 A'+B+C+D'+E'



***1 point***

Reduce the expression A(B+C'(AB+AC')')

 AB



 AB+C



 AC



 A



***1 point***

Simplify the expression ((AB)'+A'+AB)'

 0



 1



 A



 A'



***1 point***

Simplify the expression Y=AB +AB'(A'C')'

 A'



 A



 0



 1



***1 point***

If all the inputs of a NAND gate are connected together then the resulting circuit is:

  OR gate



 AND gate



 NOT gate



Express the boolean function F= A+B'C in SSOP form

 ABC + ABC'+ AB'C + AB'C'+ A'B'C



 ABC + A'BC'+ AB'C + AB'C'+ A'B'C



 A'BC + A'BC'+ AB'C + AB'C'+ A'B'C



 ABC + A'BC'+ AB'C + AB'C'+ A'B'C'



***1 point***

Minterm designation for AB'C' is:

 m3



 m4



 m5



 m6



***1 point***

Express the boolean function F= A+B'C in sum of minterms

 m1+m3+m5+m6+m7



 m1+m4+m5+m6+m7



 m1+m2+m4+m6+m7



 m0+m4+m5+m6+m7



***1 point***

Express the boolean function F= (X'+Y)(X+Z)(Y+Z) in SPOS form

 (X+Y+Z)(X+Y'+Z)(X'+Y+Z)(X'+Y+Z')



 (X'+Y'+Z)(X+Y'+Z)(X'+Y+Z)(X'+Y+Z')



 (X'+Y'+Z')(X+Y'+Z)(X'+Y+Z)(X'+Y+Z')



 (X+Y+Z)(X+Y'+Z)(X'+Y+Z)(X'+Y'+Z')



***1 point***

Maxterm designation for A+B+C is:

 M1



 M0



 M7



 M2



***1 point***

Express the boolean function F= (A+B+C')(A+B'+C)(A'+B+C)(A'+B'+C') as product of maxterms

 M1.M2.M4.M7



 M6.M5.M3.M0



 M7.M5.M3.M0



 M1.M3.M5.M7



***1 point***

Convert the SOP expression F=A'B'C'+ A'BC'+ A'BC + AB'C+ ABC to equivalent POS expression

 (A+B+C)(A'+B'+C')(A'+B'+C)



 (A+B+C)(A'+B+C')(A'+B'+C)



 (A+B+C')(A'+B+C)(A'+B'+C)



 (A'+B+C)(A'+B'+C')(A'+B'+C)



***1 point***

For 3 variable Boolean expression, the number of cells in K-map is:

 4



 16



 32



 8



***1 point***

For 5 variable Boolean expression, the number of cells in K-map is:

 4



 16



 32



 8



***1 point***

The encoding technique used for placing the Max/Min terms in K-map is:

 Excess 3 code



 BCD Code



 Gray Code



 8421 code



***1 point***

Use K-Map to minimize the expression F= AB'C +A'BC + A'B'C +A'B'C' + AB'C'

 B'+A'C



 B+A'C



 B+AC



 B'+A'C'



***1 point***

Use K-Map to minimize the expression F= m1+m3+m5+m7+m9+m12+m13

 A'C+ABC'+C'D



 A'C+ABC'+C'D'



 AC+ABC'+C'D



 A'D+ABC'+C'D



***1 point***

Q\_14::Use K-Map to minimize the expression F= ∏M(0,1,3,5,6,7,10,14,15)

 (A'+C'+D)(B'+C')(A+D')(A'+B'+C)



 (A'+C'+D)(B'+C')(A+D')(A'+B+C)



 (A'+C'+D')(B'+C')(A+D')(A+B+C)



 (A'+C'+D)(B'+C')(A+D')(A+B+C)



***1 point***

Use K-Map to minimize the expression F= ∏M(0,1,4,5,6,8,9,12,13,14)

 C+(B'+D)



 C+(B'+D')



 C'+(B'+D)



 C'+(B'+D')



***1 point***

Use K-Map to minimize the expression F= ∏M(0,1,3,5,6,7,10,14,15)

 (A'+C'+D)(B'+C')(A+D')(A'+B'+C)



 (A'+C'+D)(B'+C')(A+D')(A'+B+C)



 (A'+C'+D')(B'+C')(A+D')(A+B+C)



 (A'+C'+D)(B'+C')(A+D')(A+B+C)



Use the tabulation method to minimize the following standard SOP expression F(A,B,C,D,E)=Σm(0,1,4,8,12,13,15,16,17,23,29,31)

 A'D'E'+BCD+BCE+A'CDE



 A'D'E'+B'C'D'+BCE+ACDE



 A'D'E'+BCD+B'C'E'+A'CDE



 A'D'E'+B'C'D'+B'C'E'+A'CDE



***1 point***

Use the tabulation method to minimize the following standard SOP expression F(A,B,C,D,E)=Σm(2,5,6,7,8,9,10,12,13,14,18,21,22,23,25,26,30)

 DE'+B'CE+A'BD'+BC'D'E



 D'E'+B'CE+A'B'D'+BC'D'E



 DE'+B'CE+A'BD'+BCD'E



 D'E'+B'CE+A'BD'+BC'D'E



***1 point***

Use tabulation method to minimize the expression F= Σm(5,7,8,10,13,15) +d(0,1,2,3)

 BD+B'D'



 AC+A'C'



 BD+A'C'



 AC+B'D'



***1 point***

Use tabulation method to minimize the expression F= Σm(1,3,5,7,9,12,13)

 A'C+ABC'+C'D



 A'C+ABC'+C'D'



 AC+ABC'+C'D



 A'D+ABC'+C'D



***1 point***

Use tabulation method to minimize the expression F= Σm(0,2,3,4,6,8,10,11,12,14)

 D'+B'C'



 D'+B'C



 B'D'+B'C'



 BD+B'C'



A flip flop is a \_\_\_\_\_ element which stores a binary digit as low or high voltage.

 Memory



 Switching



 Active



 Clock



***1 point***

A flip flop is a device with \_\_\_\_\_stable states

 Single



 Two



 Three



 Multiple



***1 point***

In flip flop, when the circuit is level clocked, the output can change while the clock is\_\_\_\_\_.

 Only High



 Only Low



 high or Low



 Both the state



***1 point***

Binary state of the flip flop after applying single pulse is referred as \_\_\_\_\_\_\_.

 Output State



 Input State



 Next State



 Current State



***1 point***

Binary state of the flip flop before applying single clock pulse is referred \_\_\_\_\_\_\_.

 Output State



 Present State



 Next State



***1 point***

If an NOR based SR latch has a 1 on the S input and 0 on the R input and then S input goes to 0 then the latch will be

 Set



 Reset



 invalid Clear



***1 point***

If an NOR based SR latch has a 0 on the S input and 1 on the R input and then S input goes to 0 then the latch will be

 Set



 Reset



 invalid Clear



***1 point***

In a NAND based S-R latch, if S=1 & R=1 then the state of the latch is \_\_\_\_\_\_\_\_\_\_\_\_

 Set



 Reset



 invalid



 memory



***1 point***

The logic circuits outputs at any instant of time depends only on the present input but also on the past outputs are called

 Sequential circuits



 Combinational Circuits



***1 point***

The invalid state of an NOR based S-R latch occurs when

 S is 0,R is 0



 S is 1,R is 0



 S is 0,R is 1



 S is 1,R is 1



***1 point***

The purpose of clock input to a flip-flop is to

 clear



 Set



 always cause the output to change states



 cause the output to assume a state dependent on the controlling inputs



***1 point***

By cross-coupling \_\_\_\_\_\_\_\_\_\_logic gates, a basic SR Flip Flop Can be constructed?

 AND or OR



 NAND or AND



 NOR or OR



 NAND or NOR



The disadvantage of SR Flip Flop is

 no enable input



 no clock signal



 Invalid State



 has Race Condition



***1 point***

In SR FLip-Flop 'S' stands for

 static



 System



 Set



 stable



***1 point***

Two cross Coupled NAND gates makes

 SR flip-Flop



 SR Latch



 D FLip FLop



Which circuit operation is faster?

 Combinational circuits



 Sequential circuits



 Latches



 Flip-flops



**1 point**

In JK flip flop, when J is high and K is High, the flip flop is \_\_\_\_\_ state.

 Abort



 Toggle



 Set



 Reset



**1 point**

In JK flip flop, when J is low and K is low, the flip flop is \_\_\_\_\_ state.

 No Change



 Toggle



 Set



 Reset



**1 point**

T flip flop is a \_\_\_\_\_input version of the \_\_\_\_\_ flip flop.

 Multiple and RS



 Single and JK



 Single and RS



 Multiple and JK



**1 point**

A feature that distinguish JK flip-flop from SR Flip-Flop is

 No Change



 Toggle



 Set



 Reset



**1 point**

In JK flip flop when J & K are 1, the output oscillate between 0 qnd 1 and the situation is referred as?

 Inversion condition



 Race around condition



 Lock out state



 Reset state



**1 point**

Which of the following flip-flops is free from the race around problem?

 D flip-flop



 SR flip-flop



 Master-Slave Flip-flop



 T flip-flop



**1 point**

S-R type flip-flop can be converted into D type flip-flop if S is connected to R through \_\_\_\_\_\_\_\_\_\_\_\_

 OR Gate



 AND Gate



 NOT Gate



 NAND gate



**1 point**

T type flip-flop can be converted into D type flip-flop if D and Q is connected to T through \_\_\_\_\_\_\_\_\_\_\_\_

 OR Gate



 AND Gate



 EOR Gate



 NAND gate



**1 point**

JK type flip-flop can be converted into D type flip-flop if D is connected to K through \_\_\_\_\_\_\_\_\_\_\_\_

 OR Gate



 AND Gate



 NOT Gate



 NAND gate



Shift registers are classified into \_\_\_\_\_\_\_ categories based on binary information is entered or shifted.

 2



 3



 4



 5



**1 point**

In a parallel in/parallel out shift register, D0 = 1, D1 = 0, D2 = 0, and D3 = 1. After three clock pulses, the data outputs are \_\_\_\_\_\_\_\_

 1001



 0001



 1100



 1000



**1 point**

Consider a 4-bit bidirectional shift registers and intially the values os Q0=1,Q1=1,Q2=0,Q3=0. Assume 1 on serial data-input line. If the RIGHT/LEFT is HIGH for 3 clock pulses and LOW for next two clock pulses what are the content after five clock pulses?

 1101



 0001



 1111



 1001



**1 point**

The bit sequence 1001 is entered serially(right most bit first) into a 4 bit parallel out shift registers. What is the Q outputs after two clock pulses

 1100



 1001



 0100



 1001



**1 point**

Assume that a 4-bit serial in/serial out shift register is initially clear and wish to store the nibble 1110 (right most bit first). What is the Q outputs after two clock pulses?

 1100



 0011



 0000



 1111



**1 point**

How many clock pulses will be required to completely load serially a 5-bit shift register?

 2



 3



 4



 5



**1 point**

Ripple counters are also called \_\_\_\_\_\_\_\_\_\_\_\_

 SSI counters



 Asynchronous counters



 Synchronous counters



 VLSI counters



**1 point**

A modulus-14 counter must have \_\_\_\_\_\_\_\_

 2 flip-flops



 4 Flip-flops



 6 flip-flops



 14 Flip-Flops



**1 point**

A decimal counter has \_\_\_\_\_\_ states.

 5



 10



 15



 20



**1 point**

A modulus-6 counter must have \_\_\_\_\_\_\_\_

 2 flip-flops



 4 Flip-flops



 6 flip-flops



 3 Flip-Flops



The carry propagation of half adder can be expressed as \_\_\_\_\_\_\_\_.

 A.B



 A + B



 A XOR B



 A + B'



**1 point**

The difference between half-adders and full-adders?

 Full-adders are made up of two half-adders



 Full adders can handle 3 digit numbers



 Full adders have a carry input capability



 Half adders can handle only single-digit numbers



**1 point**

The ripple carry adder is

 The carry output of the lower order stage is connected to the carry input of the next higher order stage



 The carry input of the lower order stage is connected to the carry output of the next higher order stage



 The carry output of the higher order stage is connected to the carry input of the next lower order stage



 The carry input of the higher order stage is connected to the carry output of the lower order stage



**1 point**

BCD addition can be done through \_\_\_\_\_\_\_\_\_\_\_\_

 BCD adder



 Full adder



 Ripple carry adder



 Carry look ahead



**1 point**

3 bits full adder contains :

 8 possible inputs



 6 possible inputs



 4 possible inputs



 3 possible inputs



**1 point**

The simplified expression of full adder carry is \_\_\_\_\_\_\_\_\_\_\_\_

 AB+AC+BC



 AB+AC



 AB+BC



 A'B+BC



**1 point**

The Decimal digit in BCD can be represented as:

 1 input lines



 2 input lines



 3 input lines



 4 input lines



**1 point**

If the inputs to a full adder are A=1, B=1, CIN=1 what will be the logic states on the outputs S and COUT?

 0,0



 0,1



 1,0



 1,1



**1 point**

If the inputs to a full adder are A=0, B=0, CIN=1 what will be the logic states on the outputs S and COUT?

 0,0



 0,1



 1,0



 1,1



**1 point**

If the inputs to a full adder are A=1, B=0, CIN=1 what will be the logic states on the outputs S and COUT?

 0,0



 0,1



 1,0



 1,1



A digital decoder is a combinational circuit that selects binary information from (M-Inputs, N- Combinations)

 1:N

 N:1

 M:N

 N:M

**1 point**

A digital encoder is a combinational circuit that selects binary information from

 1:N

 N:1

 N:2^N

 2^N:N

**1 point**

A digital multiplexer is a combinational circuit that selects binary information from (M-Inputs, N- Combinations)

 1:N

 N:1

 M:N

 N:M

**1 point**

A digital demultiplexer is a combinational circuit that selects binary information from

 1:N

 N:1

 N:2^N

 2^N:N

**1 point**

To implement a 4: 16 decoder circuit how many 1:2 decoders are needed

 15

 13

 11

 9

**1 point**

To implement a 4: 16 decoder circuit how many 2:4 decoders are needed

 5

 3

 7

 9

**1 point**

To implement a 32: 1 multiplexers circuit how many 4:1 multiplexes are needed

 8

 10

 12

 6

**1 point**

To implement a 64: 1 multiplexers circuit how many 8:1 multiplexes are needed

 8

 9

 10

 11

**1 point**

To implement the boolean function f(A,B,C,D)=m0+m2+m6+m10+m11+m12+m13 + d(m3+m8+m14) using 8:1 multiplexer what will be the input to I0-I7?

 1,0,1,1,A,A,1,0

 0,0,1,1,A,A,1,0

 0,0,1,1,A,A,1,A

 0,0,1,1,A,A,1,1

**1 point**

To implement the boolean function f(A,B,C,D)=M0+M3+M5+M6+M8+M9+M10+M12+M14 using 8:1 multiplexer what will be the input to I0-I7?

 0,A',A',A,A',A,0,1

 0,A',A,A,A',A,0,1

 0,A',A,A,A',A,0,0

 0,A',A',A,A',A,

**1 point**

\_\_\_\_\_\_\_\_\_\_\_ is Combinational circuit that assign highest priority to the input whose subscript has largest numerical value.

 Priority encoder

 Encoder

 Decoder

 Multiplexers

**1 point**

To send data from Personal computer to printer/plotter/Inkjetprinter/Fax machine which MSI cicuit is the best choice?

 Decoder

 Encoder

 Multiplexer

 Demultiplexer

**1 point**

To implement Octal to Binary converter circuit which MSI cicuit is the best choice?

 Decoder

 Encoder

 Multiplexer

 Demultiplexer

**1 point**

To implement Parallel to serial converter which MSI is the best choice?

 Decoder

 Encoder

 Multiplexer

 Demultiplexer

**1 point**

To implement serial to parallel converter which MSI is the best choice?

 Decoder

 Encoder

 Multiplexer

 Demultiplexer

Microprocessor consists of?

 ALU

 Register array

 Control unit

 All of the above

***1 point***

8085 is capable to process \_\_\_\_\_\_\_\_\_ data.

 4-bit

 8-bit

 16-bit

 32-bit

***1 point***

Microprocessor used for data processing and computation are called \_\_\_\_\_\_\_\_\_\_\_.

 Reprogrammable systems

 Embedded Systems

 Microcontroller

***1 point***

8085 is a reprogrammable systems.

 True

 False

***1 point***

Microprocessors used in Washing machine is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

 Reprogrammable System

 Microcontroller

***1 point***

\_\_\_\_\_ number of buses are used in microprocessor based systems.

 2

 3

 4

 5

***1 point***

Registers are used to store \_\_\_\_\_\_\_\_\_\_\_\_ during executions of instructions

 data

 memory

 instructions

***1 point***

The function of Decode stage in a microprocessor based operation is

 Conversion of program to machine code

 Identifying the operation to be performed

 Conversion of HLL to Assembly code

***1 point***

The signal used to synchronize the slower peripherals with microprocessor

 RESET

 READY

 INTERRUPT

 Hold

***1 point***

System Software used to convert high level language to Object code

 Compiler

 Assembler

 Loader

 Linker

***1 point***

If a microprocessor has 16 address lines , what is the maximum memory location that can be addressable

 1KB

 32KB

 64KB

 128KB

***1 point***

System Software used to convert assembly code to machine code

 Compiler

 Assembler

 Loader

 Linker

***1 point***

If a microprocessor has 20 address lines , what is the maximum memory location that can be addressable

 1MB

 32MB

 64MB

 128MB

***1 point***

If a microprocessor has 30 address lines , what is the maximum memory location that can be addressable

 1GB

 32GB

 64GB

 128GB

***1 point***

The microprocessor \_\_\_\_\_\_\_\_\_\_\_ the instructions from the memory

 Fetch

 Decode

 Execute

 None of the above

An 16 bit Microprocessor has a word length of \_\_\_\_\_\_\_\_\_\_\_?

 1 byte

 2 byte

 3 byte

 4 byte

**1 point**

8085 Microprocessor has a word length of \_\_\_\_\_\_\_\_\_\_\_?

 1 byte

 2 byte

 3 byte

 4 byte

**1 point**

The maximum addressable location of 8085 microprocessor is

 8KB

 64KB

 128KB

 32KD

**1 point**

The maximum number I/O devices that can be interfaced with 8085 microprocessor is:

 32

 64

 128

 256

**1 point**

The 16 bit register pairs used in 8085 are:

 BC,DE,HL

 BE,CD,HL

 BC,DH,DL

 BH,DE,CL

**1 point**

\_\_\_\_\_\_\_\_\_\_\_ regiter pair act as memory pointer.

 DE

 HL

 CD

 BC

**1 point**

The register holds the address of the next instruction is

 PC

 SP

 IR

 Accumulator

**1 point**

\_\_\_\_\_\_\_\_\_\_\_\_\_\_ register used to store the return address of the main program when a subroutine is called.

 PC

 SP

 IR

 Accumulator

**1 point**

Temporary registers not available for user access in 8085

 B and C

 W and Z

 H and L

 D and E

**1 point**

The non maskable interrupt is \_\_\_\_\_\_\_\_\_

 INTR

 RST5.5

 RST6.5

 TRAP

**1 point**

The pin generates a signal to notify the processor that more than one request is present to access the data and address bus

 HOLD

 HLDA

 INTA

 READY

**1 point**

The operation of the data bus is \_\_\_\_\_\_\_\_\_\_\_\_\_ when IO/M=0,S1=1,S0=1

 Memory read

 I/O read

 Interrupt Acknowledge

 Opcode Fetch

**1 point**

The operation of the data bus is \_\_\_\_\_\_\_\_\_\_\_\_\_ when IO/M=1,S1=1,S0=1

 Memory read

 I/O read

 Interrupt acknowledge

 Opcode Fetch

**1 point**

The Pin that gets enabled at the time when the address is present at the multiplexed address and data bus is

 ALE

 WR

 RD

 IO/M

**1 point**

Array of memory locations organized as \_\_\_\_\_\_\_\_ in stack

 LIFO

 FIFO

 FILO

 LILO

A combinational circuit that selects binary information from (M-Inputs, N- Combinations)

 Decoder

 Encoder

 Multiplexer

 Demultiplexer

**1 point**

To implement a 5:32 decoder circuit how many 2:4 decoders are needed

 10 decoder with enable input

 10 decoder

 9 decoder with enable input

 9 decoder

**1 point**

To implement a 5:32 decoder circuit how many 1:2 decoders are needed

 31 decoder with enable input

 31 decoder

 30 decoder with enable input

 30 decoder

**1 point**

To implement a Full adder circuit how many 3:8 decoders are/is needed

 4

 3

 2

 1

**1 point**

The maximum Addressable location in 8085 is

 1024

 2048

 8192

 65536

**1 point**

ALE goes high at T1-state to indicate

 ADO-AD7 multiplexed bus contains address

 ADO-AD7 multiplexed bus contains data

 A8-A15 address bus contains address

**1 point**

The number of T-states required to execute Opcode Fetch Cycle

 2

 3

 4

 5

**1 point**

The number of T-states required to execute Memory Read/ Write Operations

 2

 3

 4

 5

**1 point**

The number of address lines required to interface memory devices with 8192 registers

 10

 12

 13

 14

**1 point**

The number of address lines required to interface memory devices with 1024 registers

 10

 12

 13

 14

Identify the Addressing mode of the instruction "CMA"

 Immediate

 Direct

 Indirect

 Implicit

**1 point**

Identify the Addressing mode of the instruction "MVI C,9FH"

 Immediate

 Direct

 Indirect

 Implicit

**1 point**

Identify the Addressing mode of the instruction "LDA 9000H"

 Immediate

 Direct

 Indirect

 Implicit

**1 point**

Identify the Addressing mode of the instruction "MOV A,M"

 Register

 Direct

 Indirect

 Implicit

**1 point**

Identify the Addressing mode of the instruction "MOV A,C"

 Register

 Direct

 Indirect

 Implicit

**1 point**

Assume A=35H B=55H and the carry is set. What will be the output after executing the instruction " ADC B"

 90H

 91H

 8AH

 8BH

**1 point**

Assume H=35H L=00H and the memory location [3500] contains 12 . What will be the output after executing the instruction " INR M"

 (H,L,Mem)(35,00,12)

 (H,L,Mem)(35,01,12)

 (H,L,Mem)(35,00,13)

 (H,L,Mem)(35,01,13)

**1 point**

Assume H=35H L=00H and the memory location [3500] contains 12 . What will be the output after executing the instruction " INX M"

 (H,L,Mem)(35,00,12)

 (H,L,Mem)(35,01,12)

 (H,L,Mem)(35,00,13)

 (H,L,Mem)(35,01,13)

**1 point**

Assume H=35H L=00H and B=35H C=01H and the memory location [3500] and [3501] contains 12H and 13H respectively. What will be the output in the location [3500] and [3501] after executing the instruction " DAD B"

 (6A01,3501)

 (7101,3501)

 (25,13)

 (12,15)

**1 point**

Assume H=35H L=00H and D=35H E=01H and the memory location [3500] and [3501] contains 12H and 13H respectively. What will be the output in the location [3500] and [3501] after executing the instruction " XCHG"

 (3500,3501)

 (3501,3500)

 (12,13)

 (13,12)

Assume A=55H and B=AAH. What will be the output after executing the instruction "ANA B"

 00H

 FFH

 55H

 AAH

**1 point**

Assume A=55H and B=AAH. What will be the output after executing the instruction "ORA B"

 55H

 AAH

 FFH

 00H

**1 point**

Assume A=55H. What will be the output after executing the instruction "XRA A"

 00H

 11H

 55H

 AAH

**1 point**

Assume A=55H and carry is set. What will be the output after executing the instruction "RLC"

 82H

 2AH

 ABH

 AAH

**1 point**

Assume A=55H and carry is set. What will be the output after executing the instruction "RRC"

 82H

 2AH

 ABH

 AAH

**1 point**

Assume A=55H and carry is set. What will be the output after executing the instruction "RAR"

 82H

 2AH

 ABH

 AAH

**1 point**

Assume A=55H and carry is set. What will be the output after executing the instruction "RAL"

 82H

 2AH

 ABH

 AAH

**1 point**

When "NOP" instruction is executed the following action(s) takes place

 PC is incremented and fetch the next instruction

 Accumulator will be cleared

 All the register values are cleared

**1 point**

\_\_\_\_\_ instruction is used to send data serially on SOD line in microprocessor.

 RIM

 SIM

 EI

 DI

**1 point**

\_\_\_\_\_ instruction is used to receive data serially on SID line of microprocessor.

 RIM

 SIM

 EI

 DI