

Logic Analyzer for Embedded Interfaces (PGY-LA-EMBD)

User Guide

Issue Date: 01st Sept 2022

Contents

1	Executive Summary	6
1.1	Purpose	6
1.2	Document Support.....	6
1.3	Technical Support	6
1.4	How to Order	6
1.5	Technical Support	6
2	PGY-LA-EMBD Overview	7
2.1	PGY-LA-EMBD Package Contents.....	9
2.2	Introduction to PGY-LA-EMBD	9
2.3	Front Panel of PGY-LA-EMBD Hardware Unit	11
2.4	Side Panel of PGY-LA-EMBD Hardware Unit	11
3	Installation	15
3.1	Installation of PGY-LA-EMBD Software	15
4	Navigating the Software	16
4.1	File Menu	18
4.1.1	New	18
4.1.2	Open.....	18
4.1.3	Reset HW.....	18
4.1.4	Save	18
4.1.5	Save As	18
4.1.6	Exit.....	19
4.2	Configuration	19
4.2.1	Connect to Host	19
4.2.2	Setup	19
4.2.3	Acquire	27
4.2.4	Stop	28
4.3	Trigger View	28
4.3.1	Auto Trigger	28
4.3.2	Pattern Trigger	28
4.3.3	Protocol Aware Trigger	29
4.3.4	Timing Parameter Trigger	30
4.4	View Menu	30

4.4.1	Protocol View (P-View)	30
4.4.2	Timing View (T-View)	32
4.4.3	Logic View (L-View)	32
4.5	Analytics	33
4.6	Report	34
4.7	About.....	35
5	PGY-LA-EMBD Modal Menu Navigation	36
5.1	Connect	36
5.2	Acquire	36
5.3	Stop	36
5.4	Decode Offline	37
5.5	Zoom In	37
5.6	Zoom Out	37
5.7	Pan	37
5.8	Fit	38
5.9	Undo.....	38
5.10	V-Cursors.....	38

Table of Figures

Figure 1	Logic analyzer for embedded interfaces- PGY-LA-EMBD	7
Figure 2.	PGY-LA-EMBD Unit.....	9
Figure 3.	Front panel of PGY-LA-EMBD Hardware Unit	11
Figure 4.	Side Panel.....	11
Figure 5:	Status LED Indications.....	12
Figure 6.	USB Connector	13
Figure 7.	USB Connection to Host PC.....	13
Figure 8.	Probe Cable.....	14
Figure 9.	Power Supply	14
Figure 10.	PGY-Logic Analyzer for Embedded Interface Software Icon	15
Figure 11.	PGY-LA-EMBD GUI.....	16
Figure 12.	File Menu	18
Figure 13.	Configuration Menu.....	19
Figure 14.	Setup	20
Figure 15.	LA Mode	21
Figure 16.	State/Synchronous – Clock Source 1	22
Figure 17.	State/Synchronous - clock Source -1 and 2	22
Figure 18.	State/Synchronous - Individual.....	23

Figure 19. Timing View - Glitch	32
Figure 20. Timing View – Zoom View of Glitch	32
Figure 21.T-View	32
Figure 22.L-View	32
Figure 23.Analytics.....	33
Figure 24.Report Menu.....	34
Figure 25. Report - Advanced	35

Limited warranty

Prodigy Technovations Pvt Ltd. provides the warranty for deliverables as follows:

- PGY-LA-EMBD Hardware unit is one year from the date of invoice.
 - PGY-LA-EMBD Software unit is one year from the date of Invoice.
- Probe cables are warranted for 3 months for any manufacturing defects from the date of invoice.
All other accessories are not covered in warranty. They are considered as consumable.

Legal Notice

TBD

Legal statements

TBD

Security statement

TBD

1 Executive Summary

1.1 Purpose

This document provides product description for the PGY-LA-EMBD. LA-EMBD stands for Logic Analyzer for Embedded Interface. PGY-LA-EMBD logic analyzer application can be used to debug timing problems and perform simultaneous protocol analysis of I2C, SPI, UART, I3C, RFFE and SPMI interfaces in embedded designs.

1.2 Document Support

In case, you are not able to follow the document and face difficulties; you may contact +91-80-42126100

1.3 Technical Support

For technical support, contact your local customer support team. See the support web site <http://www.prodigytechno.com/> for contact information.

1.4 How to Order

To order documents, contact your local sales representative or use the support web site <http://www.prodigytechno.com/>

1.5 Technical Support

For technical support, contact your local customer support team. See the support web site <http://www.prodigytechno.com/> for contact information.

2 PGY-LA-EMBD Overview

PGY-LA-EMBD is an industry first logic analyzer in its category which enables engineers to debug hardware problems using state and timing analysis while providing simultaneous protocol analysis of I2C, SPI, UART, I3C, RFFE and SPMI interfaces in embedded designs.

PGY-LA-EMBD offers 1GS/sec asynchronous (Timing) analysis and 100MHz synchronous (State) analysis which makes it an ideal debug tool to address the digital design problems. Designers can now easily analyze setup and hold time issues, glitches, and synchronous data activities apart from analyzing protocol issues. Embedded design teams need to take timely action to meet the intended objectives of the product. PGY-LA-EMBD simultaneously decodes I2C, SPI, UART, I3C, RFFE and SPMI bus and displays the protocol activity with time stamp information. PGY-LA-EMBD is an ideal instrument to debug the hardware and embedded software integration issues and optimize the software performance.

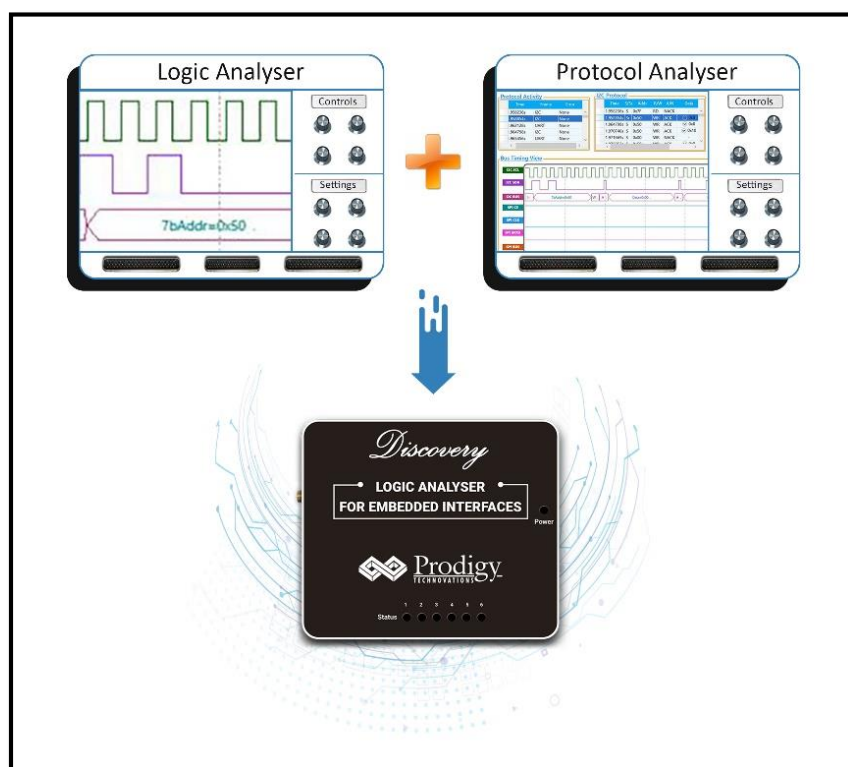


Figure 1 Logic analyzer for embedded interfaces- PGY-LA-EMBD

Key Features

- 1GS/Sec Timing (Asynchronous) Analysis.
- 100MHz State (Synchronous) Analysis.
- 16 channels Logic Analyzer.
- Simultaneous Protocol Analysis of I2C, SPI, UART, I3C, RFFE and SPMI.
- Detailed Trigger capabilities: Auto, Pattern, Protocol aware (I2C, SPI, UART, I3C, RFFE and SPMI) and timing (pulse width and delay).
- Smart streaming of data from Protocol. Analyzer to host computer for long duration capture using USB3.0 interface.
- Innovative easy to use Graphical user interface.
- Error Analysis of Protocol packet
- Provides timing, waveform, listing and Protocol listing views.
- Detailed filtering capability for protocol decoded data.
- PDF and CSV report format.

2.1 PGY-LA-EMBD Package Contents

Following items are shipped for PGY-LA-EMBD

1. PGY-LA-EMBD Hardware unit
2. PGY-LA-EMBD Software in CD
3. 16 Channel flying leads Probe.
4. USB 3.0 Cable
5. 5V Power supply

2.2 Introduction to PGY-LA-EMBD

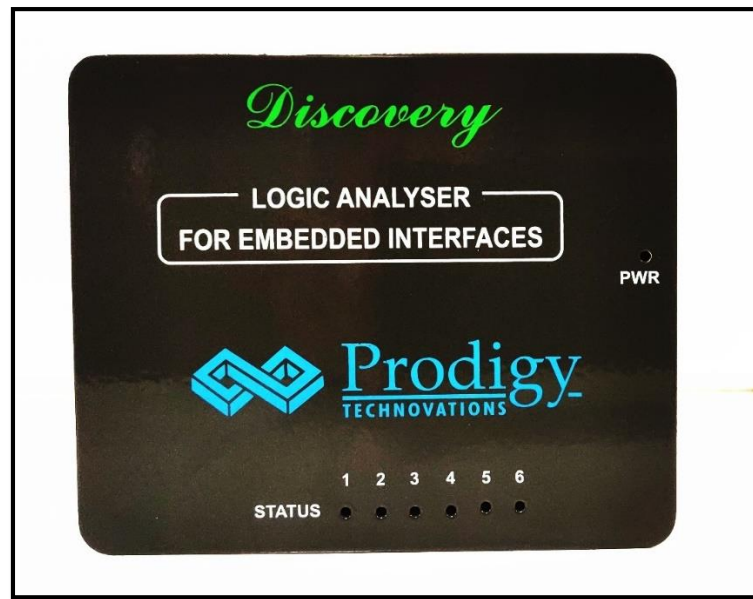


Figure 2. PGY-LA-EMBD Unit

The device allows to

- 1GS/Sec Timing (Asynchronous) Analysis
- 100MHz State (Synchronous) Analysis
- 16 channels Logic Analyzer.
- Simultaneous Protocol Analysis of I2C, SPI, UART, I3C, RFFE and SPMI.

Hardware Features

PGY-LA-EMBD Specifications	Features
Timing Speed	1 GS/ Sec Timing (Asynchronous) Analysis
State Speed	100 MS/S (Synchronous) Analysis
Channels	16 Channels Logic Analyzer
Protocol Decode Support	I2C, SPI, UART, I3C, RFFE and SPMI
Host Connectivity	USB 3.0

Voltage level support	1.2 V to 5.0 V, Flexibility to define logic threshold
Error	Insufficient Bit Error Display
Capture Duration	Smart Continuous streaming of data to host HDD/SSD of Host computer.
External Triggers	Trigger Out SMA Connector
Connector Type	Flying Lead probe cable, female. #16 clip-on banana connectors as optional accessories.

Software Features

Views	<ul style="list-style-type: none"> • Timing View • Logic View • Protocol Listing
Protocol Listing	<ul style="list-style-type: none"> • Packet Details with Error Detection and Frequency calculation • Markers
Waveform Plot	<ul style="list-style-type: none"> • Bus diagram, Annotation representation for Decoded Protocol • Pan, Zoom, Cursor & V-Cursors of waveform
Others	<ul style="list-style-type: none"> • Filter Capability • Report with Protocol Listing, Waveform Listing, etc.
Trigger View	<ul style="list-style-type: none"> • Auto • Pattern • Protocol Aware • Timing Trigger

2.3 Front Panel of PGY-LA-EMBD Hardware Unit

Front Panel provides below listed interfaces and indications:



Figure 3. Front panel of PGY-LA-EMBD Hardware Unit

- **ON/OFF:** To turn on/off the power to the PGY-LA Unit.
- **5 V DC Plug:** Connect the 5V Power Supply along with the device.
- **USB 3.0 Connector:** User can connect PGY-LA-EMBD main unit to host computer using USB3.0 interface.
Note: PGY-LA-EMBD does not draw power through USB interface.
- **TRG:** At this connector PGY-LA-EMBD will provide a pulse output, whenever a PGY-LA-EMBD unit triggers on any of the set trigger condition.
- **RESET:** To Reset the PGY-LA Analyzer Unit.

2.4 Side Panel of PGY-LA-EMBD Hardware Unit

Other side of the hardware Unit looks like following image.



Figure 4.Side Panel

- **LA2:** Allows the user to connect 16 Channel flying lead Probe.
- **Status LED:** Indicates operation status of the analyzer.

PGY-LA-EMBD Hardware unit has a set of comprehensive status LEDs.



Figure 5: Status LED Indications

- **PWR:** When PWR LED will glowing, it indicates the analyzer is power ON status.
- **LED1:** Indicates capture starts.
- **LED 2:** Indicates trigger found.
- **LED3:** 2GB DDR 3 memory full indication
- **LED4:** Indicates capture stop.
- **LED5:** Reserved
- **LED6:** Indicates FPGA Booting.

Step 1: USB Connection

Connect USB 3.0 Type C to the USB3 Connector in Discovery unit and USB 3 Type A to the Host Computer

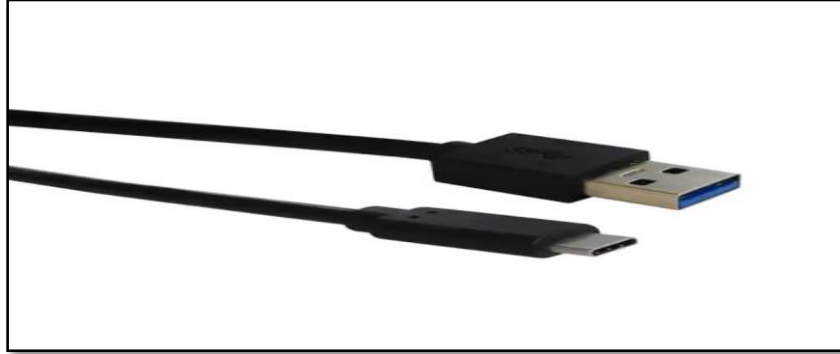


Figure 6.USB Connector

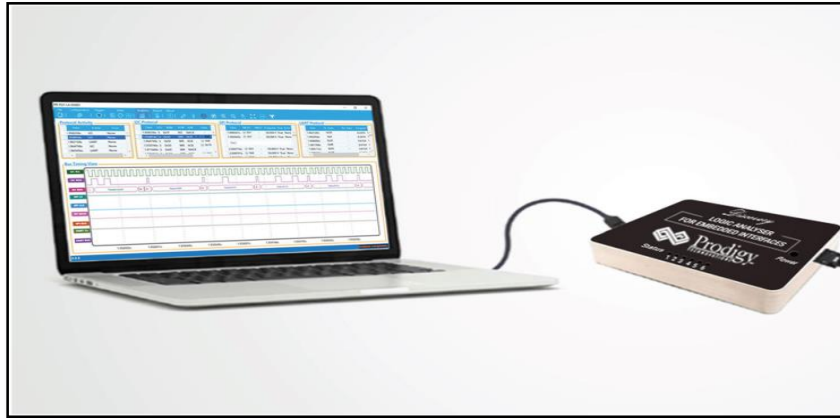


Figure 7.USB Connection to Host PC

Step 2: Probe Connection

Insert flying lead probe head to Analyzer port of the Discovery unit. The blue color flying leads are signals lines. These are labelled as D1 to D16. Black wire flying leads are ground leads.

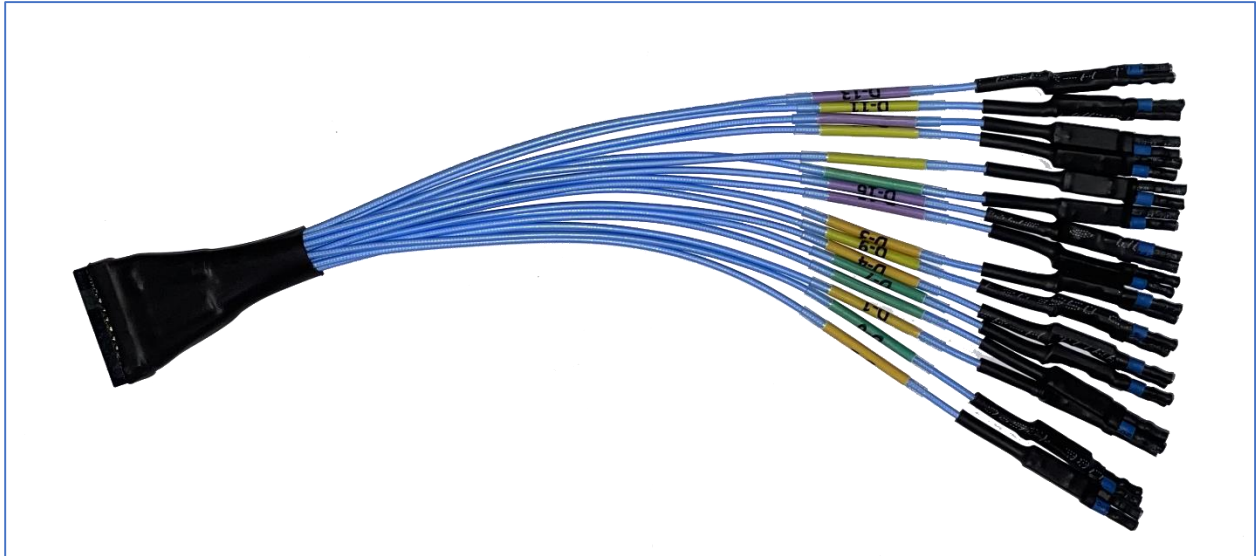


Figure 8. Probe Cable

Step 3: Power Supply

The Discovery unit is provided with 5V power adaptor, connect that to power socket, output pin to the Discovery unit and switch it ON.



Figure 9. Power Supply

Upon switching ON the device, PWR LED will be Turn ON and after few seconds LED 6 will glow. It confirms the boot activity is completed in Discovery unit.

3 Installation

3.1 Installation of PGY-LA-EMBD Software

Prerequisites

To install the PGY-LA-EMBD Software, following are the pre-requisites required for the computer system:

- Windows PC with Intel i3 processor or higher
- Supported Operating System, Windows7 or Windows 10
- Minimum system RAM, 16 GB (Minimum of 8 GB required)
- USB 3.0 port
- Hard Drive 50 GB
- .NET Framework 4.5

If .Net Framework is not available in the System, it can be download from below link.

<https://www.microsoft.com/en-in/download/details.aspx?id=30653>

Installation

- a) Double click **PGY-LA-EMBD.exe**. Follow the instructions on screen to install the software.
- b) Driver Installation: WinUSB driver is required to use PGY-LA-EMBD over USB3.0 interface. To install Prodigy WinUSB drivers select the WinP4.1.3 after successful installation of PGY-Logic Analyser for Embedded Interface software.
- c) On successful installation, FX3 needs to be displayed in Device Manager under USB Devices.
- d) On successful installation of PGY-LA-EMBD, an icon PGY-Logic Analyser for Embedded Interface will be created and appear on desktop.

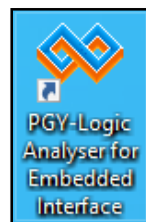


Figure 10. PGY-Logic Analyser for Embedded Interface Software Icon

4 Navigating the Software

The below PGY-LA-EMBD Main Menu Navigation

This section provides a detailed view of navigation across menus in PGY-Logic Analyzer for Embedded Interface Software. On launching the PGY-Logic Analyzer for Embedded Interface Software, the menu screen is as follows:

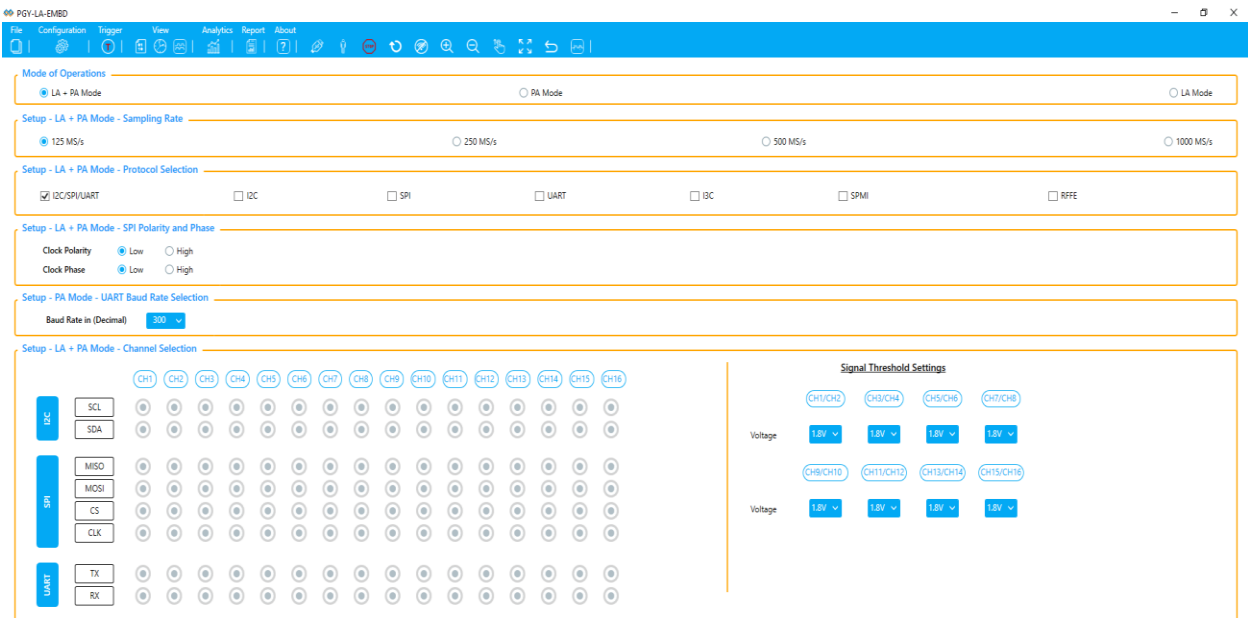


Figure 11.PGY-LA-EMBD GUI

The software has menu bar and different windows/tabs to configure the application and display the results.

Menu Bar

Menu bar has the following menu options:

Menu Item	Sub Menu	Description
File	New	New option will load previously saved setup settings.
	Open	Open option allows user to open an existing trace file and setup file.
	Reset HW	To reset the hardware Unit
	Save	Save the setup and trace file in default location.
	Save AS	Enables the user to choose the location where the setup and trace file can be saved
	Exit	Close the application
Configuration	Connect to Host	Allows to establish connection with hardware.

	Setup	Setup menu provides the option to configure the PGY-LA-EMBD to capture the different protocol data.
	Acquire	It starts captures the signal and decode packets based on protocol.
	Stop	Stop captures the signal.
Trigger	Auto	This is the default selection. No trigger pattern is used and all the packets from DUT are analyzed.
	Pattern	Pattern trigger looks at a serial data stream and triggers after a given serial pattern is matched.
	Protocol Aware	User can set trigger conditions in listed protocols and their parameters as per user requirements.
	Timing	Delay: Delay triggering is used to trigger when time differences between signal transitions either fail to meet minimum thresholds or exceed maximum thresholds. Pulse Width: This trigger enables user to trigger exclusively on pulses with a specified range of widths.
View	Protocol View	Protocol view window provides the decoded packet information for all the selected protocols in details with their error information.
	Timing View	Timing view is a unique capability of the PGY-LA-EMBD which enables users to get detailed insights to their signals timing information. 1GS/Sec Timing (Asynchronous) Analysis.
	Logic View	State view helps user to see the actual signal behavior. 100MHz State (Synchronous) Analysis.
Analytics	Analytic view	Gives information about Frame and error count.
Report	Standard	Allows to generate the report in PDF or CSV format
	Advanced	Allows to generate the customized PDF report.
	Append	It allows the user to merge the individually generated reports.
About	About	Gives the product information. Software Version number and Hardware Version Number details.
	View Help	Help option provides PGY LA-EMBD User Manual document.
Other Controls	Connect	Allows to Establish connection with hardware
	Acquire	Start captures the signal and decode packets based on protocol
	Stop Capture	Stop captures the signal.
	Decode Offline	Allows to view offline Trace File decoded result
	Zoom In	Enable user to "Zoom" the waveform.
	Zoom Out	Zoom out the waveform
	Pan	Enable user to move the waveforms left or right.
	Fit	Enable user to fit the selected message in the plot vies.
	V-Cursors	Enable the vertical cursors to measure the time difference.

This allows the user to access different functionalities of the application.

4.1 File Menu

Click File to view the selections in File menu:

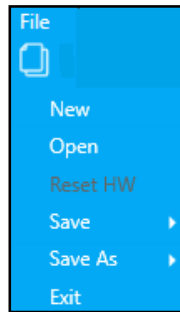


Figure 12.File Menu

4.1.1 New

This option will load previously saved setup settings.

4.1.2 Open

This opens the browse menu. Allows user to open an existing trace & setup files. The trace will result in two files, i.e., ProdigyCapture1 folder and ProdigyCapture1.xml. User can choose the XXXX.xml file using Open.

4.1.3 Reset HW

Use to reset the hardware unit.

4.1.4 Save

This saves the captured trace file & Setup. Any captured trace can be saved only after decoding the complete trace file or whatever is decoded when user clicks on 'Stop' button.

- Setup: Allows user to save current/ active setup in default location
- Trace File: If Save Trace file is selected, then the Trace file will be saved in Default path "C:\Prodigy_Technovations\ **PGY-MiniCooper Analyzer** \Trace file".

4.1.5 Save As

- Setup: Enables the user to choose the location where the setup can be saved.
- Trace File: Enables the user to choose the location where the Trace Files can be saved.
- By default the save location is C:\Prodigy_Technovations\ **PGY-MiniCooper Analyzer** \Trace file". If the user would like to change the path to a desired location other than the default path, the user would need to follow the steps as mentioned below.
- After launching the software, click on "File" and select "Save As" and select "Trace File Path" and create a folder and create an XXXX.xml file.
- Any captured trace can be saved only after decoding the complete trace file or whatever is decoded when user clicks on 'Stop' button. After stop capture, the user needs to click on "File" and click on "Save" button and after that go to saved location their user will get saved trace files.
- The trace will result in two files, i.e., Capture1 (folder name) and Capture1.xml (Name of .xml file).

4.1.6 Exit

This closes the application.

4.2 Configuration

Configuration menu options are as follows:

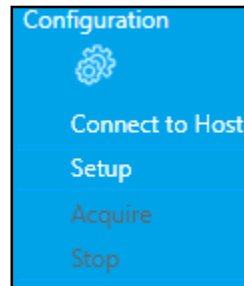


Figure 13.Configuration Menu

This has Connect to Host, Setup, Acquire and Stop selections.

4.2.1 Connect to Host

Connect to host provides the option of connecting the host computer to PGY-LA-EMBD hardware using the USB3.0 interface. Click on Connect to Host icon. If connection is established between the host computer and Discovery hardware unit, the Status pane displays Connection Successful.

4.2.2 Setup

The Setup menu provides the option to configure the PGY-LA-EMBD hardware to capture the different digital data signals. Users can easily configure the Logic Analyzer for embedded interfaces by either selecting Logic Analysis (LA) mode or Protocol Analysis (PA) mode or a combined (LA+PA) mode.

When user clicks on Setup icon from the configuration tab the following window will displays.

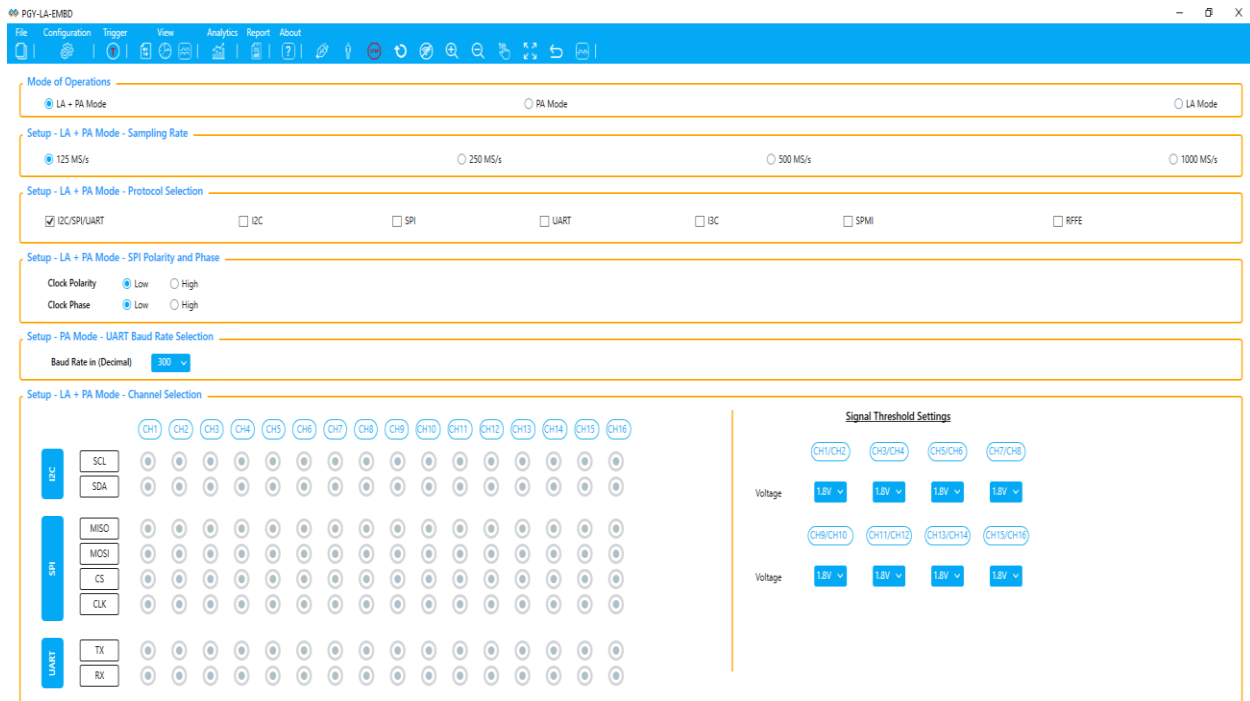


Figure 14.Setup

Mode of Operation

Mode of operations are divided into three categories:

- LA + PA Mode (Default)
- PA Mode
- LA Mode

LA Mode: LA mode is divided into two sub-sections as shown below.

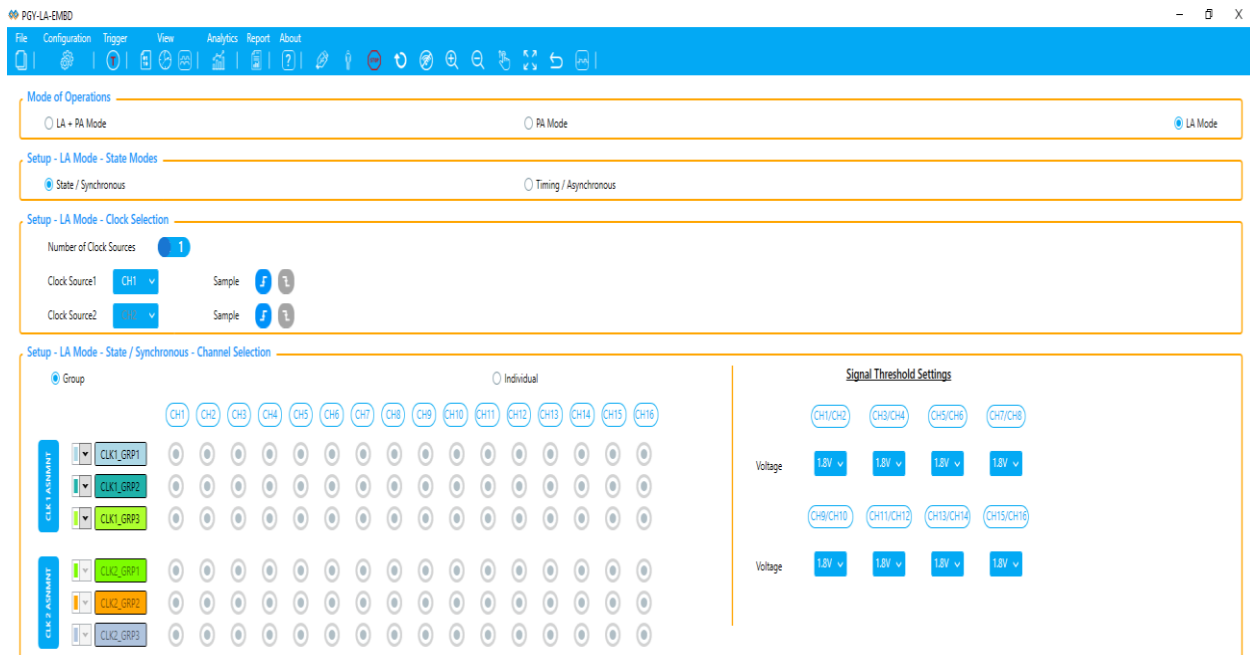


Figure 15.LA Mode

State/ Synchronous

Number of Clock Sources: Based on number of clock sources connected in DUT, the user has provision to select CLK1 Assignment or CLK2 assignments.

If Number of clock source 1 is selected, then provide connected clock channel number to clock source 1. The available channels are CH1 to CH16 and their corresponding signals can be set in the in different groups available in CLK1 assignment as shown below.

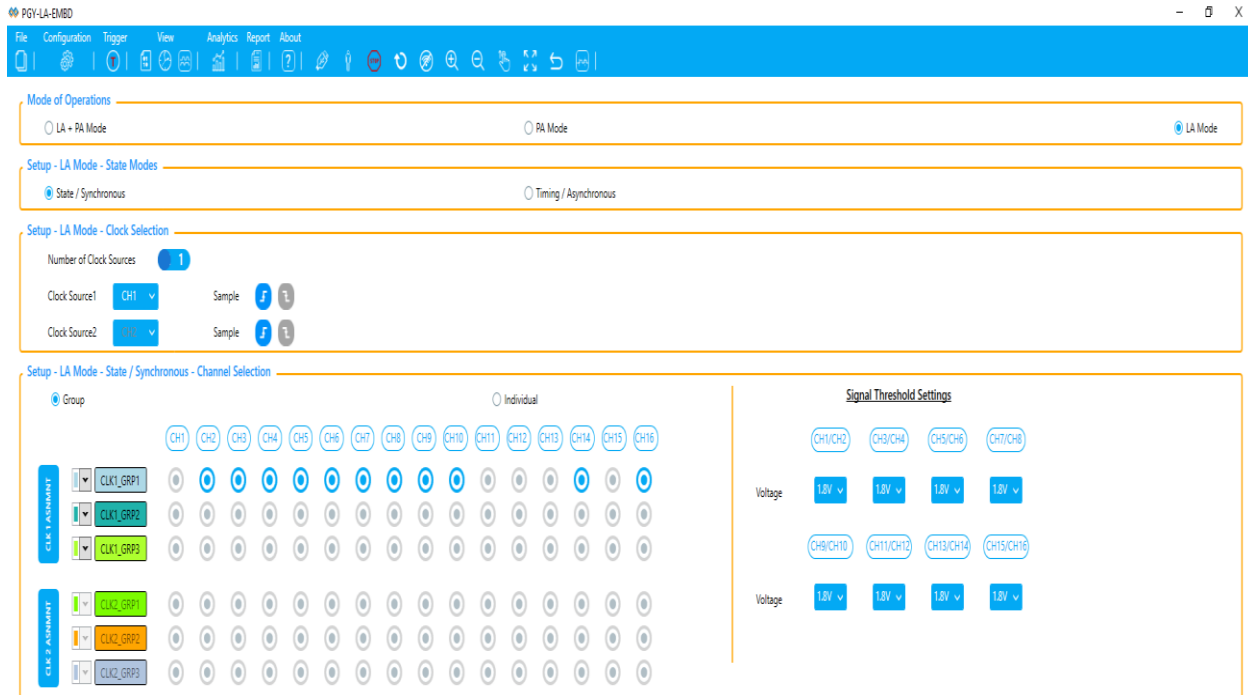


Figure 16.State/Synchronous – Clock Source 1

If Number of clock source 2 is selected, then provide connected clock channel number to clock source 1 and clock source 2. The available channels are CH1 to CH16 and their corresponding signals can be set in the different groups available in CLK1 & CLK2 assignment, as shown below.

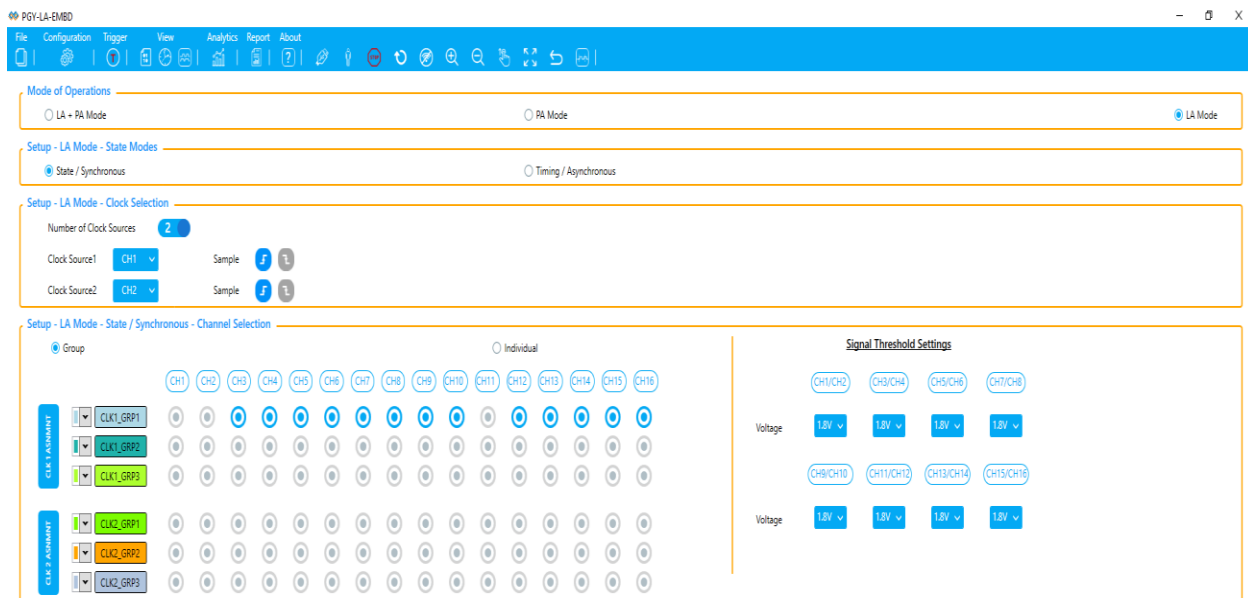


Figure 17.State/Synchronous - clock Source -1 and 2

Sample: User can select sample w.r.t rising/ falling edge.

Group: Out of available signals user can make selected signals as a group for better analysis.

Individual: If user will select Individual option, selected channels will be displayed as shown below.

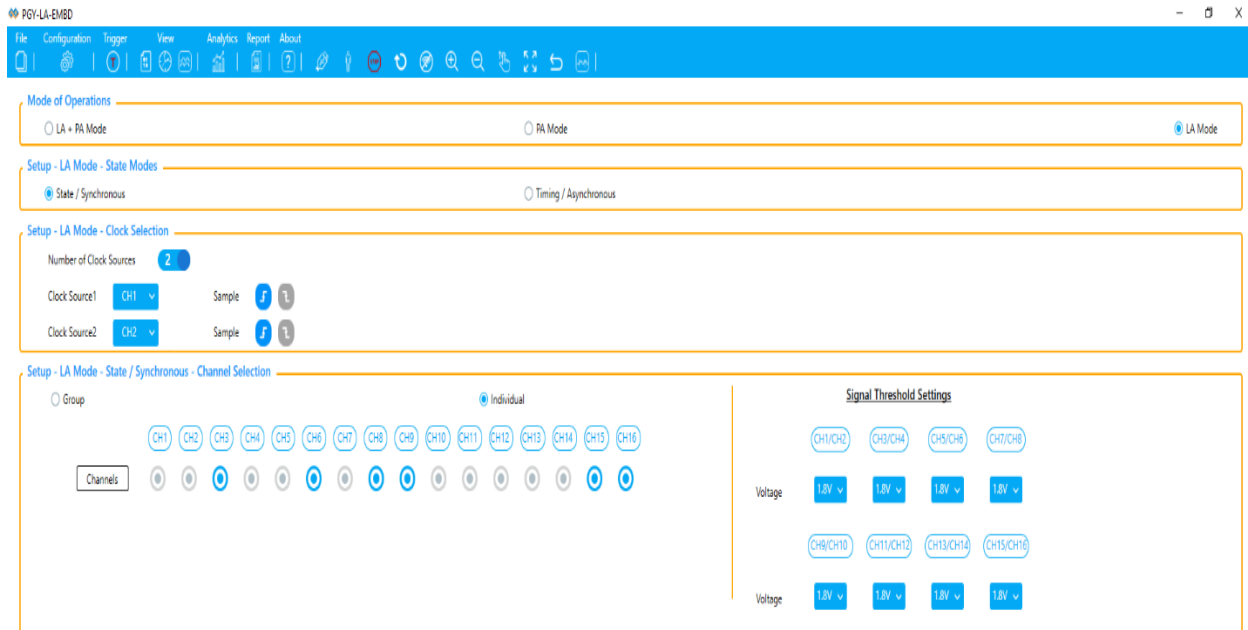


Figure 18.State/Synchronous - Individual

Signal Threshold Settings: Allows the user to select logic threshold generated by the DUT. Available options are 1.2,1.8,2.5,3.3 and 5.0V.

Once setting done, analyzer is ready to acquire the data from DUT.

NOTE: If user selects same channel, then it will display conflict message “Channel Already Selected”.

Changing the Bus Data Format (Hex, Decimal, etc.) in State Plot View:

By default, all protocols will be displayed in Hexadecimal format. To change the Bus Data Format, right click on the State Plot View GUI of the software and then go to Bus Data Format option, select the desired radix: Ascii, Hex, Binary, Decimal, and so on.

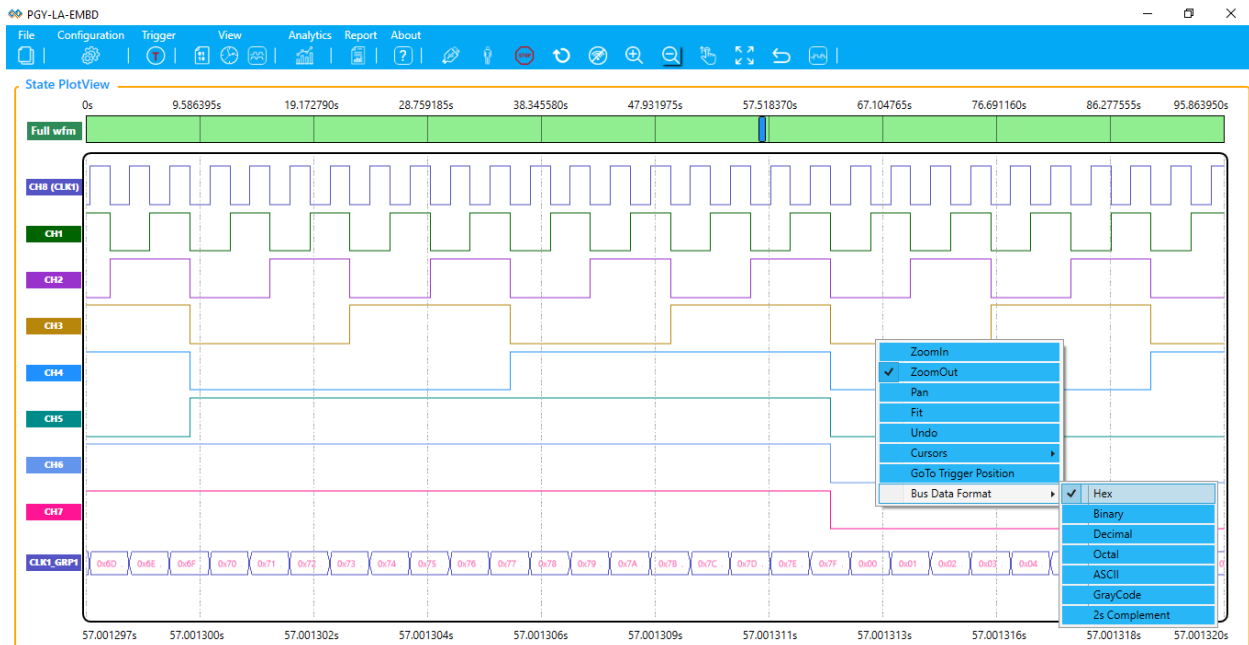


Figure 19. Different data formats in LA mode.

Data formats can also be changed according to the user's preference in the waveform listing view by selecting the dropdown menu as shown

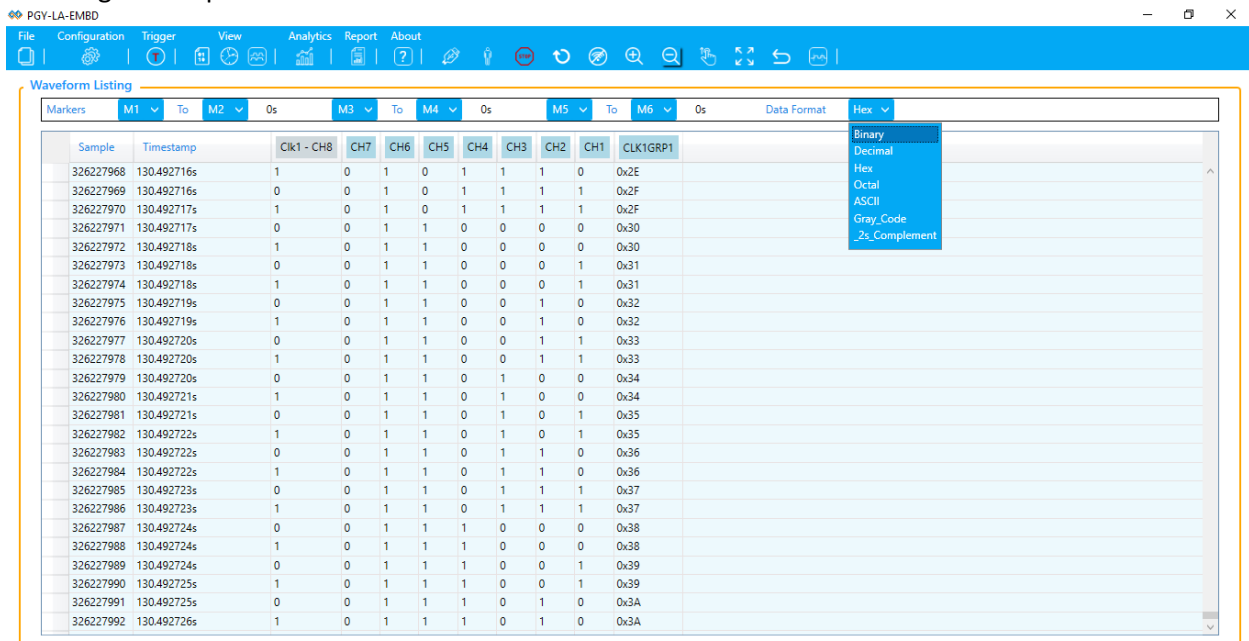


Figure 20. Different data formats in Listing View

Timing/Asynchronous

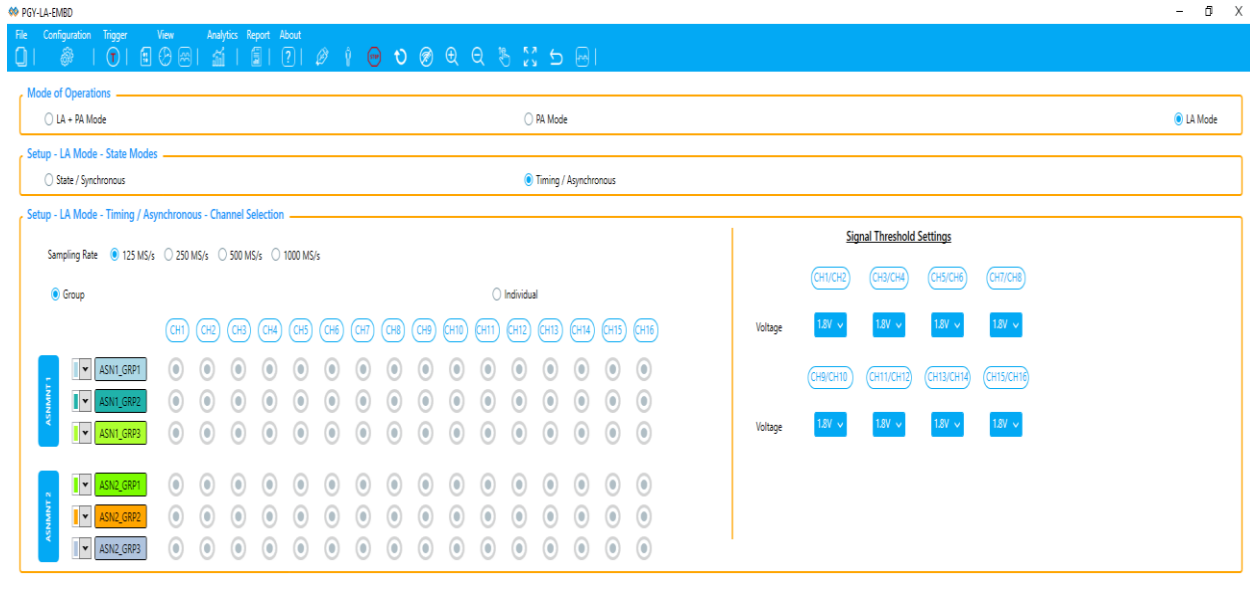


Figure 21. Timing/ Asynchronous

Sampling Rate: The sample rate radio button allows user select how fast to sample data—how many times per second signal is measured. Default selection is 125MS/s. PGY-LA-EMBD supports up to 1GS/S capture.

Group: Out of available signals user can make selected signals as a group for better analysis

Individual: If user will select Individual option, selected channels will be displayed as shown below

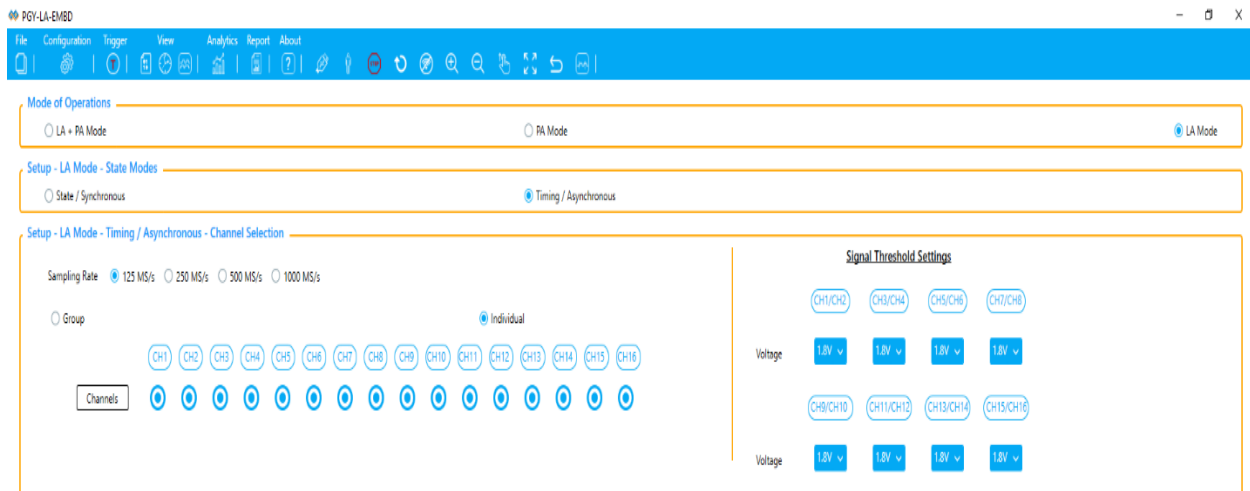


Figure 22. Timing/Asynchronous - Individual

Signal Threshold Settings: Allows the user to select logic threshold generated by the DUT. Available options are 1.2,1.8,2.5,3.3 and 5.0 V.

PA Mode

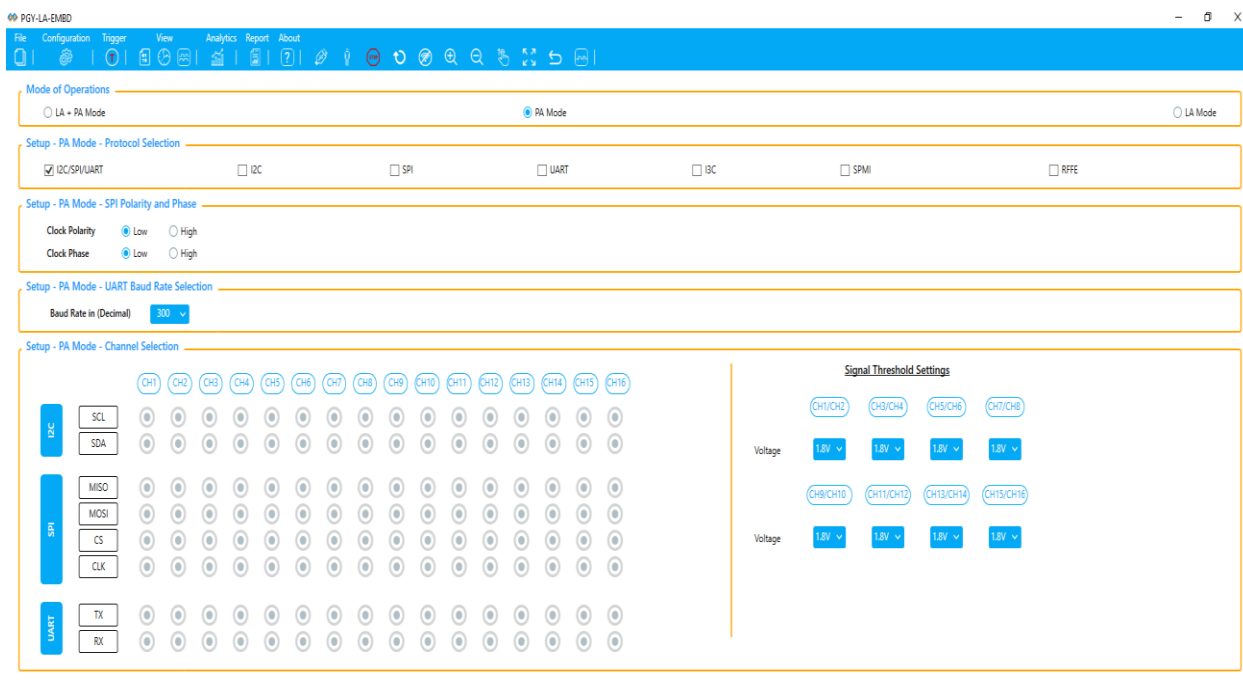


Figure 23. PA Mode

Setup-PA Mode Protocol Selection: By default, all three-protocol checkbox is selected i.e. I2C/SPI/UART/I3C/RFFE/SPMI. User can select individual protocols, combination of multiple protocols or default selection as per their requirement.

Setup-PA Mode-SPI Polarity and Phase: This option will provide user to select SPI polarity and phase based on the user requirements. By Default, Clock Polarity and Clock Phase is LOW.

Setup-PA Mode-UART Baud Rate Selection:

The rate at which information is transferred in a communication channel. Flexibility to set different baud rates for UART. Use drop-down menu to select baud rate as per requirement.

Setup-PA Mode-Channels Selection: Based on the connected channels and selected protocols user can select channels accordingly.

LA + PA Mode (Default)

By selecting LA + PA mode, user can analyze both mode results together. As explained individual mode of operation.

4.2.3 Acquire

It starts captures the signal and decode packets based on protocol.

4.2.4 Stop

Stop captures the signal.

4.3 Trigger View

PGY-LA-EMBD supports Auto, Pattern, Protocol aware and Timing parameter trigger capabilities. Users can trigger on any of the trigger features. User can set different trigger conditions to capture protocol activity at specific event. Trigger location will be indicated by a symbol “T” in the decoded result window. Trigger menu provides option to set different Trigger condition and view them as follows:

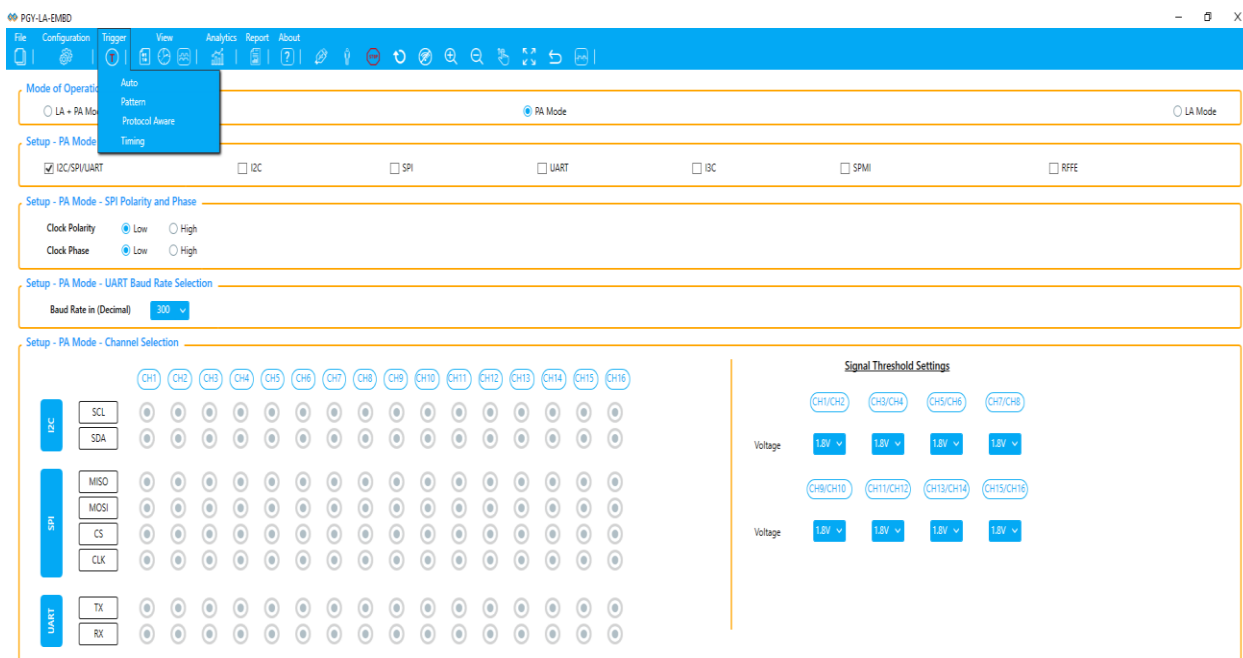


Figure 24. Trigger Menu

Trigger Type

Select one of the Trigger Types from the following:



Figure 25. Trigger Type

4.3.1 Auto Trigger

This is the default selection. No trigger pattern is used. In Auto mode analyzers start capturing digital signals on clicking 'Acquire' button.

4.3.2 Pattern Trigger

Pattern trigger looks at a serial data stream and triggers after a given serial pattern is matched.

Figure 26. Pattern Trigger

A pattern trigger allows user to configure the device to monitor the logic analyzer inputs for a specific pattern. When the device acquires entered pattern, the device asserts the pattern trigger. In Pattern Trigger out of 16 channels based on connection user can give the pattern in binary format. After setting the pattern click on Acquire icon to view the trigger result.

4.3.3 Protocol Aware Trigger

Trigger conditions can be given to listed protocols and their parameters. To trigger on any specific Protocol with specific packet content select 'Protocol Aware Trigger'.

Figure 27. Protocol Aware Trigger

- **I2C:** In Protocol Aware Trigger Type, choose the I2C Protocol type from the drop-down menu to Trigger any of the I2C packets, select the available options from the user interface. Available options are like **Address, Data, ACK, NACK, Repeated Start, Stop, Start, Address +Data**, etc.
- **SPI:** In Protocol Aware Trigger Type, choose the SPI Protocol, to trigger on MOSI and MISO data.
- **UART:** User can set trigger on UART Data by selecting the correct parity. Parity can be selected based on number of 1's in given data, If Data contains EVEN number of 1's then select Low Parity, for ODD number of 1's Select High Parity
For Example: Data C2 in Hex, in given Example Data contain Odd number of 1's so select High Parity.
- **I3C:** In Protocol Aware Trigger Type, Choose the I3C Protocol to Trigger on any Broadcast, Directed or private Message.
- **RFFE:** In Protocol Aware Trigger Type, choose the RFFE Protocol type from the drop-down menu to trigger any RFFE commands such as Ext. Reg. Write, Ext. Reg. read and so forth message.

- **SPMI:** In Protocol Aware Trigger Type, choose the SPMI Protocol type from the drop-down menu to trigger any SPMI commands such as Reg Write, SLEEP or WAKE UP.

After setting the trigger conditions click on **Acquire Button** icon to view the Trigger result.

4.3.4 Timing Parameter Trigger

Helps the user to set trigger condition on Pulse width and delay trigger.

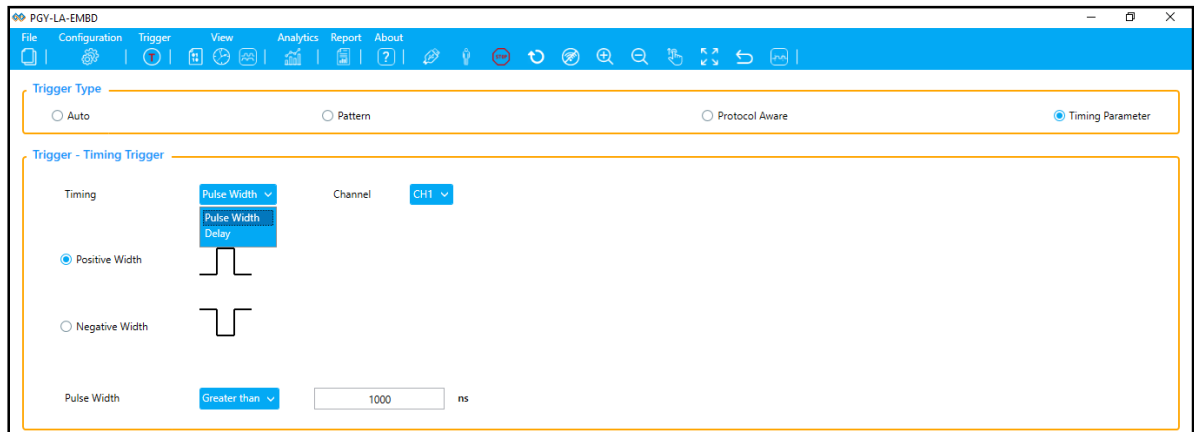


Figure 28. Timing Parameter Trigger

Delay Trigger: Delay trigger is used to trigger when time differences between signal transitions either fail to meet minimum thresholds or exceed maximum thresholds.

Pulse Width: This trigger enables user to trigger exclusively on pulses with a specified range of widths. User can also trigger on a pulse width condition where a particular channel is Greater than or less than for a specified amount of time.

NOTE: Timing Parameter trigger will be used for **Timing/ Asynchronous under LA Mode.**

4.4 View Menu

The captured signals are decoded and displayed to the end user in a user-friendly manner. This view section divided into three sub-sections:

- Protocol View (P-View)
- Timing View (T-View)
- Logic View (L-View)

4.4.1 Protocol View (P-View)

Protocol view window provides analyzed data along with their bus timing information. This gives the system level insight to the users. Selected frame in Protocol listing window will be highlighted in bus timing view for better analysis.

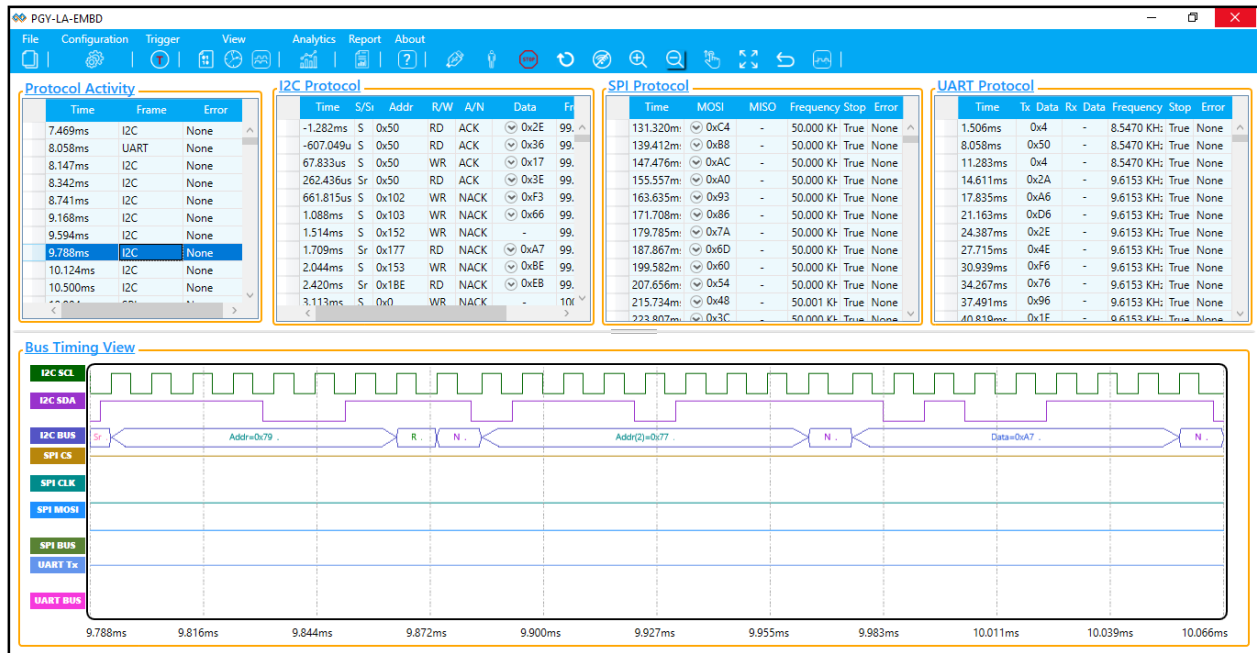


Figure 29. P-View

The protocol activity view gives high level abstract view of the frame, which contains the following fields.

Header	Description
Time	Relative Timestamp at which the packet was captured. This gives you time stamp information.
Frame	It defines the type of Frame (I2C/SPI/UART/I3C/RFFE/SPMI).
Error	In case of any error detected in Frame, it will get displayed over here.

Bus Timing View: Allows user to view the waveforms and bus diagram in the bus timing view. Right Click on bus timing view window, it will display following controls.

Controls	Description
Zoom In	Zoom the waveform
Zoom Out	Zoom Out the waveform
Pan	Enable user to move the waveforms left or right.
Fit	Enable user to fit the selected message in the plot vies.
Undo	Enable user to undo the last operation in the waveform window.
Cursors	V-Bar: Enable the vertical cursors to measure the time difference. Markers: To measure the delta time between two markers.
Go to Trigger Position	Click 'Go to Trigger' to view the trigger condition.

4.4.2 Timing View (T-View)

Timing view is a unique capability of the PGY-LA-EMBD which enables designers to get detailed insights to their signals timing information. The flexible sampling rate selection enables designers to investigate Glitches which can cause issues in the functioning of their designs. User can select different sampling rates available in the user interface. Software helps the user to select max sampling rate up to 1GS/sec.

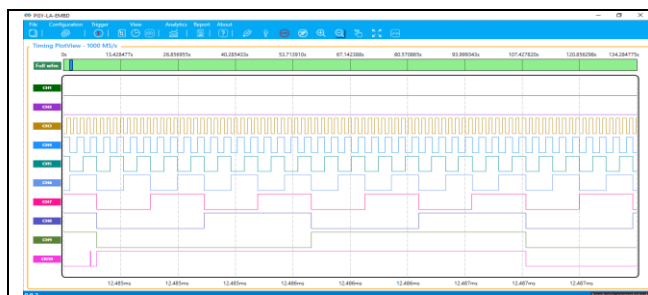


Figure 19. Timing View - Glitch

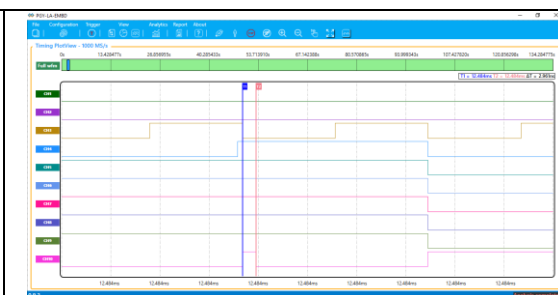


Figure 20. Timing View – Zoom View of Glitch

Figure 21.T-View

4.4.3 Logic View (L-View)

In Logic View, user gets the digital information of all analyzed signals, as shown in below image.

Sample	Timestamp	CH6 -UART TX	CH5 -SPI Clk	CH4 -SPI MOSI	CH3 -SPI CS	CH2 -I2C Data	CH1 -I2C Clk
8389030	46.618046s	1	0	0	1	1	0
8389031	46.618051s	1	0	0	1	1	1
8389032	46.618056s	1	0	0	1	1	0
8389033	46.618061s	1	0	0	1	1	1
8389034	46.618066s	1	0	0	1	1	0
8389035	46.618071s	1	0	0	1	1	1
8389036	46.618076s	1	0	0	1	1	0
8389037	46.618082s	1	0	0	1	1	1
8389038	46.618087s	1	0	0	1	1	0
8389039	46.618089s	1	0	0	1	0	0
8389040	46.618092s	1	0	0	1	0	1
8389041	46.618097s	1	0	0	1	0	0
8389042	46.618100s	1	0	0	1	1	0
8389043	46.618102s	1	0	0	1	1	1
8389044	46.618107s	1	0	0	1	1	0
8389045	46.618109s	1	0	0	1	0	0
8389046	46.618112s	1	0	0	1	0	1
8389047	46.618117s	1	0	0	1	0	0
8389048	46.618122s	1	0	0	1	0	1
8389049	46.618127s	1	0	0	1	0	0
8389050	46.618130s	1	0	0	1	1	0
8389051	46.618132s	1	0	0	1	1	1
8389052	46.618137s	1	0	0	1	1	0
8389053	46.618142s	1	0	0	1	1	1
8389054	46.618147s	1	0	0	1	1	0

Figure 22.L-View

4.5 Analytics

Analytics provide the summarized view of the entire protocol activity captured over a long duration. Click Analytics icon to view the summarized protocol activity.

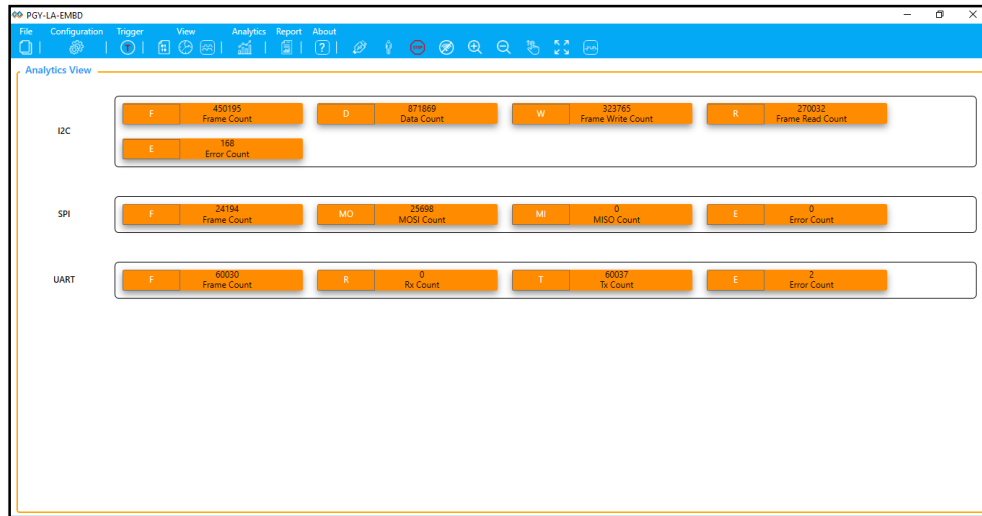


Figure 23. Analytics

Analytics View provides following options:

I2C

- Frame count: Provides the count of decoded I2C packet.
- Data Count: Provides the count of data received.
- Frame Write Count: Total no of packets received which has write operation.
- Frame Read Count: Total no of packets received which has read operation.
- Error Count: Indicates received error packets.

SPI

- Frame Count: Provides the count of decoded SPI packet.
- MOSI Count: Total number of MOSI Data received
- MISO Count: Total number of MISO Data received.
- Error count: Indicates received error packets.

UART

- Frame Count: Provides the count of decoded UART packet.
- RX Count: Provides the count of decoded RX packet.
- TX Count: Provides the count of decoded TX packet.
- Error count: Indicates received error packets.

4.6 Report

To generate a report, click Report from 'Report' menu.

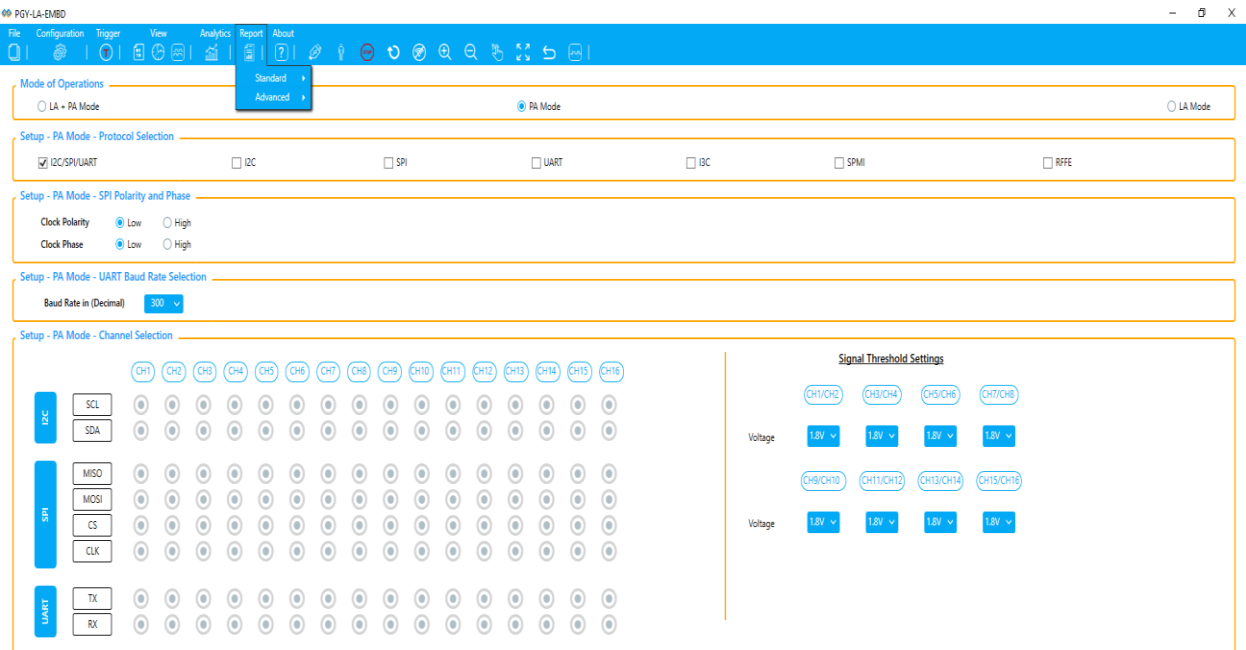


Figure 24.Report Menu

Report generation consists of two sections:

1. **Standard Report:** Select Standard option from the Report Menu. Report will be generated based on the user selected format i.e., PDF/CSV in user specified location.
2. **Advanced:** It allows the user to generate the report of the analyzed data in PDF format with details of all the setup information, and custom details like name of the company, logo, Engineer name, date, and time to ensure designers can document all details.

Figure 25. Report - Advanced

- Enter the information you want in the Report Header such as Company name, company logo, etc.,
- Protocol View: Based on report requirement select / deselect protocol view.
- Logic View: Based on report requirement select / deselect logic view.
- Select Range: Select whether any specific range of packets or all the analyzed packets needs to be saved.
- Click on the Generate Report button to generate the report.
- It will popup one “**Save As**” window which enables the user to choose the location where the report can be saved in PDF format. Report generation takes few minutes depending on the captured data.

Note: You can generate report only after the user clicks ‘Stop’ in the user interface.

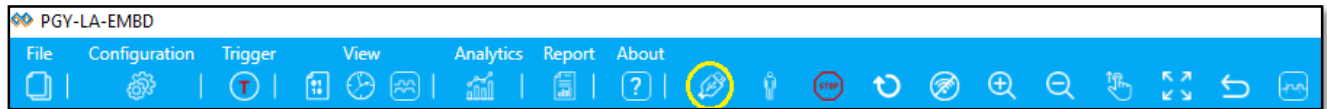
4.7 About

- **About:** About option gives information about the software and hardware version of the product.
- **View Help:** View Help option provides PGY LA-EMBD User Manual document.

5 PGY-LA-EMBD Modal Menu Navigation

The modal menu options will by default appear side of the main menu.

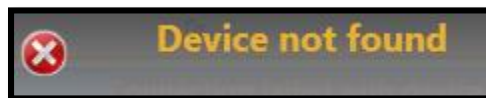
5.1 Connect



Quick access to connect. Click Connect icon to establish a connection between Host computer and Discovery hardware unit. On Successful Connection, software will display on the screen connection message on status bar.



On the failure case, the following popup window will appear on the screen with the message “Device Not found” as shown below.



This could be because of one of following reason,

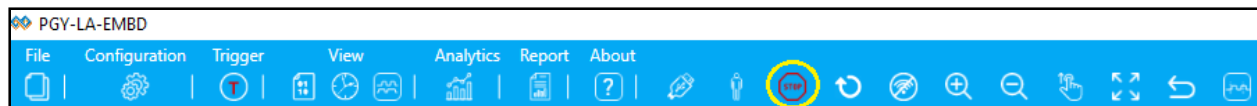
- Make sure the USB cable is connected properly.
- Make sure the computer is installed with USBPCap driver.
- Device is Power On.
- USB is properly recognized in Device Manager.

5.2 Acquire



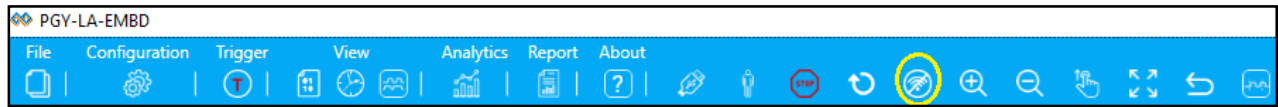
To arm the PGY-LA-EMBD Hardware unit to capture the data, click ‘Acquire’. The PGY-LA-EMBD hardware unit starts capturing the data.

5.3 Stop



To stop the acquisition of Protocol data from DUT, click ‘Stop’. PGY-LA-EMBD hardware stops capturing the data.

5.4 Decode Offline



Allows to view offline Trace File decoded result. In the offline mode of operation, protocol activity that was previously captured and stored can be analyzed.

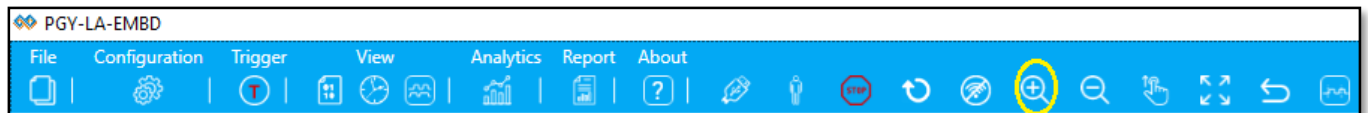
Perform the following step by step approach to do an offline analysis of trace file:

1. Ensure you have both xxxx.xml and xxxx.dat files folder.

Name	Date modified	Type	Size
ProdigyCapture1	29-Oct-20 5:55 PM	File folder	
ProdigyCapture1.xml	29-Oct-20 5:56 PM	XML Document	6 KB

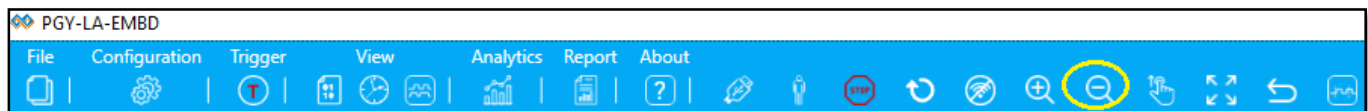
2. Select Decode offline icon present in the main menu, the Browse menu opens. Select the XXXX.xml file using the Browse menu. Result will display.

5.5 Zoom In



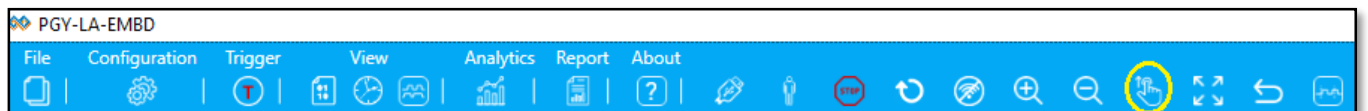
Allow the users to "Zoom" the waveform.

5.6 Zoom Out



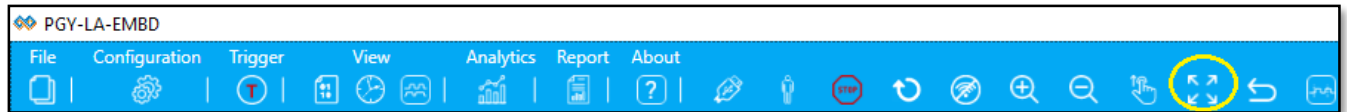
Allow the users to Zoom out the waveform.

5.7 Pan



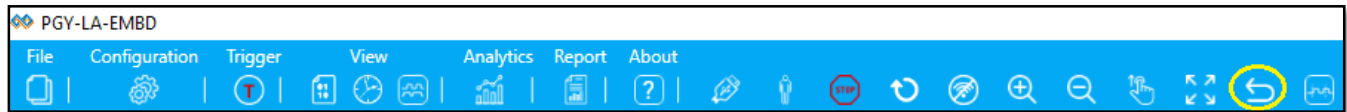
Enable user to move the waveforms left or right.

5.8 Fit



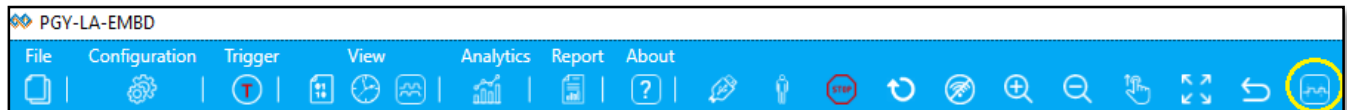
Enable user to fit the selected message in the plot vies.

5.9 Undo



Enable user to undo the last operation in the waveform window.

5.10 V-Cursors



The vertical cursors allow the users to measure the time difference.