Charchita Kuppa
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Summary

Software test professional with 3+ years of experience. Took a break for maternity and relocation to USA. Last 6 months, started learning JavaScript, HTML, CSS and DOM the foundation needed to perform browser driven automated testing.

Technical Skills

Programming languages: C, C++, JavaScript, HTML, CSS, SQL, Verilog
Databases: MySQL
Tools and Technologies: GIT, CANTATA++, Vector Cast, Tasking Compiler, MPLAB, Xilinx ISE.
Operating System: Linux, Windows
Hardware: Embedded Platforms - AVR Atmega128 from Atmel

Certification:

ISTQB - Foundation Level Certified in Software Testing (Certificate No: ITB-CTFL-0072711)

Work Experience

Software engineer, Cyient Limited, Hyderabad, India (September 2015 – August 2016)

- Worked on implementation of various features of European Rail Traffic Management system.
- Requirement analysis, Development of test plan and test cases are performed for different baselines by using Vector Cast Tool. Test cases are implemented using C++.

Contract assignee, CMC Limited, Hyderabad, India (October 2013 – July 2015)

- Involved in Implementation of System Mode Controller and Steering Torque controller of Electric Power Steering System.
- Requirement Analysis, Test Plan Preparation and Unit testing activity are performed for different baselines of the EPS Software by using CANTATA++ tool, test cases are implemented using C.

Freelance – Developer, Servomax India private limited, Hyderabad, India (October 2012 – September 2013)

- Developed sensing and data logging systems for the analysis of solar panel performance. The voltage and current generated by panels are measured and logged in different test conditions to derive the performance curve for generated power vs. time.
- Designed voltage, current sensing circuits and Data logger design using C, MPLAB8 IDE tool. Performed analysis based on graphs obtained from data.

Assistant software engineer, Silicon interfaces, Mumbai, India (March 2012 - August 2012)

- Handled the RTL Design and Verification of USB2.0 Transceiver Macro cell Interface also developed test benches using Verilog and Intel UTMI specification.
- This block handles the low-level USB protocol and signaling. The primary focus of this block is to shift the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic in the ASIC.

Education

- **Center for Development of Advanced Computing, NAGPUR, India (August 2011 - March 2012)**
  PG Diploma in VLSI 72.78%
- **Jawahar Lal Nehru Technological University, Kakinada, India (October 2006 - May 2010)**
  Bachelor of technology in Electronics and Communication Engineering. 77.49%