

ADC and Sensors

ADC, DAC, Sensor interfacing

- ADC
- DAC
- signal conditioning
- Sensors
- Glossary:
 - <http://www.maxim-ic.com/app-notes/index.mvp/id/641>

ADC: Analog-to-digital converter

- Input:
 - analog signal with a voltage
e.g., pressure, light intensity,
temperature, sound
- Output
 - digital value representing the voltage
 - 8-bit, 10-bit, 12-bit, 16-bit, 24-bit etc
depends on the specific ADC's precision

Purposes of ADC

- Digitize a signal
 - The world is analog; computer is digital
=> bridge the real world & computer
- Benefits
 - no more noise due to processing
 - can be stored/retrieved like any data
 - separate timing handling from processing

Types of ADCs

- Integrating ADC (not very fast)
 - outputs pulses, freq. proportional to V
- Successive Approximation ADC (common)
 - "binary search"
- Flash ADCs aka parallel ADCs
 - parallel comparison; fast but expensive

Bit resolution and sampling rate

- n bits $\Rightarrow 2^n$ levels
 - 8 bits: 256 gives 0.39° res. for $0-100^\circ\text{C}$
 \Rightarrow "jumping" problem if $\pm 0.5^\circ$ is needed!
- Sampling rate
 - should be $\geq 2\times$ higher than signal's highest freq. component (Nyquist freq)
 - otherwise, get aliasing problem

Analog, sinusoidal signals

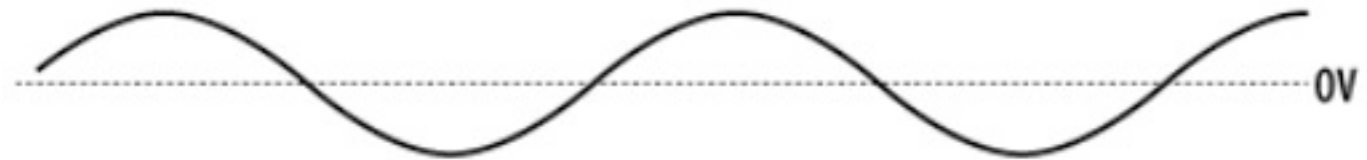
- Alternating current (AC)



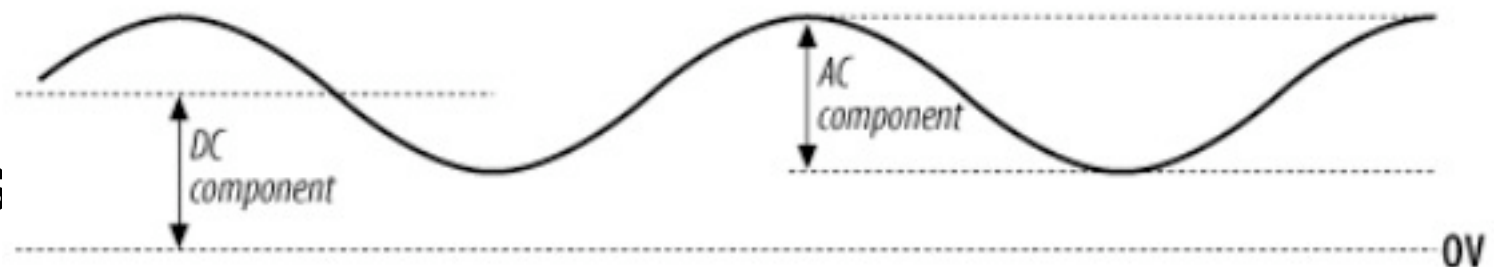
- Unipolar => either positive or negative, not both



- Bipolar => both positive and negative



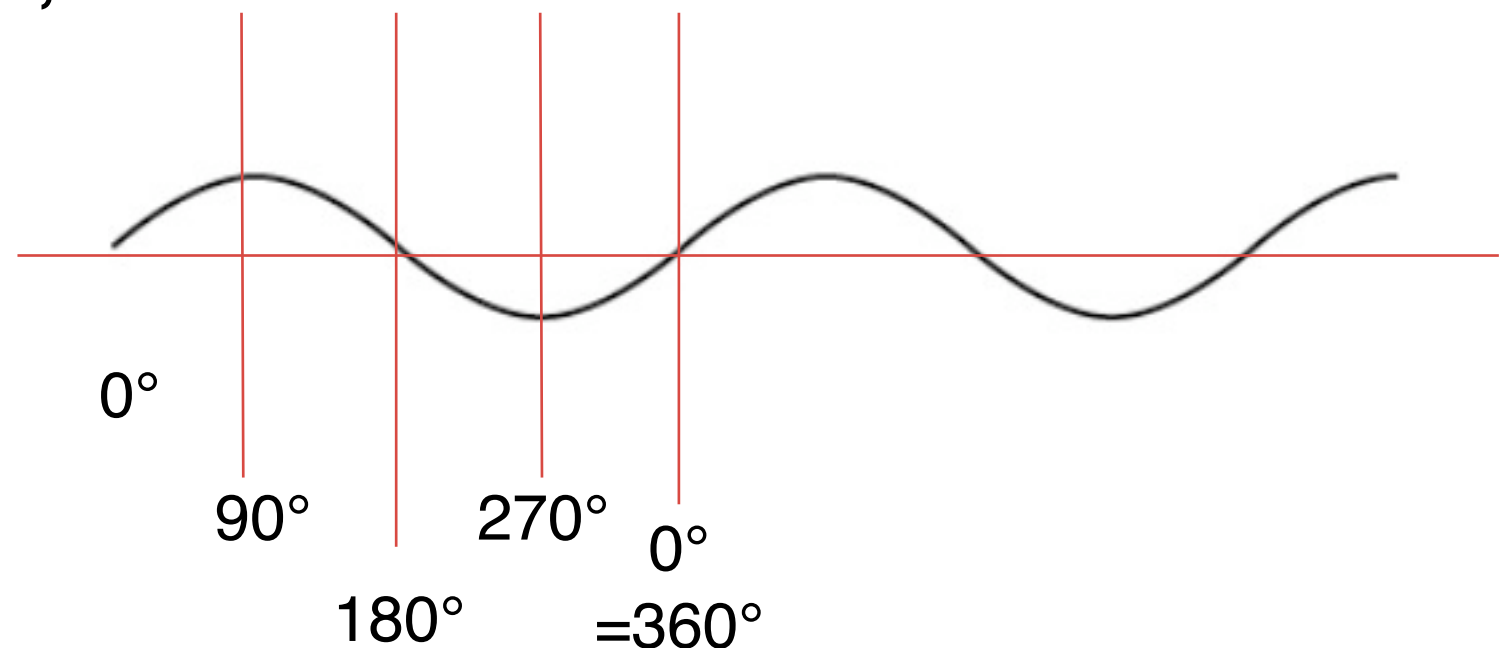
- Decompose into AC and DC components



Amplitude and phase of periodic signals

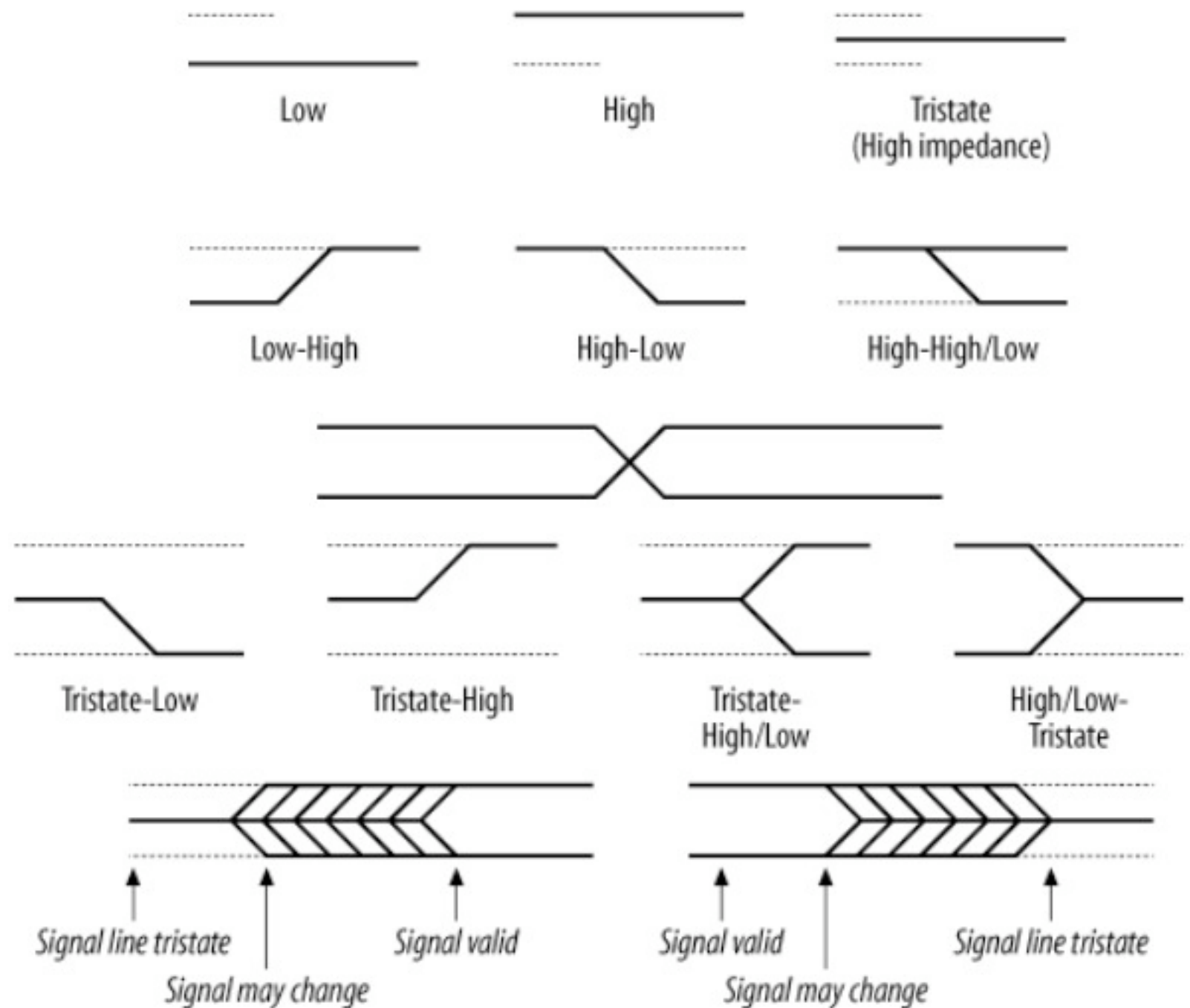
- Amplitude:
Amplify, attenuate. Unit: dB = $10 * \log_{10} \text{dif}$
 - $1x = 0\text{dB}$, $10x = 10\text{dB}$, $100x = 20\text{dB}$,
 $1000x = 30\text{dB}$
 $1/10 = -10\text{dB}$, $1/100 = -20\text{dB}$

- Phase
- Degrees



Timing diagram convention

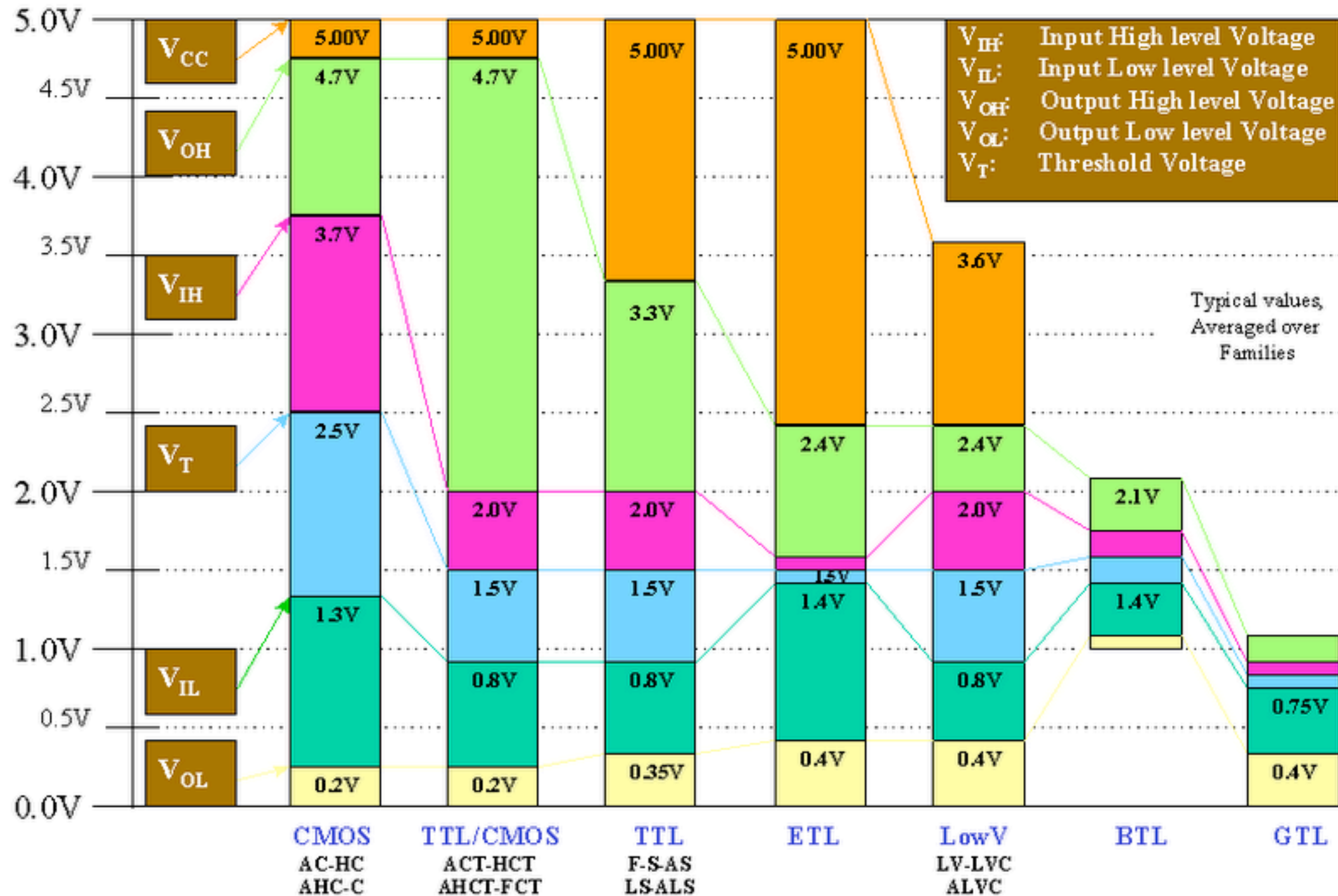
- Logic levels
- Transitions
 - known values
 - combination
- w/ Tristates
- valid period



Digital logic

- Interpret a voltage as a binary value
 - above a threshold \Rightarrow '1'
 - below a threshold \Rightarrow '0'
- Threshold is technology dependent!
 - Check data sheet to be sure
 - TTL, CMOS, ...

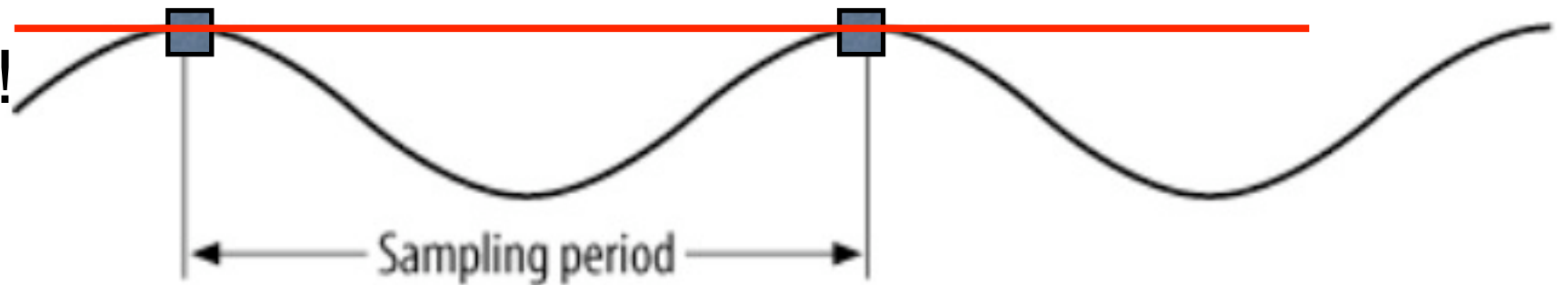
Voltage Thresholds



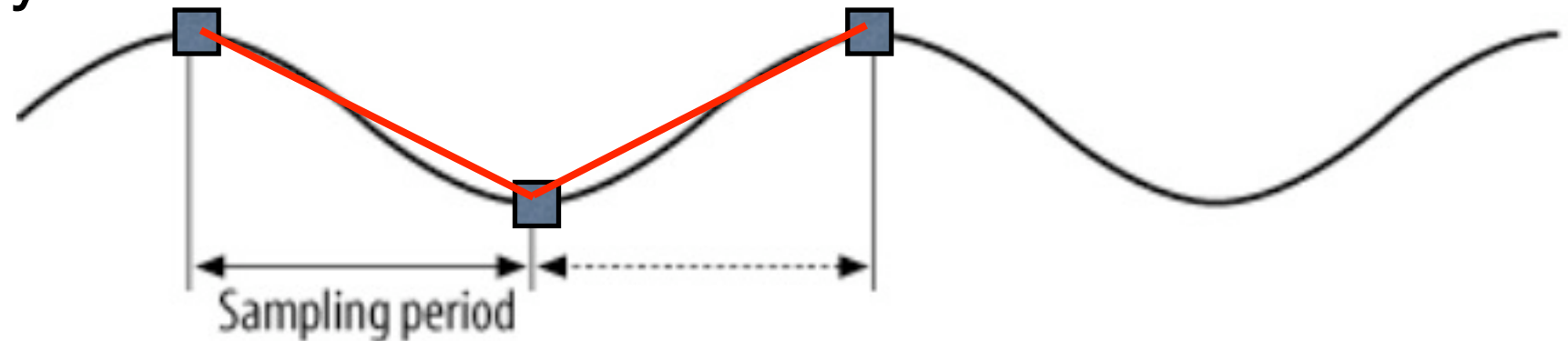
Credit: http://www.interfacebus.com/voltage_threshold.html

Sampling rate

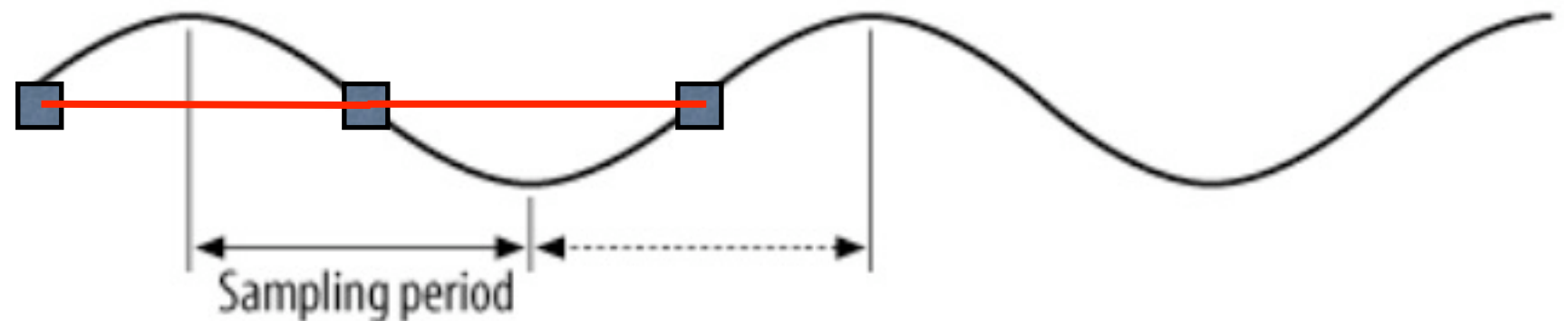
- Too low:
looks like
a straight line!



- Minimum
2x of frequency



- Still not sure
if you hit the
peak!
still could be
straight line

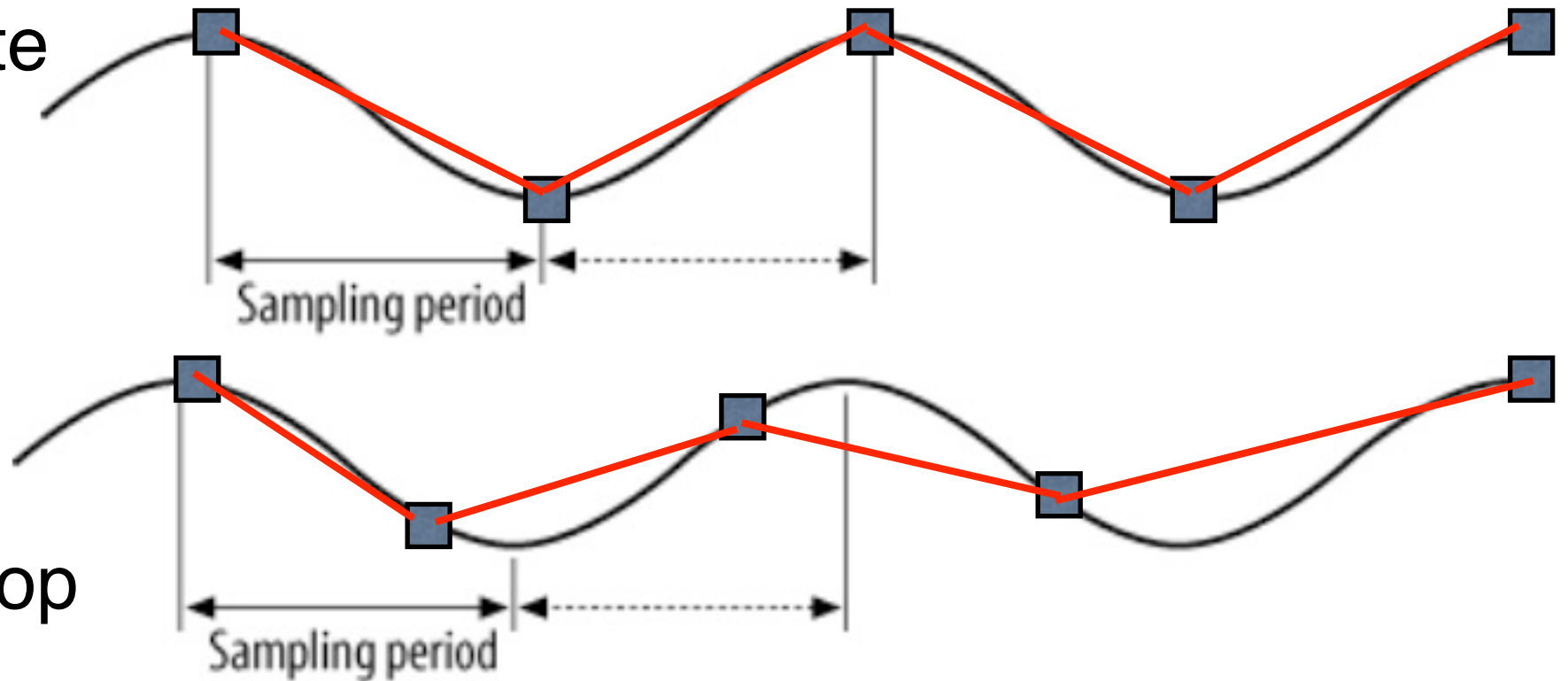


Jitter

- Unstable rate

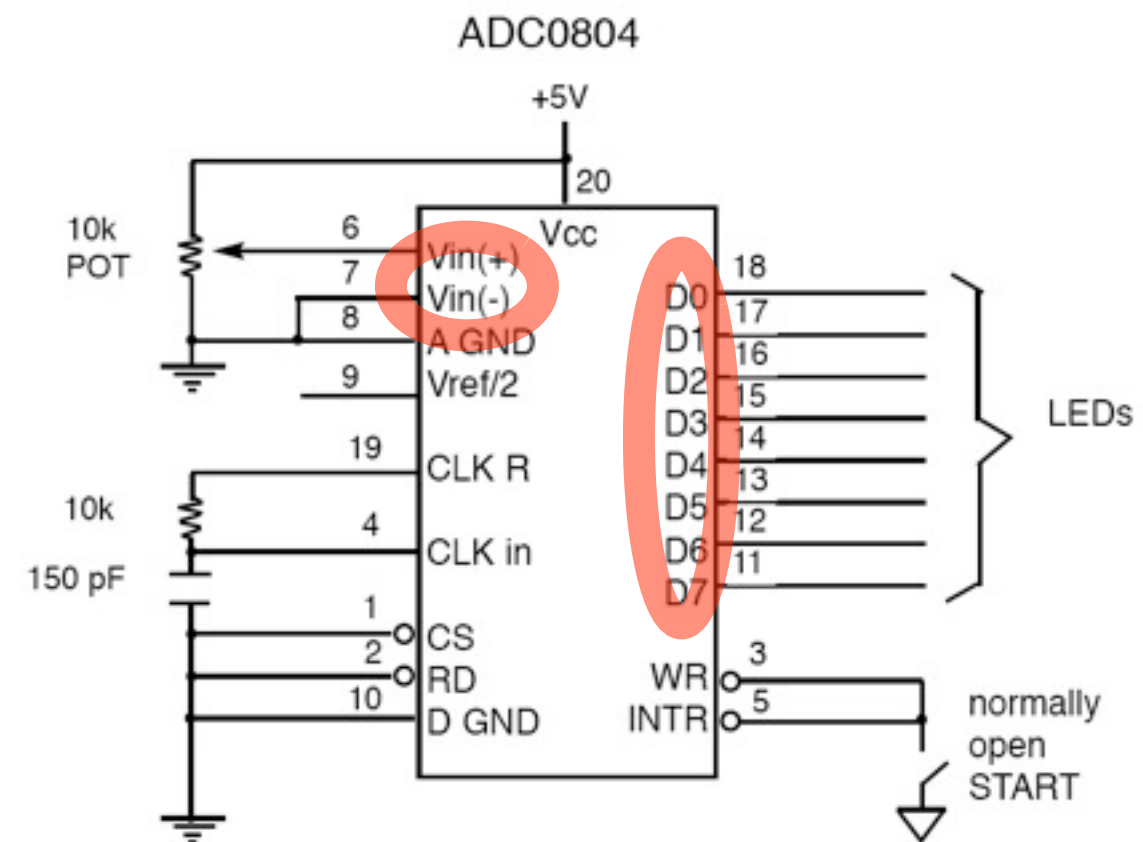
- wrong reading

- Solution:
hardware loop



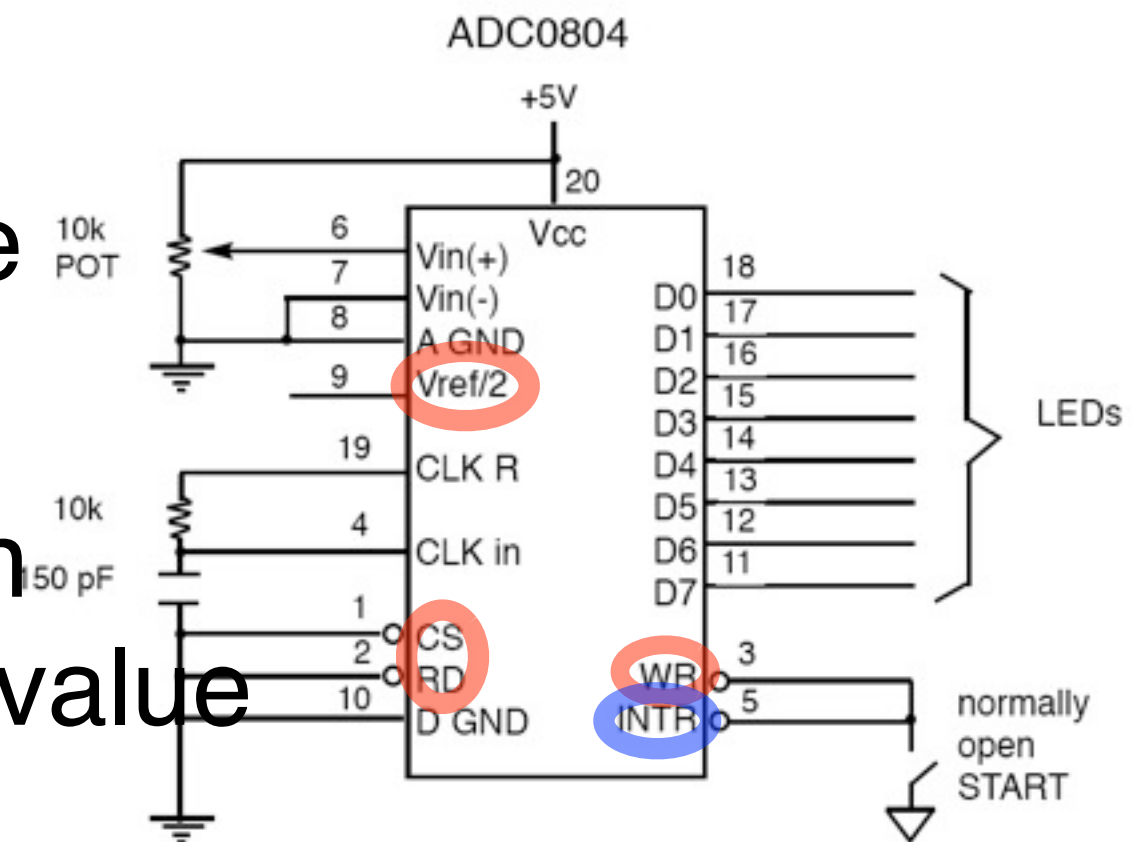
Example: ADC0804 (National Semicond.)

- input signals
 - single ended $V_{in}(+)$ vs. differential pair $V_{in}(+)(-)$
- output signal
 - 8-bit value representing voltage

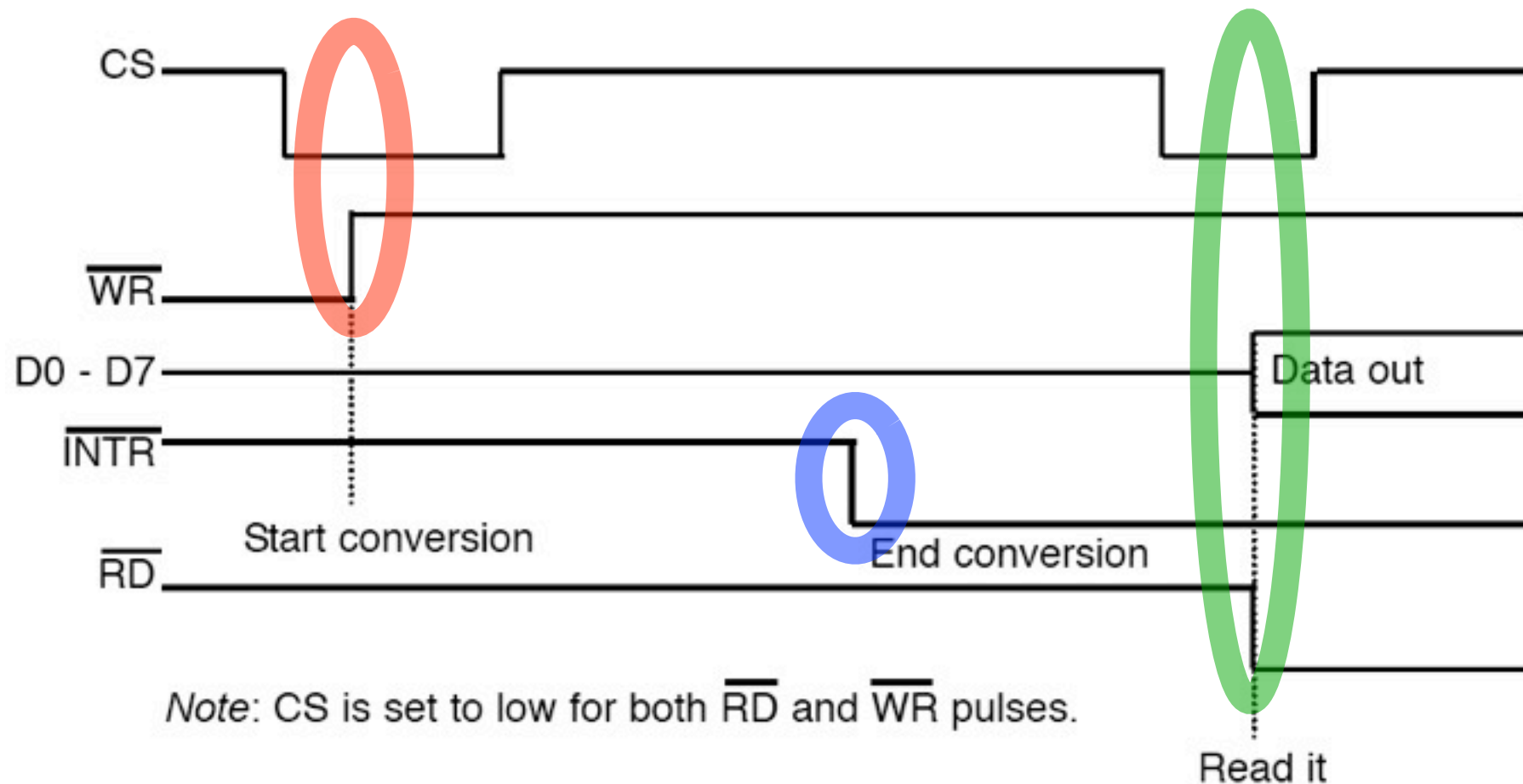


Example: ADC0804 (National Semicond.)

- Input control:
 - $V_{ref}/2$ to set the range
 - /CS: chip select
 - /WR: start conversion
 - /RD: read converted value
- Output control:
 - /INTR: interrupt line
indicating end-of-conversion



Timing Diagram for ADC transaction



1. rising \overline{WR}
during \overline{CS}

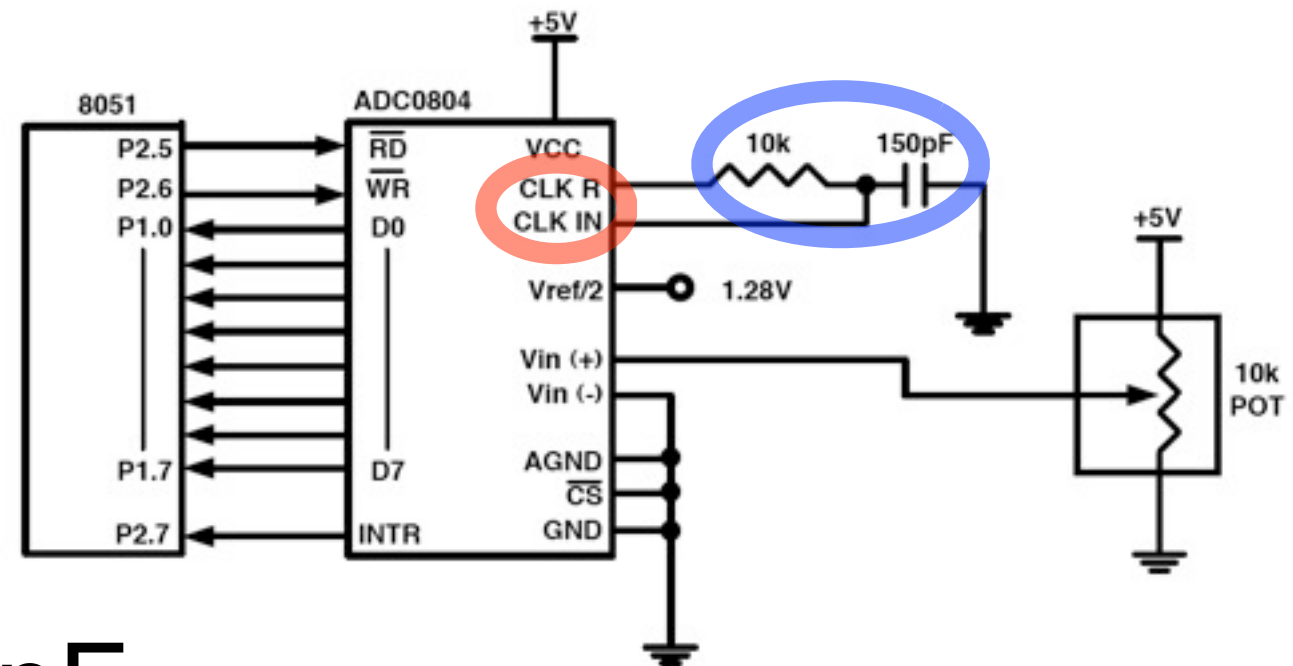
2. ADC finishes
conversion

3. assert \overline{RD}
during \overline{CS}

Could also assert \overline{CS} the whole time w/out pulsing!

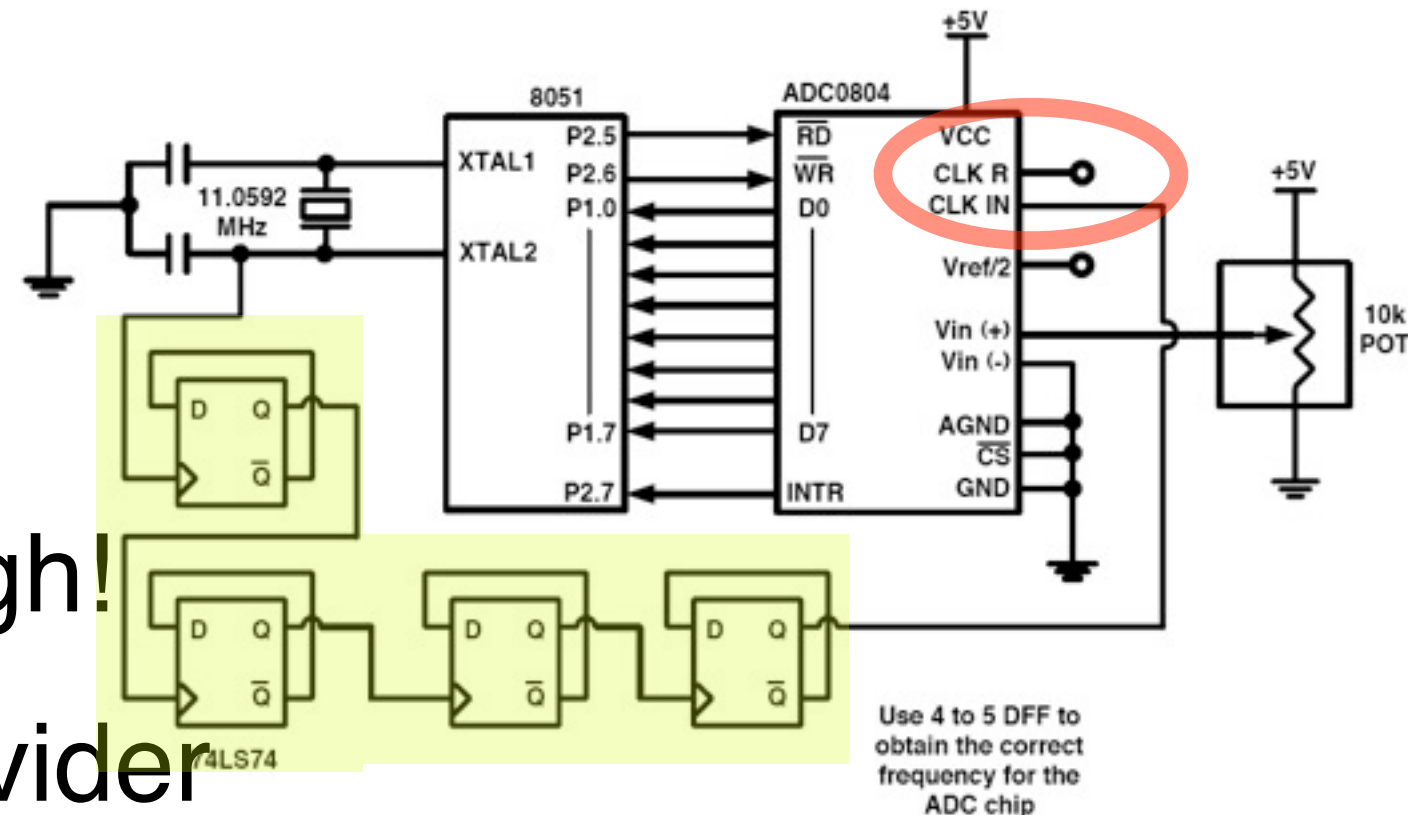
CLK IN and CLK R

- Opt. 1: internal clock
- Set the R, C value
 $f = 1/(1.1 RC)$
- $R = 10K\Omega$, $C = 150pF$
 $f = 1/(1.1 * 10^4 * 150 * 10^{-12})$
 $= 606060.6 \Rightarrow 606KHz$,
or $1.65\mu s$ cycle time
- Option 2: external clock



External clocking scheme for ADC0804

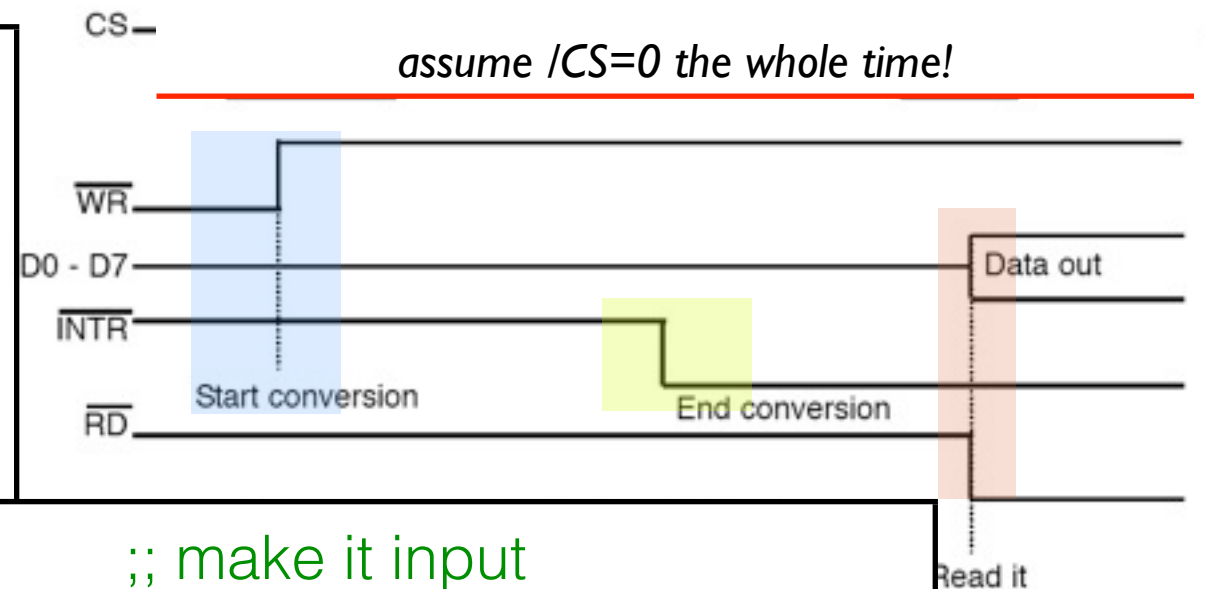
- Could use the same crystal as for 8051
- Issue: freq too high!
- Solution: clock divider



- cascaded D-flipflops:
next one is clocked by the prev's Q,
each feeds /Q to its own D

Assembly for ADC0804

RD	BIT	P2.5
WR	BIT	P2.6
INTR	BIT	P2.7
MYDATA	EQU	P1



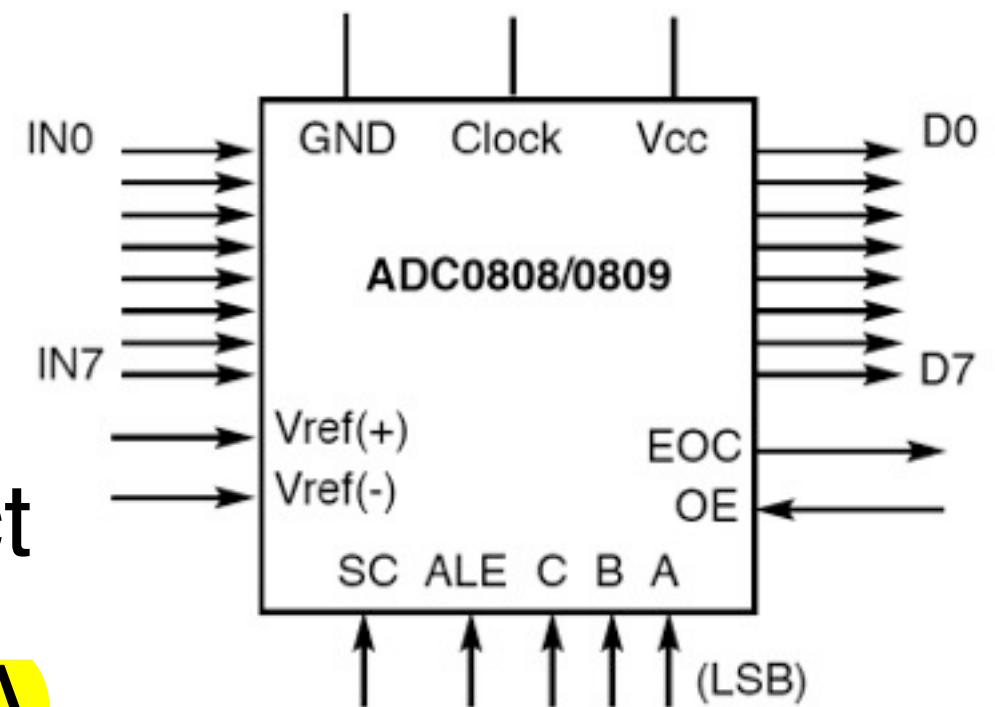
	SETB	INTR	:: make it input
BACK:	CLR	WR	:: pulse WR by lowering first
	SETB	WR	:: conv starts on rising edge
HERE:	JB	INTR, HERE	:: poll for /INTR to go low
	CLR	RD	:: assert output enable
	MOV	A, MYDATA	:: read conv value from port
	ACALL	CONVERSION	:: Chap.6 routine to ASCII
	ACALL	DATA_DISPLAY	:: Chap. 12 routine to display
	SETB	RD	:: de-assert output enable
	SJMP	BACK	:: do it again

ADC0808/0809: multi-(analog)-channel

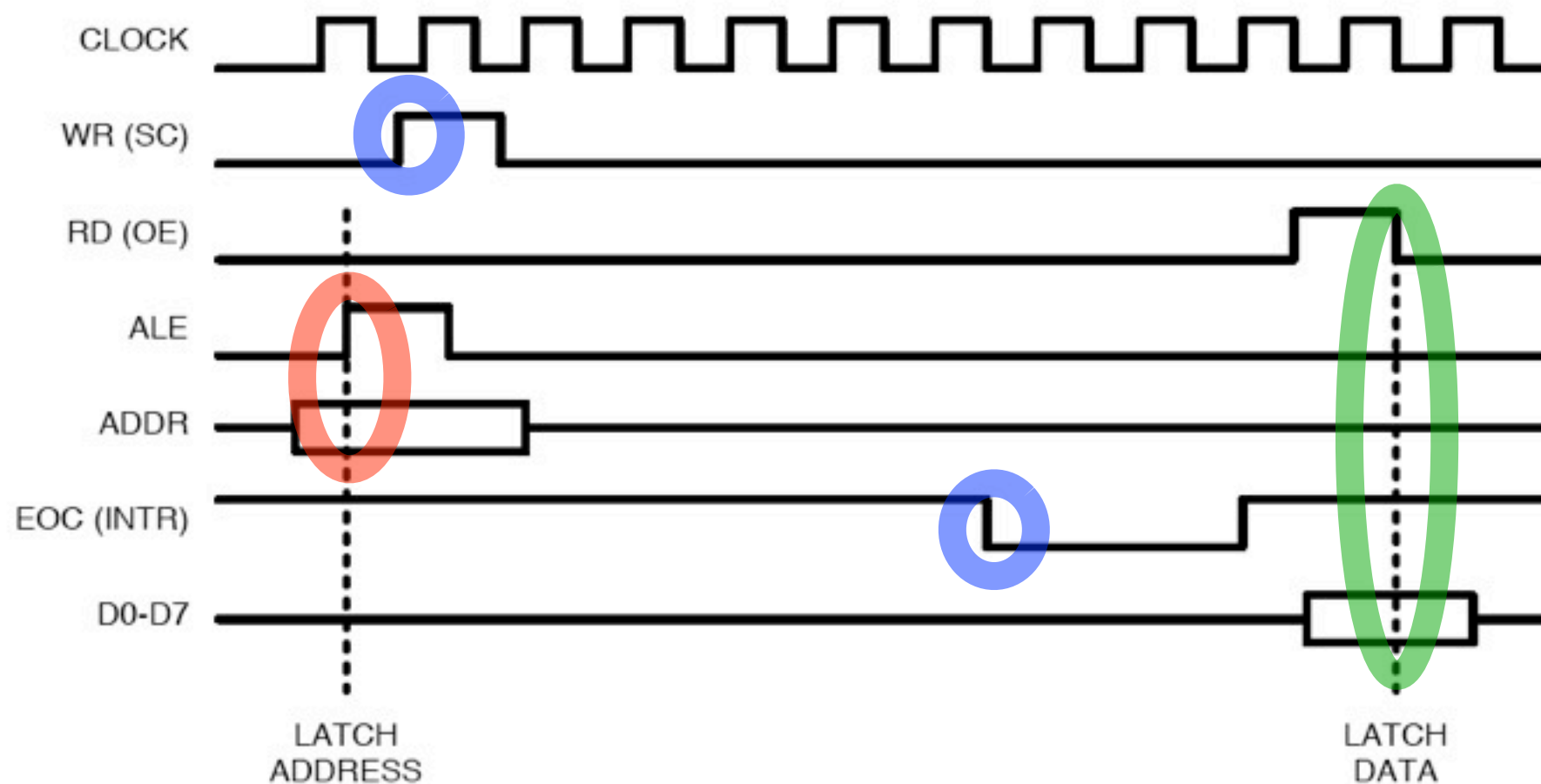
- 8 analog input lines
 - Selected by 3-bit, internally share 1 ADC
 - Conceptually, analog multiplexor on input
 - ALE latches the address
- 8-bit output port
 - similar to the single-channel ADC

Pin interface on ADC0808/0809

- IN0..IN7: analog input channels
- SC, EOC: (=WR, INTR)
start conv, end-of-conv
- OE: (=RD) output enable
- C B A : 3-bit channel select
- ALE: clock for latching CBA
- $V_{ref}(+)$, $V_{ref}(-)$: max and "gnd"



Timing Diagram for the ADC0809



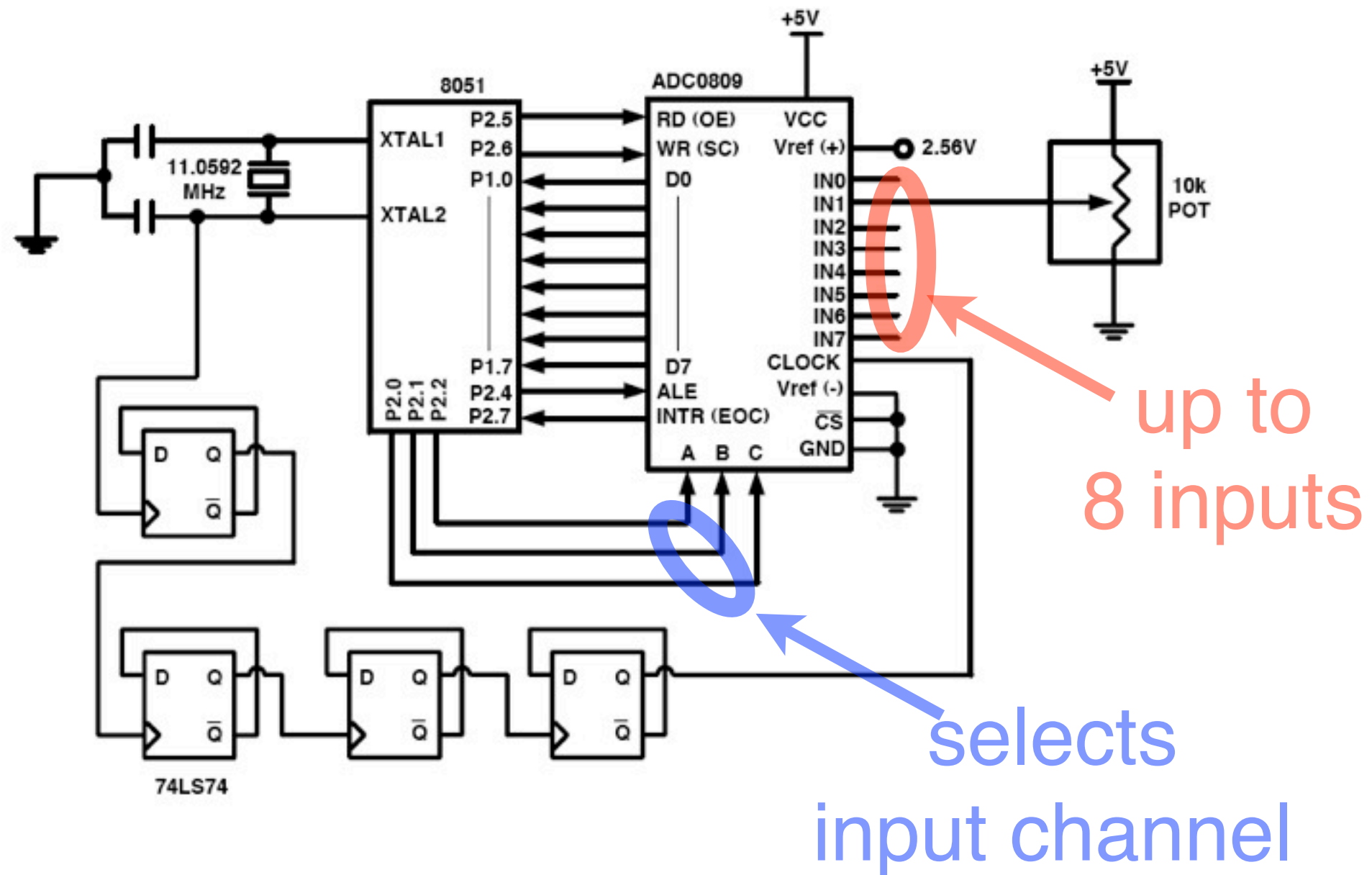
1. set ADDR,
pulse ALE

2. pulse SC,
wait for EOC

3. read data
during OE

ADDR is formed by C B A

Schematic for 8051 connected to ADC0809



Reference voltages

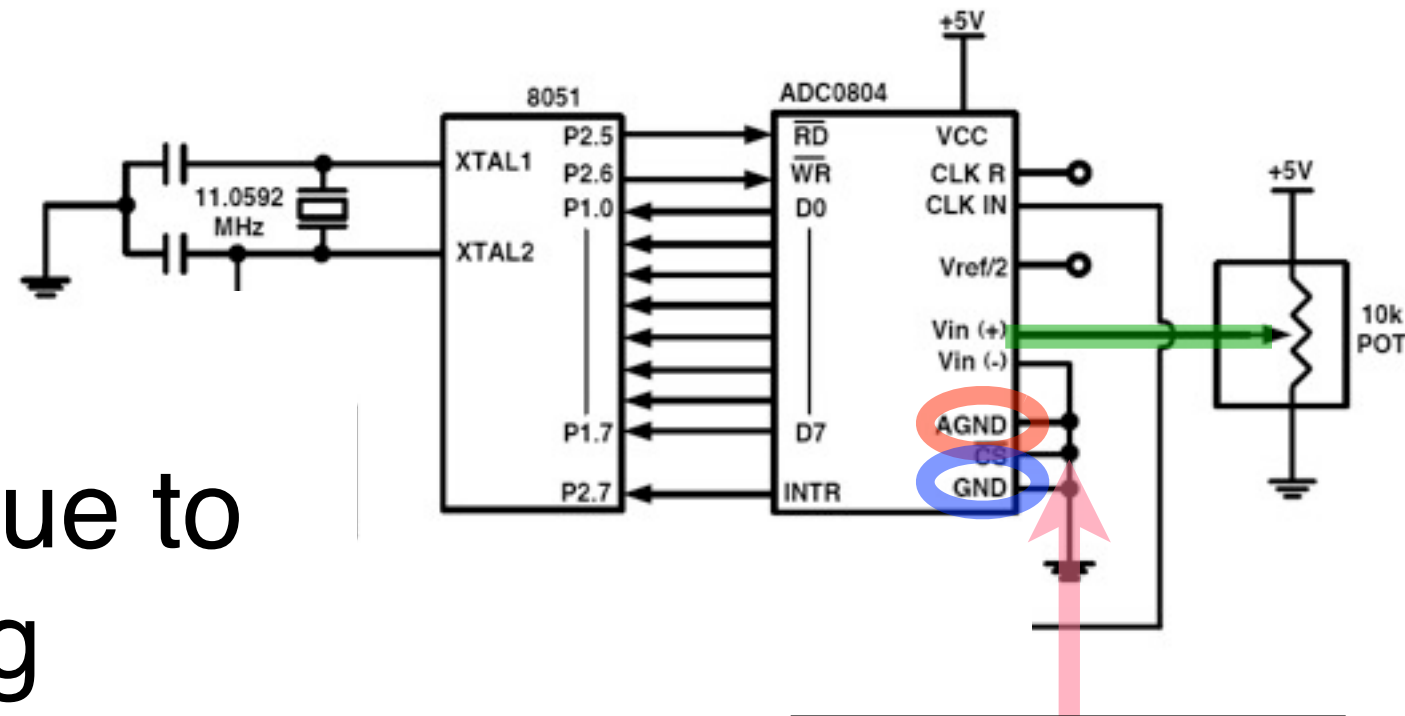
- $V_{\text{ref}}/2$ (*e.g.*, ADC0804): half the max voltage
e.g., $V_{\text{ref}}/2=2.5\text{V} \Rightarrow \text{max voltage} = 5.0\text{V}$
 \Rightarrow each step is $5.0\text{V} / 2^8 = 19.53\text{mV}$
- Assumes same GND as signal source
- $V_{\text{ref}}(+)$, $V_{\text{ref}}(-)$ differential pair (*e.g.*, ADC0808/9)
 - $V_{\text{ref}}(-)$ serves as GND for signal source
possible to tie $V_{\text{ref}}(-)$ to same GND
 - voltage step = $(V_{\text{ref}}(+)-V_{\text{ref}}(-)) / 2^8$

Single-ended vs Differential Pair input

- Single ended: relative to (common) GND
 - Problem: ground noise, $\sim 10\text{mV}$
- Differential pair: $V_{in}(+)$, $V_{in}(-)$
 - Advantages: no ground noise, also "common mode noise rejection"
- More info: http://www.eettaiwan.com/ARTICLES/2002MAR/PDF/2002MAR01_AMD_DSP_AN53.PDF

Digital vs Analog Ground

- **AGND**: analog
- **GND**: digital
- Digital => noisy due to frequent switching
- Analog: sensitive to noise
- Solution: separate AGND & GND
- Keep analog signal lines short



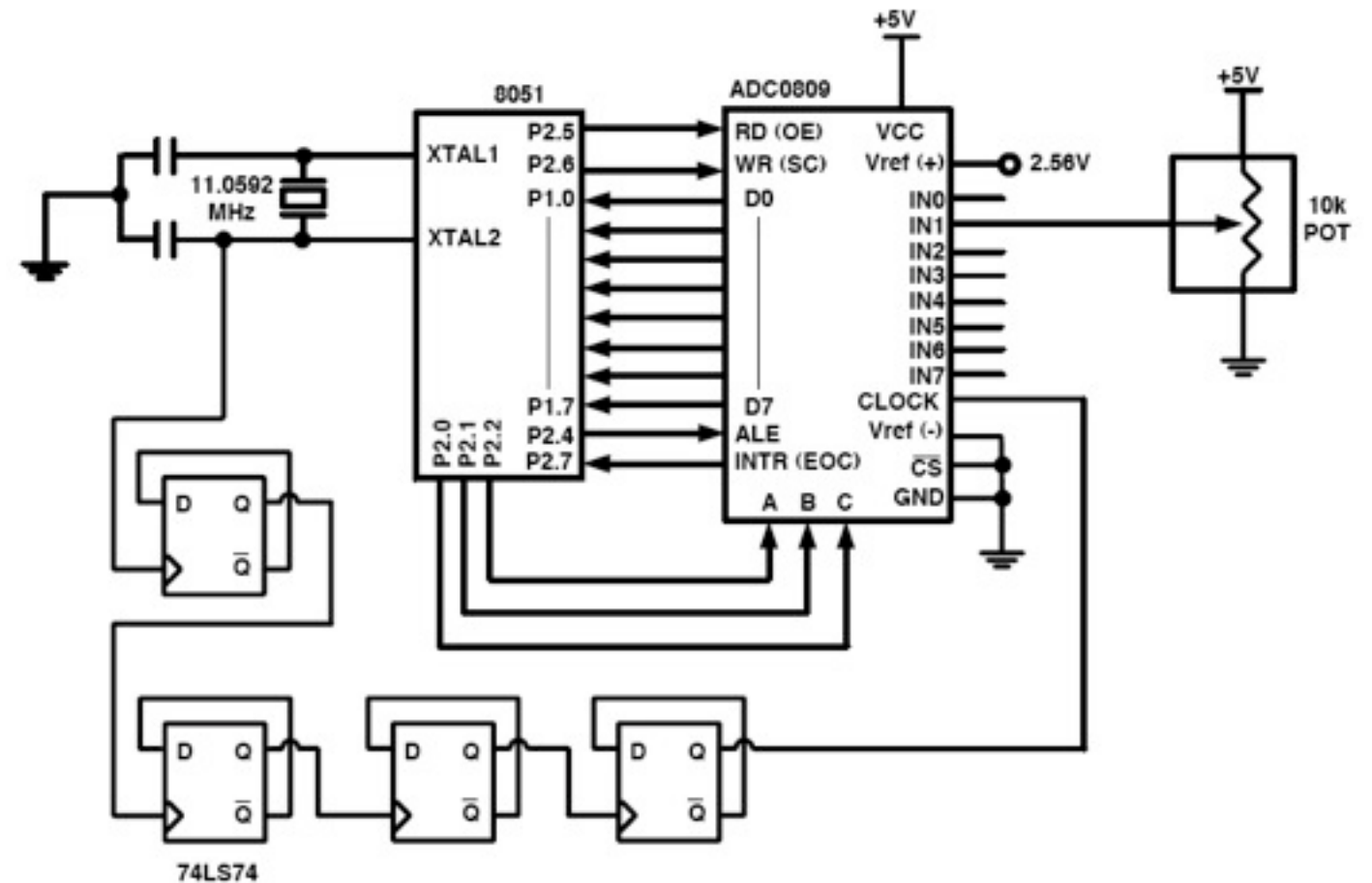
bad idea
to tie them
together!

Assembly for ADC0809

ALE	BIT	P2.4
OE	BIT	P2.5
SC	BIT	P2.6
EOC	BIT	P2.7
ADDR_A	BIT	P2.0
ADDR_B	BIT	P2.1
ADDR_C	BIT	P2.2
MYDATA	EQU	P1

```

ORG 0H
SETB EOC    ;; input
CLR  ALE
CLR  SC
CLR  OE
    
```



Assembly for ADC0809

```

BACK: CLR   ADDR_C
      CLR   ADDR_B
      SETB  ADDR_A
      ACALL DELAY
      SETB  ALE
      ACALL DELAY
      SETB  SC
      ACALL DELAY
      CLR   ALE
      CLR   SC
    
```

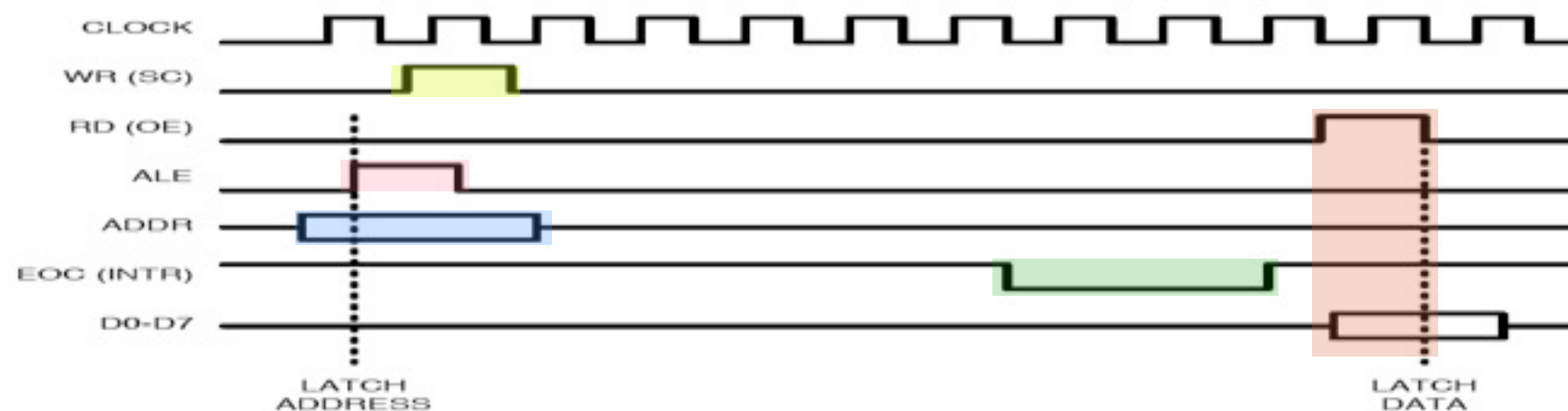
;; sel ch=1

;; latch addr

;; start

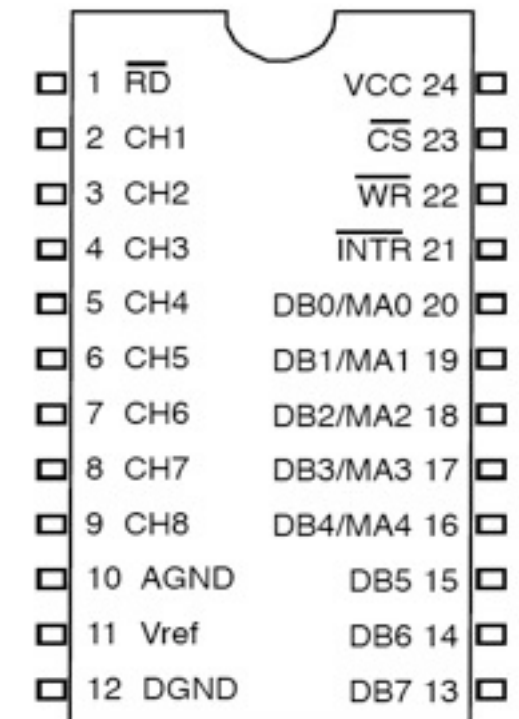
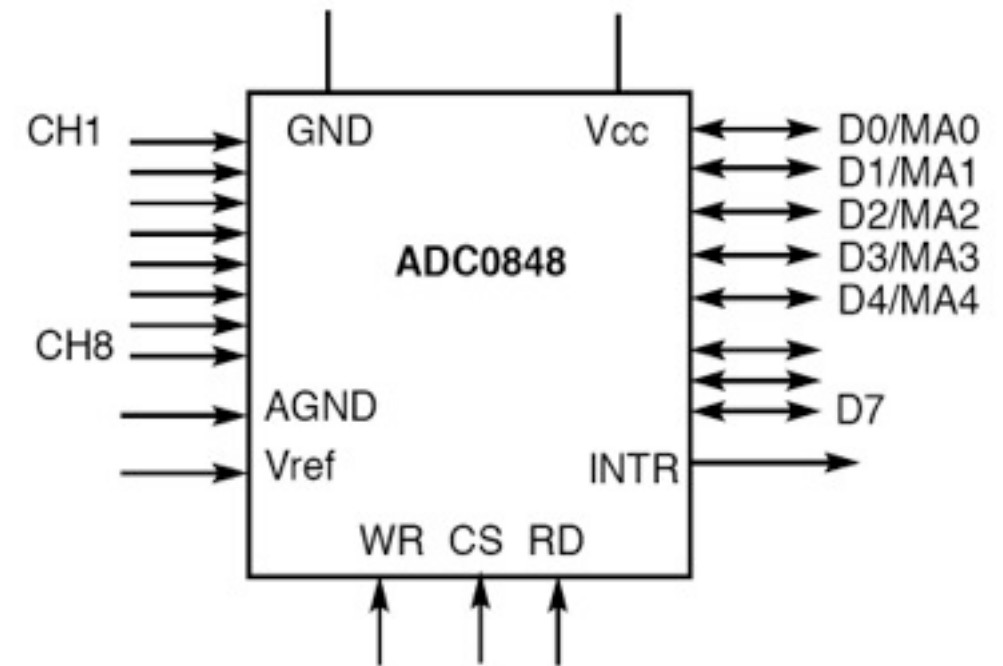
```

HERE: JB   EOC, HERE
HERE1: JNB  EOC, HERE1
      SETB  OE
      ACALL DELAY
      MOV   A, MYDATA
      CLR   OE
      ACALL CONVERSION
      ACALL DATA_DISPLAY
      SJMP  BACK
    
```



ADC0848: 8-channel ADC

- /CS: Chip select
- /RD: Read /WR: Write
- Vref: reference voltage
- DB0-DB7
- MA0 - MA4: multiplexed address
- CH1 - CH8: analog inputs
- /INTR: end-of-conversion



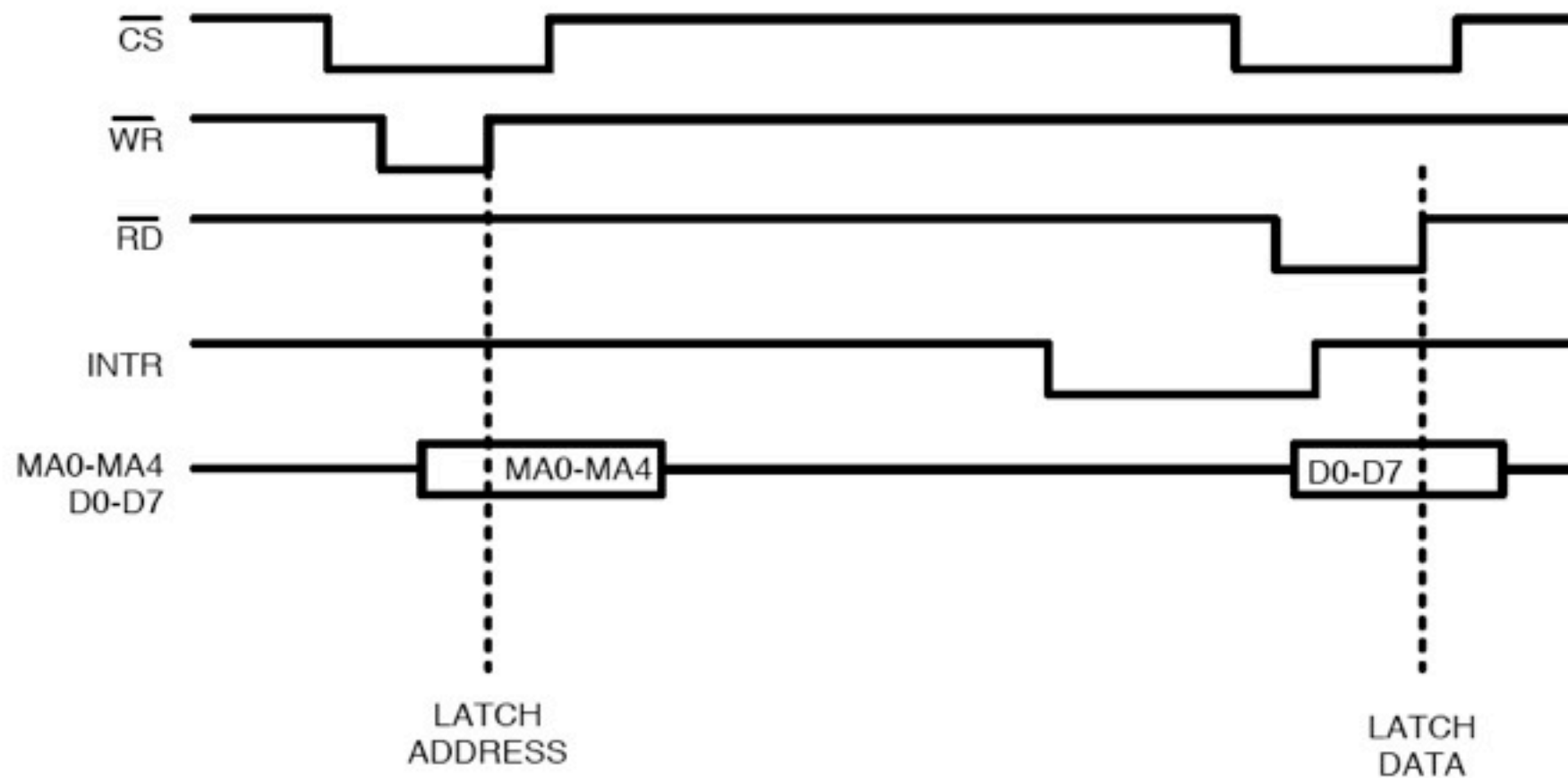
Channel selection

Mode	Chan	MA4	MA3	MA2..0
single ended	1	0	1	0

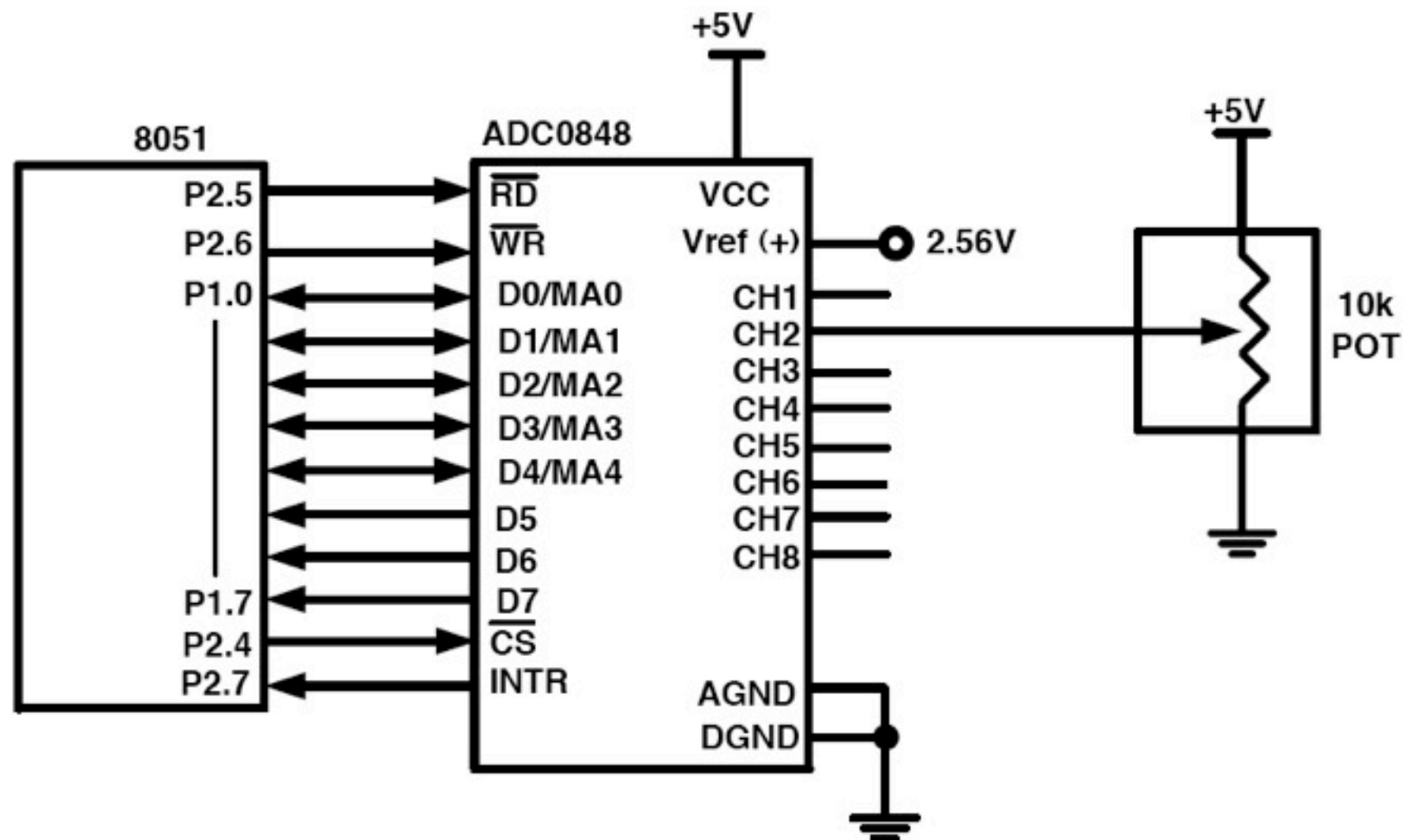
	8			111
differ- ential	CH1(+),CH2(-)	don't care	0	?

	CH7(+), CH8(-)			?

Timing Diagram for ADC0848

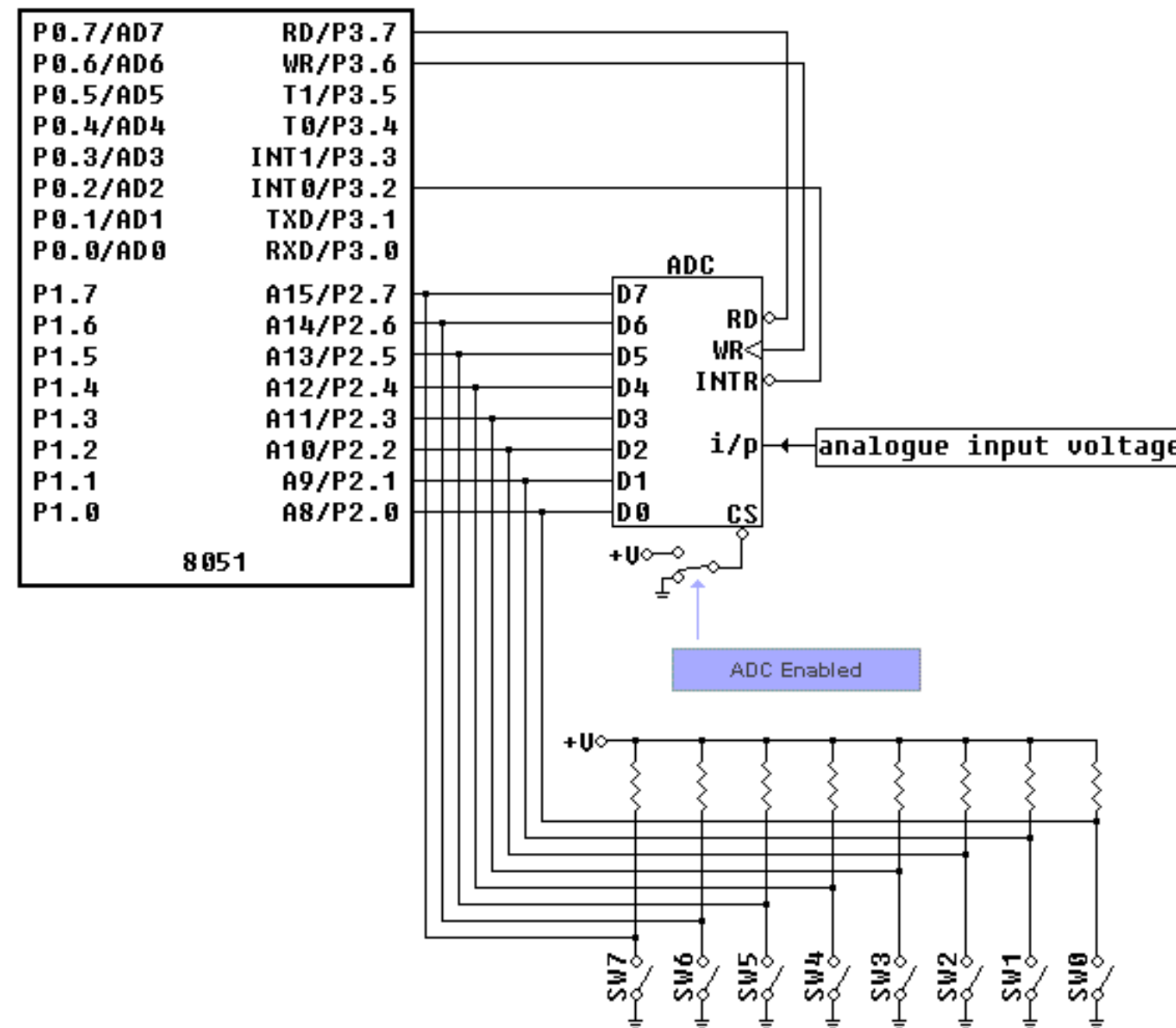


Connection of ADC8048 to 8051



8-bit ADC on EdSim

- /CS always asserted
- /INTR interrupts MCU upon finishing conversion
- WR to start conversion
- /RD to output
- D7-D0: digital data

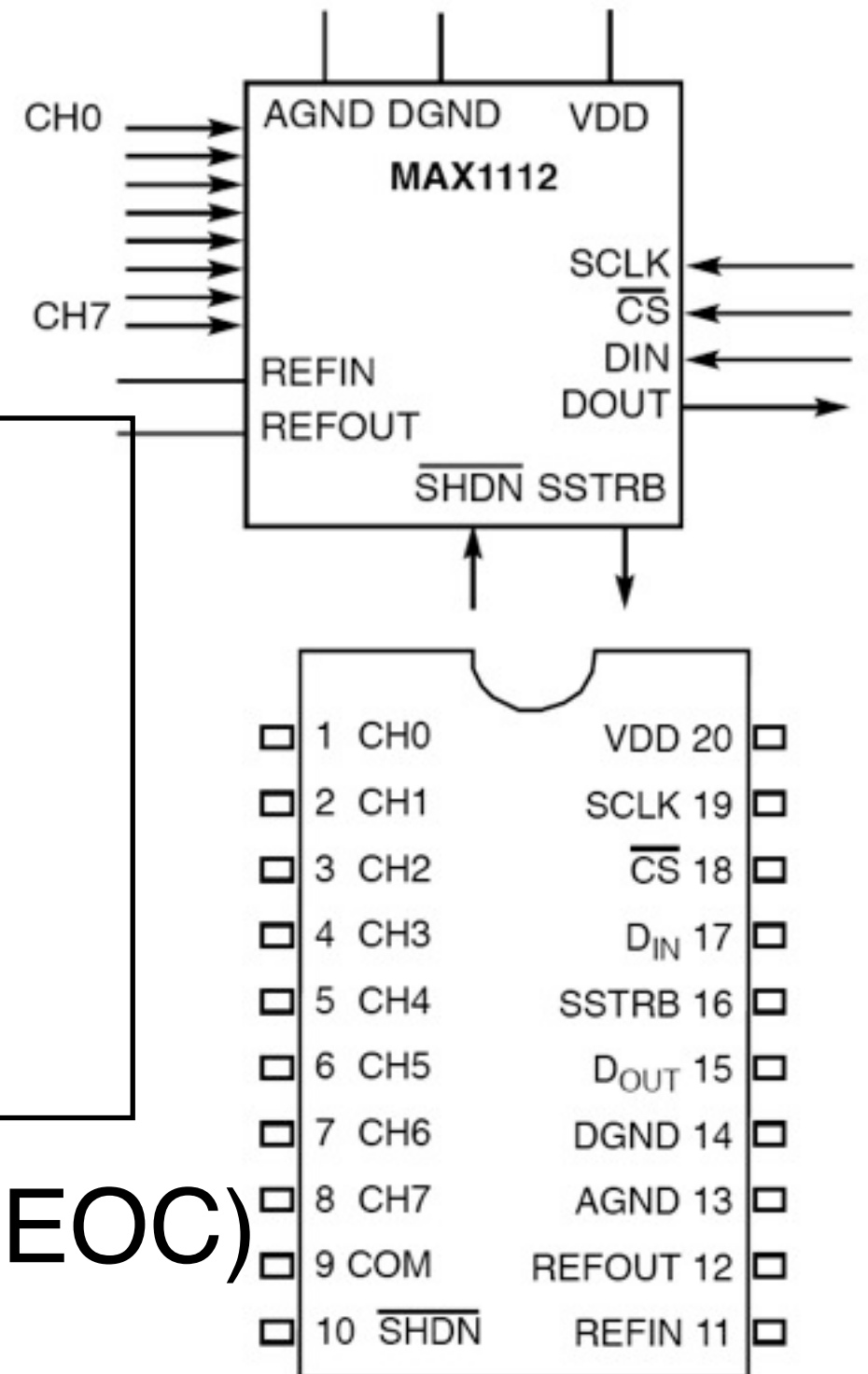


MAX 1112: Serial ADC

Looks familiar?

- COM: analog GND for single-ended

- /CS: chip select
- SCLK: serial clock (input)
- Dout: serial data out
- Din: serial data in
- SSTRB: serial strobe out (EOC)



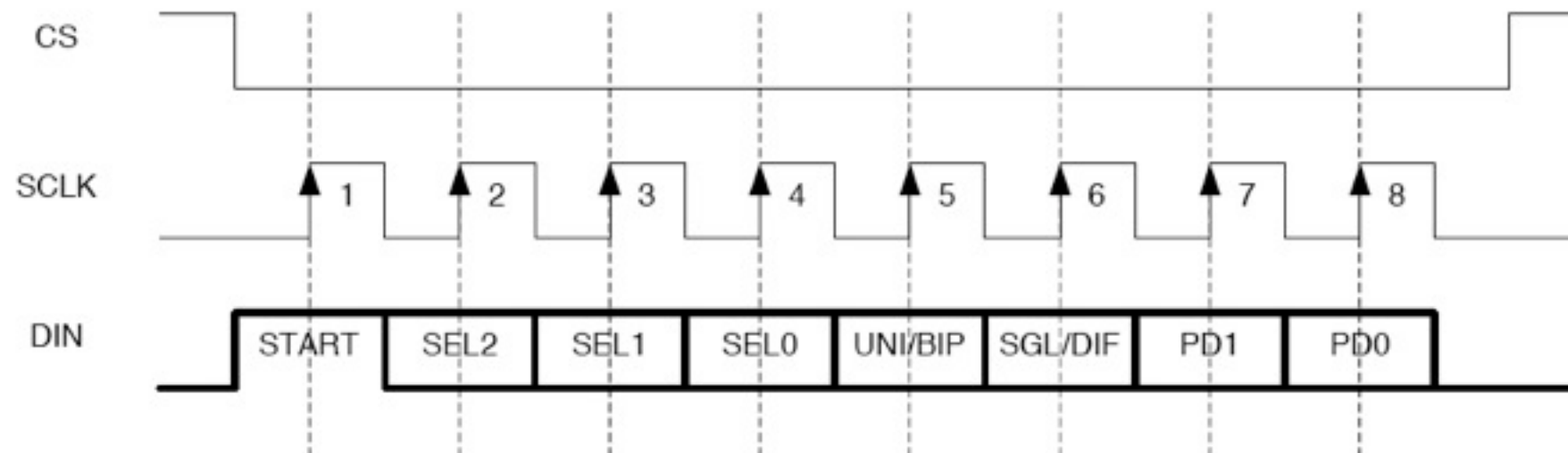
<http://datasheets.maximintegrated.com/en/ds/MAX1112-MAX1113.pdf>

More pins of MAX 1112

- /SHDN: shutdown
- REFIN: reference voltage input
- REFOUT: internal reference voltage output
- VCOM: 0V for unipolar, $V_{ref}/2$ for bipolar
- AGND, DGND: analog/digital ground
 - Note: AGND is for MAX112, whereas COM is for signal's GND (unrelated to AGND)

Configure MAX 1112: send Control Byte

- unipolar or bipolar
- Single-ended or Differential
- power-down or operational
- external clock or internal clock



Format of Control Byte

Start	SEL2	SEL1	SEL0	UN/BIP	SGL/DF	PD1	PD0
-------	------	------	------	--------	--------	-----	-----

Start The MSB (D7) must be high to define the beginning of the control byte. It must be sent in first.

SEL2 SEL1 SEL0 CHANNEL SELECTION (SINGLE-ENDED MODE)

0	0	0	CHAN0
0	0	1	CHAN1
0	1	0	CHAN2
0	1	1	CHAN3
1	0	0	CHAN4
1	0	1	CHAN5
1	1	0	CHAN6
1	1	1	CHAN7

UNI/BIP 1 = unipolar: Digital data output is binary 00 - FFH.

0 = bipolar: Digital data output is in 2's complement.

SGL/DIF 1 = single-ended: 8 channels of single-ended with COM as reference

0 = differential: Two channels (eg., CH0 - CH1) are differential.

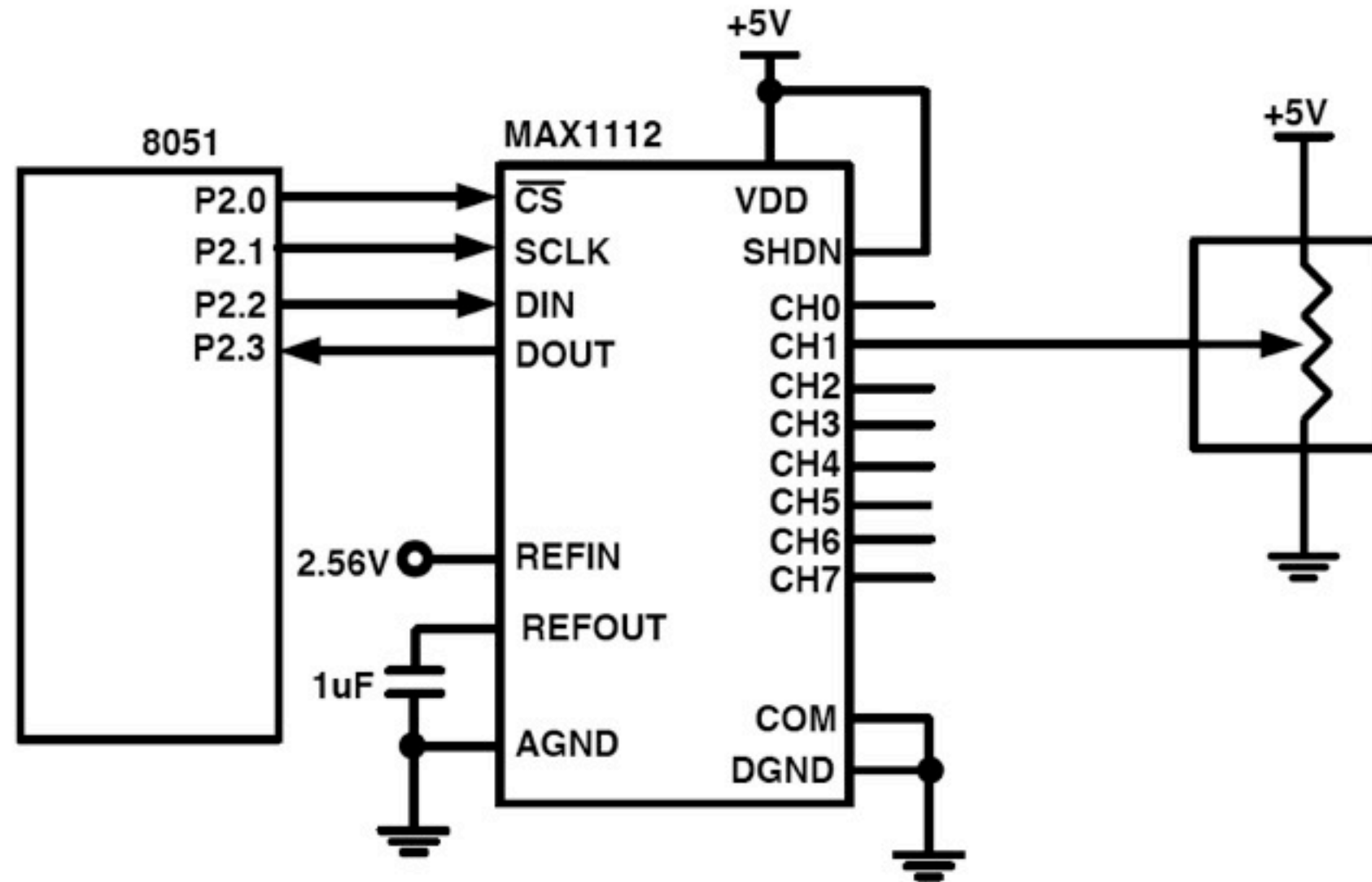
PD1 1 = fully operational

0 = power-down: Power down to save power using software.

PD0 1 = external clock mode: The conversion speed is dictated by SCLK.

0 = internal clock mode: The conversion speed is dictated internally, and the SSTRB pin goes high to indicate end-of-conversion (EOC).

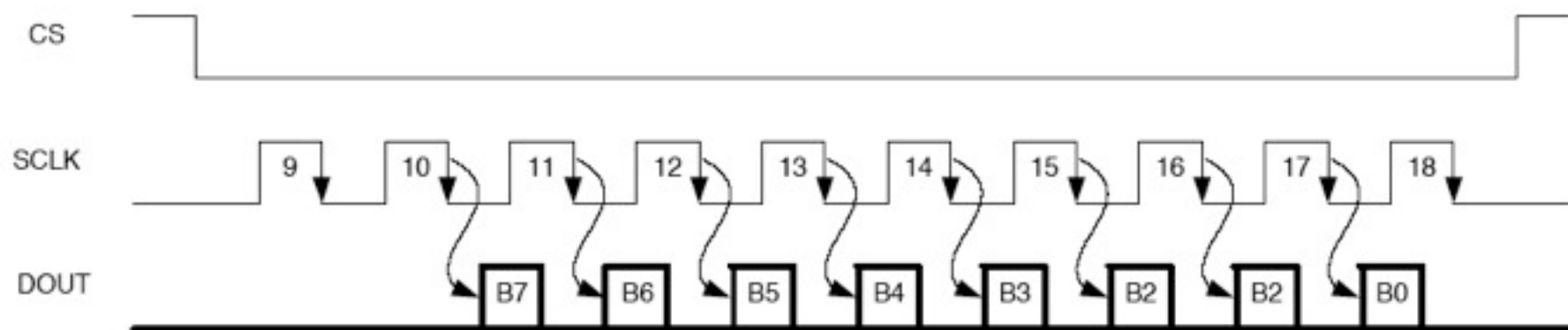
Connecting MAX 1112 to 8051



essentially SPI port!
emulated using GPIO if hardware SPI not available

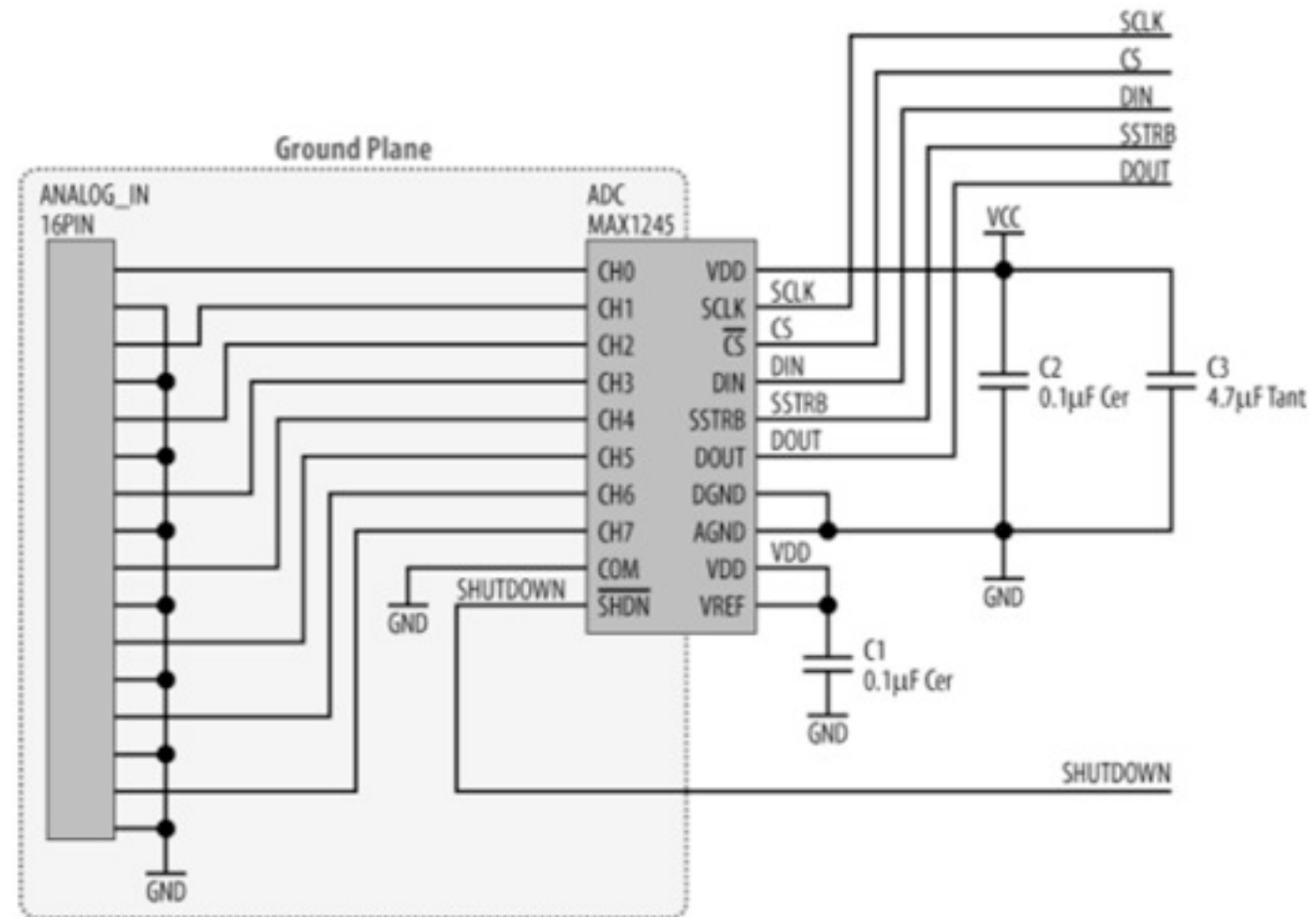
Read cycle: extra SCLK pulse

MAX1112 Internal Clock Mode Timing Diagram
Reading Data ADC Byte From MAX1112



Ex: Max1245 ADC

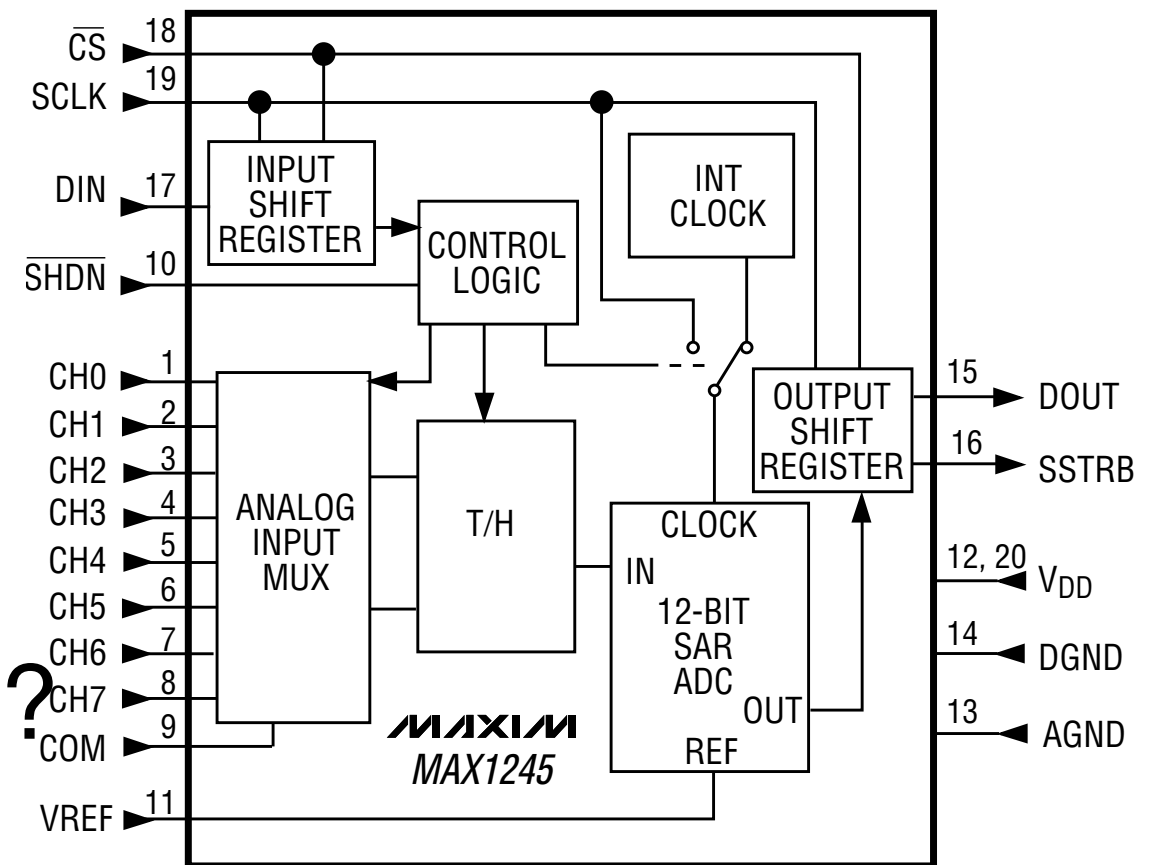
- SPI, 8 channels
- 12 bits, up to 100k sps ($7.5\mu\text{s}$ conv time)
- track-and-hold type (aka sample & hold) unipolar or bipolar input
- Ground sep. betw. input lines



<http://datasheets.maxim-ic.com/en/ds/MAX1245.pdf>

Detailed Description

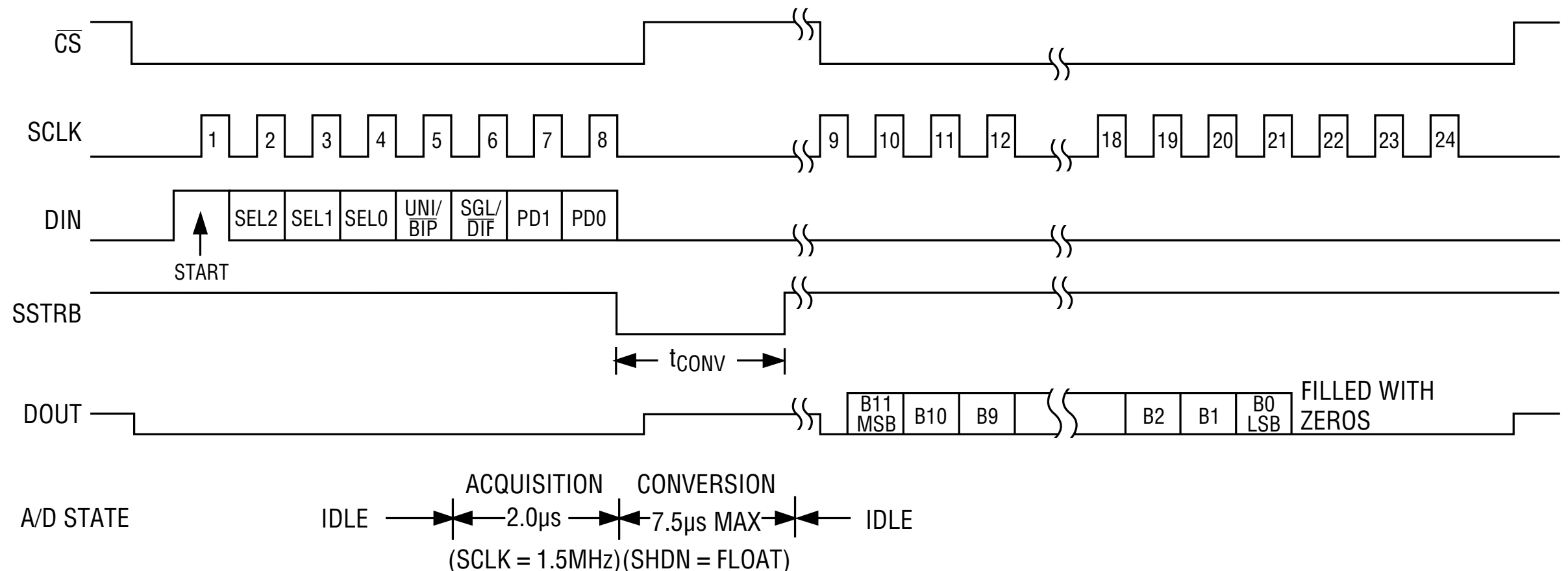
- Single-ended: 0 to Vref
- pseudo-differential:
-Vref/2 to +Vref/2
- What's pseudo-differential?
- only IN+ is sampled
- IN- must remain stable w.r.t. AGND during conv.



- Control byte:
bit7 = start,
bits6..4 = channel,
bit3=unipolar or bipolar
bit2=single ended or dif
bit 1..0=mode

Basic Transaction

- Send control byte, ignore received byte
- Clock in all 0s byte, get higher-order byte
- Clock in all 0s byte, get lower-order byte

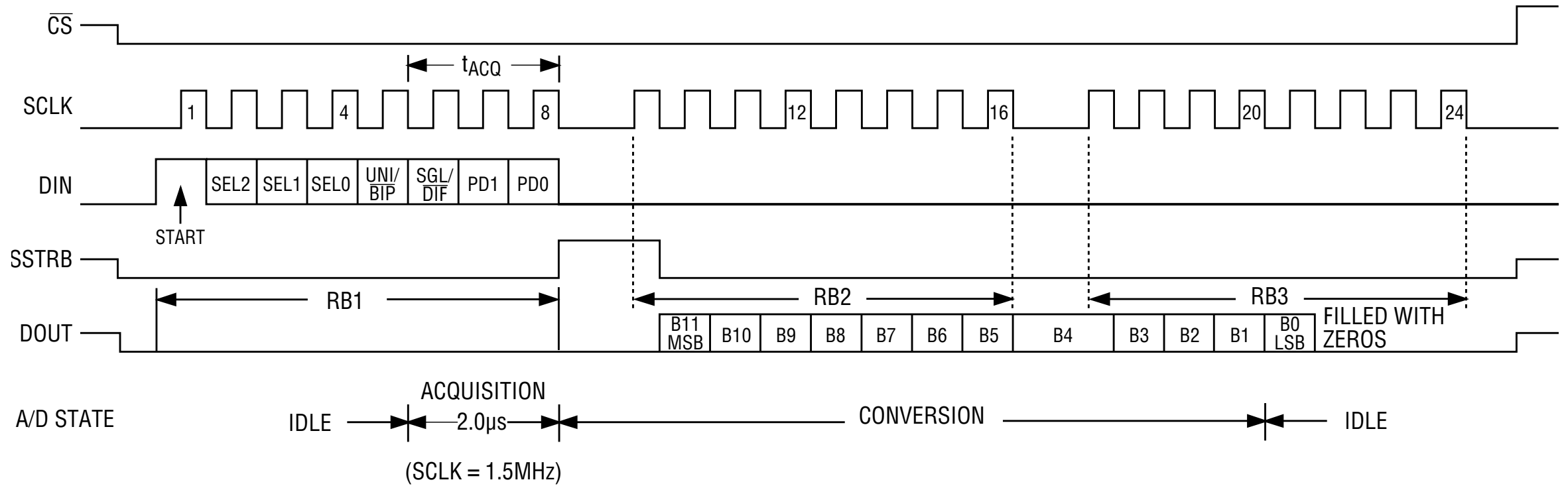


Clock options of Max 1245

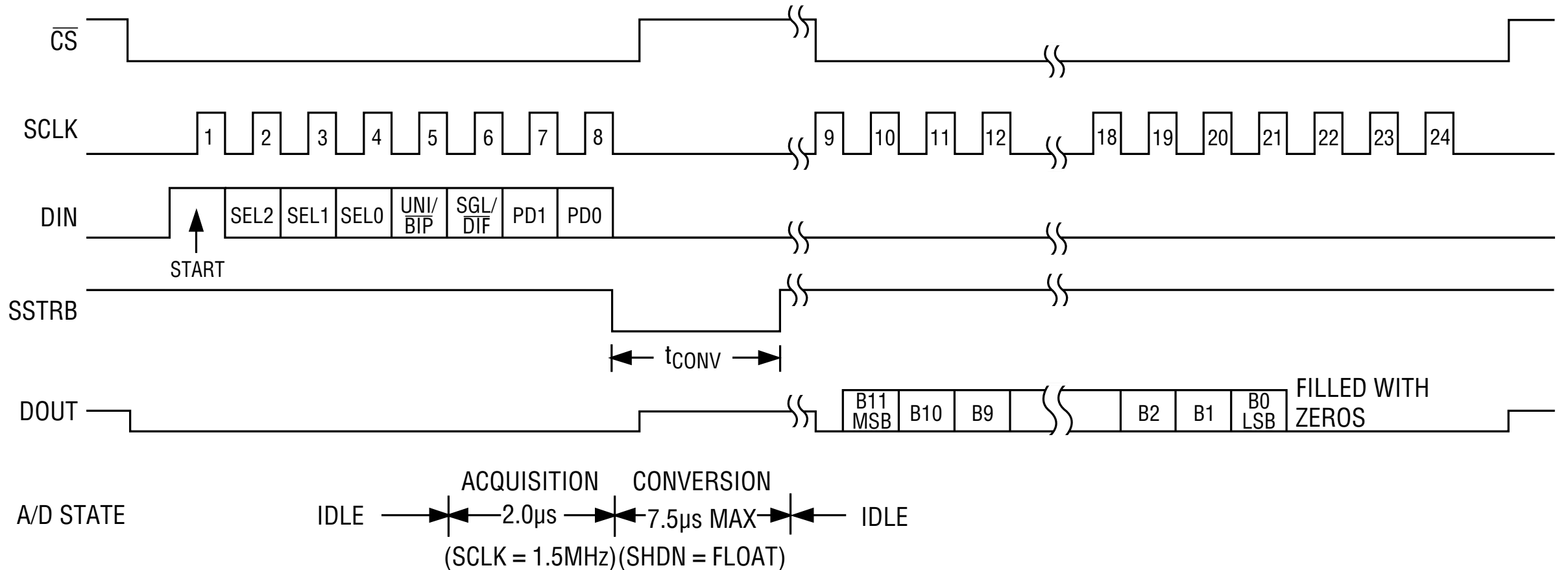
- Internal clock option
 - 1.5 MHz or 225 KHz
- External clock option
 - mode uses SPI SCLK as conversion clock!
 - SSTRB: data ready (can be an interrupt)
 - Clock can't be too slow or else capacitor loses value (for track-and-hold)

External vs. Internal clk

External

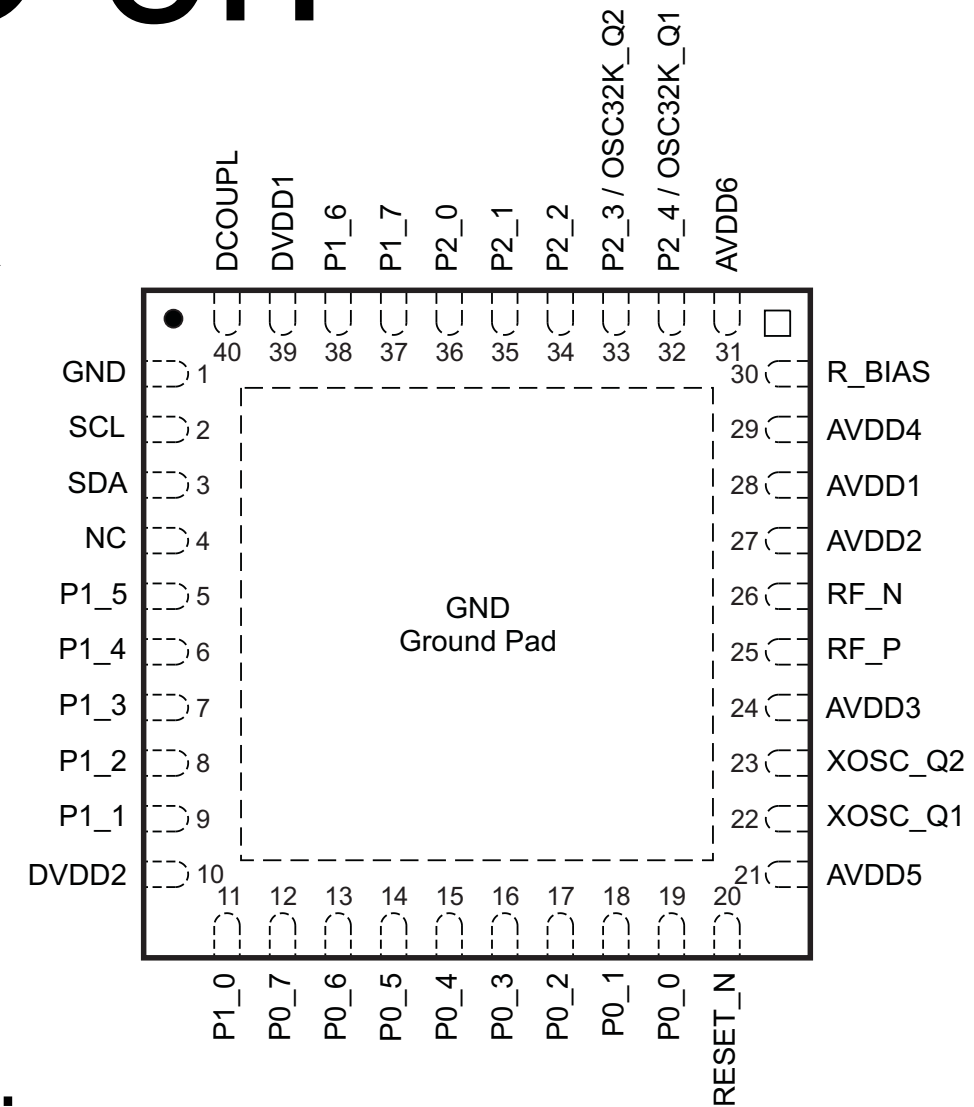


Internal



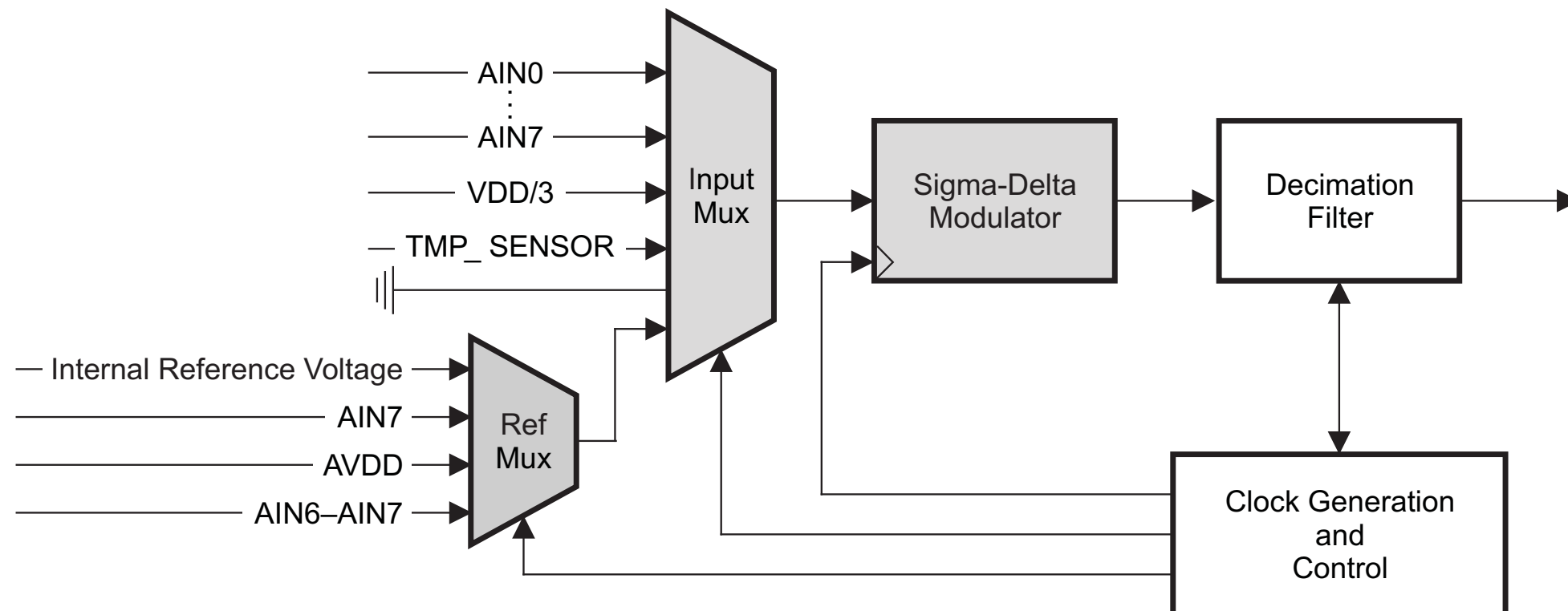
Built-in ADC on CC254x

- Input pins:
A7-0 same as P0.7-0.0
- T = ADC trigger
- SFR: APCFG (analog peripheral configuration)
- Single ended or differential pair



Periphery/ Function	P0								P1								P2				
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	4	3	2	1	0
ADC	A7	A6	A5	A4	A3	A2	A1	A0													T
Operational amplifier						O	-	+													
Analog comparator			+	-																	

Using Built-in ADC on CC254x



Register Name	SFR Address	Module	Description
ADCCON1	0xB4	ADC	ADC control 1
ADCCON2	0xB5	ADC	ADC control 2
ADCCON3	0xB6	ADC	ADC control 3
ADCL	0xBA	ADC	ADC data low
ADCH	0xBB	ADC	ADC data high
RNDL	0xBC	ADC	Random number generator data low
RNDH	0xBD	ADC	Random number generator data high

Using built-in ADC of CC254x

- Channels 0-7: single-ended
- Channels 8-11: differential inputs
- Channel 12: GND
- Channel 13: Reserved
- Channel 14: on-chip temperature sensor as input
 - Configure TR0.ADCTM and ATEST.ATESTCTRL bits
- Channel 15: AVDD5/3 as input
 - Can implement battery monitor

Using ADC of CC254x

- ADCCON1.EOC
 - '1' when end-of-conversion, '0' when ADCH read
- ADCCON1.ST
 - set to starts conversion, auto cleared when completed.
- ADCCON1.STSEL: selects triggering event for ADC
 - Rising edge of P2.0
 - End of previous sequence
 - Timer 1 ch 0, or
 - ADCCON1.ST = '1'

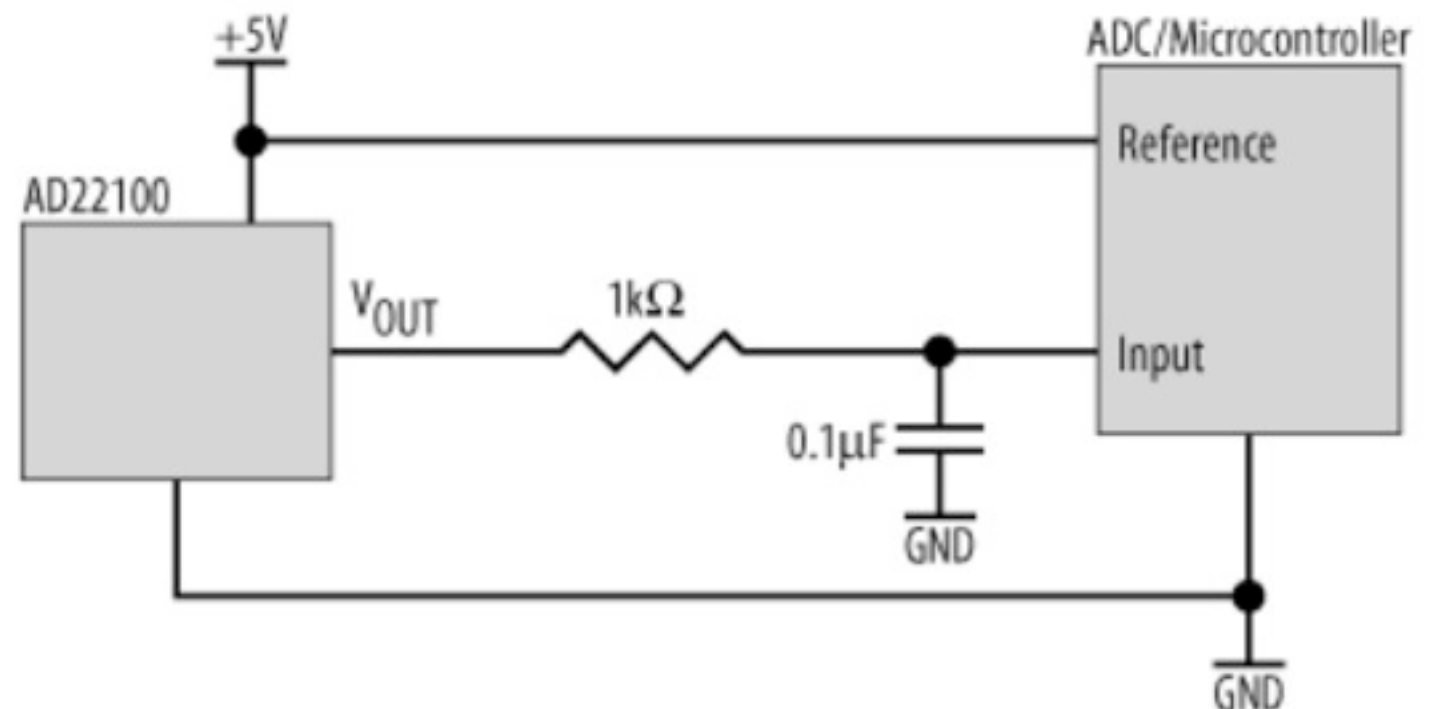
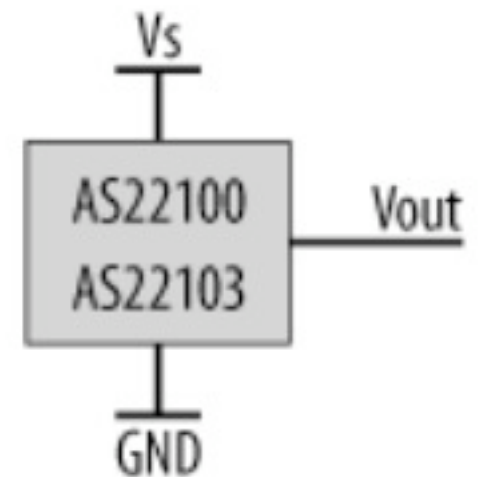
Sensors

Sensors, transducers, actuators

- Sensor
 - converts physical signal (temperature, etc) to electrical (voltage or current)
- Actuator
 - converts electrical signal to physical signal
- Transducer
 - converts one form of energy to another

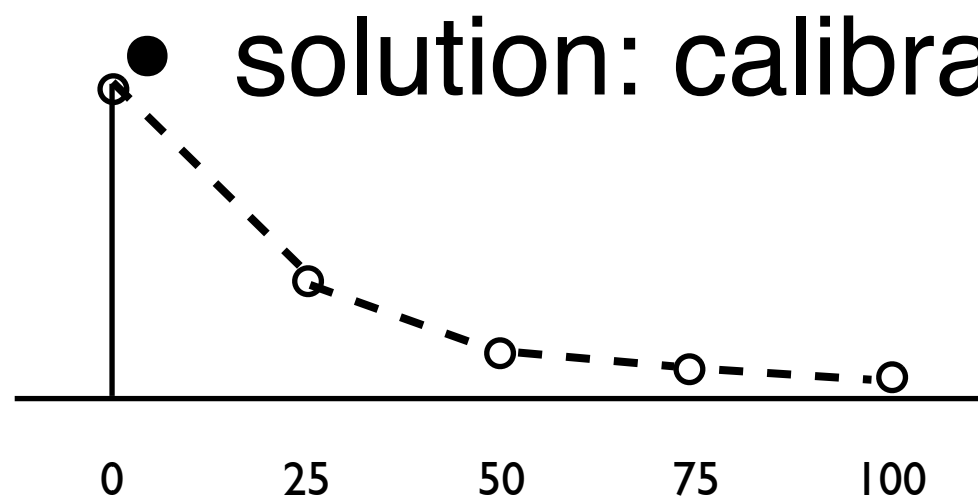
Temperature sensor

- AD 22100: -50°C to $+150^{\circ}\text{C}$
 - 3 pin device: power, gnd, Vout
 - linear in 5V range
- can add an RC filter to remove noise



Linearity

- Characteristics of transducer over its operating range
- Example: thermistor
 - varies resistance over temperature but not "linear"



Temperature (C)	Tf (K ohms)
0	29.490
25	10.000
50	3.893
75	1.700
100	0.817

From William Kleitz, *Digital Electronics*

LM34 & LM35

temperature sensors

Part	Temperature Range	Accuracy	Output
Scale			
LM34A	−50 F to +300 F	+2.0 F	10 mV/F
LM34	−50 F to +300 F	+3.0 F	10 mV/F
LM34CA	−40 F to +230 F	+2.0 F	10 mV/F
LM34C	−40 F to +230 F	+3.0 F	10 mV/F
LM34D	−32 F to +212 F	+4.0 F	10 mV/F

Note: Temperature range is in degrees Fahrenheit.

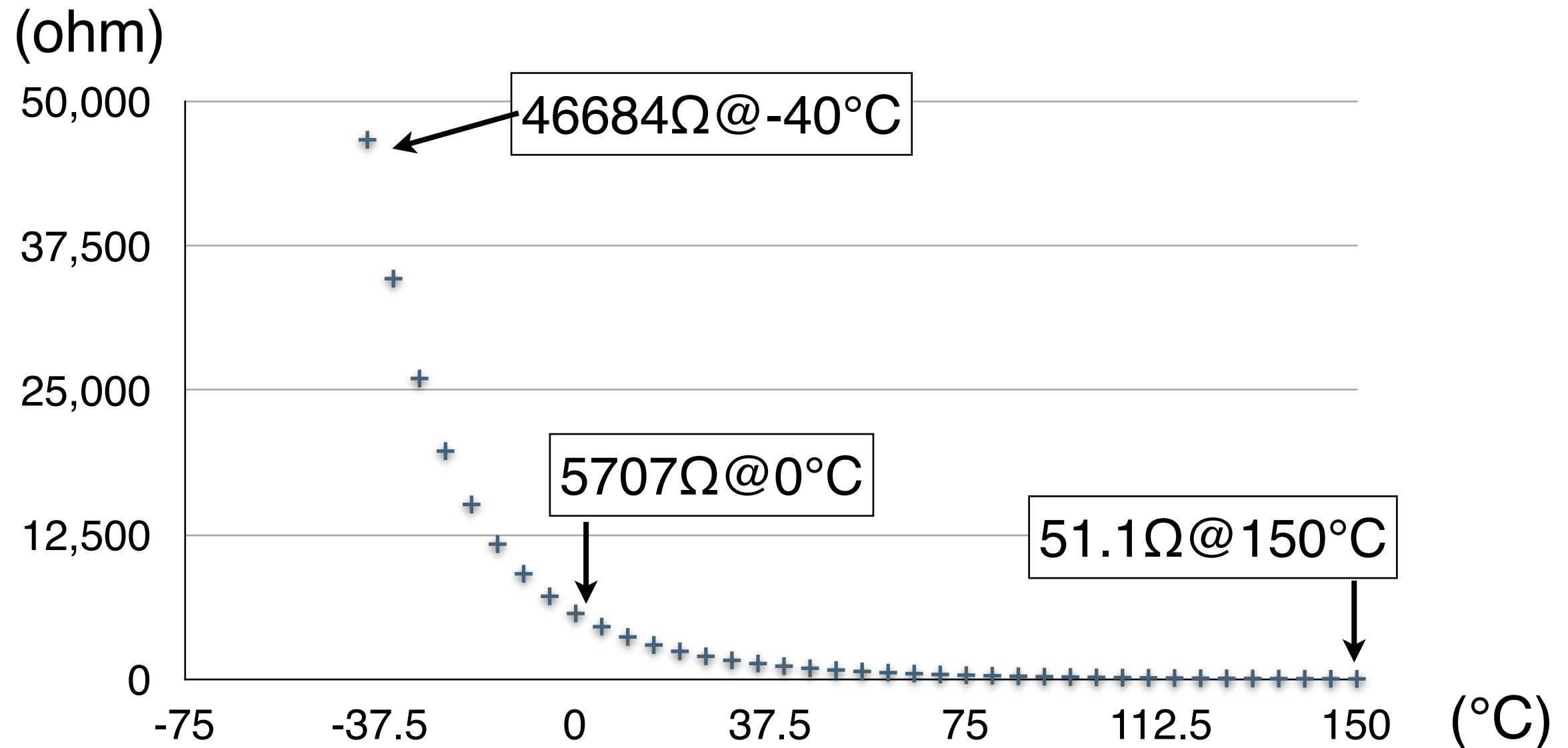
Part	Temperature Range	Accuracy	Output Scale
LM35A	−55 C to +150 C	+1.0 C	10 mV/C
LM35	−55 C to +150 C	+1.5 C	10 mV/C
LM35CA	−40 C to +110 C	+1.0 C	10 mV/C
LM35C	−40 C to +110 C	+1.5 C	10 mV/C
LM35D	0 C to +100 C	+2.0 C	10 mV/C

Note: Temperature range is in degrees Celsius.

Thermistor

- Temperature sensitive resistor
 - cheap, stable
- Problem: non-linear $\Rightarrow \sim \log$ scale
 - can distinguish low temperature more than high temperature
 - need a table or formula to remap value

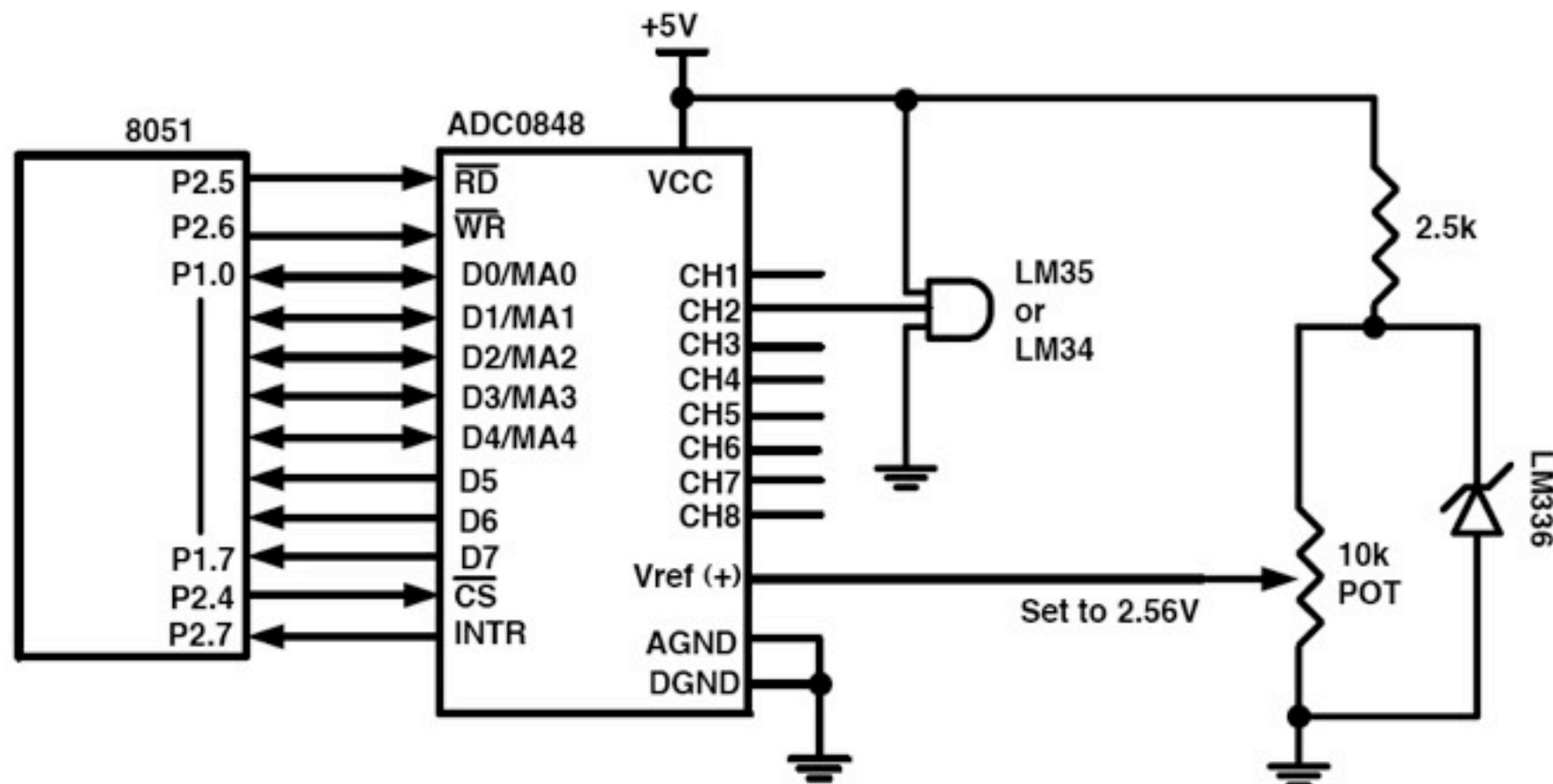
Resistance vs. Temperature plot



Data source taken from
<http://rocky.digikey.com/WebLib/BC%20Components/Web%20Data/2322%20640%205%20NTC%20Thermistors.pdf>

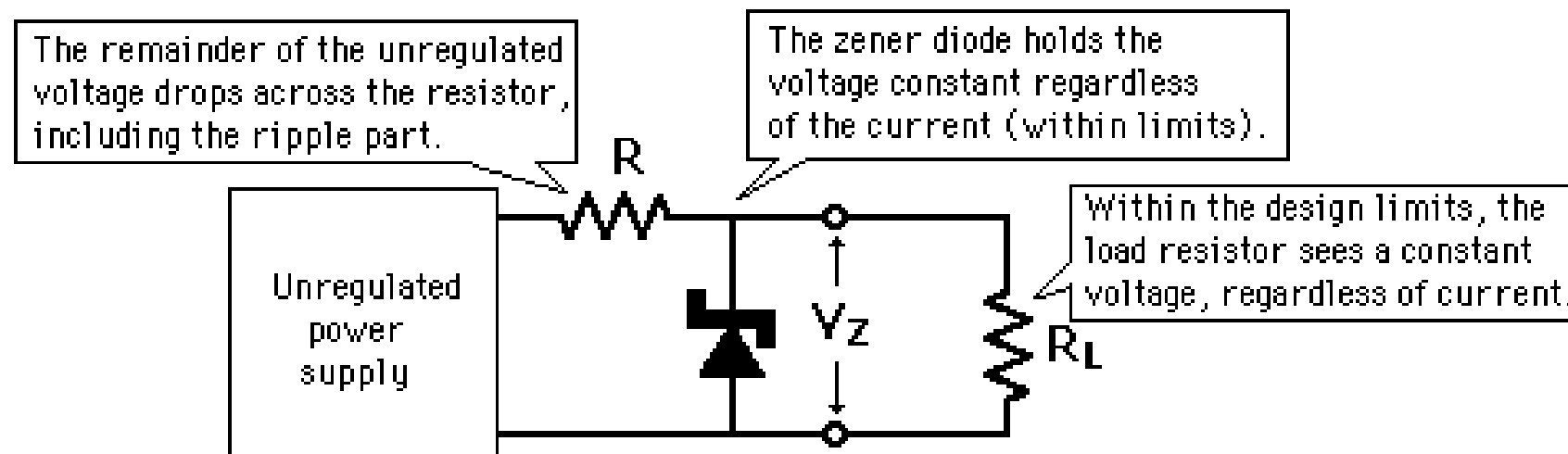
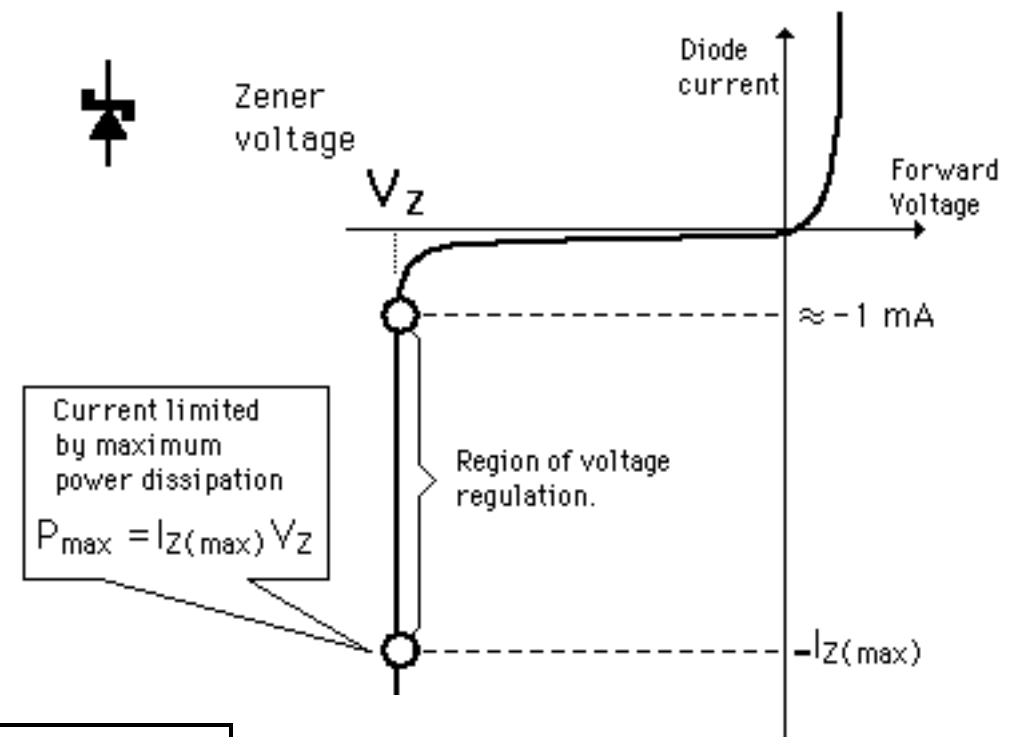
Signal Conditioning

- Step between transducer and ADC
- e.g., keep power clean for reference voltage
LM336 Zener diode keeps voltage stable



Zener diode

- in reverse voltage
- applications:
 - regulators



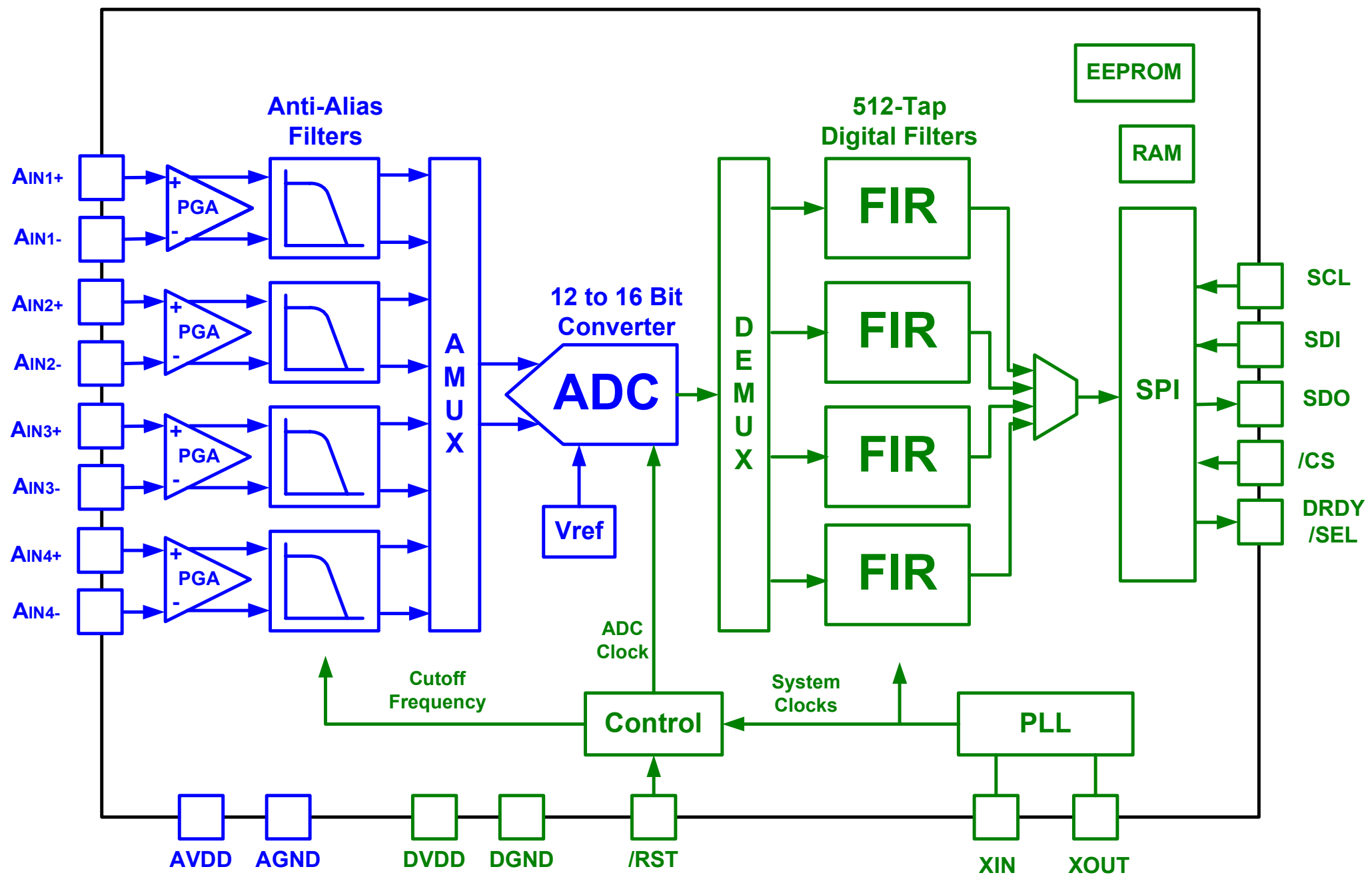
Credits: <http://hyperphysics.phy-astr.gsu.edu/hbase/solids/zener.html>

Example: QuickFilter

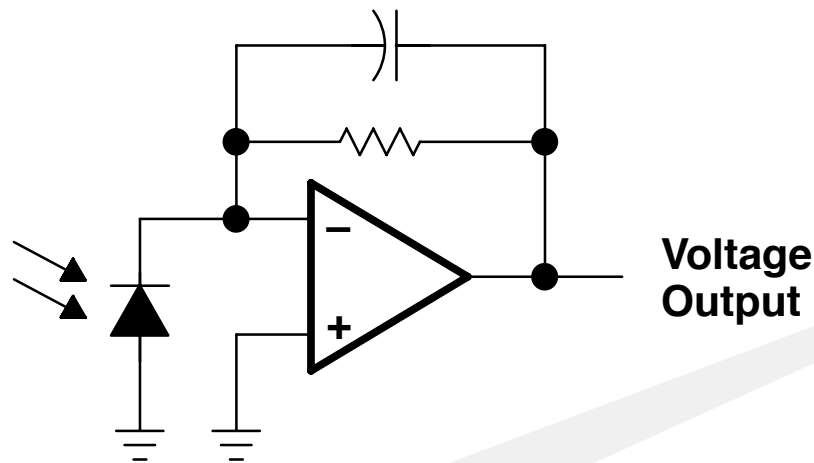
QF4A512

- Combo Signal Conditioner + ADC
 - 4-channel 16-bit ADC
 - 4 programmable gain amplifiers
 - Anti-aliasing filter per channel
 - internal Vref
 - Four 512-tap digital FIR filter
 - SPI output
- <http://www.quickfiltertech.com/files/QF4A512%20Data%20Sheet.pdf>

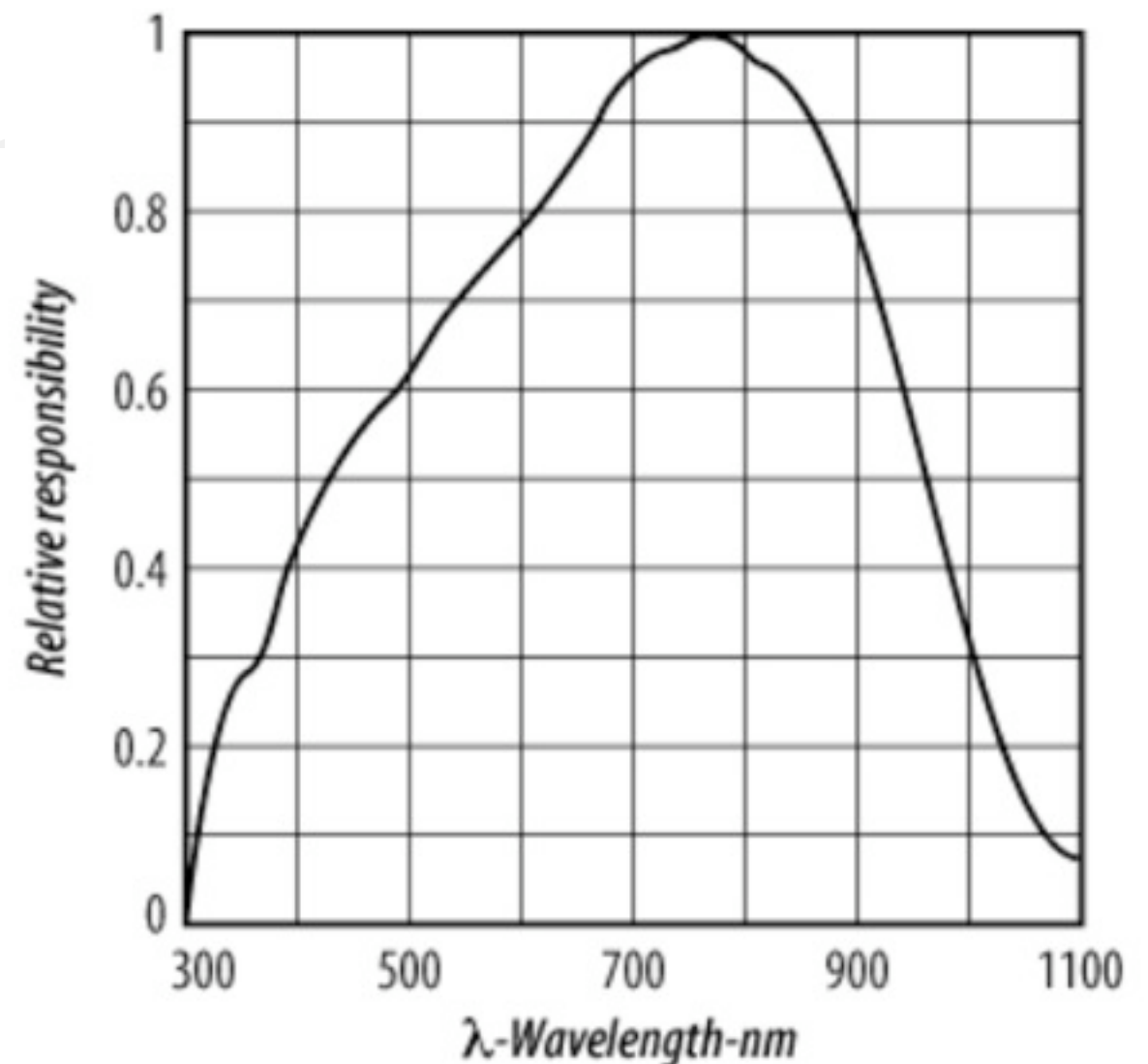
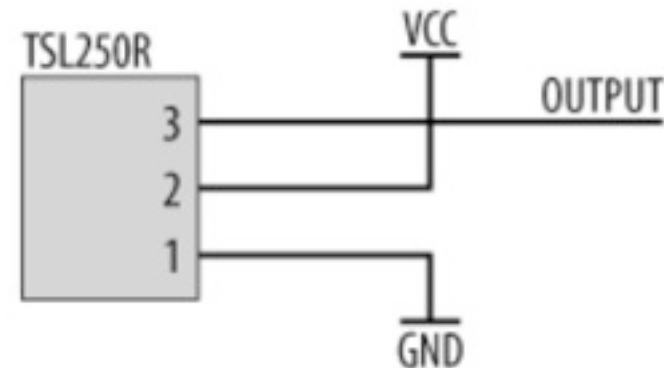
QF4A512 block diagram



Light Sensor TSL250R



- interface Similar to thermometer chip
- Vcc, GND, Vout
- responds to visible light spectrum

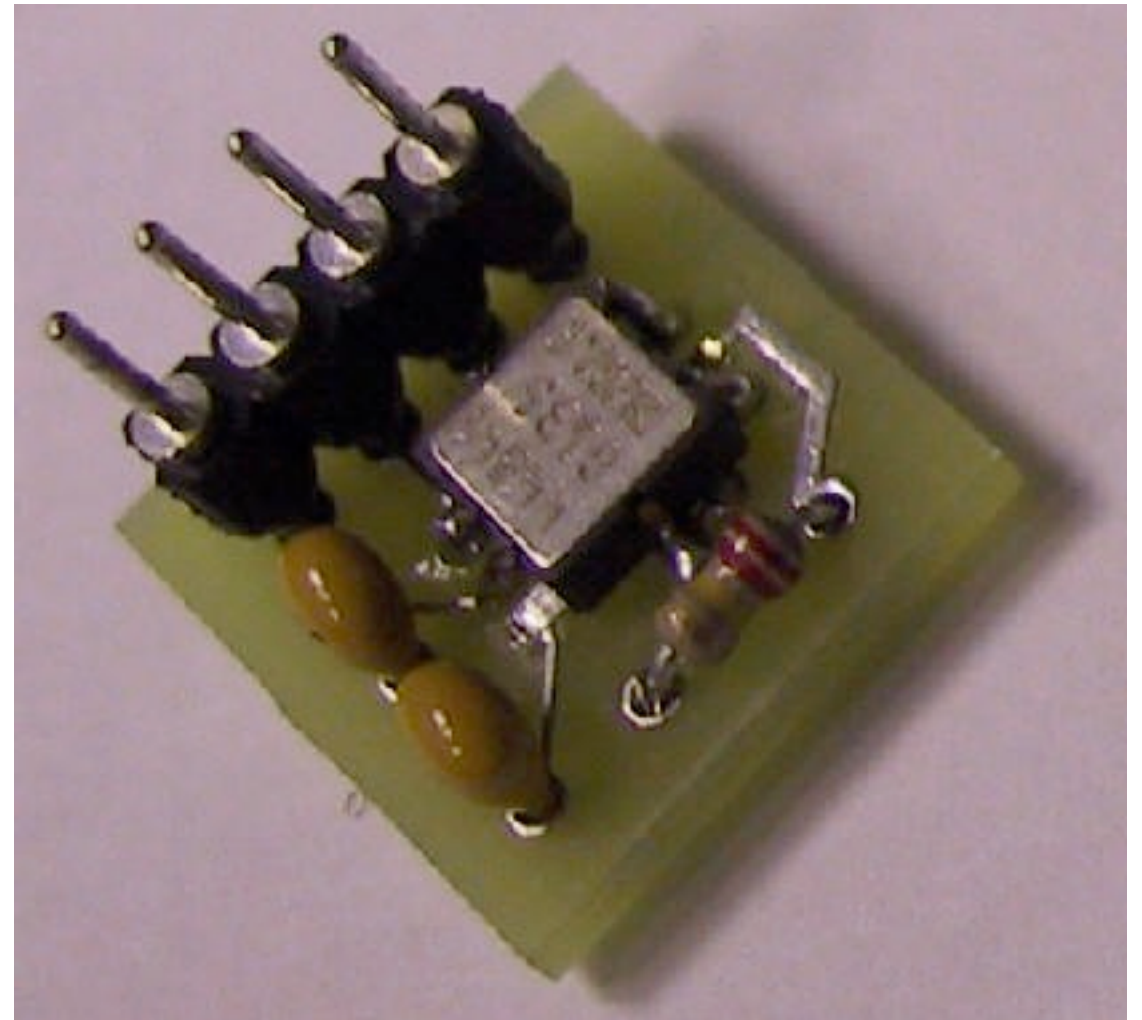


Accelerometer

- Technologies: MEMS, Piezoelectric
- Axes: 1, 2, 3
- Output types: analog, digital
- Threshold Detection
- Self Calibration

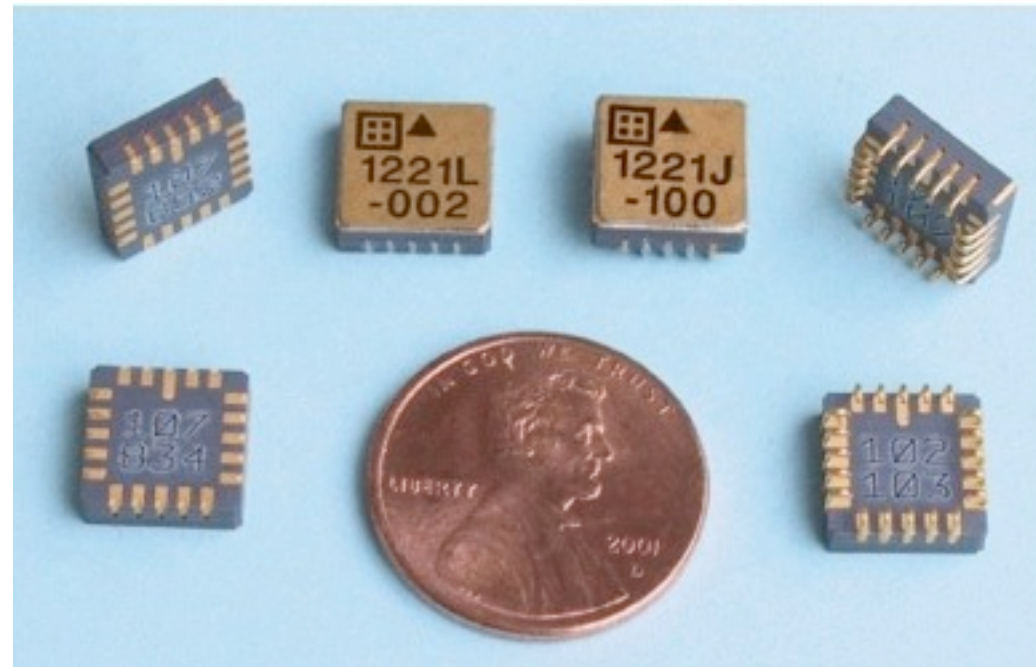
ADXL accelerometers

- ADXL 202E
 - "2" => 2-axes
- Low cost, designed for airbags
- Analog output
- Issue: drift



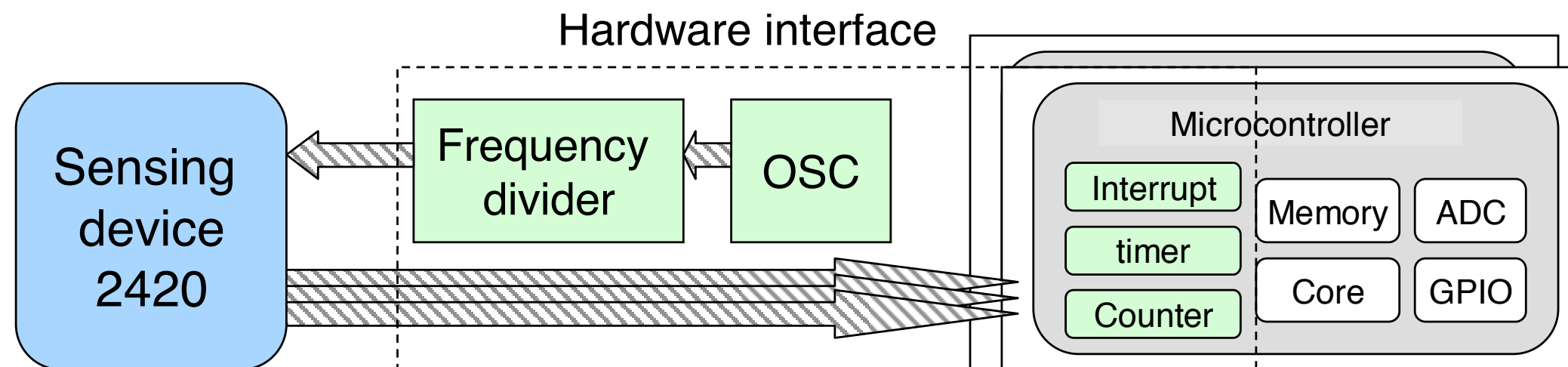
Silicon Designs accelerometer

- High accuracy
 - $\pm 2g \sim \pm 400g$,
 - DC to 200Hz
 - Self calibration
 - Expensive!
- SD 1221: Analog
- SD 2420: pulse freq



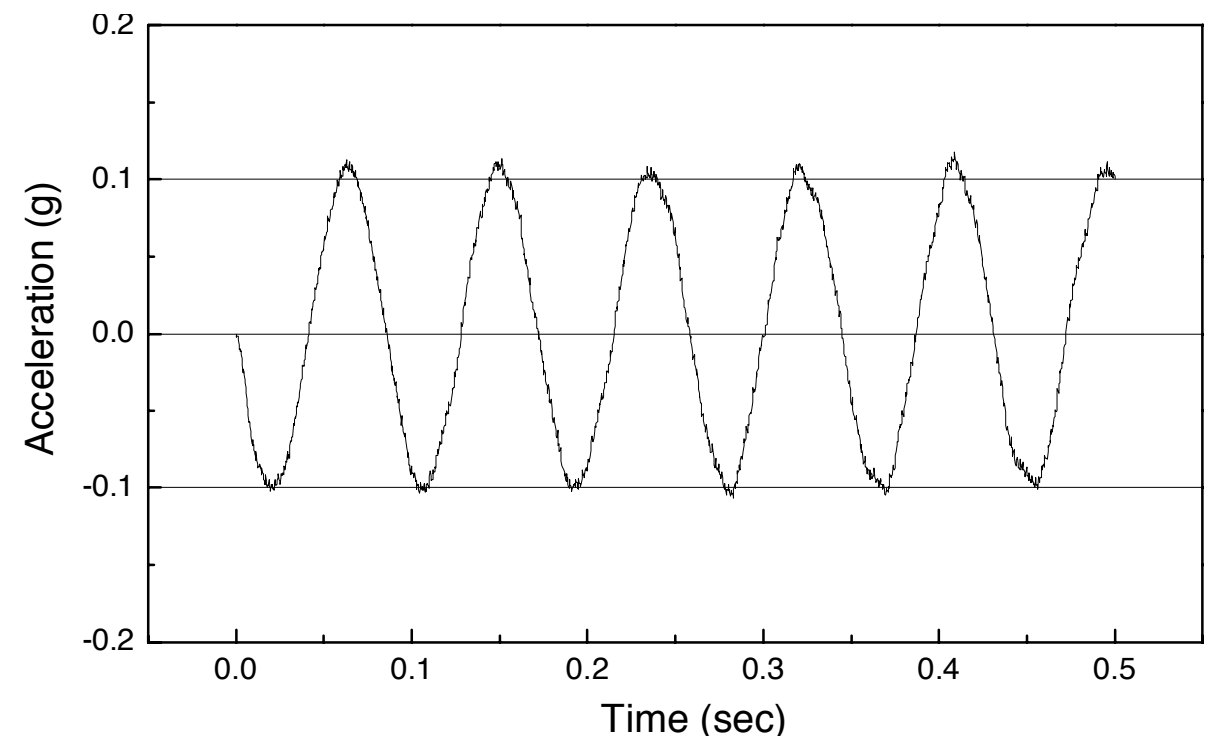
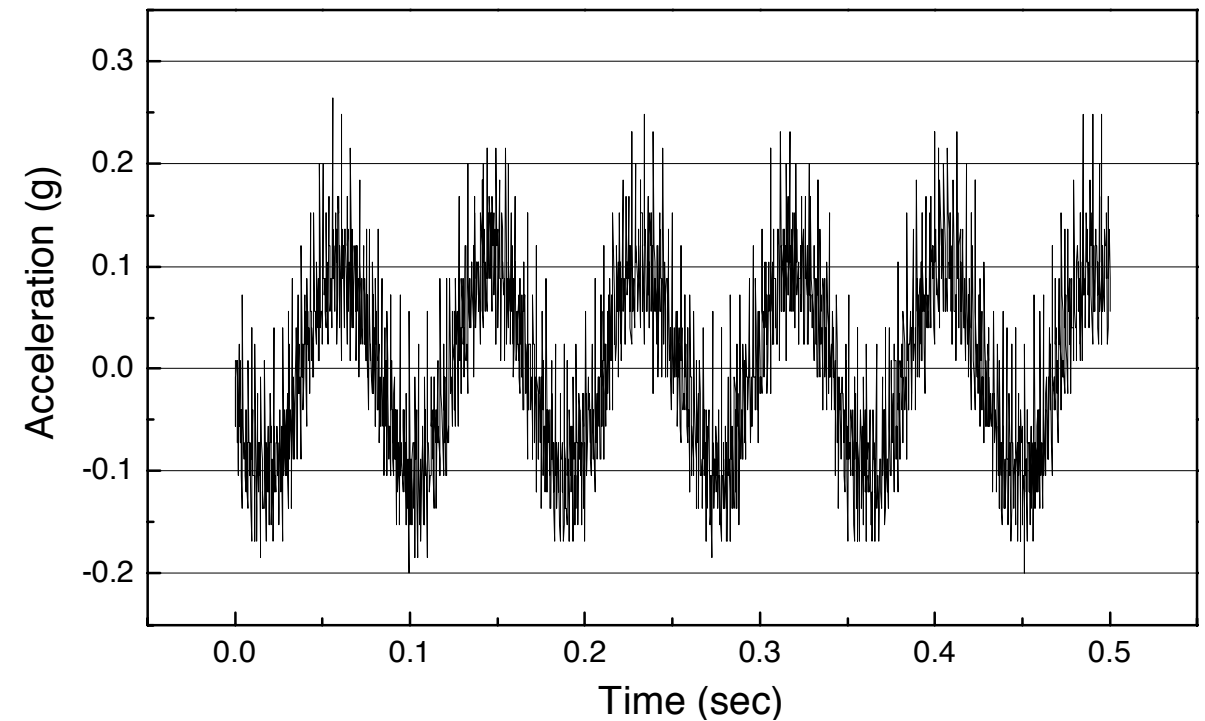
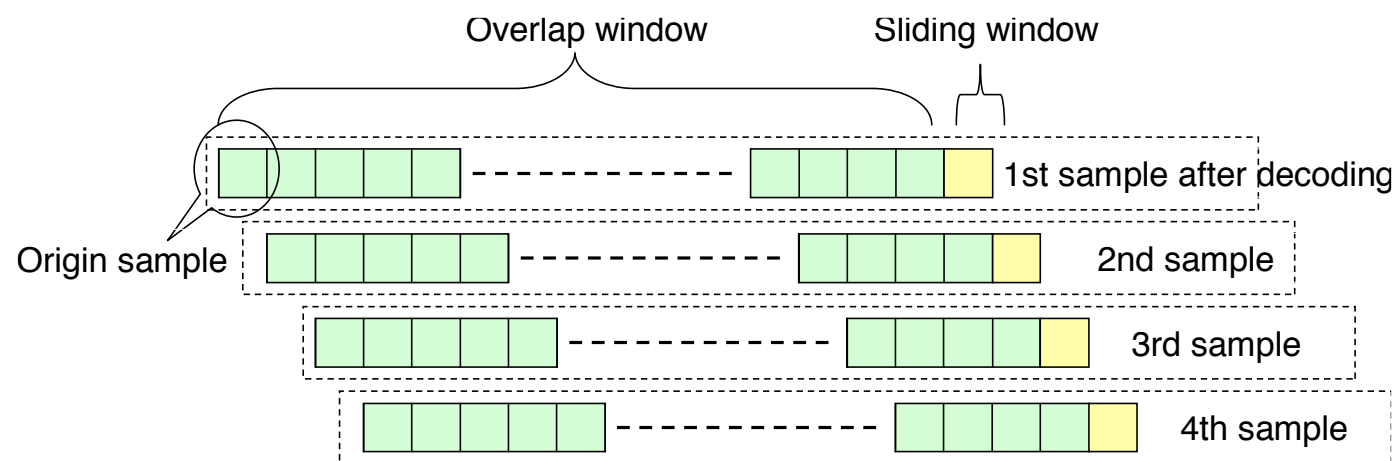
Decoding the 2420

- Input: pulses
- Count pulses, calculate ratio of #1's : #all pulses



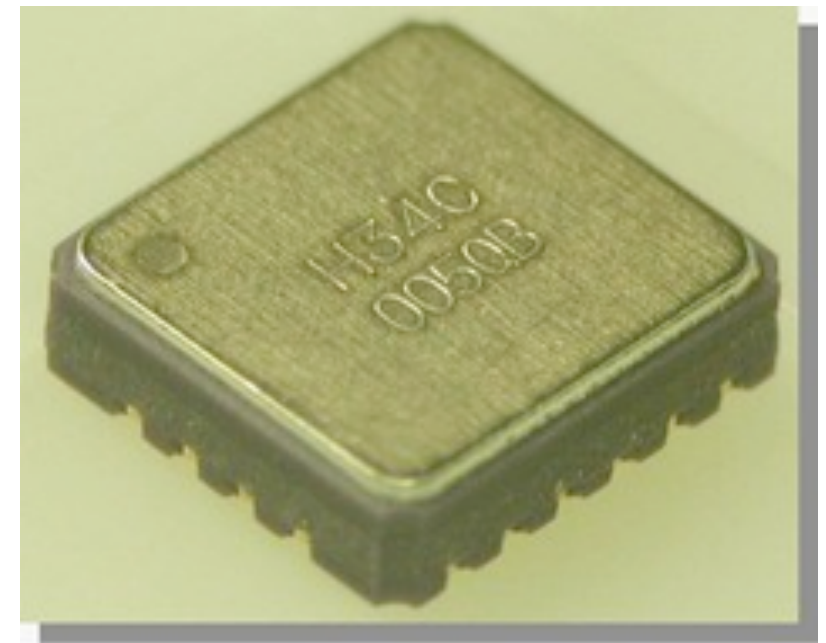
Problem: unfiltered data

- Discretization
- Solution: FIR filter
 - overlapping window
 - smoothes out data



Hitachi Metals H34C accelerometer

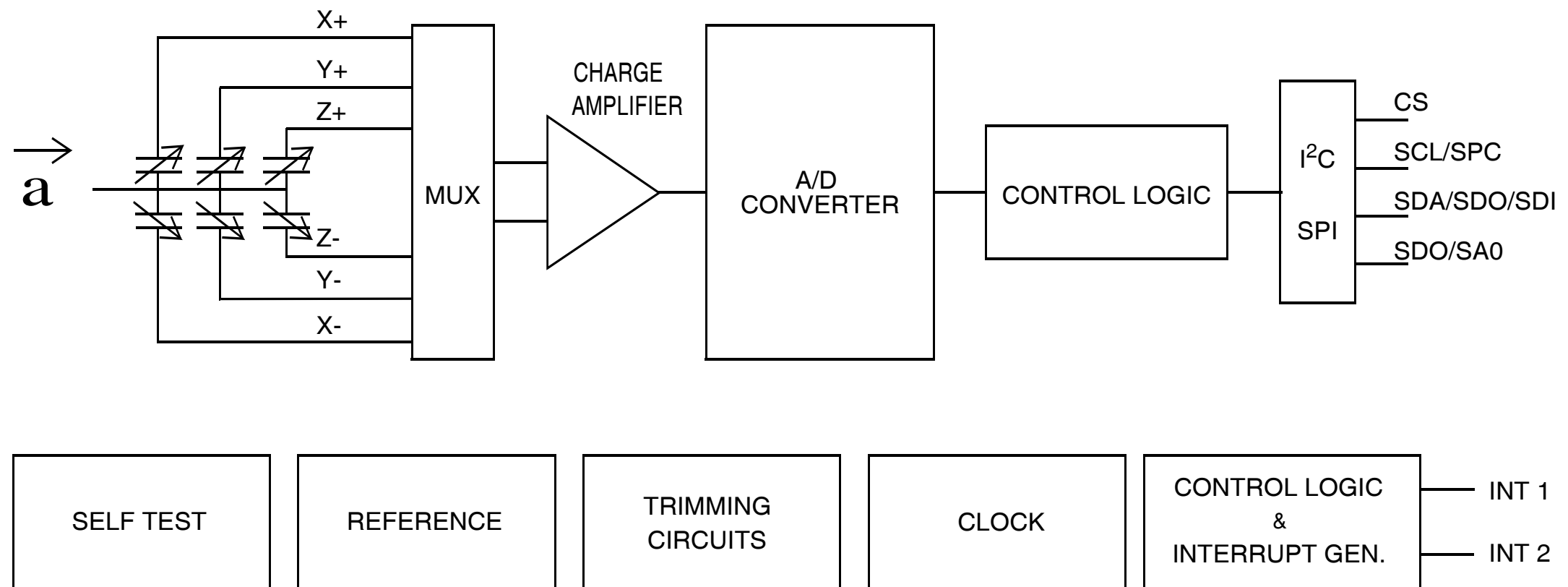
- $\pm 3g$ triaxial
- analog output
- built-in temperature sensor for self calibration
- small size:
3.4x3.7x0.92mm



ST LIS331DLH accelerometer

- Range ± 2 , ± 4 , ± 8 g
- Size 3 x 3 x 1 mm³
- built-in 12-bit ADC, 0.5 Hz to 1 KHz sampling rate
- SPI or I2C output
- Threshold detection (inertial) and Freefall detection
 - User-defined threshold
 - AND/OR of 3 axes
 - separate interrupt output for threshold & freefall

Block diagram of LIS331DLH

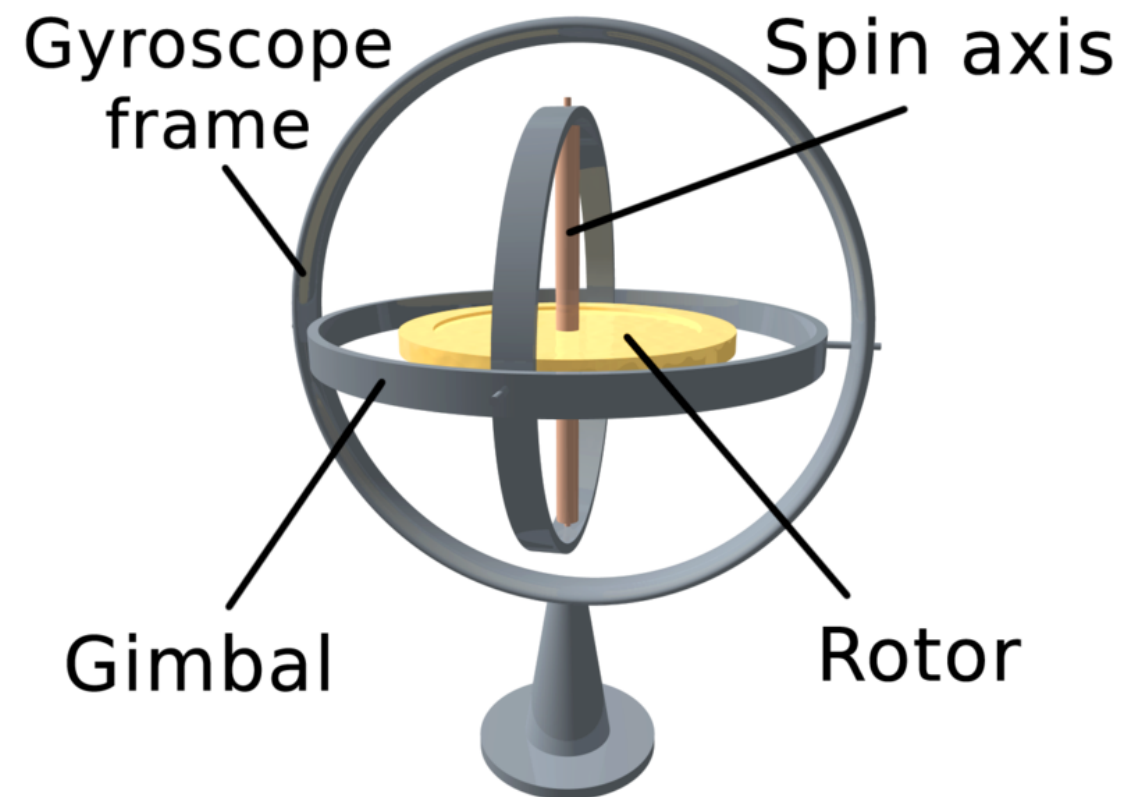


Other sensors

- Pressure sensors
- Magnetic sensors
- Displacement
- Bending sensors
- Gyroscope, Inertial Measurement Unit, Compass
- Humidity
- poisonous gas

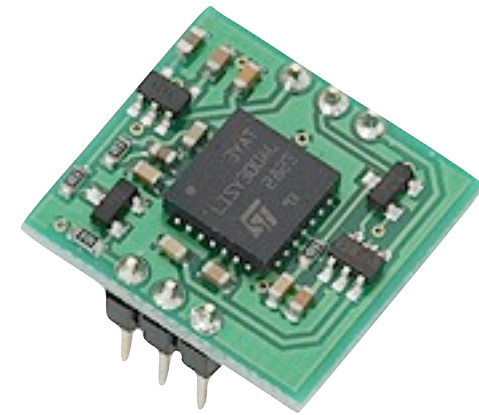
Traditional Gyroscope

- Maintains orientation
 - due to angular momentum
- One fixed axis
 - measure tilt, orientation



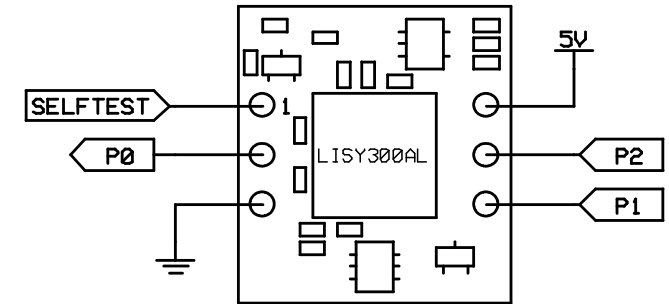
MEMS Gyroscope: LISY300 (Parallax)

- Vibrating mass, no rotor
- single axis yaw-rate
- $\pm 300^\circ/\text{s}$ full scale, up to 88 Hz
- SPI (4 MHz max),
using built-in 10-bit ADC
- 3.4-6.5V DC (5V typ)
@5.25mA
- 19x17x12mm³



<http://www.parallax.com/Portals/0/Downloads/docs/prod/sens/27922-LISY300GyroscopeModuleV1.0.pdf>

LISY300 Gyroscope



- Internally 1.6V when stable
- clockwise => voltage drops
- counterclockwise => voltage rises
- 3.3 mV/degrees/sec, about 88 sps
- internal 10-bit ADC