DATA SHEET

凌陽科技
SUNPLUS

SPC81A

80KB Sound Controller

SEP. 06, 2001

Version 1.6

Table of Contents

SPC81A

80KB SOUND CONTROLLER

1. GENERAL DESCRIPTION

The SPC81A is a CPU based two-channel speech/melody synthesizer including CMOS 8-bit microprocessor with 69 instructions, 80K-byte ROM for speech and melody data (Speech is compressed by a 4-bit ADPCM with approx. 26 sec speech duration @ 6KHz sampling rate) and 128-byte working SRAM. It includes two Timer/Counters, 20 Software Selectable I/Os, two 8-bit current outputs D/A (or one PWM audio output) and serial interface I/O port. It provides Multi-Duty-Cycle output for remote control purposes. Volume control is also provided. For audio processing, melody and speech can be mixed into one output. It operates over a wide voltage range of 2.4V - 5.5V. In addition, SPC81A has a Clock Stop mode for power savings. The power savings mode saves the RAM contents, but freezes the oscillator, causing all other chip functions to be inoperative. The Max. CPU clock frequency is 6.0MHz. It has an Instruction Cycle Rate of 2 clock cycles (min.) - 6 clock cycles (max.). The SPC81A includes, not only the latest technology, but also the full commitment and technical support of Sunplus.

2. BLOCK DIAGRAM
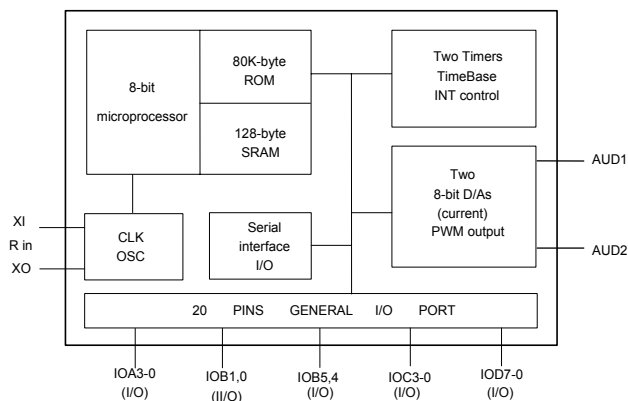
3. FEATURES

- 8-bit microprocessor
- **Provides 80K-byte ROM for program and audio data**
- **128-byte working SRAM**
- Software-based audio processing
- Wide operating voltage: 2.4V - 3.6V @ 4.0MHz
  3.6V - 5.5V @ 6.0MHz
- Supports Crystal Resonator or Rosc
  (with Mask option)
- Max. CPU clock: 4.0MHz @ 2.4V - 3.6V
  6.0MHz @ 3.6V - 5.5V
- Standby mode (Clock Stop mode) for power savings.
  Max. 2μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- **Provides 20 general I/Os**
- Two 12-bit timer/counters
- 6 INT sources
- Key wake-up function
- **Approx. 26 sec speech**
  @ 6KHz sampling rate with 4-bit ADPCM
- **One PWM audio output (single speaker)**
- **Two DA output**
- **Serial interface I/O port**
- **Multi-duty-cycle mode**
- **Volume control function**

4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
      Spelling (English or Chinese)
      Math
- High end toy controller
- Talking instrument controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS*

Mnemonic	PIN No.	Type	Description
VDD	14, 18	I	Power VDD
VSS	7, 13	I	Power VSS
XI	16	I	Oscillator crystal input or RESISTOR (Resistor should be connected to VDD)
XO	15	O	Oscillator crystal output
RESET	8	I	This pin is an active low reset for the chip.
AUD1	17	O	AUDIO OUTPUT
AUD2	19		
TEST	20	I	TEST MODE
IOA0	6	I/O	Port A is a 4-bit bi-directional programmable Input / Output port with Pull-high or Open-drain option. As inputs, Port A can be in either the Pure or Pull-high states. As outputs, Port A can be either Buffer or Open-drain NMOS types (Sink current).
IOA1	5	I/O	
IOA2	4	I/O	IOA0: SIO clock output
IOA3	3	I/O	IOA2: Multi-duty cycle output.
			**See note 1 and 2 below.
IOB0	29	I/O	Port B is a 4-bit bi-directional programmable Input / Output port with Pull-low or Open-drain option. As inputs, Port B can be in either the Pure or Pull-low states. As outputs, Port B can be either Buffer or Open-drain NMOS types (Sink current).
IOB1	30	I/O	
IOB4	1	I/O	
IOB5	2	I/O	**See note 1 and 2 below.
IOC0	12	I/O	Port C is a 4-bit bi-directional programmable Input / Output port with Pull-high or Open-drain option. As inputs, Port C can be in either the Pure or Pull-high states. As outputs Port C can be a Buffer or Open-drain NMOS type.
IOC1	11	I/O	IOC0: SIO Data I/O
IOC2	10	I/O	IOC1: EXT INT PIN
IOC3	9	I/O	IOC2: EXT COUNT IN
			**See note 1 and 2 below.
IOD0	28	I/O	Port D is an 8-bit bi-directional programmable Input / Output port with Pull-low or Open-drain option. As inputs, Port D can be either Pure or Pull-low states. As outputs, Port D can be either Buffer or Open-drain PMOS type (send current). Also, Port D can be software programmed for wake-up I/O pins.
IOD1	27	I/O	
IOD2	26	I/O	
IOD3	25	I/O	(Key Change, Wake-up I/O).
IOD4	24	I/O	
IOD5	23	I/O	
IOD6	22	I/O	
IOD7	21	I/O	**See note 1 and 2 below.

* Refer to SPC Programming Guide for complete information.

Note2: 1.) Two input states can be specified; Pure Input, Pull-High or Pull Low.

2.) Three output states can be specified as Buffer output, Open Drain PMOS output (send), or Open Drain NMOS output <sink>.

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The SPC81A 8-bit microprocessor is a high performance processor equipped with Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure). SPC81A is able to perform with 6.0MHz (max.) depending on the application specifications.

6.2. Oscillator

The SPC81A supports AT-cut parallel resonant oscillated Crystal / Resonator or RC Oscillator or external clock sources by mask option (select one from those three types). The design of application circuit should follow the vendors' specifications or recommendations. The diagrams listed below are typical X'TAL/ROSC circuits for most applications:

(a) Crystal or Ceramic Resonator Connections

(b) RC Oscillator Connections
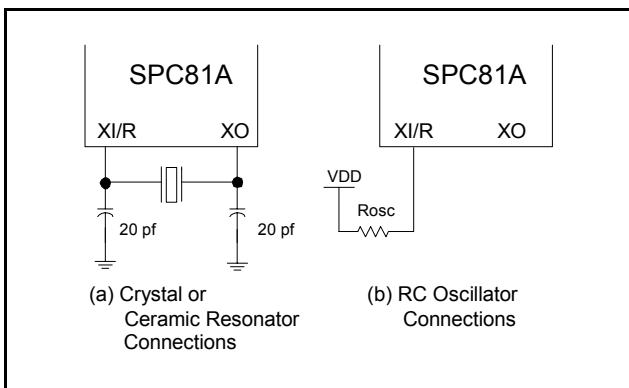
6.3. Mask Option

The SPC81A has the following mask option:

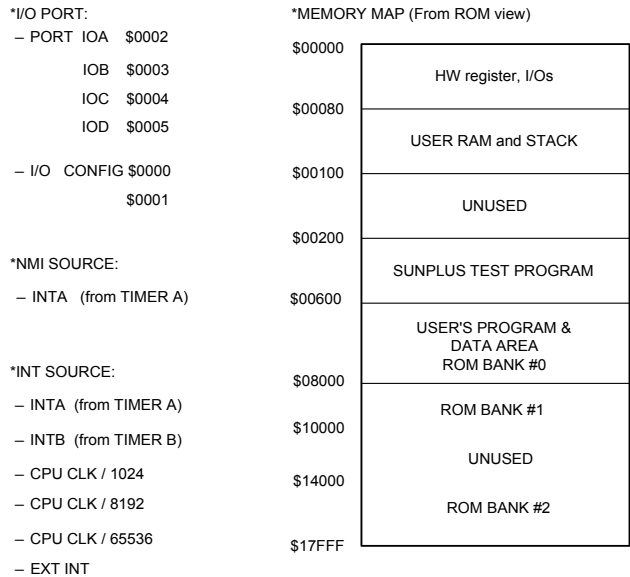• Supports Crystal Resonator or Rosc (with mask option).

6.4. ROM Area

The SPC81A provides an 80K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data.
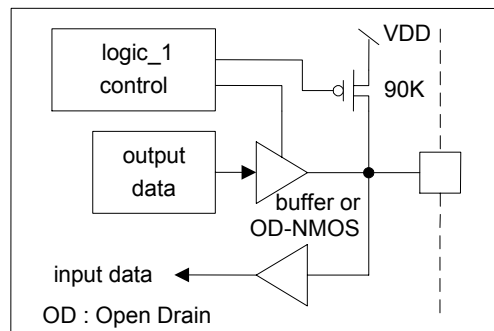
6.5. RAM Area

The SPC81A total RAM consists of 128 bytes (including Stack) at locations from $80 through $FF.

6.6. Map of Memory and I/Os

*I/O PORT:
– PORT IOA $0002
        IOB $0003
        IOC $0004
        IOD $0005
– I/O CONFIG $0000
             $0001

*NMI SOURCE:
– INTA (from TIMER A)

*INT SOURCE:
– INTA (from TIMER A)
– INTB (from TIMER B)
– CPU CLK / 1024
– CPU CLK / 8192
– CPU CLK / 65536
– EXT INT

*MEMORY MAP (From ROM view)

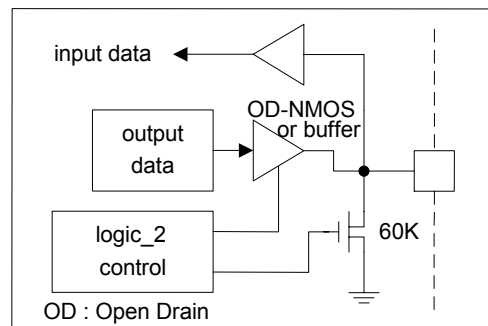| Address	Region
$00000	HW register, I/Os
$00080	USER RAM and STACK
$00100	UNUSED
$00200	SUNPLUS TEST PROGRAM
$00600	USER'S PROGRAM & DATA AREA ROM BANK #0
$08000	ROM BANK #1
$10000	UNUSED
$14000	ROM BANK #2
$17FFF	

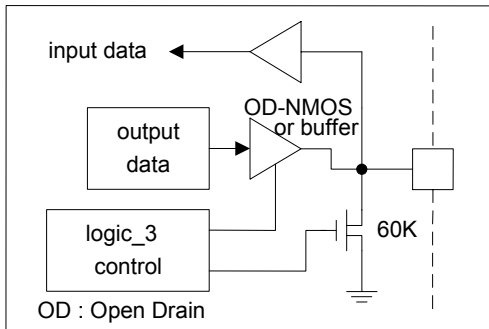## 6.7. I/O Port Configurations*

Input/Output IOA port : IOA3 - 0

Input/Output IOB port : IOB1 - 0

Input/Output IOB port : IOB5 - 4

OD : Open Drain

Input/Output IOC port : IOC3 - 0

OD : Open Drain

Input/Output IOD port : IOD3 - 0

OD : Open Drain

Input/Output IOD port : IOD7 - 4

OD : Open Drain

*Values shown are for VDD = 5.0V test conditions only.
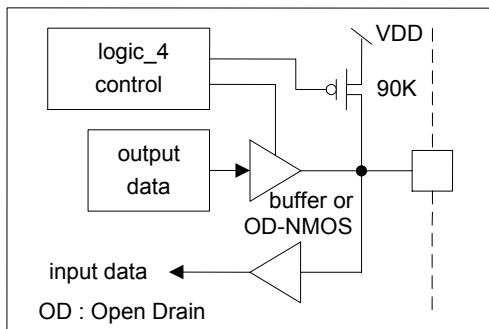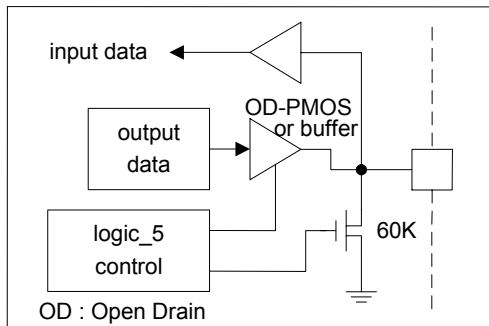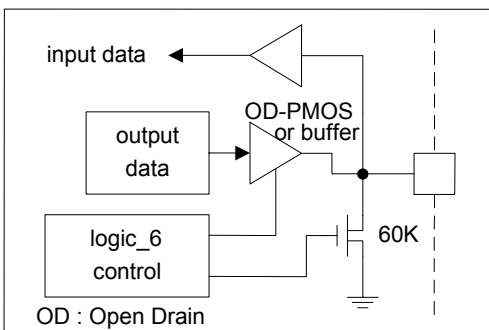
6.8. Speech and Melody

Since the SPC81A provides a large ROM and wide range of CPU operation speeds, it is most suitable for speech and melody synthesis.

For speech synthesis, the SPC81A can provide NMI for accurate sampling frequency. Users can record or synthesize the sound and digitize it into the ROM. The sound data can be played back in the sequence of the control functions as designed by the user's program. Several algorithms are recommended for high fidelity and compression of sound including PCM, LOG PCM, and ADPCM.

For melody synthesis, the SPC81A provides the dual tone mode. After selecting the dual tone mode, users only need to fill either TMA or TMB, or both TMA and TMB to generate expected frequency for each channel. The hardware will toggle the tone wave automatically without entering into an interrupt service routine. Users are able to simulate musical instruments or sound effects by simply controlling the envelope of tone output.

6.9. Volume Control Function

The SPC81A contains a volume control function that provides an 8-step volume controller to control current D/A output. A volume control function selector (Enable/Disable) register and controller register is provided.

6.10. Serial Interface I/O

The SPC81A provides serial interface I/O mode for those applications required large ROM/RAM. Serial Interface I/O Port can be used to read/write data from/to extra memory. The interface I/O Register is the control register for programming interface I/O.

6.11. Multi-Duty-Cycle Mode

The SPC81A provides three output waveforms, 1/2, 1/3, and 1/4 duty cycles. The Control Register should be used to select 1/2, 1/3 or 1/4 duty cycle and the IOA2 should be programmed as the multi-duty cycle output port. Users can use the combinations of these duty cycles for remote-control purposes.

6.12. 1/2, 1/3, 1/4 Duty Cycle Outputs
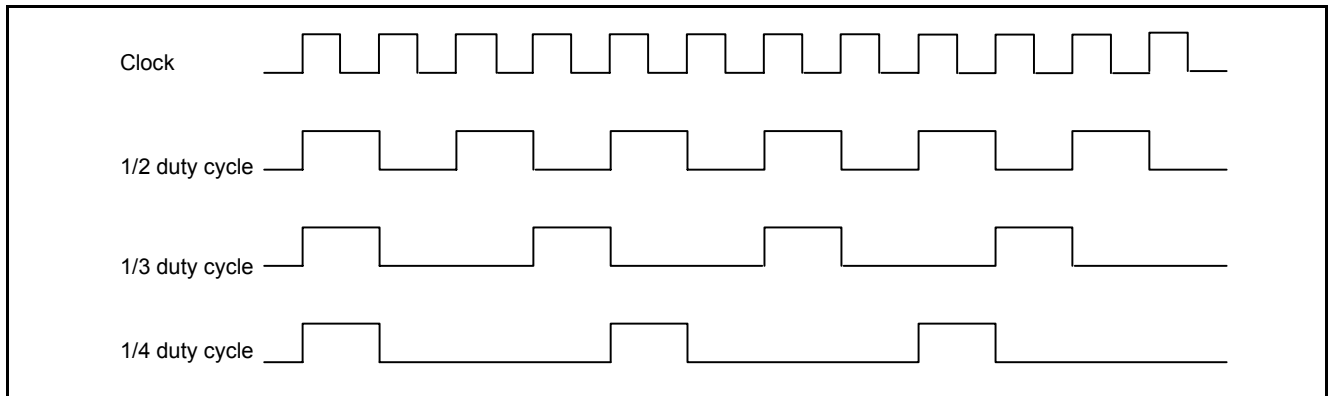
6.13. Power Savings Mode

The SPC81A provides a power savings mode (Standby mode) for those applications that require very low stand-by current. To enter standby mode, the Wake-Up Register should be enabled and then stop the CPU clock by writing the STOP CLOCK Register. The CPU will then go to the stand-by mode. In such a mode, RAM and I/Os will remain in their previous states until being awakened. Port IOD7-0 is the only wake-up source in the SPC81A. After the SPC81A is awakened, the internal CPU will go to the RESET State (Tw $\geq$ 65536 x T1) and then continue processing the program. Wakeup Reset will not affect RAM or I/Os (FIG.1).
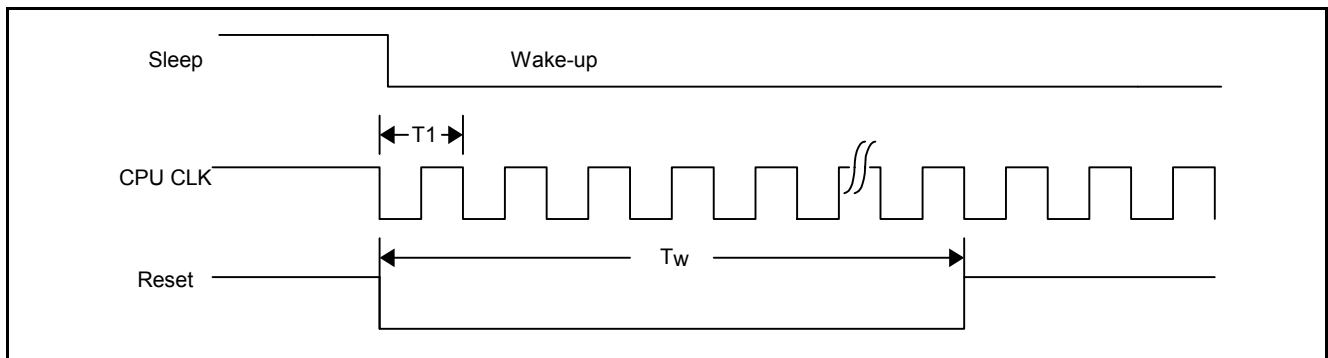

FIG. 1

T1 = 1 / (F$_{CPU}$), Tw $\geq$ 65536 x T1

6.14. Timer/Counter

The SPC81A contains two 12-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer or a counter, but TMB can only be used as a timer. In the timer mode, TMA and TMB are re-loaded up-counters. When timer overflows from $0FFF to $0000, the carry signal will make the timer automatically reload to the user's pre-set value and be up-counted again. At the same time, the carry signal will generate the INT signal if the corresponding bit is enabled in the INT ENABLE Register. If TMA is specified as a counter, users can reset by loading #0 into the counter. After the counter has been activated, the value of the counter can also be read from the counters at the same time.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	12-BIT TIMER	CPU CLOCK (T) or T/4
	12-BIT COUNTER	T/64, T/8192, T/65536 or EXT CLK
TMB	12-BIT TIMER	T or T/4
MODE SELECT REGISTER		TMA only, select timer or counter
TIMER CLOCK SELECTOR		Select T or T/4

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC2}	-	2.0	4.0	MHz	VDD = 2.4V - 3.6V, 2-battery
		-	4.0	6.0	MHz	VDD = 3.6V - 5.5V, 3-battery

7.3. DC Characteristics (VDD = 3.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	1.5	2.0	mA	F_{CPU} = 3.0MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
Audio output current	I_{AUD}	-	-1.5	-	mA	VDD = 3.0V, one-channel
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I IOA, IOB, IOC, IOD	I_{OH}	-1.0	-	-	mA	VDD = 3.0V V_{OH} = 2.0V
Output Sink I IOA, IOB, IOC, IOD	I_{OL}	2.0	-	-	mA	VDD = 3.0V V_{OL} = 0.8V
Input Resistor IOB, IOD	R_{IN}	-	100	-	Kohm	Pull Low VDD = 3.0V

7.4. DC Characteristics (VDD = 5.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	4.0	5.0	mA	F_{CPU} = 4.0MHz @ 5.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5.0V
Audio output current	I_{AUD}	-	-3.0	-	mA	VDD = 5.0V, one-channel
Input High Level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Output High I IOA, IOB, IOC, IOD	I_{OH}	-1.0	-	-	mA	VDD = 5.0V V_{OH} = 4.2V
Output Sink I IOA, IOB, IOC, IOD	I_{OL}	4.0	-	-	mA	VDD = 5.0V V_{OL} = 0.8V
Input Resistor IOB, IOD	R_{IN}	-	60	-	Kohm	Pull Low VDD = 5.0V

7.5. The Relationship between the R_{OSC} and the F_{OSC}
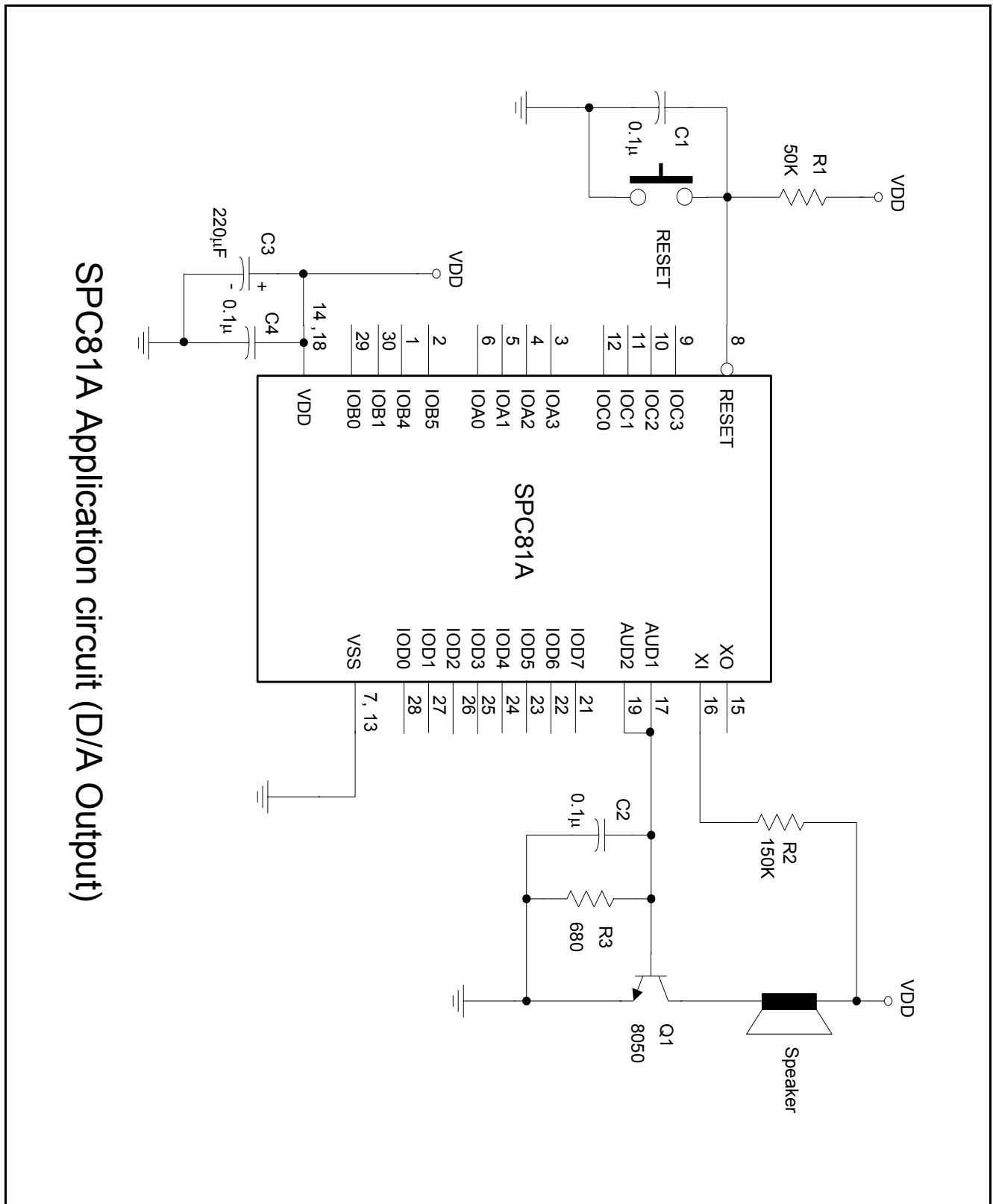
7.5.1. VDD = 3.0V, T_A = 25℃
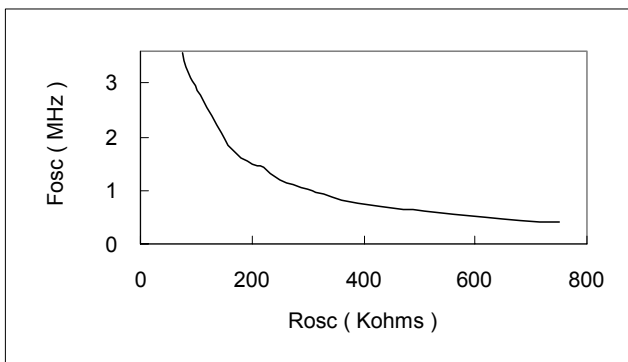
7.5.2. VDD = 4.5V, T_A = 25℃
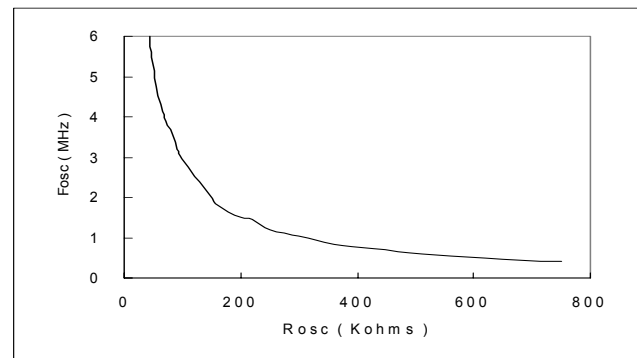
8. APPLICATION CIRCUITS

8.1. Application Circuit - (1)

SPC81A Application circuit (D/A Output)

![SUNPLUS 凌陽科技 logo]

SPC81A

8.2. Application Circuit - (2)

SPC81A Application circuit with X'TAL

8.3. Application Circuit - (3)
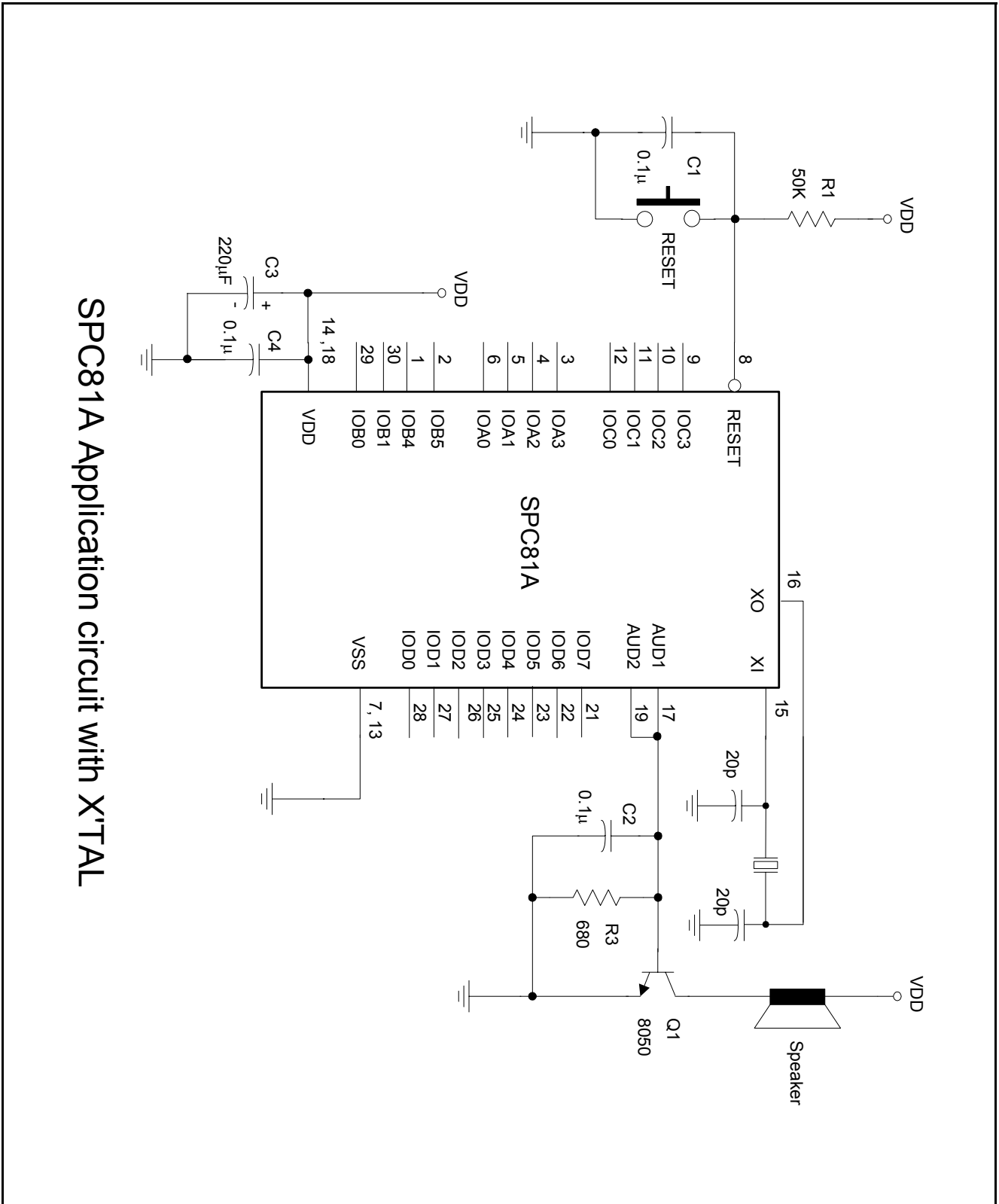

SPC81A Application circuit with Serial Interface I/O Application
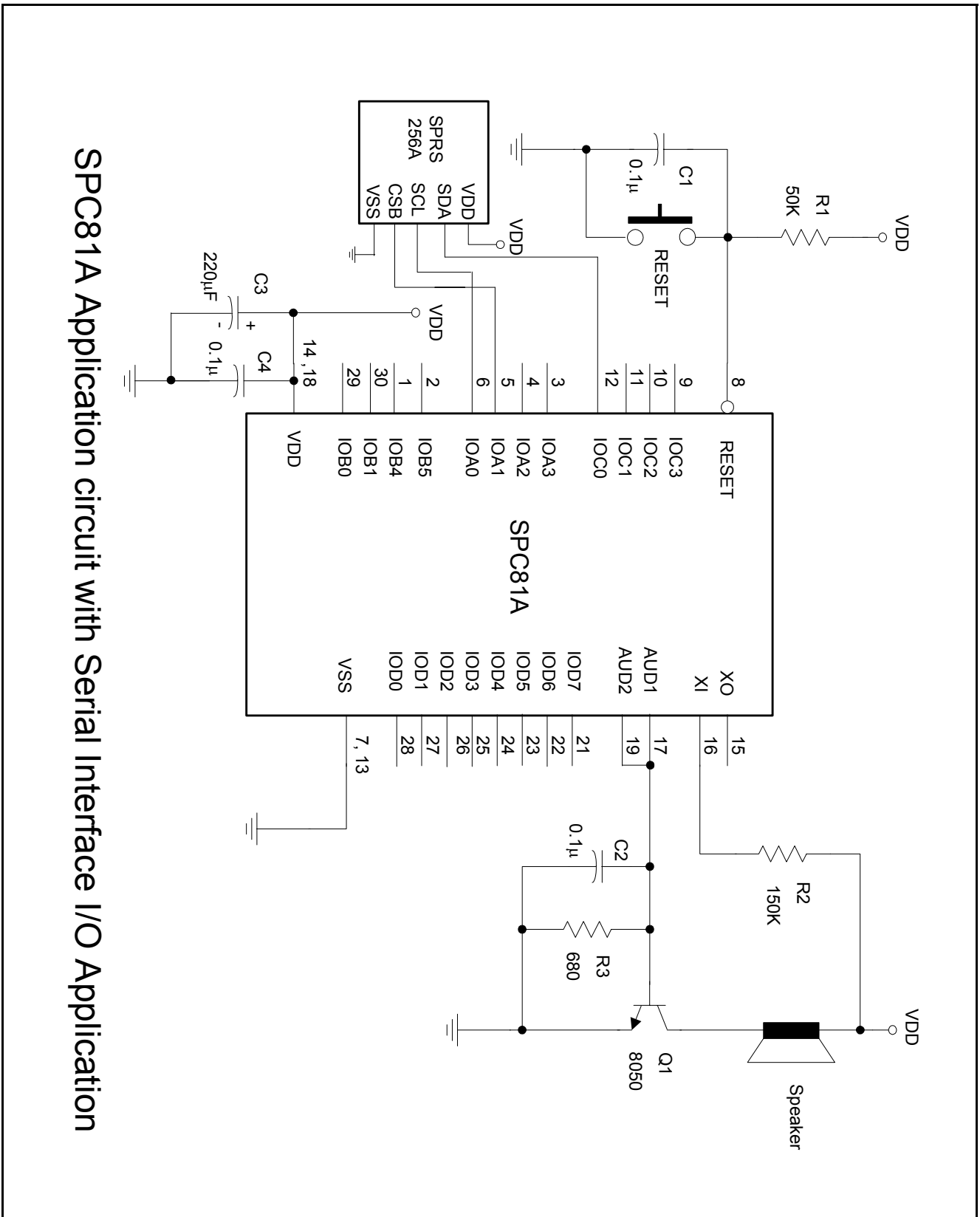
8.4. Application Circuit - (4)

SPC81A Application circuit (PWM Output)

8.5. Application Circuit - (5)

SPC81A Application circuit with Serial Interface I/O Application
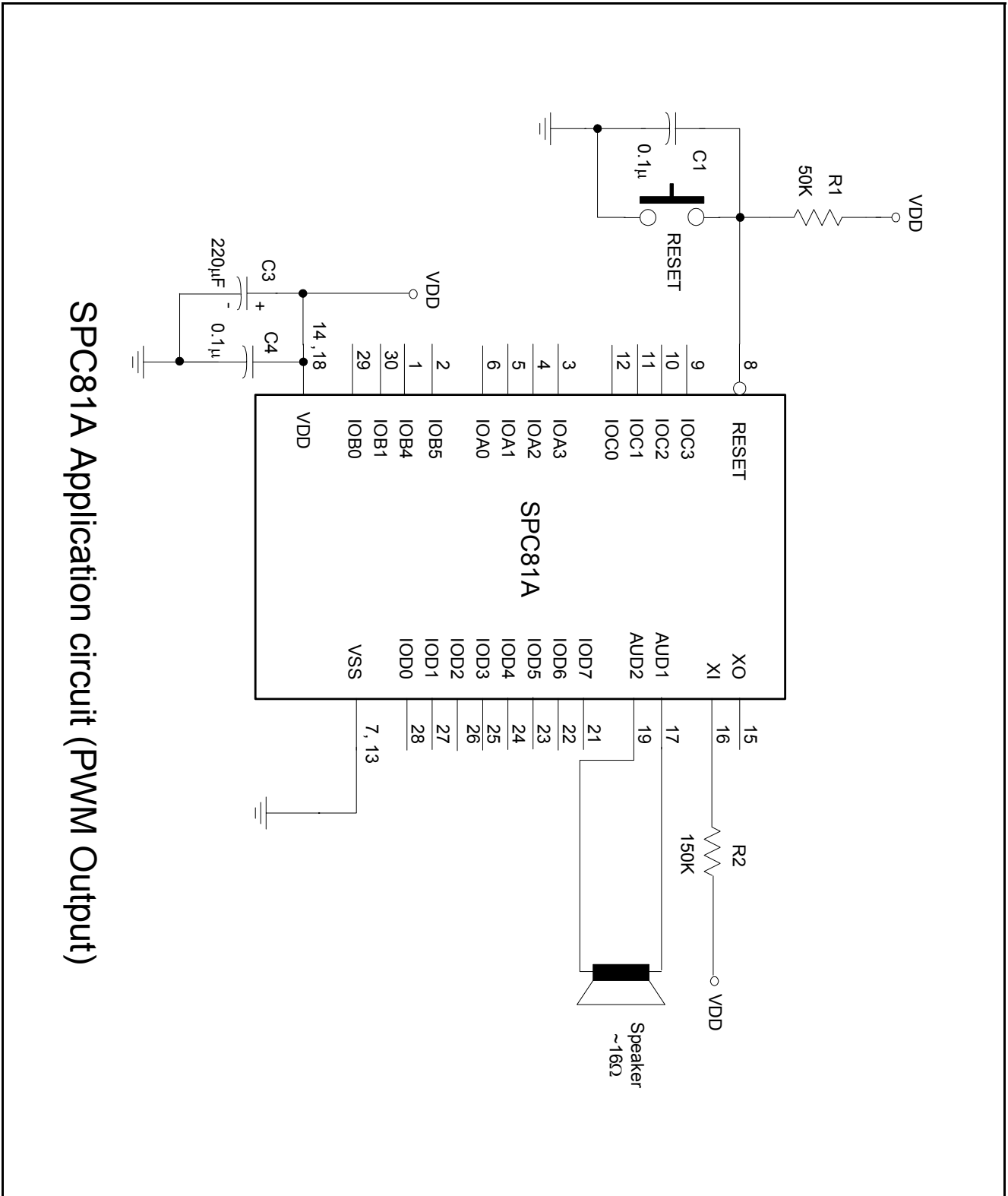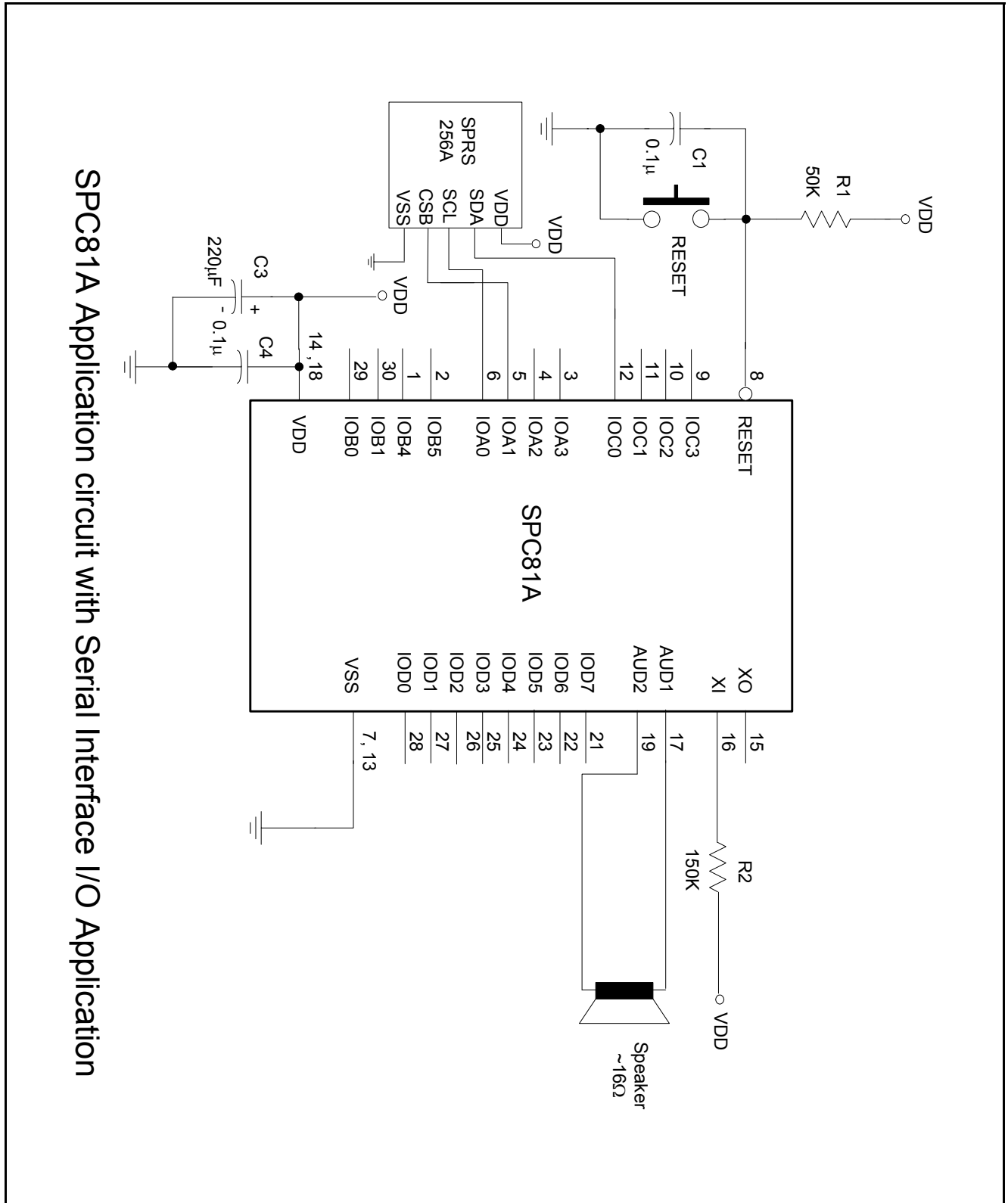
9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment
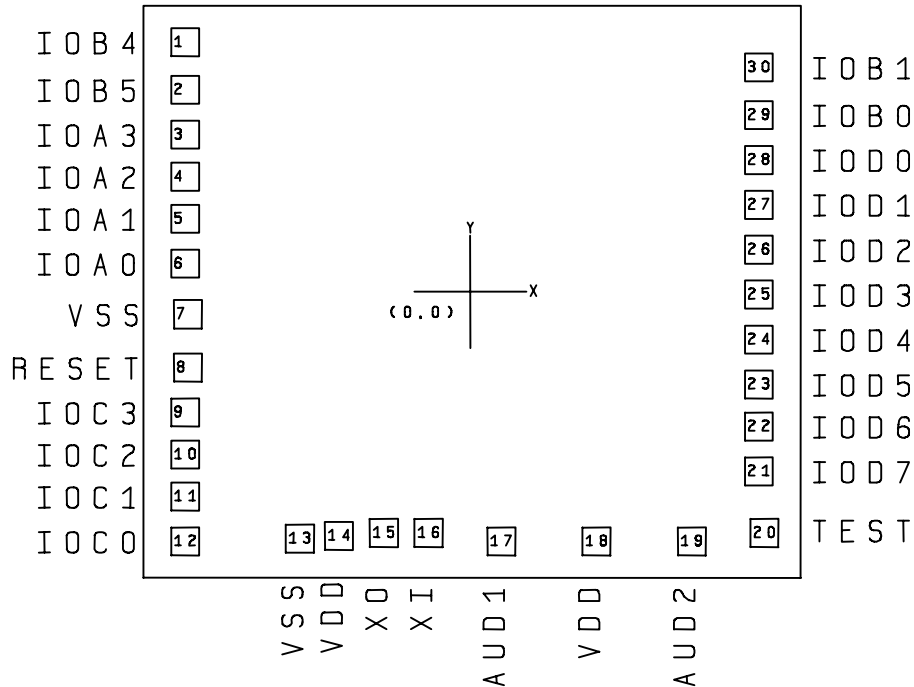
Chip Size: 2450μm x 2190μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: To ensure that the IC functions properly, bond all VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPC81A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (A = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y
1	IOB4	-1029	886
2	IOB5	-1029	725
3	IOA3	-1029	562
4	IOA2	-1029	411
5	IOA1	-1029	256
6	IOA0	-1029	105
7	VSS	-1015	-81
8	RESET	-1017	-265
9	IOC3	-1029	-427
10	IOC2	-1029	-582
11	IOC1	-1029	-734
12	IOC0	-1029	-889
13	VSS	-610	-875
14	VDD	-470	-874
15	XO	-319	-862
16	XI	-153	-862
17	AUD1	108	-894
18	VDD	447	-894
19	AUD2	786	-894
20	TEST	1041	-862
21	IOD7	1026	-640
22	IOD6	1026	-481
23	IOD5	1026	-329
24	IOD4	1026	-170
25	IOD3	1026	-14
26	IOD2	1026	155
27	IOD1	1026	312
28	IOD0	1026	471
29	IOB0	1026	627
30	IOB1	1026	797

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11. REVISION HISTORY

Date	Revision #	Description	Page
DEC. 30, 1996	0.1	Original	
MAR. 10, 1997	0.2	1. Add "*PAD ASSIGNMENT*" 2. Add "*PAD LOCATIONS*"	10 12 - 13
MAR. 24, 1997	0.3	1. Modify Fosc2 (max.) value: 3.0MHz @ 3.0V to 3.58MHz @ 3.0V 2. Modify IOB4, IOB5 type description: Input pin -> Input/Output pin	
OCT. 01, 1997	0.4	1. Delete OPT pin 2. Modify "*APPLICATION CIRCUITS*" 3. Modify "*PAD ASSIGNMENT*" 4. Modify "*PAD LOCATIONS*"	3 10 12 13
DEC. 04, 1997	0.5	1. Renew to a new document format 2. Add "The Relationship between the R_{OSC} and the F_{OSC}"	
MAR. 02, 1998	1.0	Delete "*PRELIMINARY*"	
MAR, 19, 1998	1.1	1. Correction audio output current typical value: -3.0mA to -2.7mA 2. Modify audio output current test description	
MAY. 13, 1998	1.2	Add "Note2: To ensure that the IC functions properly, bond all VDD and VSS pins."	
JUN. 03, 1998	1.3	1. Revise the grammars and spelling in "*GENERAL DESCRIPTION*", "*FEATURES*", "*FUNCTIONAL DESCRIPTIONS*", "*TIMER/COUNTER*", "*SPEECH AND MELODY*", and "*APPLICATION CIRCUITS*" 2. Add four features in the "*FEATURES*" 3. Revise the block diagram 4. Add pin description of IOA0, IOA2	2 2 3
SEP. 15, 1999	1.4	Renew to a new document format	
NOV. 08, 2000	1.5	1. VDD = 2.4V - 3.6V for 2-battery application. 2. Speech duration @ 6KHz sampling rates with 4-bit ADPCM. 3. Approx. 26 sec. speech.	
SEP. 06, 2001	1.6	1. Correct chip size 2. Add Note1 and Note3 in the "*9.1 PAD Assignment*" 3. Renew to a new document format	15 15