EE 114 Design Project
Fall 2014

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Figure 1: Design project specifications, given specs and achieved specs

	Given	Achieved
(Gain x Bandwidth) / (Power dissipation)	1600 kΩ.MHz/mW	2812.69 kΩ.MHz/mW
Power dissipation	$\leq$ 2 mW	1.1489 mW
Small-signal trans-resistance gain (A = v out /i in)	$\geq$ 40 kΩ	40.3187 kΩ
-3dB Bandwidth	$\geq$ 80 MHz	80.1489 MHz
Common mode output voltage	-0.5 V $\leq V_{out} \leq$ 0.5 V	-0.4998061 V
Gate overdrive (V_{ov})	$\geq$ 150 mV	$\geq$ 255 mV
$L_{current\_source}$	$\geq$ 2 µm	$\geq$ 2 µm
Matching parameters? (A vs. B)	Yes	Yes
Integer widths and lengths?	Preferred	Utilized (except for L_{M-L2} = 1.6 µm)
Core Circuit Area[1] (including resistance)		450.4 $(\mu m)^2$
Resistor Area (W = 1 µm)		360 $(\mu m)^2$

*Enrolled in EE114

**Please note our page numbers are off by 1; google docs can't remove page # on coverpage

[1] No percentage-wise breakdown of area was calculated since the 114 project did not have a bias circuit.

Page 2: Design Outline

- Initial Design Strategy
  - Stage Breakdown: 3 stages - CG (loaded by R_u,R_d, and ML-1), CS, and CD, each have a current set by the bias transistor.
    - 1st Stage: Common Gate provides current gain of 1, but impedances seen at its output, V_x, creates a transresistance gain from i_{in} to V_x.
    - 2nd Stage: Common Source loaded by a diode connected (ML-2) transistor. It is also degenerated by the bias transistor, Mbias-2.
    - 3rd Stage: Common Drain, loaded by impedance of Mbias-3, C_L and R_L.
  - Differential-Mode Half Circuit: The half-circuit had some key implications
    - Current bias transistors (Mbias-1, Mbias-2, Mbias-3, ML-1) → AC GND
      - V_{gs} became 0, so only AC effect was r_o
    - AC grounded M2 source, voiding source degeneration effects.
    - Output sees $2C_L$ and $.5R_L$, due to the "ground-line" in differential mode.
  - Potential Bottlenecks:
    - τ contribution at V_x.
      - Large impedances (Ru and Rd) to drive voltage gain
      - High input capacitance due to Miller effect. CG stage is basically the sole voltage amplifier stage (CG, and CD have ~unity gain)
    - Body effect (towards top of the circuit)
      - NMOS bulks are tied to V_{ss}
        - V_{SB} term gets large for transistors at the top of circuit
          - Increased V_{t0} and g_m terms
- 1st Iteration: Low-frequency Gain Calculation
  - Assumptions
    - Set Vbias-Gen_{NMOS} to -1V and Vbias-Gen_{PMOS} to 1V
    - Ignored intrinsic & extrinsic capacitances, CLM, and Body effect
    - Each bias transistor spits out the same current - about 50μA per branch
      - The first stage PMOS and NMOS also provide this same current.
  - LF Gain: $(R_u \parallel R_d) * (g_{m2}/g_{mL-2})$ → Maximize R_u,R_d, & $(W/L)_{M2}/(W/L)_{ML-2}$
    - ~26kΩ, ~40MHz (half of desired parameters)
  - Next Iterations: More power for M3 (BW), less for M1 (generate tradeoff curves)
- Optimization Strategy
  - Find wiggle-room in circuit, make trade-off equations/curves, implement, repeat
    - Drop assumptions through each iteration
      - i.e. Body effect should be considered for top transistors;
  - When there's no more obvious wiggle room, run MATLAB script
    - Sweep across ~5 key variables to meet parameters and minimize power
- Tradeoff Considerations (a few)
  - Gain-Bandwidth trade-off at V_x; Higher gain → Higher input capacitance (Miller)
  - Power-G, BW trade-off at V_{out}; Lesser power → lower g_m, output impedance
  - $(W/L)_{ML-1}$,τ trade-off for ML-1; Larger size → Higher capacitance & impedance

Trade-off Curves (Figures 2 and 3):

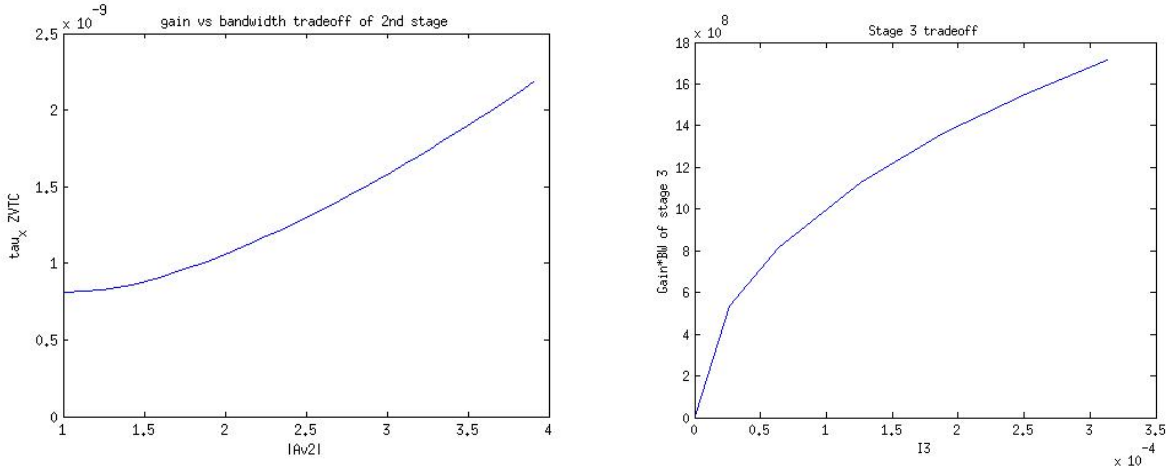


Figure 2: Gain-time constant trade-off of 2nd stage by scaling W2. Increasing gain requires an increase in W2 size and increasing capacitance and Miller effect

Figure 3: Power-GBW trade-off of stage 3.

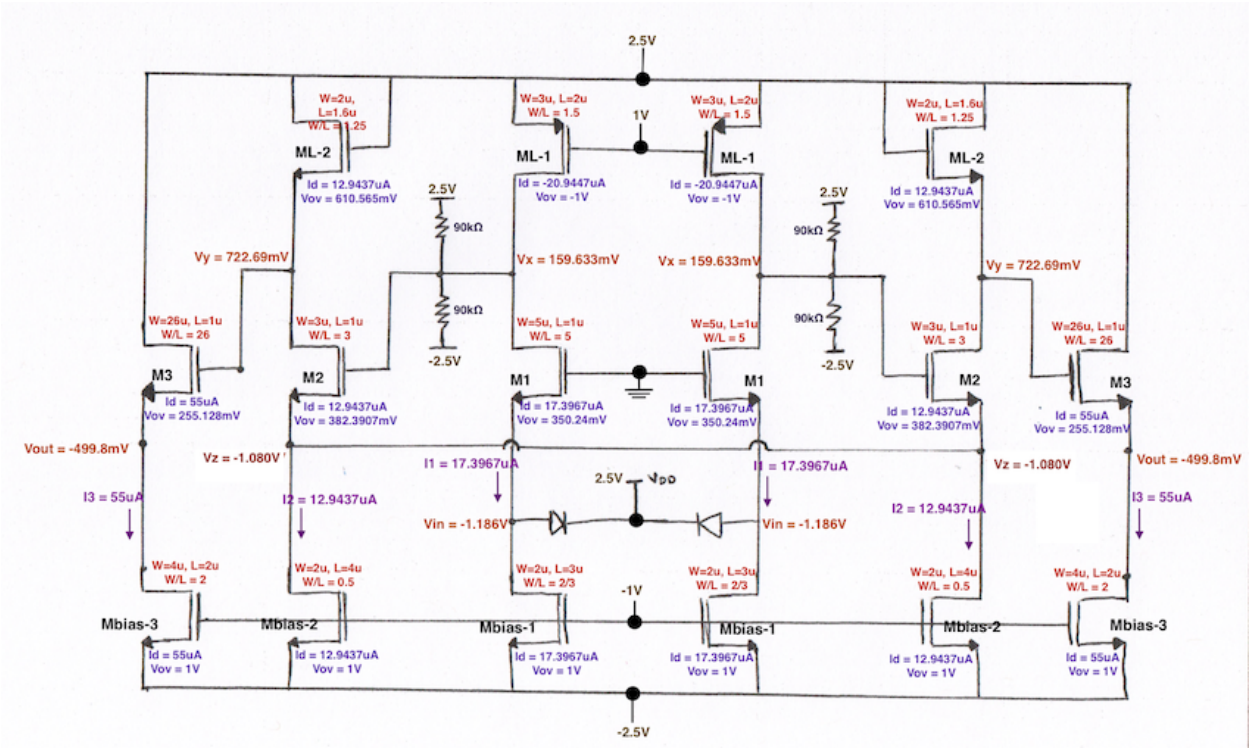


Figure 4 - Schematic of Circuit

Design Calculations

Technology Parameters and Relevant Equations

$k_n = 50\frac{\mu A}{V^2}$ $k_p = 25\frac{\mu A}{V^2}$ $C_{ox} = 2.3\frac{fF}{\mu m^2}$ $C_{ov}' = 0.5\frac{fF}{\mu m}$ $\gamma = 0.6V^{0.5}$ $\varphi_f = 0.4V$

$V_{ss} = -2.5V$ $V_{dd} = 2.5V$ $MJ = 0.5$ $MJSW = 0.33$ $PB = 0.95V$ $CJSW = 0.5\frac{fF}{\mu m}$

$CJ = 0.1\frac{fF}{\mu m^2}$ $L_{diff} = 3\ \mu m$ $L_{bias-min} = 2\ \mu m$ $L_{min} = 1\mu m$ $W_{min} = 2\mu m$ $\frac{g_{mb}}{g_m} \approx 0.2$

$C_{gs} = \frac{2}{3}WLC_{ox} + WC_{ov}'$ $C_{gd} = WC_{ov}'$ $C_{db} = \frac{AD \cdot CJ}{(1+\frac{V_{DB}}{PB})^{MJ}} + \frac{PD \cdot CJSW}{(1+\frac{V_{DB}}{PBSW})^{MJSW}}$

$C_{sb} = \frac{AS \cdot CJ}{(1+\frac{V_{SB}}{PB})^{MJ}} + \frac{PS \cdot CJSW}{(1+\frac{V_{SB}}{PBSW})^{MJSW}}$

Design Simplifications

We first started the design by aiming for a 40 kΩ gain by approximating a large W2/L2 and Ru, Rd. However, Not considering other loading effects, our gain and bandwidth was severely limited. Moving forward, we made the following justified design simplifications.

1. Minimum Channel Lengths: $L_1 := L_2 := L_3 := L_{min} = 1\mu m$
   Decreases capacitance. Other W, L chosen to minimize area given W/L (either $W = 2\ \mu m$ or $L = 2\ \mu m$)
2. Matching ML-1 and Mbias1: $(\frac{W}{L})_{L-1} = \frac{k_n}{k_p}(\frac{W}{L})_{bias1} = 2(\frac{W}{L})_{bias1}$
   Allows us to DC bias V_x using only the Ru/Rd ratio.
3. Diode-connected load: $W_{L-2} := L_{L-2} := 2\ \mu m$
   Minimizes capacitance without sacrificing gain of stage 2
4. Bias voltage: $V_{biasn} = -1V$ and $V_{biasp} = 1V$
   Provides 3V signal swing (-1.5V to 1.5V) while bias MOSFETS are in saturation. Also simplifies calculations ($V_{ov} = 1V$) and keeps sizes appropriate ($25\ \mu A \rightarrow (\frac{W}{L}) = 1$)
5. Drain resistors: $R_u := R_d$
   Biases $V_x \approx 0V$, which provides swing to -0.5V for M2 common source stage.
6. M1 Common gate has unity current gain.

Design Parameters - First Sweep

After implementing the design simplifications, we noticed parameters that had room to change but were non-vital to gain and bandwidth as well as those that did. For example, decreasing I_2 or even I_1 had little effect on gain and bandwidth, while decreasing I_3 severely limited both gain and bandwidth. This helped us understand that we had a close-to-dominant pole at the output but also that we could sacrifice current in other areas. We also recognized that to reach the required gain we could automatically scale the values of $R_u \parallel R_d$ given other parameters.

Using these insights, we wrote out equations for gain, bandwidth, and power, which appear in the transconductances and ZVTC page, and we swept the following variables to maximize for bandwidth with a decent power.

1. W_{bias1} , W_{bias2} , W_{bias3}
   Control bias currents and power linearly. Power vs gain-bandwidth (GBW) trade-off
2. W_2
   Controls stage 2 gain (grows with $\sqrt{W_2}$), but scales Miller C_{gd2} . Gain vs BW tradeoff
3. W_1
   Controls stage 1 gain (grows with $\sqrt{W_1}$), but adds capacitance. Gain vs BW tradeoff
4. $R_u \parallel R_d$
   Given Av_2 and Av_3 , we can calculate the needed $R_u \parallel R_d$ to get a 40 kΩ gain.

Design Parameters - Second Sweep

We reached great SPICE-simulated specifications following the MATLAB sweep, except our V_{out} was out of range at about -700 mV. To put V_{out} , the source of M3, into the desired range without affected bias currents, we increase the gate voltage V_y and increase $(W/L)_3$ to decrease the voltage drop from V_y to V_{out}. Thus, we sweep the following to achieve appropriate V_{out}.

1. W_3
   Controls output voltage and affects M3 gain minorly. Can be large due to Miller cancellation of Common Drain.
2. L_{L-2}
   Changes on the order of 0.2μm. Increases in L_{L-2} decrease Vgs_{L-2} and increase V_y to increase V_{out}

Approximations of Parameters

The following equations were used to approximate different parameters while sweeping sizes. The calculated numbers show the approximate parameter values given the final sizing.

Transconductances

M2 - Common Source Stage

$$Av_2 = \frac{v_y}{v_x} \approx -\frac{g_{m2}}{g_{mL-2}+g_{mbL-2}} = \frac{\sqrt{2k_n(\frac{W}{L})_2 I_2}}{1.2\sqrt{2k_n(\frac{W}{L})_{L-2} I_2}} = \frac{\sqrt{(\frac{W}{L})_2}}{1.2\sqrt{(\frac{W}{L})_{L-2}}} = \frac{\sqrt{3}}{1.2\sqrt{1.25}} = 1.291$$

M3 - Common Drain stage

$$Av_3 = \frac{v_{out}}{v_y} \approx \frac{g_{m3}R_L/2}{(g_{m3}+g_{mb3})R_L/2+1} = \frac{g_{m3}R_L}{(g_{m3}+g_{mb3})R_L+2} \leq \frac{g_{m3}}{g_{m3}+g_{mb3}} \approx 0.8$$

$Av_3 \approx 0.75$ for medium g_m values

M1 - Common Gate stage

$$Av_1 = \frac{v_x}{i_{in}} = R_u \parallel R_d \parallel r_{oL-1} \parallel r_{o1} \approx R_u \parallel R_d$$

$$Av_1 = \frac{40\ k\Omega}{Av_2 \cdot Av_3} \approx 45\ k\Omega = 90\ k\Omega \parallel 90\ k\Omega$$
$$Av = Av_1 \cdot Av_2 \cdot Av_3 = 45\ k\Omega \cdot 1.291 \cdot 0.75\ = 43.5\ k\Omega$$

ZVTC Bandwidth approximation

Input pole

$$C_{input} = C_{in} + C_{gs1} + C_{sb1} + C_{gdBias1} + C_{dbBias1} = 119.78\,fF \approx C_{in} = 100\,fF$$
$$R_{input} = r_{oBias1} \parallel r_{o1} \parallel \frac{1}{g_{m1}+g_{mb1}}\left(1 + \frac{R_u \| R_d \| r_{oL-1}}{r_{o1}}\right) = 9.42\ k\Omega \approx \frac{1}{g_{m1}+g_{mb1}} = \frac{1}{\sqrt{2kp_n(\frac{W}{L})_1 I_1}}$$
$$\tau_{in} = R_{input} \cdot C_{input} = 1.128\ ns$$

Insight: Increase $(W/L)_1$ or I_1 to improve BW. Cin is relatively fixed.

Vx pole (gate of M2)

$$C_x \approx C_{gd1} + C_{dbL1} + C_{gdL1} + C_{gs2} + C_{gd2}(1 - Av_2) = 16.93\,fF$$
$$R_x = R_u \parallel R_d \parallel r_{oL-1} \parallel r_{o1} \approx R_u \parallel R_d$$
$$\tau_x = C_x \cdot R_x = 0.824\ ns$$

Insight: We have GBW trade-offs with the choice of resistors and Av_2 increasing C_{gd2}, assuming (1-Av2)Cgd2 dominantes. There exists a major gain-bandwidth trade-off at V_x. The gain of stages M1 and M2 and the Vx pole can be are proportional to:

$$Av_1 \cdot Av_2 \propto R_x \cdot \sqrt{\frac{W_2}{W_{L-2}}}$$
$$\tau_x = R_x \cdot C_x \approx R_x Av_2 C_{gd2} \propto {R_x}^2 \cdot \sqrt{\frac{{W_2}^3}{W_{L-2}}}$$

Vy pole (gate of M3)

$$C_y \approx C_{db2} + C_{gd2}\left(1 - \frac{1}{Av_2}\right) + C_{sbL2} + C_{gsL-2} + C_{gs3}(1 - Av_3) + C_{gd3} = 45.14\,fF$$
$$R_y = \frac{1}{g_{mL2}+g_{mbL2}} \parallel r_{o2} \parallel r_{oL2} = 19.4\ k\Omega \approx \frac{1}{g_{mL2}+g_{mbL2}} = \frac{1}{1.2\sqrt{2k_n(\frac{W}{L})_{L-2} I_2}}$$
$$\tau_y = C_y \cdot R_y = 0.877\ ns$$

Insight: The effect of C_{gs3} goes to 0 due to Miller effect. Increase $(W/L)_2$ or I_2 to decrease impedance.

Output pole

$$C_{out} = 2C_L + C_{sb3} + C_{gs3}\left(1 - \frac{1}{Av_3}\right) + C_{gdBias3} + C_{dbBias3} = 496\,fF \approx 2C_L = 500\,fF$$
$$R_{out} = \frac{1}{g_{m3}+g_{mb3}} \parallel r_{o3} \parallel r_{oBias3b} \parallel \frac{R_L}{2}\ = 1.836\ k\Omega \approx \frac{1}{g_{m3}+g_{mb3}} \parallel \frac{R_L}{2} = \frac{1}{1.2\sqrt{2k_n(\frac{W}{L})_3 I_3}} \parallel 10k\Omega$$
$$\tau_{out} = C_{out} \cdot R_{out} = 0.911\ ns$$

ZVTC calculation

$$\tau_{zvtc} = \tau_{in} + \tau_x + \tau_y + \tau_{out} = 3.739\ ns$$
$$Bandwidth \approx \frac{1}{2\pi\tau_{zvtc}} = 46.83\ MHz$$

Power and Bias Current Calculation

$$I_1 = \tfrac{1}{2}\mu_n C_{ox}(\tfrac{W}{L})_1(V_{biasn} - V_{SS} - V_t)^2(1 + \lambda \cdot (V_{in} - V_{SS})) \approx \tfrac{1}{2}\mu_n C_{ox}(\tfrac{W}{L})_1(V_{biasn} - V_{SS} - V_t)^2 + 1\ \mu A = 17.7\ \mu A$$
$$I_2 = \tfrac{1}{2}\mu_n C_{ox}(\tfrac{W}{L})_2(V_{biasn} - V_{SS} - V_t)^2(1 + \lambda \cdot (V_z - V_{SS})) \approx \tfrac{1}{2}\mu_n C_{ox}(\tfrac{W}{L})_2(V_{biasn} - V_{SS} - V_t)^2 + 1\ \mu A = 13.5\ \mu A$$
$$I_3 = \tfrac{1}{2}\mu_n C_{ox}(\tfrac{W}{L})_3(V_{biasn} - V_{SS} - V_t)^2(1 + \lambda \cdot (V_{out} - V_{SS})) \approx \tfrac{1}{2}\mu_n C_{ox}(\tfrac{W}{L})_3(V_{biasn} - V_{SS} - V_t)^2 + 1\ \mu A = 51\ \mu A$$
$$I_R = \frac{V_{DD} - V_{SS}}{R_U + R_D} = 24.58\ \mu A$$
$$Power = (V_{DD} - V_{ss}) \cdot (I_1 + I_2 + I_3 + I_R) = 1.0674\ mW$$

Comparison of Hand-Calculations with SPICE Simulations

Parameter	Hand-Calculation	SPICE Simulation	% Error	Main Factors
Gain	43.5 kΩ	40.3187 kΩ	7.9%	CLM
Bandwidth	46.83 Mhz	80.1489 MHz	-41.5%	ZVTC Estimate
Power	1.0674 mW	1.1489 mW	-7.1%	CLM, Mismatch

Sources of Error

Gain

We assumed $r_o >> R, \frac{1}{g_m}$. However, r_o is finite and decreases node impedance at important gain stages.

Bandwidth

The Zero-Value Time Constant method underestimates the bandwidth, especially when there is no dominant pole. All time constants were within +-20% of 1 ns, so the circuit has no dominant pole.

Power

A closed-form solution for the drain currents is difficult because the channel-length modulation depends on the drain voltage, which often circularly depends on the bias drain current. A conservative estimate corresponding, 1μA was added to each bias drain current. Additionally, there is a slight mismatch due to channel-length modulation of the drain currents between M_{bias1} and M_{L-1}.

PAGE 7: Simulated Bode Plot

- At 100Hz, roughly DC, there is 92.11 dBV ≈ 40.32 kΩ
- 3dB below the DC gain is 92.11-3=89.11dBV
    - This happens at 80.151MHz
- Our ZVTC-predicted BW is 46.54Mhz, as shown on the plot. ZVTC underestimated the 3dB frequency because there are multiple poles at similar low frequencies. This is shown through the τ values being close together.

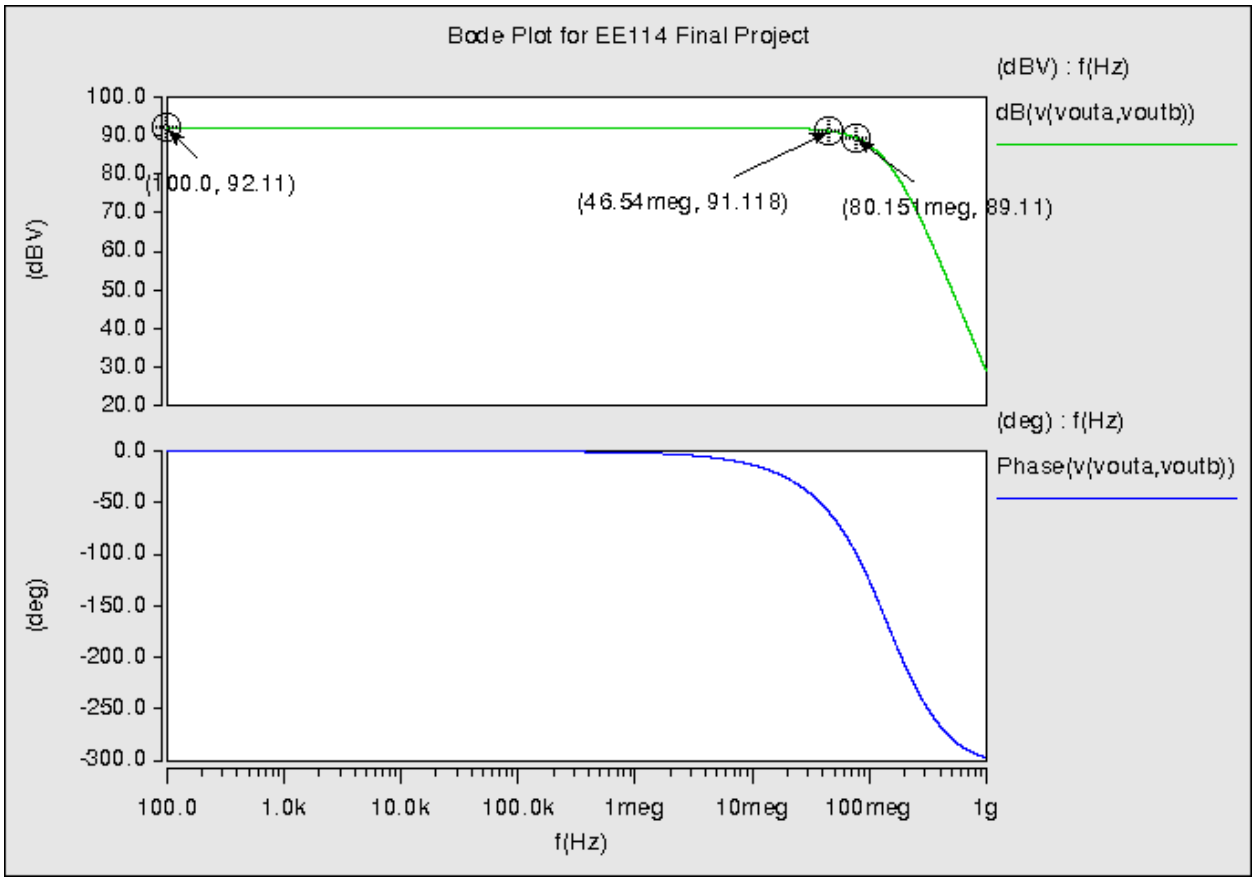
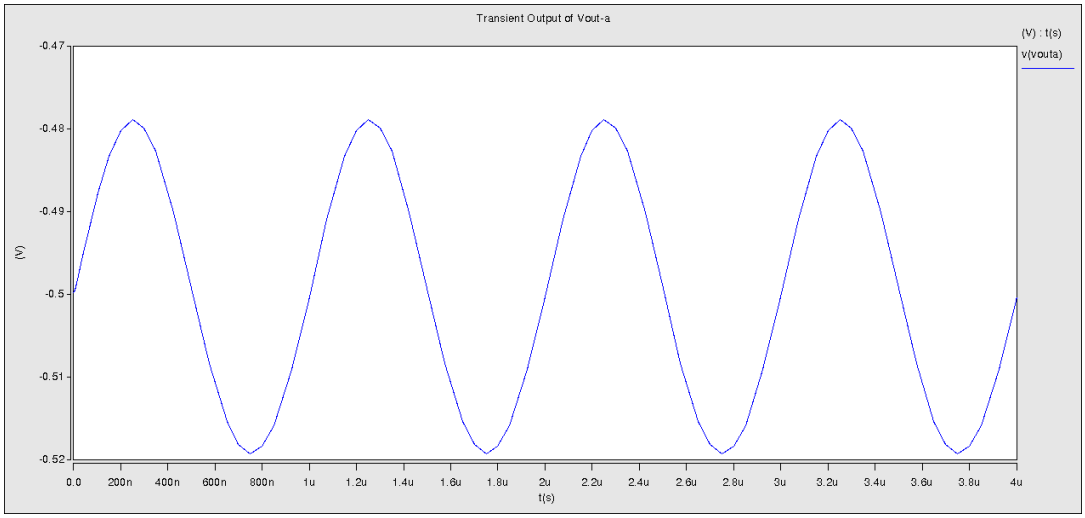


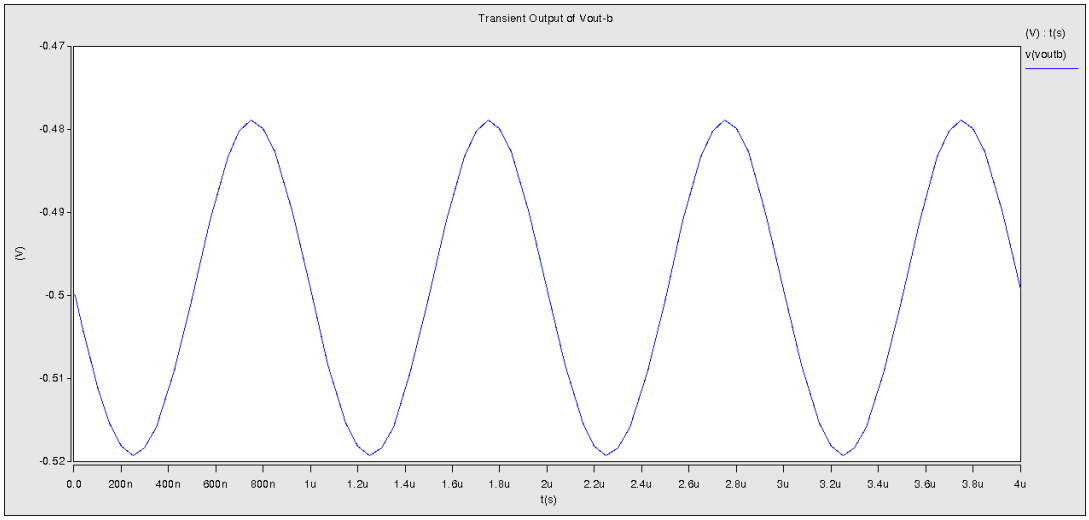
Figure 5 - Bode Plot

As we can see, the magnitude has a distinct roll-off and goes straight down, showing that there are no very high frequency poles.

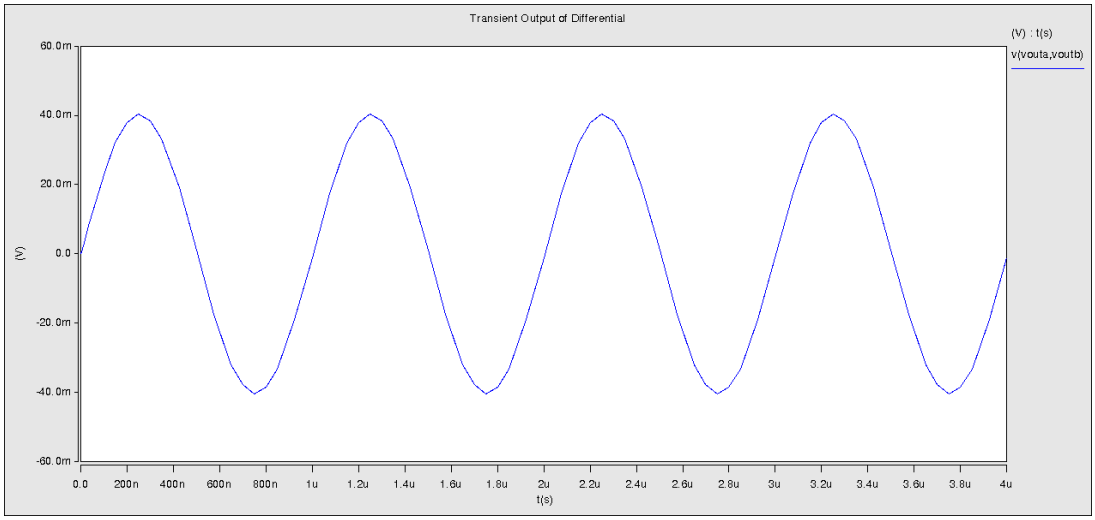
PAGE 8:TRANSIENT OUTPUTS, starting with V_{out-a} (Figure 6):



V_{out-b} (Figure 7):



$V_{DIFFERENTIAL}$ (Figure 8):



Page 9: Comments and Conclusions

Overall, we enjoyed this project as it was a cumulative application to the few semesters we've spent on transistor theory. It's nice to have all these ideas and principles come together during a project, and there is additional benefit in knowing that this is practical. We learned a lot about how to abstract different kinds of amplifiers and learn how they affect a circuit and neighboring stages through power consumption, output/input impedances, bandwidth constraints, gain, parasitic effects, and even body effect. We enjoyed how despite the architecture was given to us, there was enough to investigate for us to learn how ICs work. That being said, we felt that the write-up was a bit too tedious. Although, it is necessary to show the design thinking, it doesn't have to be so in-depth. It could also be helpful to have some of the write-up required for the checkpoints. Again, all in all, it was a great project and we learned alot.

As for the results, we were pretty proud of our power consumption. There wasn't much wiggle room with bandwidth, gain, or CM output voltage in our final netlist, so we are confident that this is the best we could do given the architecture. We were able to increase the FOM significantly with a different architecture, which we felt demonstrated in-depth understanding of where issues lied with this circuit.

As for things we struggled with, starting was the hardest part. Even though we were able to see the large-scale influences, bottlenecks, and things, it was hard to randomly pick a size for a transistor and say "let's see what happens." Although, I believe our prudence allowed us to start at a good starting point, which allowed fine adjustments to reach the desired parameters. Another thing we struggled with was keeping the CM voltage above -.5V, which we were able to keep low by increasing the g_m and V_{ov} of the final transistor.

APPENDIX 1:

```
* Design Problem, ee114/214A- 2014
* Team Member 1 Name: Charles Guan
* Team Member 2 Name: Vikram Prasad
* btw(Both members enrolled in 114)
* Please fill in the specification achieved by your circuit
* before you submit the netlist.
*****************************************************************
* sunetids of team members = cguan2, vprasad2
* The specifications that this script achieves are:
* Power  =   1.1489mW
* Gain   =    40.3187 kilo-ohms
* BandWidth =   80.1489 MHz
* FOM = 2812.69 kilo-ohms*MHz/mW
*****************************************************************

** Including the model file
.include /usr/class/ee114/hspice/ee114_hspice.sp

* Defining Top level circuit parameters
.param Cin = 100f
.param CL  = 250f
.param RL  = 20k

* defining the supply voltages

vdd vdd 0 2.5
vss vss 0 -2.5

* Defining the input current source

** For ac simulation uncomment the following 2 lines**
Iina            iina    vdd     ac      0.5
Iinb            vdd     iinb    ac      0.5

** For transient simulation uncomment the following 2 lines**
*Iina           iina    vdd     sin(0 0.5u 1e6)
*Iinb           vdd     iinb    sin(0 0.5u 1e6)

* Defining Input capacitance

Cina    vdd     iina 'Cin'
Cinb    vdd     iinb 'Cin'
```

```
* Defining the differential load

RL      vouta           voutb           'RL'
CL      vouta           voutb           'CL'

*** Trans-impedance Amplifier ***
***     d       g       s       b       n/pmos114    w       l

*** A Side ***
M1a     vxa     0       iina    vss     nmos114      w='W1'   l='L1'
Mbias1a iina    vbiasn  vss     vss     nmos114      w='WB1'  l='LB1'
ML1a    vxa     vbiasp  vdd     vdd     pmos114      w='WL1'  l='LL1'
Rua     vdd     vxa     'RU'
Rda     vxa     vss     'RD'
M2a     vya     vxa     vz      vss     nmos114      w='W2'   l='L2'
Mbias2a vz      vbiasn  vss     vss     nmos114      w='WB2'  l='LB2'
ML2a    vdd     vdd     vya     vss     nmos114      w='WL2'  l='LL2'
M3a     vdd     vya     vouta   vss     nmos114      w='W3'   l='L3'
Mbias3a vouta   vbiasn  vss     vss     nmos114      w='WB3'  l='LB3'

*** B Side ***
*NAME D G S B MODEL WIDTH LENGTH
M1b     vxb     0       iinb    vss     nmos114      w='W1' l='L1'
Mbias1b iinb    vbiasn  vss     vss     nmos114      w='WB1' l='LB1'
ML1b    vxb     vbiasp  vdd     vdd     pmos114      w='WL1' l='LL1'
ML2b    vdd     vdd     vyb     vss     nmos114      w='WL2' l='LL2'
M2b     vyb     vxb     vz      vss     nmos114      w='W2'  l='L2'
Mbias2b vz      vbiasn  vss     vss     nmos114      w='WB2' l='LB2'
M3b     vdd     vyb     voutb   vss     nmos114      w='W3' l='L3'
Mbias3b voutb   vbiasn  vss     vss     nmos114      w='WB3' l='LB3'
Rub     vdd     vxb     'RU'
Rdb     vxb     vss     'RD'

*** Variables ***
.param W1 = 5u
.param L1 = 1u
.param WB1 = 2u
.param LB1 = 3u
.param WL1 = 3u
.param LL1 = 2u
.param W2 = 3u
.param L2 = 1u
```

```
.param WB2 = 2u
.param LB2 = 4u
.param WL2 = 2u
.param LL2 = 1.6u
.param W3 = 26u
.param L3 = 1u
.param WB3 = 4u
.param LB3 = 2u
.param RU = 90K
.param RD = 90K

*** Current Bias ***


*** Your Bias Circuitry here ***
vbiasn vbiasn 0 -1
vbiasp vbiasp 0 1

* defining the analysis

.op
.option post brief nomod

** For ac simulation uncomment the following line**
.ac dec 1k 100 1g

.measure ac gainmaxa max vdb(vouta)
.measure ac gaindiff max v(vouta, voutb)
.measure ac f3dba when vdb(vouta)='gainmaxa-3'

.measure ac gainmaxb max vdb(voutb)
.measure ac f3dbb when vdb(voutb)='gainmaxb-3'

** For transient simulation uncomment the following line **
*.tran 0.01u 4u
*.probe tran v(vouta,voutb)

.end

********************** END OF FILE************************
```

.op output:

```
****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:iina    =  -1.1860  0:iinb    =  -1.1860  0:vbiasn  =  -1.0000
+0:vbiasp  =   1.0000  0:vdd     =   2.5000  0:vouta   =-499.8061m
+0:voutb   =-499.8061m 0:vss     =  -2.5000  0:vxa     = 159.6333m
+0:vxb     = 159.6333m 0:vya     = 722.6924m 0:vyb     = 722.6924m
+0:vz      =  -1.0801
```

MOSFET listings:

```
**** mosfets


subckt
element  0:m1a      0:mbias1a  0:ml1a     0:m2a      0:mbias2a  0:ml2a
model    0:nmos114. 0:nmos114. 0:pmos114. 0:nmos114. 0:nmos114. 0:nmos114.
region     Saturati   Saturati   Saturati   Saturati   Saturati   Saturati
 id        17.3967u   17.3967u  -20.9441u   12.9437u   12.9437u   12.9437u
 ibs      -13.1403f    0.         0.       -14.1993f    0.       -32.2269f
 ibd      -26.5963f  -13.1403f   23.4037f  -32.2269f  -14.1993f  -50.0000f
 vgs        1.1860     1.5000    -1.5000     1.2397     1.5000     1.7773
 vds        1.3456     1.3140    -2.3404     1.8028     1.4199     1.7773
 vbs       -1.3140     0.         0.        -1.4199     0.        -3.2227
 vth      835.7268m  500.0000m -500.0000m  857.3100m  500.0000m    1.1667
 vdsat    350.2391m    1.0000    -1.0000   382.3907m    1.0000   610.5649m
 vod      350.2391m    1.0000    -1.0000   382.3907m    1.0000   610.5649m
 beta     283.6400u   34.7934u   41.8882u  177.0414u   25.8875u   69.4426u
 gam eff  600.0000m  600.0000m  600.0000m  600.0000m  600.0000m  600.0000m
 gm        99.3418u   34.7934u   41.8882u   67.6990u   25.8875u   42.3992u
 gds        1.5333u  555.5556n  937.5000n    1.0967u  312.5000n  728.1045n
 gmb       20.4973u   11.6701u   14.0497u   13.6312u    8.6829u    6.3419u
 cdtot      6.8305f    4.4161f    5.0844f    4.7074f    4.3730f    3.4405f
 cgtot     12.7936f   11.2922f   12.3111f    7.6741f   14.3922f    6.9545f
 cstot     15.2679f   14.8000f   16.5500f    9.9980f   17.8667f    8.6475f
 cbtot      9.5173f    8.0599f    9.4593f    7.1462f    8.0288f    5.1943f
 cgs       10.1667f   10.2000f   10.7000f    6.1000f   13.2667f    5.9067f
 cgd        2.5206f    1.0242f    1.5431f    1.5166f    1.0348f    1.0174f
```

subckt						
element	0:m3a	0:mbias3a	0:m1b	0:mbias1b	0:ml1b	0:ml2b
model	0:nmos114.	0:nmos114.	0:nmos114.	0:nmos114.	0:pmos114.	0:nmos114.
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	55.0005u	55.0005u	17.3967u	17.3967u	-20.9441u	12.9437u
ibs	-20.0019f	0.	-13.1403f	0.	0.	-32.2269f
ibd	-50.0000f	-20.0019f	-26.5963f	-13.1403f	23.4037f	-50.0000f
vgs	1.2225	1.5000	1.1860	1.5000	-1.5000	1.7773
vds	2.9998	2.0002	1.3456	1.3140	-2.3404	1.7773
vbs	-2.0002	0.	-1.3140	0.	0.	-3.2227
vth	967.3705m	500.0000m	835.7268m	500.0000m	-500.0000m	1.1667
vdsat	255.1280m	1.0000	350.2391m	1.0000	-1.0000	610.5649m
vod	255.1280m	1.0000	350.2391m	1.0000	-1.0000	610.5649m
beta	1.6900m	110.0010u	283.6400u	34.7934u	41.8882u	69.4426u
gam eff	600.0000m	600.0000m	600.0000m	600.0000m	600.0000m	600.0000m
gm	431.1599u	110.0010u	99.3418u	34.7934u	41.8882u	42.3992u
gds	4.2309u	2.5000u	1.5333u	555.5556n	937.5000n	728.1045n
gmb	77.2975u	36.8954u	20.4973u	11.6701u	14.0497u	6.3419u
cdtot	25.0892f	6.1701f	6.8305f	4.4161f	5.0844f	3.4405f
cgtot	66.7669f	16.4064f	12.7936f	11.2922f	12.3111f	6.9545f
cstot	68.3013f	20.4667f	15.2679f	14.8000f	16.5500f	8.6475f
cbtot	27.9453f	10.4116f	9.5173f	8.0599f	9.4593f	5.1943f
cgs	52.8669f	14.2667f	10.1667f	10.2000f	10.7000f	5.9067f
cgd	13.2392f	2.0491f	2.5206f	1.0242f	1.5431f	1.0174f

subckt				
element	0:m2b	0:mbias2b	0:m3b	0:mbias3b
model	0:nmos114.	0:nmos114.	0:nmos114.	0:nmos114.
region	Saturati	Saturati	Saturati	Saturati
id	12.9437u	12.9437u	55.0005u	55.0005u
ibs	-14.1993f	0.	-20.0019f	0.
ibd	-32.2269f	-14.1993f	-50.0000f	-20.0019f
vgs	1.2397	1.5000	1.2225	1.5000
vds	1.8028	1.4199	2.9998	2.0002
vbs	-1.4199	0.	-2.0002	0.
vth	857.3100m	500.0000m	967.3705m	500.0000m
vdsat	382.3907m	1.0000	255.1280m	1.0000
vod	382.3907m	1.0000	255.1280m	1.0000
beta	177.0414u	25.8875u	1.6900m	110.0010u
gam eff	600.0000m	600.0000m	600.0000m	600.0000m
gm	67.6990u	25.8875u	431.1599u	110.0010u
gds	1.0967u	312.5000n	4.2309u	2.5000u
gmb	13.6312u	8.6829u	77.2975u	36.8954u
cdtot	4.7074f	4.3730f	25.0892f	6.1701f
cgtot	7.6741f	14.3922f	66.7669f	16.4064f
cstot	9.9980f	17.8667f	68.3013f	20.4667f
cbtot	7.1462f	8.0288f	27.9453f	10.4116f
cgs	6.1000f	13.2667f	52.8669f	14.2667f
cgd	1.5166f	1.0348f	13.2392f	2.0491f

APPENDIX 2:

Limitations of original circuit
As noted in the ZVTC Bandwidth approximation, all poles are close together. Therefore, it is difficult to reduce power consumption without affecting the bandwidth. We can reduce the resistance at different nodes, but this method will sacrifice gain.

Motivation for improving bandwidth
Decreases in power will improve the figure of merit much more readily than increases in bandwidth. However, we can then sacrifice that improved bandwidth to decrease power.

Another limitation that was not addressed is the body effect of ML2 increasing Vth to 1.2V. This limits the swing at Vy due to Vout limitations.

Proposed change 1
The current architecture uses a PMOS current source (M_{L-1}), so Ru and Rd can semi-independently bias the gate of M2 regardless of I_1. However, this drains unnecessary current through the Ru-Rd branch. We can replace Ru, Rd, and M_{L-1} with a single drain resistor to reduce power and the the M_{L-1} capacitance.

Proposed change 2
The input node pole node is somewhat slow due to the need for a low impedance at Iin, which in turn requires a high drain current or large size at M1. In order to decrease this impedance, we replace M1 with the modified common gate using feedback from Homework 6, Problem 5. The configuration decreases input resistance by a factor of $\frac{1}{g_m r_o}$ and pushes this pole to a much higher frequency. We can then decrease power in all branches of the circuit and sacrifice some of the increased bandwidth.

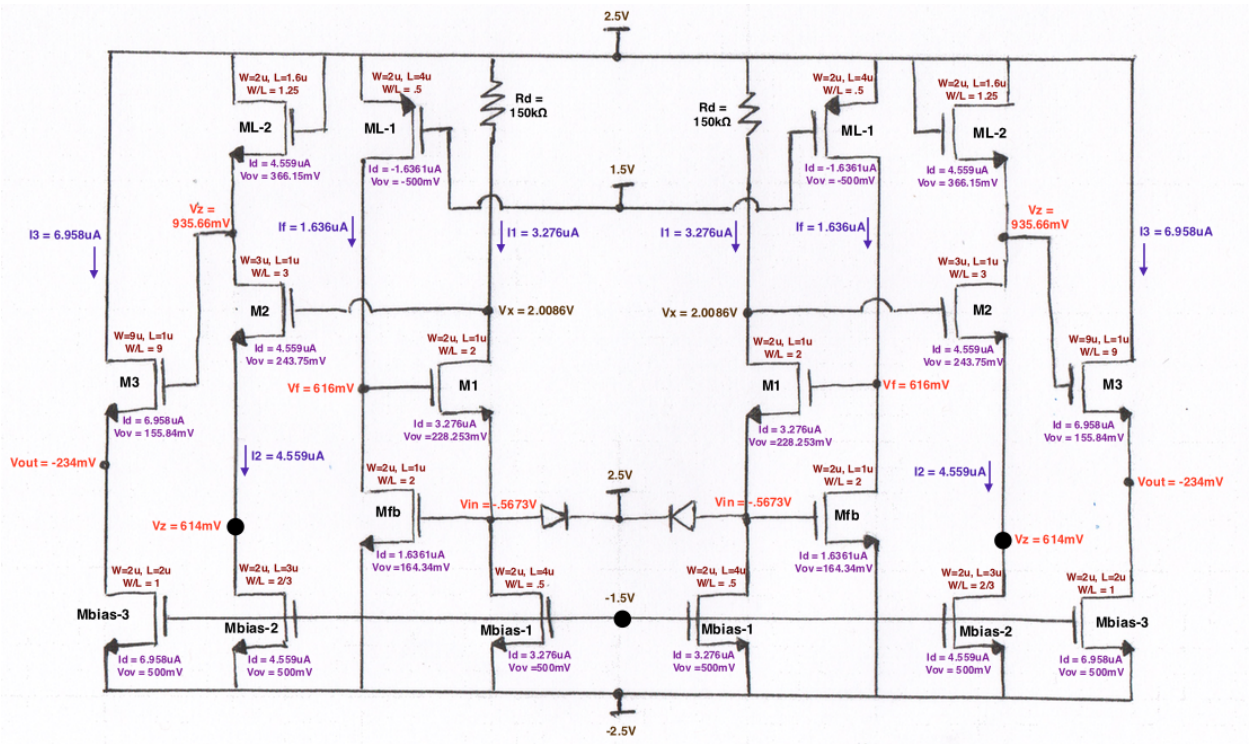


Figure 9 - Schematic of Bonus

Bonus Bode:

- At 100Hz, roughly DC, there is 98.426 dBV ≈ 83.425 kΩ
- 3dB below the DC gain is 98.426-3=95.426dBV
    - This happens at 83.895MHz

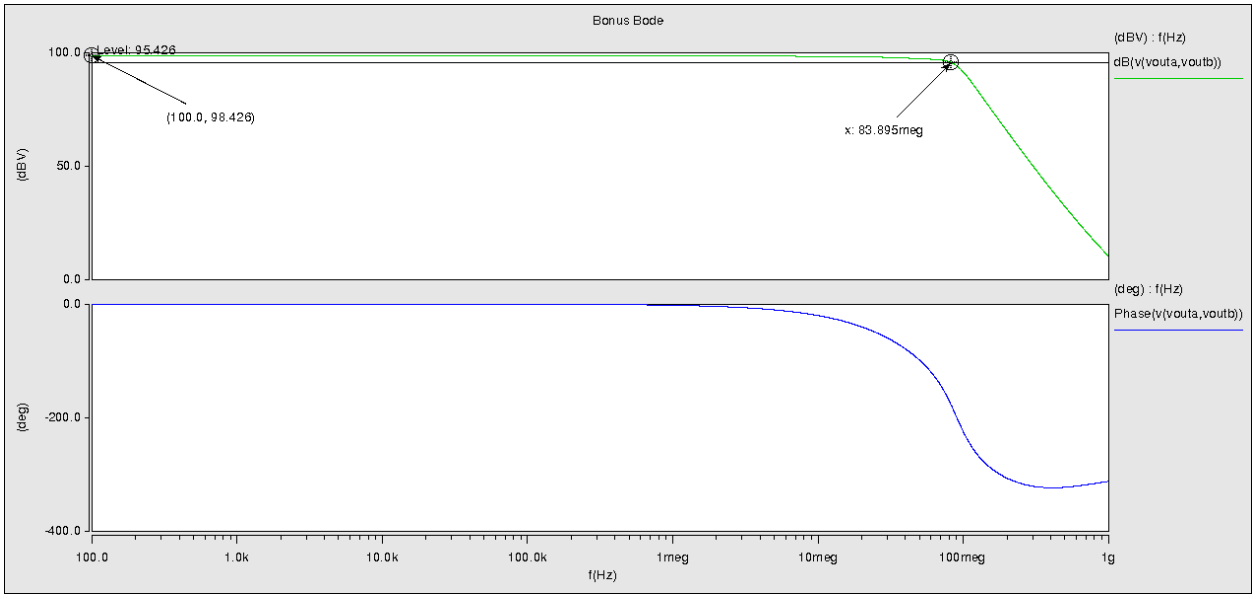


Figure 10 - Bode Plot of Bonus

Figure 11: Tabulated specifications (including comparison of given and new architecture):

	Given	Given Architecture	New Architecture
FOM: (Gain x Bandwidth) / (Power dissipation)	1600 kΩ.MHz/mW	2812.69 kΩ.MHz/mW	43357 kΩ.MHz/mW
Power dissipation	$\leq$ 2 mW	1.1489 mW	.161422 mW
Small-signal trans-resistance gain (A = v out /i in)	$\geq$ 40 kΩ	40.3187 kΩ	83.422 kΩ
-3dB Bandwidth	$\geq$ 80 MHz	80.1489 MHz	83.8974 MHz
Common mode output voltage	-0.5 V $\leq V_{out} \leq$ 0.5 V	-0.49980 V	-.234 V
Gate overdrive (V_{ov})	$\geq$ 150 mV	$\geq$ 255 mV	$\geq$ 155 mV
$L_{current\_source}$	$\geq$ 2 µm	$\geq$ 2 µm	$\geq$ 2 µm
Matching parameters? (A vs. B)	Yes	Yes	Yes
Integer widths and lengths?	Preferred	Utilized (except for L_{M-L2} = 1.6 µm)	Utilized (except for L_{M-L2} = 1.6 µm)
Core Circuit Area (including resistance)		450.4 $(\mu m)^2$	386 $(\mu m)^2$
Resistor Area (W = 1 µm)		360 $(\mu m)^2$	300 $(\mu m)^2$