DESIGN PROJECT

Check-point #1: Wednesday, November 19, 2014, 4pm PT
Check-point #2: Monday, December 01, 2014, 4pm PT
Final Deadline: Thursday, December 04, 2014, 4pm PT

1. Overview and Specifications

The first task at your new job at Photonic Interface Systems, Inc. ("PHI-SYS," a new sensor-based startup company) is to design an optical sensor circuit. The system level block diagram is shown in Figure 1. As you can see, the system is fully differential, with the photo-diode at the input modeled as a current source with a capacitor. The output is a differential RC load which typically represents the loading effect from the subsequent stages. The circuit details are shown in Figure 2.
Due to time-to-market constraints, your manager insists that you do not change the architecture of the circuit (except for the bonus part of the project). Your goal is to size all of the MOSFETS (and resistors, as needed) to meet the following objectives:

Parameter	Specification
Technology	EE114 1-µm CMOS (Nominal device parameters)
Operating temperature	25 ºC
V_{DD} / V_{SS}	+/- 2.5 V
Output load resistance (differential), R_L	20 kΩ
Output load capacitance (differential), C_L	250 fF
Input load capacitance (C_{in} from each node to V_{DD})	100 fF
Common mode output voltage	Between -0.5 and 0.5 V
Power dissipation	≤ 2 mW (**minimize as much as possible!**)
Small-signal trans-resistance gain ($A = v_{out}/i_{in}$)	≥ 40 kΩ
Magnitude response of gain in Bode plot	Should be flat and then roll-off (no overshoot)
Large-signal time-domain simulations	0.5 µA, 1 MHz sine wave
-3dB Bandwidth	≥ 80 MHz
Figure of Merit (FOM) = (Gain x Bandwidth) / (Power dissipation)	≥ (40 x 80)/2 = 1600 kΩ.MHz/mW

In addition to these primary specifications, a major goal of PHI-SYS is to create the most robust product on the market. For example, all designers at PHI-SYS must refrain from using academically small currents in biasing the circuit. In addition, the current source devices must have at least twice the minimum channel length. Your manager sets the following guidelines for you—leading you directly on both simplifying the design and for improvement of PVT performance (not considered explicitly):

Parameter	Specification
$L_{current\_source}$ (all devices used in current sources)	≥ 2 µm
Gate overdrive (V_{OV}) for all devices	≥ 150 mV
All transistors match- A & B	Matching--- pair-wise
L values match- A & B	Matching---L values
Integer device widths (and lengths) preferred	ΔL_{min}, ΔW_{min} = 0.2 µm

<u>Bonus Problem</u> (for this part, we recommend reading research papers to investigate different circuit techniques for improving gain, bandwidth and reducing power consumption of amplifiers):
(1) Do a thorough analysis of your circuit and explain what parts of the circuit limit the FOM in your design.
(2) Suggest modifications to the architecture that can help you further improve the FOM by **<u>30 %</u>** of what you achieved using the given architecture. For achieving an improvement in FOM, you can make modifications to increase the gain, increase the bandwidth or further reduce the power dissipation (or

do some combination of these). However, your circuit should still meet all the other specifications listed in the two tables above.
(3) Design and simulate your new circuit demonstrating the improvement in FOM.
(4) There is only one deadline for submitting the bonus part and that is the final deadline (Thursday, Dec 04, 2014). No check-point submissions for the bonus part.
NOTE: the grading for the bonus part will not be based merely on the FOM number you achieve finally. It will be very subjective, based on the insights you present about the limitations of your original circuit and your explanation of proposed architectural modifications. So, please refrain from blindly tweaking your circuit in spice – even if you achieve a very good FOM by doing that, you will not get any points unless you back it up with a solid explanation.

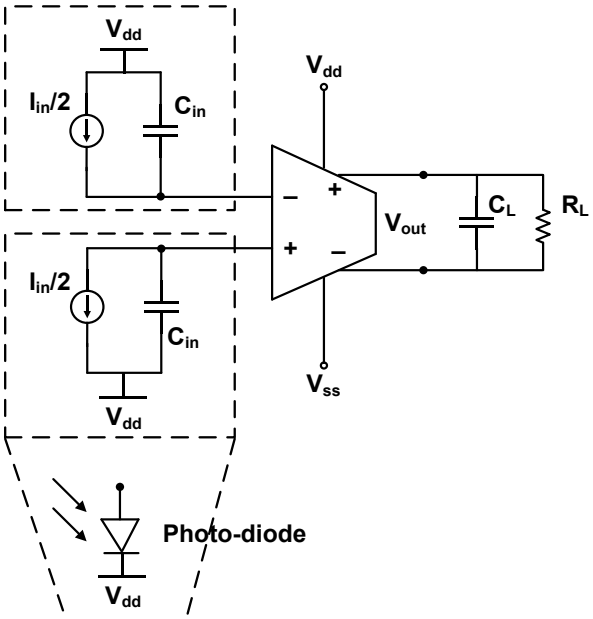

Figure 1: System Level Block Diagram (i.e. replace photo-diodes as shown)

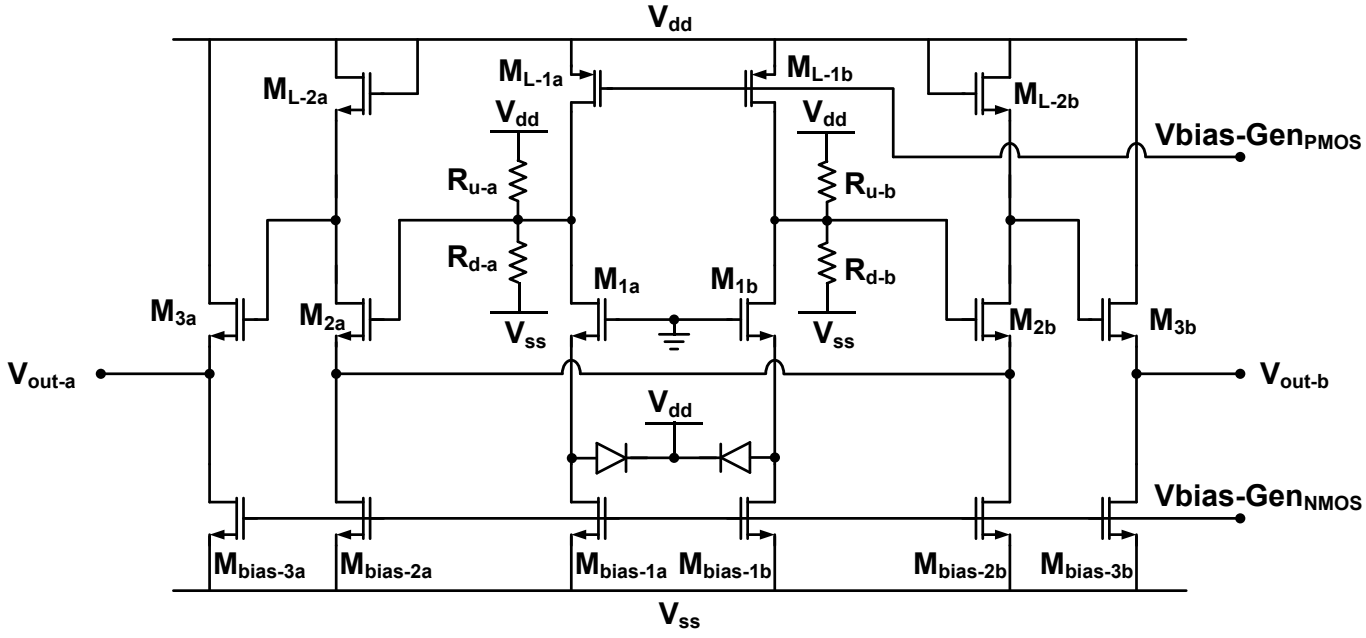

Figure 2: Circuit Architecture

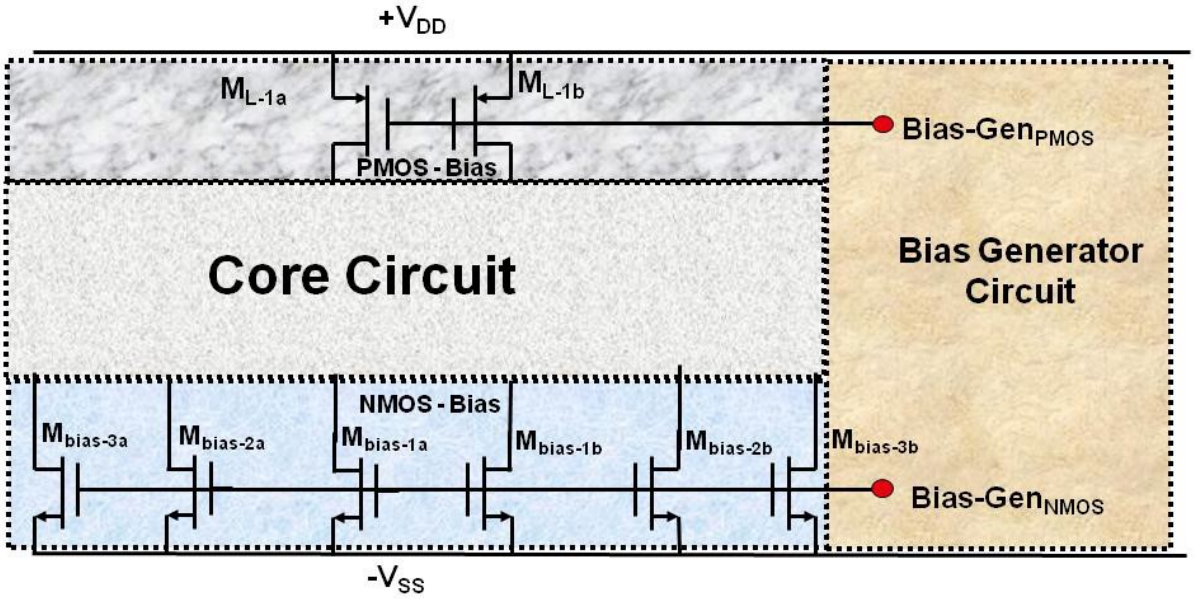

Figure 3: Complete system with bias generator circuit

In addition to the constraint mentioned about minimum L, you should keep ratios of W values in a reasonable range. That is, ratios greater that 30:1 between devices is strongly discouraged (this is an area and layout set of problems).

Say, your NMOS device in the bias generator circuit has W/L = ***y***, then

$(W/L)_{Mbias\text{-}3a + Mbias\text{-}2a + Mbias\text{-}1a + Mbias\text{-}3b + Mbias\text{-}2b + Mbias\text{-}1b} <= 30\boldsymbol{y}$

It is your job to size all devices to meet the specifications. Figure 3 shows the complete system architecture with bias generator circuit.

a. Students enrolled in EE 214A have to design a completely functional bias generator circuit to bias the core. The only ports available to you are V_{DD} and V_{SS} along with differential input and output ports.
b. Students enrolled in EE 114 need to only properly size the NMOS/PMOS current source devices. You are not required to design the rest of the bias generator circuit. You can connect ideal voltage sources to $Bias\text{-}Gen_{NMOS}$ and $Bias\text{-}Gen_{PMOS}$ nodes.

All students need to provide the supporting circuit documentation as generally outlined below. For simplicity in this short project, you are not required to verify the design across PVT variations. In practice, this would be the next logical step after getting your "nominal" design to work. You may work on this project alone or in teams of two. Each team must submit one project report as specified below. You are encouraged to discuss the design problem with other teams, but your design implementation must be unique. Under no circumstances should you exchange computer files with other teams; this would constitute a gross violation of the honor code.

2. Suggested Design Flow

a) Read this entire handout **thoroughly (all 8 pages)!**

b) Find a project partner (if you haven't already done so).

c) Familiarize yourself with the schematic in Figure 2 and try to identify how the key blocks interact. Draw simplified half-circuit models (differential) of the circuit that will allow you to identify the "main knobs" in the design.

d) Get a SPICE version of the circuit working with your best estimates (based on c) above). **Check Point #1** will be a submission of your working deck as of **Wednesday, November 19, 2014.** This is a "go-no-go" milestone that does have points associated with it; your deck will be tested but the results (i.e. power and details of biasing) will not be quantified, other than functionality. Your circuit does not necessarily have to meet all specs at this point, but it should achieve reasonable values for gain, bandwidth, power etc. (i.e. you should not have negative dB gain, very low bandwidth etc.). If your circuit does not work at all, chances are that you have made a mistake while entering the netlist (get a working Spice deck, with nominal parameters for the real circuit and keep modifying it as noted below). Please double-check your spice file before submitting for this check-point; due to the way we run the checks you will get zero points if your spice file fails to run on our side, even if it is because of a very minor mistake in the file. Also, the filename of your submission should be **CP1_<Name1>_<Name2>.sp** (e.g. CP1_Jayant_Charthad_Simon_Basilico.sp)

e) Setup a MATLAB script (or other scripting tool and the needed supporting plots, spread sheets etc.) that allows you to target your design efforts and then to optimize your design iteratively without repetitive "Spice monkeying." Identify the key variables that you will focus on (these are not W/L ratio values, that is almost as bad as "Spice monkeying"); calculate important time constants based on reasonable design choices. Make sure you develop plotting/visualization of variables (and label them with design-specific information—not "Variable 1" etc. that only you understand).

f) We will have a Design Project overview lecture with initial example of a previous trans-resistance amplifier design that illustrates the steps needed in a design process—especially the setting up of key variables used to explore the design space. But, absolutely (!!) do not wait to hear this Lecture in class, get started ASAP. The big changes here, compared to piece-meal examples given in the several homework assignments to date, are in having multi-stages (fully differential) and more complex specifications that require concurrent trade-offs.

g) Modify your design, according to "educated choices," coming from your scripting and the related design curves (see item e) and use visualization to help you!; simulate your modified design in Spice; compare the results to your hand calculations, and make adjustments. Inspect and track down unexpected discrepancies (i.e 3dB bandwidth estimate is one good example, body effects is another). Make sure all devices are operating in their desired region (i.e. Saturation!). Do not immediately blame your problems on Spice; be thorough and critical in checking your assumptions, netlists and calculations. **Check Point #2**, **Monday, December 01, 2014**; we will record data from this working Spice file which should include all biasing circuits. Once again, please double-check your spice file before submitting; you will get zero points if your spice file fails to run on our side, even if it is because of a very minor mistake in the file. Also, the filename of your submission should be **CP2_<Name1>_<Name2>_power_gain_bandwidth_FOM.sp** (e.g.

if we achieved a power of 2.0 mW, a gain of 40.0 kΩ and a bandwidth of 80.0 MHz, then our filename would be CP2_Tao_Yaoyu_Chris_Vassos_2p0_40p0_80p0_1600.sp)

h) To get you started with Hspice, we are providing a top level file (DP_2014_top_level.sp) that you can download from class website. This file has definition for input stimulus, output load along with different sections to run ac and transient simulation. You still need to write your own netlist for circuit architecture and your bias circuitry. DO NOT make changes to the existing statements in the spice file since our test uses it to simulate your design (i.e. required submissions and "check points").

i) Begin to write your project report (see below) at least several days before the deadline. Actually, as you develop and refine your approach, scripting and design targets, this is a perfect time to write that part up (before the final "crunch time"). Your grade will strongly depend on the quality of your write-up, and not just the achieved performance specifications. Write an insightful, well-documented report that clearly shows how you got your best results. Clarity in how you approach the design, meaningful figures that show the most important design trade-offs and road map of how you progressed in optimizing your design, are all critical. Your audience—the professor (a.k.a. your PHI-SYS "manager") and the TAs—want to see an insightful document, not listings of equations and raw results and tables.

A practical hint: The first design you simulate does not have to be and probably should not look exactly like the final circuit, including the full current source implementation. E.g., there is no need to implement all the complete biasing in the very beginning, but using actual MOS devices rather than idealized current sources is best. Once your simplified design works, it is fairly easy to add the supporting circuitry for setup and biasing of the current sources.

Finally, keep in mind that this project involves a great deal of just plain old labor; it takes significant amounts of time to determine suitable design choices, run all the necessary simulations and document your work; don't delay in getting started (actually, that's why we've added Check Points #1 and #2 to keep you moving! ;); there is not a new Problem Set out yet (there is only one graded homework left on Feedback and Frequency Response) so you should have lots of "free time" (for this class anyway ;)). Also, the instructional computers and printers have been known to slow down and even go down at the worst possible times. We will be largely unsympathetic to pleas for extensions arising from such problems.

3. Project Report

Your team is required to prepare a single hardcopy report. Submit your report in the same manner you submitted your homework, promptly by the stated deadline—**Thursday, December 04, 2014.** We will not grant any extensions!!

A hand-written report is fine, but neatness is critical. In case you decide to submit a computer-generated report, make sure to use font size of 12 pt. Be sure to follow the formatting instructions below ***EXACTLY (Please note that in pages 0-9 and Appendix I you should only report the non-bonus part of the project; Appendix II is for the bonus part of the project)***:

Page 0: Cover page. Clearly indicate the names of the team members. Also provide a table comparing the given specs and achieved spec (remember this is for the NON-BONUS part of the project only). You also need to provide us a percentage–wise break down of area consumed by different sections of bias circuit (NMOS-bias, PMOS-bias & Bias generator circuit) as compared to your core circuit area

(refer to Figure 3). For area calculation, use A_{MOS} = W * L. Also include the area of resistors in your design. Assume that the sheet resistance is 1 kΩ/□ and the minimum length of resistor is 1 μm.

Page 1: Outline of your design. How did you approach this problem? What are some of your key design choices? Flow charts and graphs of how the trade-offs are connected provide the best clarity in explaining (we'll show some examples in class). Half of the grading (i.e. 25 Points) is related to Design Flow, Insight and Optimization. The clarity of your discussion and insight you give, starting on Page 1, is a major factor in doing well for these 25 Points.

Page 2: Schematic diagram of your final design, with component values (i.e. W, L values etc.), node voltages and bias currents (from Spice .op simulation) clearly labeled (Spend time to make this schematic complete, readable and clear!). Show component values right next to the components, and currents next to the branches (i.e., absolutely, positively do not make us refer to a look-up table!). **Annotate all transistors** with their drain current, gate overdrive V_{OV} (from Spice .op simulation) and W/L.

Pages 3-6: Calculation of key design parameters, such as transconductances, bias currents, etc. This is the most important section of your report for giving critical discussion! Compare the most relevant hand calculated values with final Spice values in a table and discuss discrepancies (percentage differences will be clear, you need to show you understand them). Make sure to include the total power dissipation of your design (calculated value and Spice result). The lowest power designs will not automatically score the highest grades. The methodology you used to justify your design choices and component values is far more important (see section on point distribution below).

Page 7: Simulated Bode Plots of A(jω), phase and magnitude. Clearly annotate the achieved gain and bandwidth. Annotate your hand-calculated values in the same plots, noting any specific features of interest (either from the results themselves or based on what you've learned in hand calculations or scripting the design). Plots must be annotated with meaningful comments/observations.

Page 8: Show a transient simulation plot for each output individually and the differential output with a 1 MHz, 0.5 μA sinusoidal differential input current. Make sure that there is no distortion in any of these waveforms.

Page 9: Comments and conclusion. Here, you can convey issues you may have had, or things you've learned/not learned in this project.

Appendix I: Final Spice netlist and .op output. Include only the MOSFET and node voltage listing from the .op output.

Appendix II (up to 5 pages maximum): If you attempted the bonus problem, describe the limitations of the original circuit and your proposed changes to the architecture of this circuit. Draw a schematic diagram of your final design with new architecture (follow instructions similar to those for page 2) and explain how it helps you achieve a 30 % higher FOM. Include the simulated bode plots of A(jω), phase and magnitude annotating the new gain and bandwidth you achieved. On the final page, include a table comparing given specs, achieved specs using given architecture and achieved specs for your new architecture.

4. Project Milestones

Milestones	Due Date	Deliverables	Grading
Check Point #1	Nov. 19th (Wednesday), 4pm	Submit working netlist (minimal) on coursework (only non-bonus part)	5 points
Check Point #2	Dec. 1st (Monday), 4pm	Submit working netlist on Coursework (only non-bonus part). This netlist- • Should meet all specs • Might not be 100% optimized	3 points of the grading for item 4 (Power)
Final Deadline	Dec. 4th (Thursday), 4pm	Submit final netlist (and netlist for bonus part if you attempted that) on Coursework. This netlist- • Should meet all specs • Should be 100% optimal Submit Project Report in the HW dropbox.	7 points of the grading for item 4 (Power)

- Your final netlist should have filename: Final_<Name1>_<Name2>_power_gain_bandwidth_FOM.sp (e.g. Final_Jayant_Charthad_Simon_Basilico_2p0_40p0_80p0_1600.sp)**.**
- Your netlist for bonus part should have filename: Bonus_<Name1>_<Name2>_power_gain_bandwidth_FOM.sp
- For naming convention for check-point submissions, please read the instructions in section 2 of this handout.

5. Late Submission Policy

Our policy for late submission of any part of the project is similar to the homeworks. The deadline for each check-point of the project is at 4pm. After 4pm we will deduct 20% of the total score per hour for that part of the project. If you submit after 6pm, you will get zero points for that part of the project. Please note: we will follow this very strictly and there will be no exceptions. Be aware that close to deadlines, corn servers sometimes become slow. However, since we are giving you ample time for this project, we expect you to not keep things for the last minute and get into any major issues due to the server.

6. Grading

1. Design Flow, Insight and Optimization Strategy	25 points
2. Documentation	5 points
3. Specs and Practicality	10 points
4. Power (see **Check Point #2** = 3 pts.) + 7 pts. =	10 points
5. Check Point #1 (go=5 pts.; no-go=0 pts.)	5 points
6. Bonus	10 points
Total (Report and Performance Metrics)	55 points + 10 bonus

	Aspect	**Excellent**	**Not that great**	**Poor**
1.	Design Flow	Well structured, clear and reasonable decisions with plots of trade offs	Well structured, but unjustified decisions and too much un-filtered data	Unclear how design point was reached (likely poor choices in design variables)
	Discrepancies between hand analysis and simulations	Well explained and/or within reasonable bounds	Simply restating the obvious about tables and results	No discussion of discrepancies and potential sources
	Misconceptions	None	Minor	Not clear if students understand their design
2.	Schematics & annotation	Clearly labeled (someone else could easily understand it)	Somewhat unclear (only some parameters listed)	Unreadable schematics, component values missing, …
	Plots	Clear, good zoom and annotation	Somewhat sloppy, e.g. no zoom, no labels.	Some plots missing or unreadable.
3.	a) Design constraints and Practicality	All satisfied		Impractical design , e.g. tail current source in triode region, …
	b) Netlist	Looks OK and has comments that help to follow it	Raw netlist (no pointers to anything)	Clearly buggy, not clear how results were generated
	c) Specs	All met and results look consistent	One specification barely missed	Several specifications missed or design does not work
4.	Power	Computed based on ranking (0…10 points)		