TI Designs

10s Battery Pack Monitoring, Balancing, and Comprehensive Protection, 50-A Discharge Reference Design

1 TI Designs

The TI Design TIDA-00449 is a ready, tested hardware platform for 10 cells in series battery pack monitoring, balancing, and protecting for power tools. Power tools increasingly use highly power dense Li-ion or Li-iron phosphate cell-based battery packs that need to be protected from explosion due to incorrect charging or discharging. The TIDA-00449 also achieves thermal requirements for power tool battery packs when discharging at high continuous current.

2 Design Resources

TIDA-00449	Design Folder
BQ7693003DBT	Product Folder
CSD19536KTT	Product Folder
CSD23381F4	Product Folder
CSD13381F4	Product Folder
LMT01LPG	Product Folder
MSP430G2553IPW20	Product Folder
TPS3839G33	Product Folder

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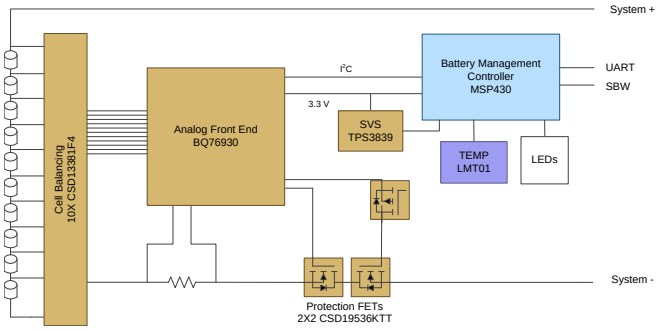
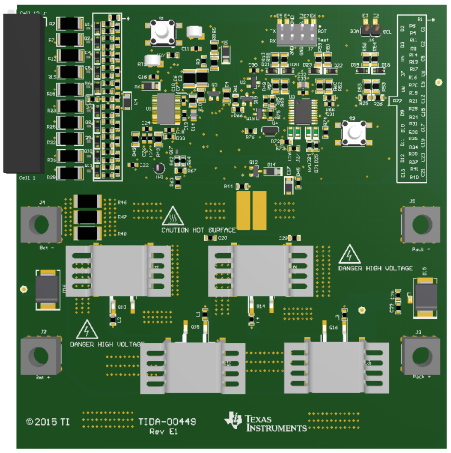
3 Design Features

- Battery Pack Designed for 36-V (10-Cell Li-Ion or Li-Iron Phosphate Based), 50-A Max Continuous Discharge Current
- Monitors Cell Voltages, Pack Current, Pack Temperatures, Balances Cells, and Protects by Controlling Charge or Discharge FETs
- Hardware Protection For Overcurrent in Discharge, Short Circuit in Discharge, Overvoltage, and Undervoltage
- Ultra-Small Footprint, Low On-Resistance, Low Q_g and Q_{gd} FemtoFET™ MOSFETs on Board for Passive Balancing Current up to 150 mA per Cell
- Low Quiescence Current, Ultra-Low Power State for Shipment
- Onboard Host Microcontroller to Enable Implementation of Battery Fuel Gauging

4 Featured Applications

- Battery-Powered Power Tools
- Battery-Powered Garden Tools
- Vacuum and Garden Robots





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5 System Description

The battery packs of power and garden tools are more often using Li-ion, Li-polymer, or Li-iron phosphate cell types. These chemistries are good in both volumetric and gravimetric energy density. While these chemistries provide high energy density and thereby lower volume and weight as an advantage, they are associated with safety concerns. Those concerns are undervoltage (UV) and overvoltage (OV), over temperature (OT), and overcurrent (OC), all which contribute to the accelerating cell degradation and may lead to thermal runaway and explosion.

Combined with the increase in number and size of the battery packs, those safety concerns lead to an increase need of protection, monitoring and balancing. Furthermore space and thermal considerations are also important in battery pack designs.

The TI Design TIDA-00449 provides a tested hardware platform for the cell monitoring, balancing, protecting, and gauging of the battery pack, which uses 10 cells of Li-ion or Li-iron phosphate in series. This design consists of:

- An analog front end (AFE) that monitors the voltage of cells and the battery pack as well as the current and temperature of the pack. The AFE also includes comprehensive protection, including UV and OV, short circuit, and OC protection. It also drives the cell balancing circuit.
- A microcontroller (MCU) used as a battery management controller enables configuring of the AFE's parameters, doing the gas gauging algorithm, doing the cell balancing scheme, handling the fault, and communicating with the system outside the battery pack.
- Protection FETs controlled by the AFE that open the circuit when a fault occurs during charge or discharge.

6 Design Features

The TIDA-00449 uses a 10S3P battery pack (30 to 42 V, 12.6 Ah).

The design must be capable of delivering a continuous discharge current of 50 A and a maximum charge current of 9 A.

The TIDA-00449 must include a comprehensive protection including:

- UV protection at 2.75 V
- OV protection at 4.3 V
- OC protection at 200 A for 40 ms
- Short circuit protection at 300 A for 200 µs

As this battery pack consist of 10 cells in series, cell balancing is also critical. The targeted balancing current is 150 mA at 4.2 V.

7 Block Diagram

Figure 1 shows the system block diagram.

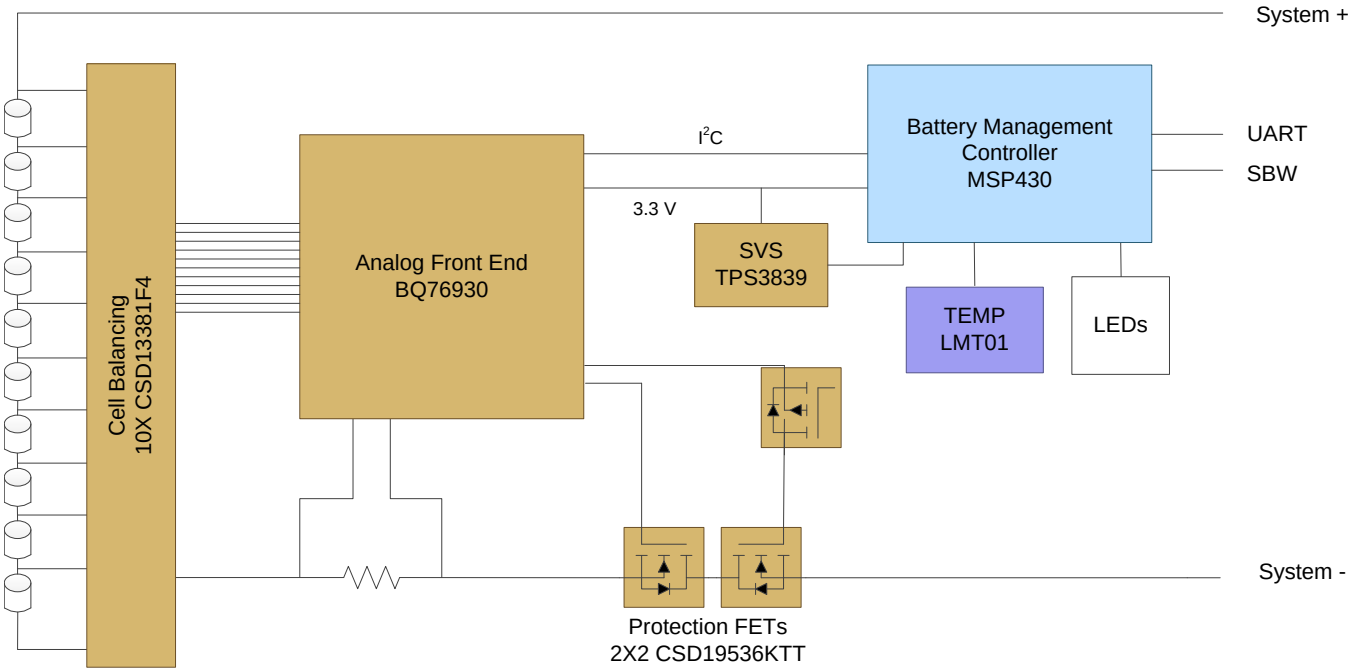


Figure 1. TIDA-00449 System Block Diagram

8 Circuit Design and Component Selection

8.1 AFE

8.1.1 Part Selection

The bq769x0 family of robust AFE devices serves as part of a complete pack monitoring and protection solution for next-generation high-power systems such as power tools. The bq769x0 is designed with low power in mind: Sub-blocks within the IC may be enabled or disabled to control the overall chip current consumption, and a SHIP mode provides a simple way to put the pack into an ultra-low power state.

The bq76930 supports up to 10-cell series or typical 36-V packs. This AFE can measure a variety of battery chemistries, including Li-ion, Li-iron phosphate, and more. Through I^2C, a host controller can use the bq76930 to implement many battery pack management functions such as monitoring (cell voltages, pack current, pack temperatures), protection (controlling charge or discharge FETs), and balancing. Integrated ADCs enable a purely digital readout of critical system parameters with calibration handled in TI's manufacturing process.

8.1.2 Current Sensing

One of the first steps when designing a battery pack monitoring, balancing, and protection circuit is to choose the sense resistor. To do this, consider what are the short circuit current limit (SCD) and the overcurrent limit (OCD) as well as the voltage threshold setting used by the AFE. Please note that further current limit thresholds could be implemented in the battery management controller for a more elaborate protection scheme (see Section 8.2.3.1).

This design aims at ~300 A for 200 μs for SCD and ~200 A for 40 ms for OCD. The voltage threshold settings are available on page 36 and 37 of the bq76930 datasheet (SLUSBK2). The maximum values for the voltage thresholds are 200 mV for SCD and 100 mV for OCD. The Ohm's law gives a 0.67-mΩ maximum sense resistor value for SCD and 0.5-mΩ maximum sense resistor value for OCD as shown in Equation 2 and Equation 3.

$$R_{SENSE} = \frac{V_{THRESHOLD}}{I_{LIM}} \quad (1)$$

So,

$$R_{SENSE\_SCD\_MAX} = \frac{200\ mV}{300\ A} = 0.667\ m\Omega \quad (2)$$

$$R_{SENSE\_OCD\_MAX} = \frac{100\ mV}{200\ A} = 0.5\ m\Omega \quad (3)$$

Therefore, R_{SENSE} was chosen equal at 0.5 mΩ.

The voltage threshold is now recalculated to have 300 A with a 0.5-mΩ sense resistor. Reusing Equation 2 gives a 150-mV voltage threshold for SCD. 150 mV is not in the table on page 36 of the bq76930 datasheet (SLUSBK2), but 155 mV is; therefore, 155 mV is used to give 310 A for SCD.

The maximum continuous current of this application is 50 A, which means that with a sense resistor with 0.5-mΩ, 1.25-W power is being dissipated.

With all this taken into account, including some margin on the power dissipation, three units of 1.5 mΩ, 2512 1% 2-W resistors are used in parallel. The voltage across the sense resistor is continuously monitored using SCD and OCD comparators for the protection. This voltage is also fed to a 16-bit integrated ADC, commonly referred to as the coulomb counter (CC), which measures the accumulated charge across the current sense resistor.

8.1.3 Protection FETs

Now that the sense resistor is selected, the next step is to design the protection FETs.

The purpose of these FETs is to open the circuit in case of a fault. Table 1 shows when the discharge FET (DSG) and the charge FET (CHG) are set to open.

Those two FETs are controlled separately to use the battery pack in a safe condition even if some fault occurs. For example, if the battery pack is fully discharged, the UV fault will be triggered, which opens the DSG FET, preventing further discharge current to flow. Meanwhile, the CHG FET stays closed, allowing a charging current to flow once applied.

Table 1. CHG and DSG Response to Different Events

EVENT	CHG FET OPEN	DSG FET OPEN
OV fault	Yes	—
UV fault	—	Yes
OCD fault	—	Yes
SCD fault	—	Yes
ALERT override	Yes	Yes
DEVICE_XREADY is set	Yes	Yes
Enter SHIP mode from NORMAL	Yes	Yes

In cases where protection FETs are not required, the TIDA-00449 provides two pads for the user to bypass the protection FETs. More details are provided in Section 11.4.

8.1.3.1 FET Selection

To select a FET, take four main parameters into account: the voltage, current, thermal performance, and the switching time of the FET.

The voltage rating of the FET must be higher than approximately 5-V DC per cell in series and 10-V transient per cell in series. In this design, 10 cells are used in series, which means that the FETs (Q13, Q14, Q15, and Q16) should be rated higher than 50-V DC and 100-V transient.

The current requirements of the TIDA-00449 are 75-A continuous, 300 A for 400-µs, and 200 A for 40-ms transient.

Concerning the thermal performance, an R_{DSON} value as low as possible is preferred to minimize the power losses across those FETs. The package is also a key element, as it should be capable to withstand the thermal losses and to dissipate effectively the thermal losses to the PCB or heat sink.

Finally, the time required to turn on and off the FET is critical. It is mainly impacted by the strength of the gate driver in the BQ76930 AFE and on the gate charge of the FET (more details in Section 8.1.3.2).

With all these parameters in mind, this design uses two CSD19536KTT in parallel. The CSD19536KTT is a 100-V, 2-mΩ, ultra-low Q_g and Q_{gd} D^2PAK (TO-263) NexFET™ power MOSFET.

8.1.3.2 FET Driver

The bq769x0 family has FET control outputs referenced to V_{SS} as described in its datasheet. The CHG and DSG outputs are powered from a 12-V supply regulated from the REGSRC supply. When high, the outputs will be 12 V nominal; when low, the output will be 0 V.

The DSG pin can connect directly to the low-side N-channel FET gate of the DSG FETs (Q13 and Q15).

The CHG pin cannot be directly connected to the low-side N-channel FET gate of the CHG FETs (Q14 and Q16). If the DSG FETs and CHG FETs are open, the voltage at the pack connector may be lower than the ground of the board. This means that when the internal driver of the AFE tries to keep the CHG FETs open by applying 0 V on the gate, if the source of the CHG FETs is lower than the board ground, then the CHG FETs will be wrongly closed.

To solve this issue, connect the CHG pin to the CHG FET gates through a circuit to allow them to operate properly in several phases of operation. Connect the circuit by adding a P-channel FET (Q12) between the CHG pin and the gate of the FETs, with the gate of Q12 connected to ground. This way, when the CHG pin is high, Q12 is then closed, which closes the CHG FETs. When the CHG pin is low, Q12 is now open and the pulldown resistor (R45) is opening the CHG FETs. The value of R45 has to be a trade-off between the switching speed and the current consumed when the FETs are close.

More details could be found in the *bq769x0 Family Top 10 Design Considerations*[1].

Some ringing on the gate of MOSFET could be caused by the drain and gate stray inductance and the Miller capacitance, even more when FETs are paralleled. To prevent this, chip ferrite beads (L1, L2, L3, and L4) are added in series with the gate of the protection FETs.

8.1.4 Balancing Circuit

More details on how to choose the balancing current, timing, and conditions are in Section 8.2.6.3.

It is recommended to use an external cell balancing circuit with the bq76930 to achieve the desired balancing scheme. This circuit consists for each cell of

- a balancing resistor, setting the balancing current
- a FET, switched to draw current through the balancing resistor
- a Zener diode for gate protection
- a gate resistor to limit the current the current when the diode is conducting
- an RC input filter

In the TIDA-00449, the targeted balancing current is 150 mA at 4.2 V. A resistor value of 28.7 Ω is then chosen for the balancing resistors (R2, R7, R12, R15, R18, R23, R28, R32, R36, and R39). To withstand the dissipated power, a 2010, 0.75-W package is used.

Then comes the choice of the balancing FET, as discussed in the *bq769x0 Family Top 10 Design Considerations*[1]. N-FETs are here chosen for Q1, Q2, Q4, Q5, Q6, Q7, Q8, Q9, Q10, and Q11. The FemtoFET CSD13381F4 is then selected due to its low on-resistance, low Q_g and Q_{gd}, and ultra-small footprint (1.0 × 0.6 × 0.35 mm).

The input filter capacitor (C1, C2, C5, C8, C9, C12, C15, C17, C19, C20, C21, and C22) is chosen at 0.22 μF. A higher value will make the filter stronger but might affect the cell measurement during cell balancing. The value may be tuned according to the cell balancing algorithm and during test.

8.1.5 Internal LDO

In a 10s battery pack, the maximum voltage may be significantly higher than the maximum voltage of the REGSRC pin (36 V). A circuit is then required to reduce the voltage to a suitable value for the IC. The FET also dissipates the power resulting from the load current and dropped voltage external to the IC.

An FET (Q3) is used as a source follower. A diode (D1) is also used to prevent REGSRC from dropping during heavy load or short circuit. A resistor (R5) is added in parallel to the diode to discharge any transient seen by the diode. More details could be found in the *bq769x0 Family Top 10 Design Considerations*[1].

8.1.6 Temperature Measurement and Wake-up

The BQ76930 uses two external 10-kΩ NTC 103AT thermistors to measure the temperature of the battery pack. A third temperature measurement point was added to the battery management controller thanks to an LMT01, as described in Section 8.2.3.3.

The bq76930 is then using a 14-bit ADC reading in TS1 and TS2 to determine the resistance of the external 103AT thermistor, according to the following equations:

$$V_{TSx} = (\text{ADC in decimal}) \times 382 \frac{\mu V}{\text{LSB}} \quad (4)$$

$$R_{TSx} = \frac{10000 \times V_{TSx}}{3.3 \times V_{TSx}} \quad (5)$$

Use the thermistor manufacturer's datasheet to convert this resistor value into temperature.

A 4.7-nF capacitor is placed in parallel to the thermistors to stabilize the voltage as the TSx pins are switched.

To wake the bq76930 from SHIP mode, a voltage greater than VBOOT needs to be applied to TS1 because a pushbutton (S1) was added between TS1 and the positive pin of the bottom cell, as well as a resistor (R27), to limit the current into TS1 once S1 is pushed.

8.2 Battery Management Controller

8.2.1 Part Selection

A battery management controller is required to set the protection registers, enable FETs, recover from faults, and provide a balancing algorithm if desired. The MCU can also implement a gauging algorithm and provide display or communication appropriate for the system.

The TI MSP430™ family of ultra-low-power MCUs consists of several devices, featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve an extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.

Wide operation supply-voltage range of 1.8 to 3.6 V and ultra-low power consumption with active mode 230 µA at 1 MHz 2.2 V, standby mode 0.5 µA and off mode 0.1 µA features make the MSP430G2553 a perfect fit for battery powered applications including battery management systems.

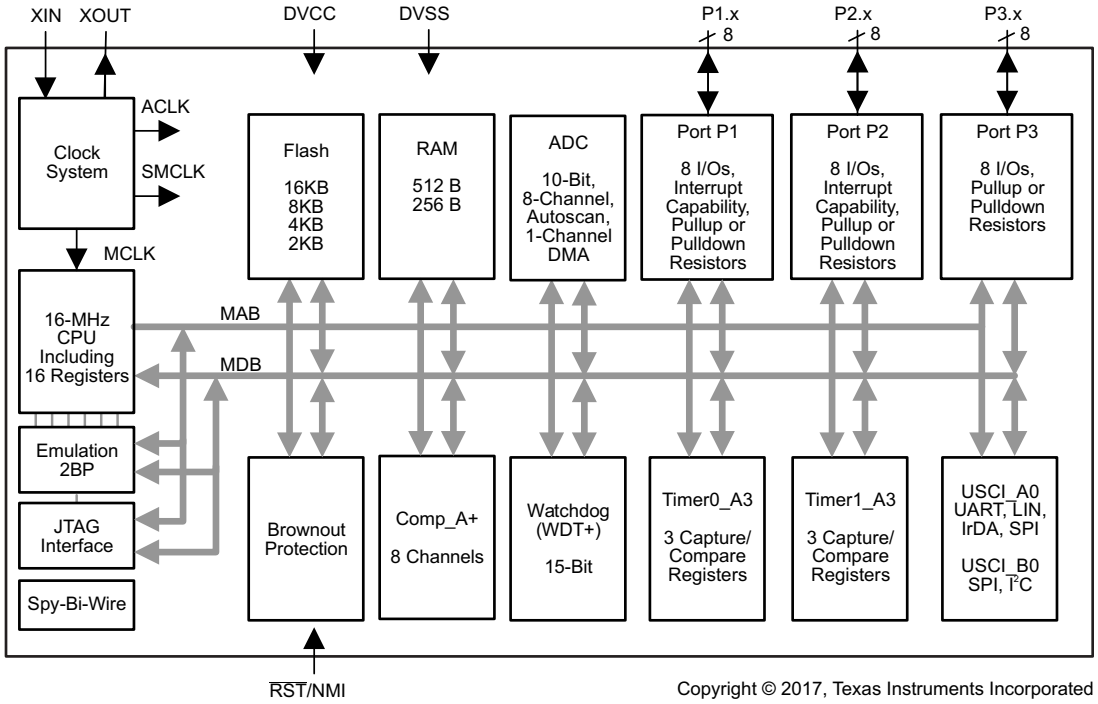


Figure 2. MSP430G2553 Block Diagram

8.2.2 Communication

Three communications channels are implemented in the TIDA-00449.

8.2.2.1 I²C

I²C communication is used for the AFE and controller to communicate together. Jumper J6 can be used to access the I²C communication. A full description and code example is provided in the application report *I²C Communication Sample Code for the bq76940 with a CRC Option Based on the MSP430G2553*[4].

8.2.2.2 Spy-Bi-Wire

Spy-Bi-Wire communication is used to program the MSP430. A pullup resistor (R68) and capacitor (C31) are required on the /RST pin of the MSP430.

If needed, jumper J7 may also be used to reset the MSP430.

8.2.2.3 UART

A simple UART communication protocol is implemented between the TIDA-00449 and a computer to monitor the system status as well as control the actions of the BMS system.

With the communication protocol, the MCU sends out system status in a data frame of 32 bytes including one byte of checksum at the end of the frame every 500 ms.

The UART data format is set to:

- Baud rate: 9600 bps
- Parity: None
- Data bit: 8 bits
- Stop bit: 1 bit

The TX frame (sent from MCU to the GUI) definition is listed in Table 2.

Table 2. TX Frame

BYTE NUMBER	NAME	DESCRIPTION
1	Header	Sent from MCU to GUI, fixed to 0xAA
2	Status/Fault	This byte contains the value of the status register of bq769x0 in manual mode and fault status of the system in auto mode
3	Cell 1 voltage	Battery cell voltage of cell 1 of the battery pack Note: Value is related with GUI_CELL_VOLTAGE_DISLAY_MIN value in resolution of 10 mV
4	Cell 2 voltage	Battery cell voltage of cell 2 of the battery pack
5	Cell 3 voltage	Battery cell voltage of cell 3 of the battery pack
6	Cell 4 voltage	Battery cell voltage of cell 4 of the battery pack
7	Cell 5 voltage	Battery cell voltage of cell 5 of the battery pack
8	Cell 6 voltage	Battery cell voltage of cell 6 of the battery pack
9	Cell 7 voltage	Battery cell voltage of cell 7 of the battery pack
10	Cell 8 voltage	Battery cell voltage of cell 8 of the battery pack
11	Cell 9 voltage	Battery cell voltage of cell 9 of the battery pack
12	Cell 10 voltage	Battery cell voltage of cell 10 of the battery pack
13	Pack voltage	Battery pack voltage Note: Value is related with GUI_PACK_VOLTAGE_DISPLY_MIN value in resolution of 100 mV
14	Temperature 1	This byte contains temperature information for temperature channel 1 Range from –50°C to 77°C in resolution of 0.5°C
15	Temperature 2	This byte contains temperature information for temperature channel 2 Range from –50°C to 77°C in resolution of 0.5°C
16	Total coulomb counter 0	0 to 7 bits of the total coulomb counter
17	Total coulomb counter 1	8 to 15 bits of the total coulomb counter
18	Total coulomb counter 2	16 to 23 bits of the total coulomb counter
19	Total coulomb counter 3	24 to 31 bits of the total coulomb counter
20	ADC gain	ADC gain reading from the bq769x0 device Note: Value is related with ADCGAIN_BASE value in resolution of 1 µV
21	ADC offset	ADC Offset reading from the BQ769x0 device with resolution of 1 mV
22	Cell balance index 0	Bit 0 to 7 represents the cell balancing status of cell 1 to cell 8 0: No cell balancing is being performed 1: Cell balancing is being performed
23	I^2C communication error	[7] Bit 7 shows the I^2C communication status between the MCU and the bq769x0 device 0: No I^2C communication error 1: I^2C communication error occurred
	Reserved	[2:6] Reserved
	Cell balance index 1	[0:1] Bit 0 to 1 represents the cell balancing status of cell 9 to cell 10 0: No cell balancing is being performed 1: Cell balancing is being performed
24	Battery level	Battery level detected by the simple gauging mechanism in percentage with resolution of 1%
25	Alert pin status	Alert pin status of the bq769x0 device 0: Alert pin is logic low 1: Alert pin is logic high
26	Battery pack temperature	This byte contains temperature information sensed by LMT01 temperature sensor Range from –50°C to 77°C in resolution of 0.5°C
27	SYSCTRL1	The value of SYSCTRL1 register of the BQ769x0 device
28	SYSCTRL2	The value of SYSCTRL2 register of the BQ769x0 device
29	Idle balance timer	Idle balance timer counter value in resolution of 1 minute
30	Balance timer 1	Cell balance timer for cell group 1 (cell 1 to 5) in resolution of 1 second
31	Balance timer 2	Cell balance timer for cell group 2 (cell 6 to 10) in resolution of 1 second
32	Checksum	Sum of byte 1 to 31 in a 8-bit range with all carries ignored

The RX frame (sent from GUI to MCU) definition is listed in Table 3.

Table 3. RX Frame

BYTE NUMBER	NAME	DESCRIPTION
1	Header	Sent from MCU to GUI, fixed to 0x55
2	Reserved	[3:7] Reserved
	Temperature sensor type (Only in manual mode)	[2] Selection of the temperature sensor type of the bq769x0 device 0: Die temperature 1: External thermistor
	ADC EN (Only in manual mode)	[1] Setting of the ADC EN bit 0: Clear ADC_EN 1: Set ADC_EN
	Operation mode	[0] Operation mode setting from the host 0: Manual mode 1: Auto mode
3	SysCtrl2 register setting (Only in manual mode)	Setting of the SysCtrl2 register to the firmware
4	Protect1 register setting (Only in manual mode)	Setting of the Protect1 register to the firmware
5	Protect2 register setting (Only in manual mode)	Setting of the Protect2 register to the firmware
6	Protect3 register setting (Only in manual mode)	Setting of the Protect3 register to the firmware
7	OV_TRIP register setting (Only in manual mode)	Setting of the OV_TRIP register to the firmware
8	UV_TRIP register setting (Only in manual mode)	Setting of the UV_TRIP register to the firmware
9	CELLBAL1 register setting (Only in manual mode)	Setting of the CELLBAL1 register to the firmware
10	CELLBAL2 register setting (Only in manual mode)	Setting of the CELLBAL2 register to the firmware
11	Reserved	[1:7] Reserved
	Settings changed	[0] Settings changed flag indicates there are changes on settings of the GUI If this bit is 0, the firmware of the MCU will not update the settings from the GUI to the system 0: No changes 1: There are changes
12	Reserved	[3:7] Reserved
	Apply settings	[2] Command to apply all register settings into the bq769x0 device 0: No action required 1: Clear total coulomb counter
	Clear total coulomb counter	[1] Command to clear total coulomb counter 0: No action required 1: Clear total coulomb counter
	Clear fault	[0] Command to clear fault status 0: No action required 1: Clear fault
13	Reserved	Byte reserved for future usage, fixed to 0x00
14	Reserved	Byte reserved for future usage, fixed to 0x00
15	Reserved	Byte reserved for future usage, fixed to 0x00
16	Reserved	Byte reserved for future usage, fixed to 0x00
17	Reserved	Byte reserved for future usage, fixed to 0x00
18	Reserved	Byte reserved for future usage, fixed to 0x00
19	Reserved	Byte reserved for future usage, fixed to 0x00
20	Reserved	Byte reserved for future usage, fixed to 0x00
21	Reserved	Byte reserved for future usage, fixed to 0x00
22	Reserved	Byte reserved for future usage, fixed to 0x00

Table 3. RX Frame (continued)

BYTE NUMBER	NAME	DESCRIPTION
23	Reserved	Byte reserved for future usage, fixed to 0x00
24	Reserved	Byte reserved for future usage, fixed to 0x00
25	Reserved	Byte reserved for future usage, fixed to 0x00
26	Reserved	Byte reserved for future usage, fixed to 0x00
27	Reserved	Byte reserved for future usage, fixed to 0x00
28	Reserved	Byte reserved for future usage, fixed to 0x00
29	Reserved	Byte reserved for future usage, fixed to 0x00
30	Reserved	Byte reserved for future usage, fixed to 0x00
31	Reserved	Byte reserved for future usage, fixed to 0x00
32	Checksum	Sum of byte 1 to 31 in a 8-bit range with all carries ignored

8.2.3 Sensing

On top of the measurement done by the AFE, some additional current, voltage, and temperature sensing circuits were added to the controller to offer more test and design options. All those measurements could be disabled, minimizing the current consumption if required.

8.2.3.1 Current

The MSP430 can directly read the current through its ADC and the current measurement circuit (Q17, R63, R64, and R67). Those current measurements could be used to implement additional current limit threshold in firmware.

8.2.3.2 Voltage

The voltage sensing circuit (Q18, Q19, R61, R65, R66, R69, and R75) could be used to measure the voltage of the full pack. The circuit can also be used for real-time calibration as described in page 22 of the bq76930 datasheet (SLUSBK2).

8.2.3.3 Temperature

In addition to the two thermistor of the BQ76930, a third temperature measurement point was added to the TIDA-00449 using the LMT01. For example, this additional point could be used to monitor the temperature of the protection FETs. This could be important in case of a short circuit event to ensure that the FETs are cooled down enough after tripping before closing them again.

The LMT01 is a high-accuracy, 2-pin temperature sensor with an easy-to-use pulse count interface, which makes it an ideal digital replacement for PTC or NTC thermistors both on and off board in automotive, industrial, and consumer markets. The LMT01 digital pulse count output and high accuracy over a wide temperature range can pair with any MCU without concern for integrated ADC quality or availability, while minimizing software overhead. TI's LMT01 achieves a flat ±0.5°C accuracy with a very fine resolution (0.0625°C) over a wide temperature range of –20°C to 90°C without system calibration or hardware or software compensation.

The sensor takes a maximum of 51 ms to convert the temperature after powering up and 50 ms to transfer the data. In this design, checking the temperature from the LMT01 is performed with period of 1 s.

In this design, the data sent by the LMT01 is captured by an analog comparator of the MSP430. When setting the comparator threshold to 0.25 × V_{CC} (0.825 V), the high- and low-level output signal of the LMT01 has to be across the comparator threshold. Because the output current (IOL and IOH) of the LMT01 is in the range from 28 to 39 µA and 112.5 to 143 µA, a 10-KΩ resistor to ground is used, which generates 390 mV of VOL_max and 1.125 V of VOH_min.

Figure 3 shows the LMT01 output data with a 10-Kohm resistor.

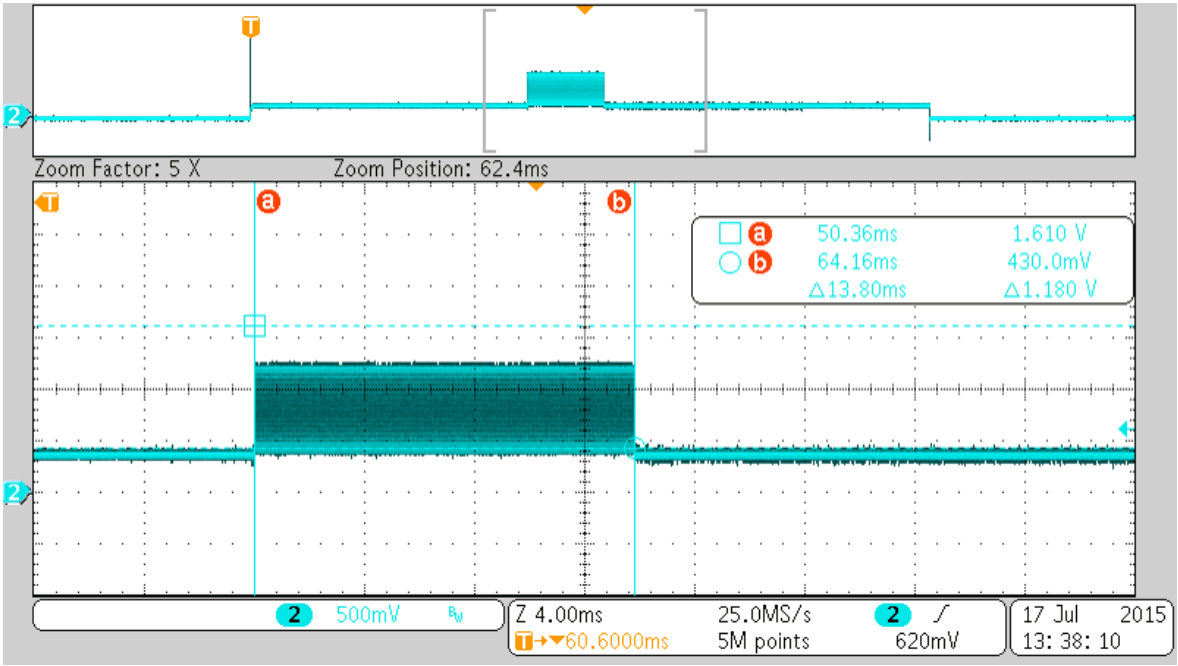


Figure 3. LMT01 Output Data

To power and read the LMT01 properly, a timing sequence is implemented in the firmware following the flowchart shown in Figure 4.

The sequence is implemented in the routine of lmt01_handler() of the file of drv_lmt01.c.

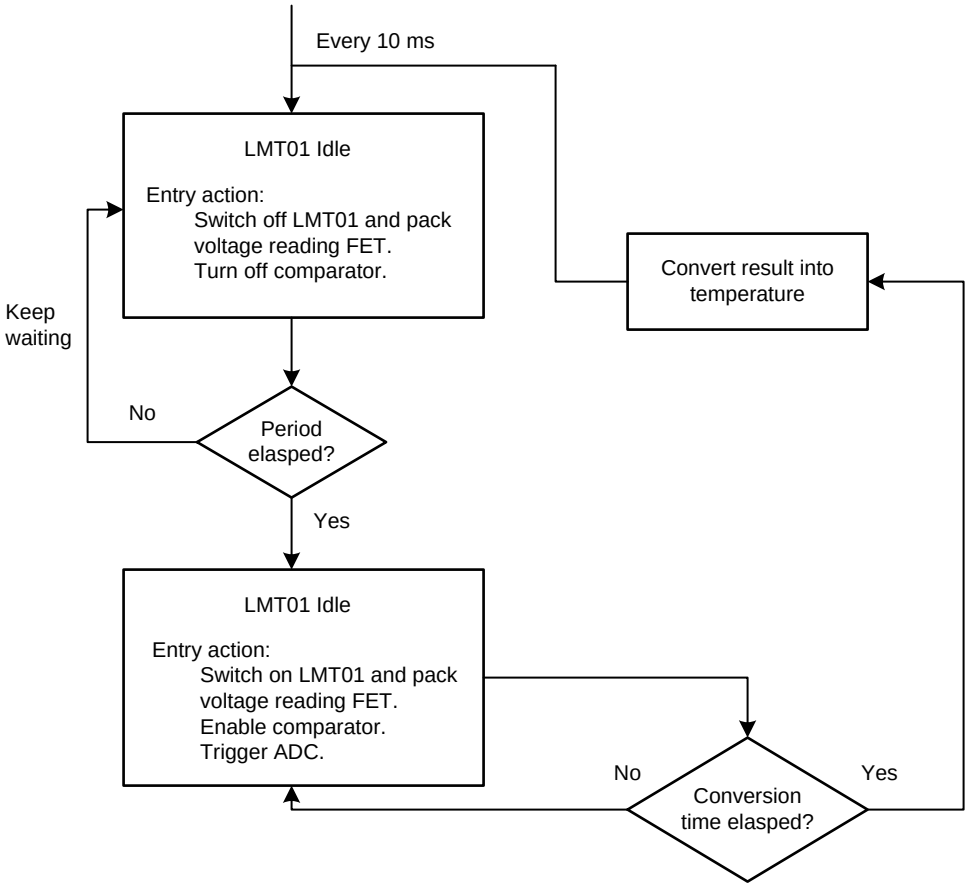


Figure 4. LMT01 Flowchart

8.2.4 Voltage Supervisor

The MSP430 requires a voltage between 1.8 and 3.6 V. As the BQ7693003 provides 3.3 V, the TPS3839G33, an ultra-low quiescent (150 nA), ultra-small voltage supervisor, monitors the supply voltage. It holds the MSP430 in reset in case its supply voltage drops below 3.08 V and the reset output remains low for 200 ms (typical) after the V_{DD} voltage rises above the threshold voltage and hysteresis.

8.2.5 LED Indication

Four LEDs (D24, D25, D26, and D27) are added to display the remaining capacity, according to the gas gauging algorithm described in Section 8.2.6.2.

To decrease power consumption, the LEDs only display the remaining capacity level when the pushbutton S2 is pushed.

8.2.6 Firmware

8.2.6.1 Overview

The firmware keeps checking the alert pin status of the bq769x0 device in a task loop every 2 ms, while I_{SENSE} (battery current through the shunt resistor) is checked with a 10-ms task loop, and battery pack temperature and voltage are checked in the same task loop within a 1-s period.

See Figure 5 for an overview of the firmware task handling procedure.

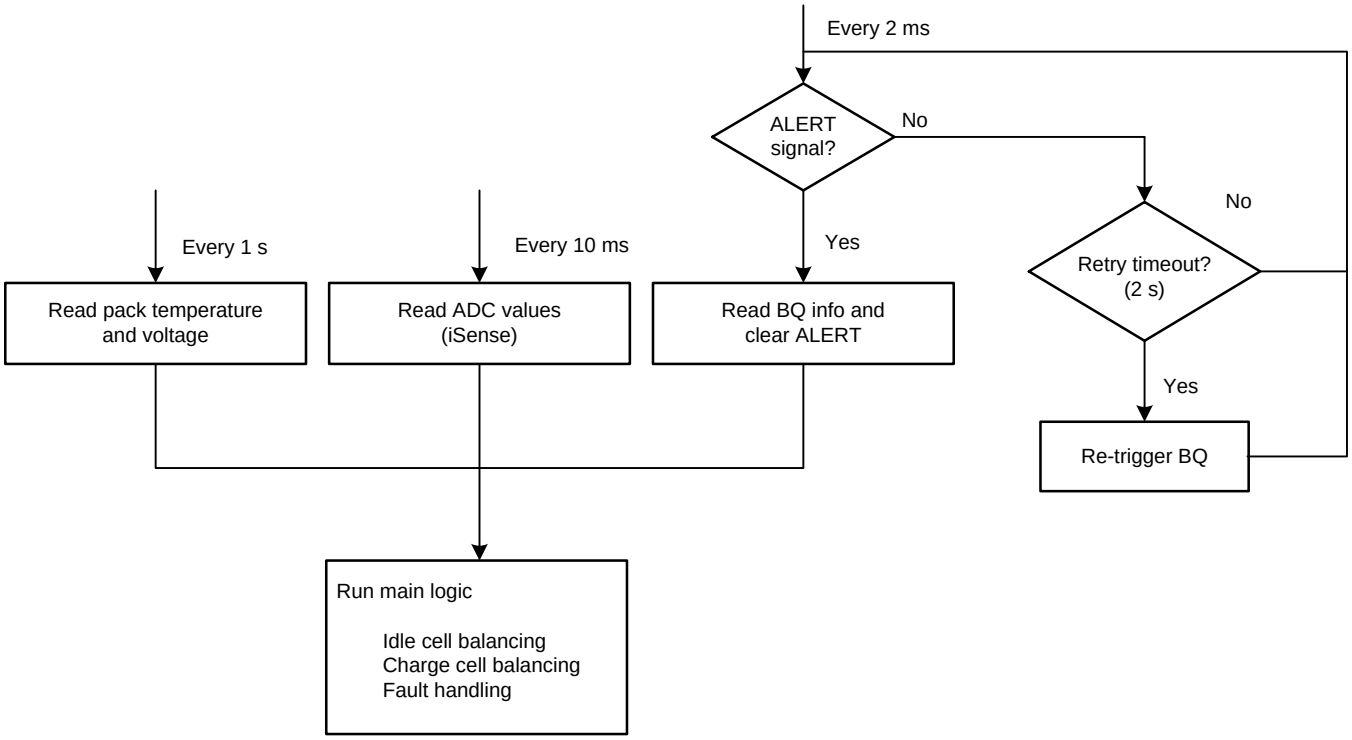


Figure 5. Task Handling Flowchart

8.2.6.2 Logic

The logic of the firmware is implemented in a single software routine called logic_handler(). This routine is called in the 10-ms task loop and performs the cell balancing, gas gauging, and fault handling in auto mode.

In manual mode, all operations are performed according to the setting from the GUI.

In auto mode, the routine first checks the fault status of the system. If there is no fault in the system, the routine ensures the CHG and DSG FETs are turned on, determines the SOC of the system at the moment by comparing the coulomb counter reading result with the COULOMB_COUNTING_SOC_THRESHOLD, and performs cell balancing to the battery cells.

8.2.6.3 Cell Balancing

8.2.6.3.1 What is Cell Imbalance

A common problem of multi-cell battery packs is cell imbalance. Cell imbalance is detrimental to the runtime and life span of the whole battery pack.

Cell imbalance is caused by:

- The capacity variation of the cells, usually around 1 to 2% cell-to-cell variation for the same model
- Difference in state of charge
- Impedance variation (up to 15%) causing voltage difference when charging and discharging current is applied
- Localized heat, which degrades some cells faster than others, especially in high cell count battery systems due to temperatures gradients and cell self-heating at high discharge rates

Unbalanced cells reduce the effective run time due to both premature charge termination and early discharge termination as shown in Figure 6.

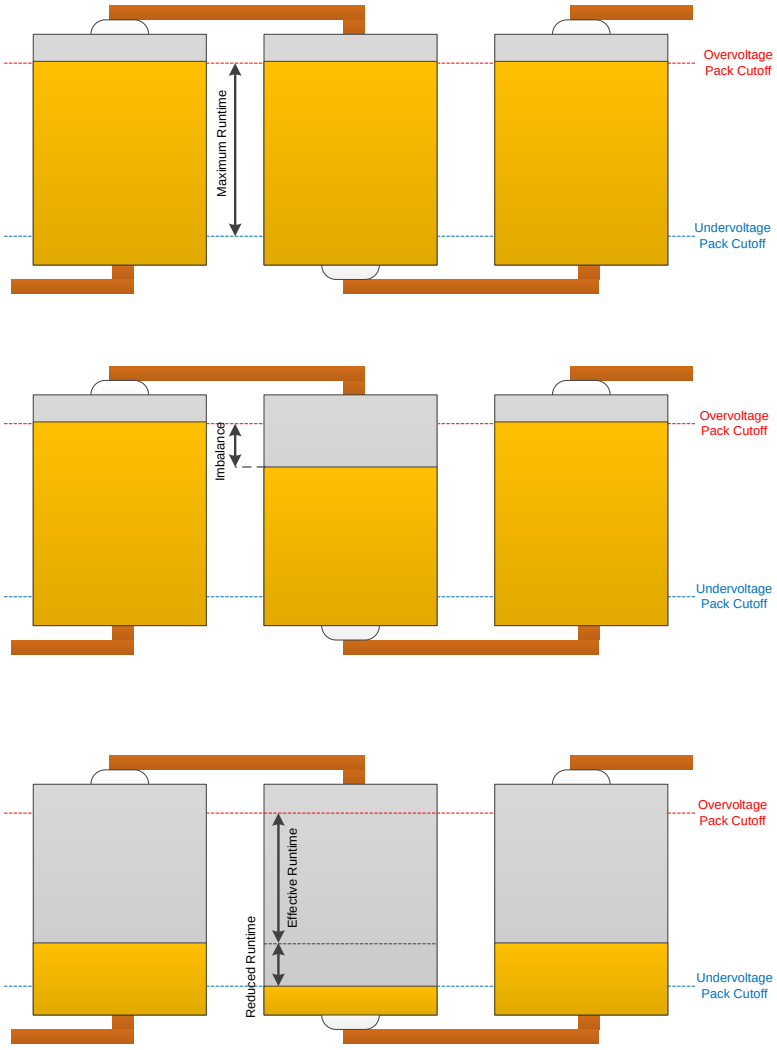


Figure 6. Effect of Cell Imbalance on Run Time

Cell balancing minimizes this problem by equalizing the cells, allowing the battery pack to operate longer. A difference in cell voltages is the most common manifestation of unbalance, which can be corrected either instantaneously or gradually through bypassing cells with a higher voltage.

8.2.6.3.2 When and How Much to Balance

Balancing is usually done during charge or idle time.

The next considerations are to determine which balancing current to use and how long to balance. Those considerations are heavily impacted by the end application and user behavior. For example, a higher balancing current and shorter balancing time will be chosen in applications where the opportunity to balance the cells is low (quick charge, low or no idle time, continuous discharge). In applications where the opportunity to balance the cells is higher, a lower balancing current over a longer balancing time may be chosen to minimize the impact on the cells (that is, self-heating during discharge).

8.2.6.3.3 How is it Implemented in the TIDA-00449

The bq76930 uses a passive balancing technique, which consists of bypassing a cell with a balancing resistor to either decrease the charging current seen by the cell (during charge) or to discharge the cell (during idle).

This design being targeted for power tools where idle time is unneglectable (storage, pack sitting charged on the charging bay, time between session, and so on), the decision was made to use a lower balancing current (150 mA at 42 V) and to balance as often as possible:

- At the end of charge when the cells reach 4 V or higher
- When the pack is in idle for longer than 30 minutes and the cell voltage is higher than 3.3 V

In those two conditions, the algorithm decides if balancing is required according to the differences between the cell voltages. If the difference exceeds the predefined threshold (here, 50 mV), bypass is activated. The bq76930 can simultaneously perform balancing on two cells, each from a different cell group (cell 1 to 5 and cell 6 to 10).

Figure 7 shows the cell balancing flowchart.

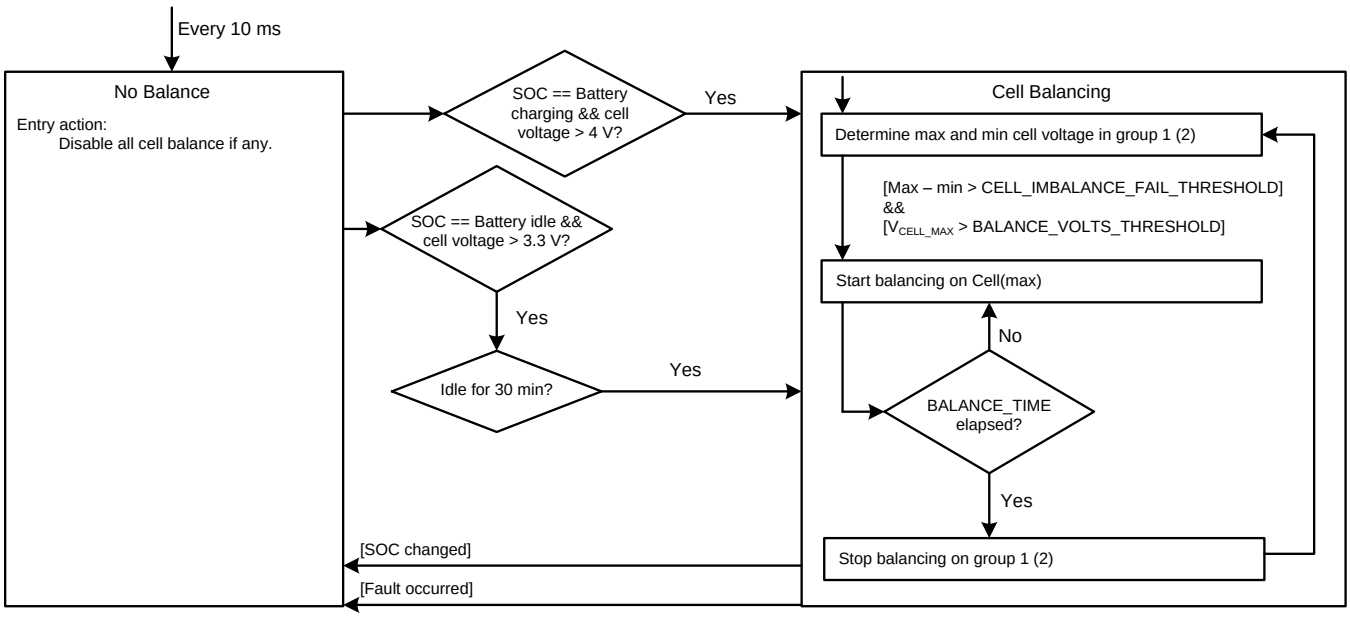


Figure 7. Cell Balancing Flowchart

8.2.6.4 Fault Handling

In this design, the system faults are detected by the bq769x0 device automatically based on the threshold settings during the initialization phase.

To change the thresholds, the user can either change the initialization values in the drv_bq76930.c file or apply the thresholds through the UART communication from the GUI or host machine.

Once a fault is detected, the bq769x0 device will automatically turn off the CHG and DSG FETs to protect the battery system.

Recovering from a fault state is dependent to the system requirement and to be implemented into the firmware. Example software procedure for fault recovery handling is provided along with the firmware.

Figure 8 shows how the firmware handles different fault status.

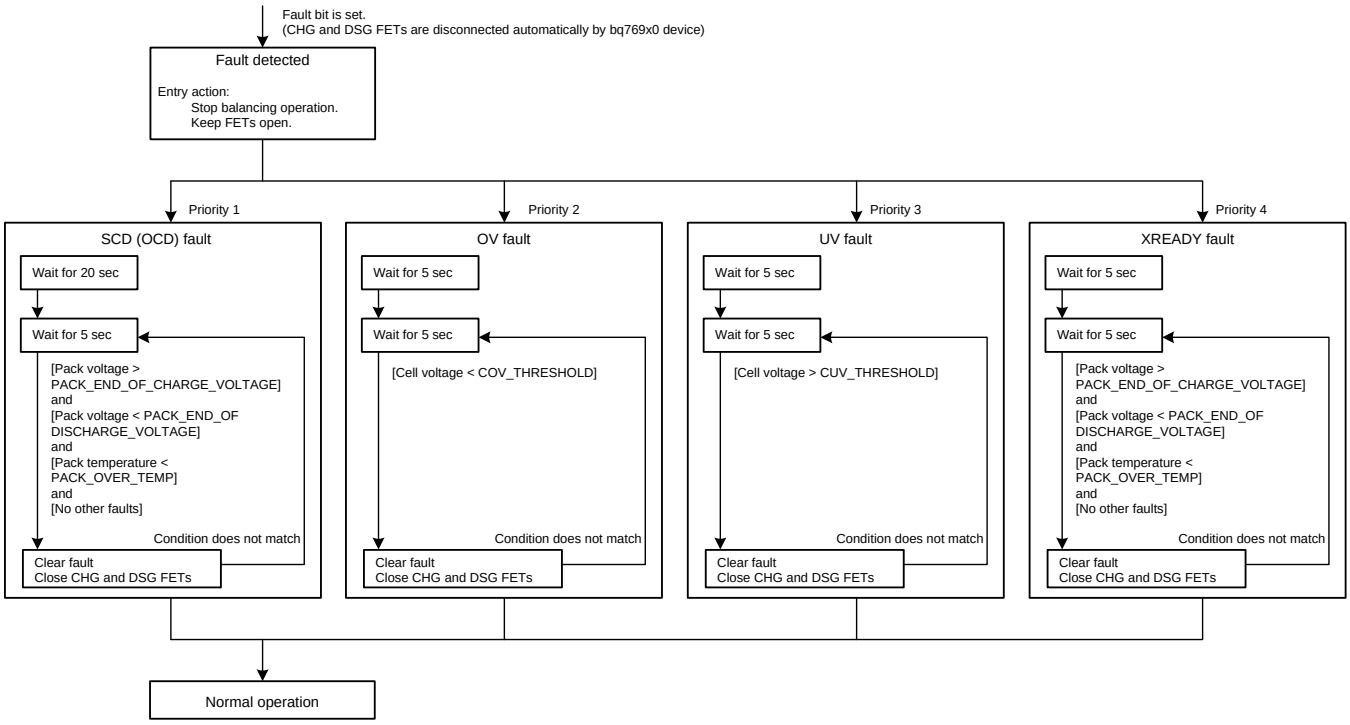


Figure 8. Fault Handling Flowchart

8.2.6.5 Gas Gauge

A simple gas gauging was implemented in the TIDA-00449; nevertheless, the hardware could also allow users to implement their own more advanced and accurate algorithm.

The algorithm implemented by default is:

- 0% of remaining capacity (no LED on) if the pack voltage is below 32 V
- 25% of remaining capacity (D29 on) if the pack voltage is between 32 and 34 V
- 50% of remaining capacity (D29 and D30 on) if the pack voltage is between 34 and 36 V
- 75% of remaining capacity (D29, D30, and D27 on) if the pack voltage is between 36 and 38 V
- 100% of remaining capacity (all LED on) if the pack voltage is above 38 V

8.3 Layout

Find more information in the bq76930 datasheet (SLUSBK2), Section 11.4 of this report, and this TI training video[5].

9 Getting Started

9.1 PCB Overview

Figure 9 shoes a picture of the PCB with the function blocks.

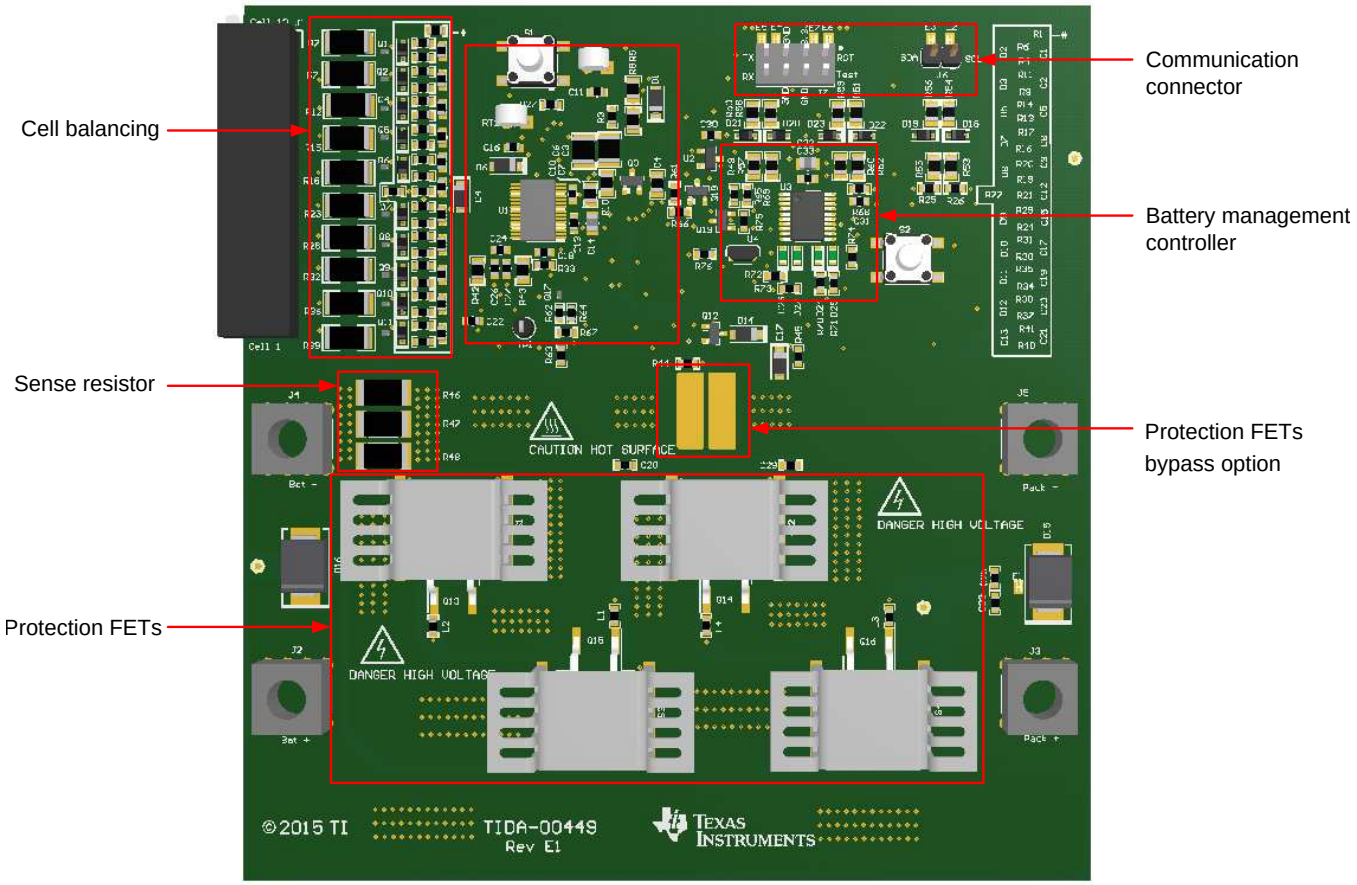


Figure 9. TIDA-00449 PCB With Functional Blocks

9.2 Connectors Settings

Table 4. Connectors Settings

CONNECTOR AND PIN ASSIGNMENTS	DESCRIPTION
J1-1	Cell 10/Bat+
J1-2	Cell 9
J1-3	Cell 8
J1-4	Cell 7
J1-5	Cell 6
J1-6	Cell 5
J1-7	Cell 4
J1-8	Cell 3
J1-9	Cell 2
J1-10	Cell 1
J1-11	Bat–
J2	Bat+
J3	Pack+
J4	Bat–
J5	Pack–
J6-1	SCL
J6-2	SDA
J7-1	/RST
J7-2	Test
J7-3	3.3 V
J7-4	GND
J7-5	GND
J7-6	GND
J7-7	TX
J7-8	RX

10 Test Data

10.1 Test Setup

Figure 10 shows the setup and test equipment used.

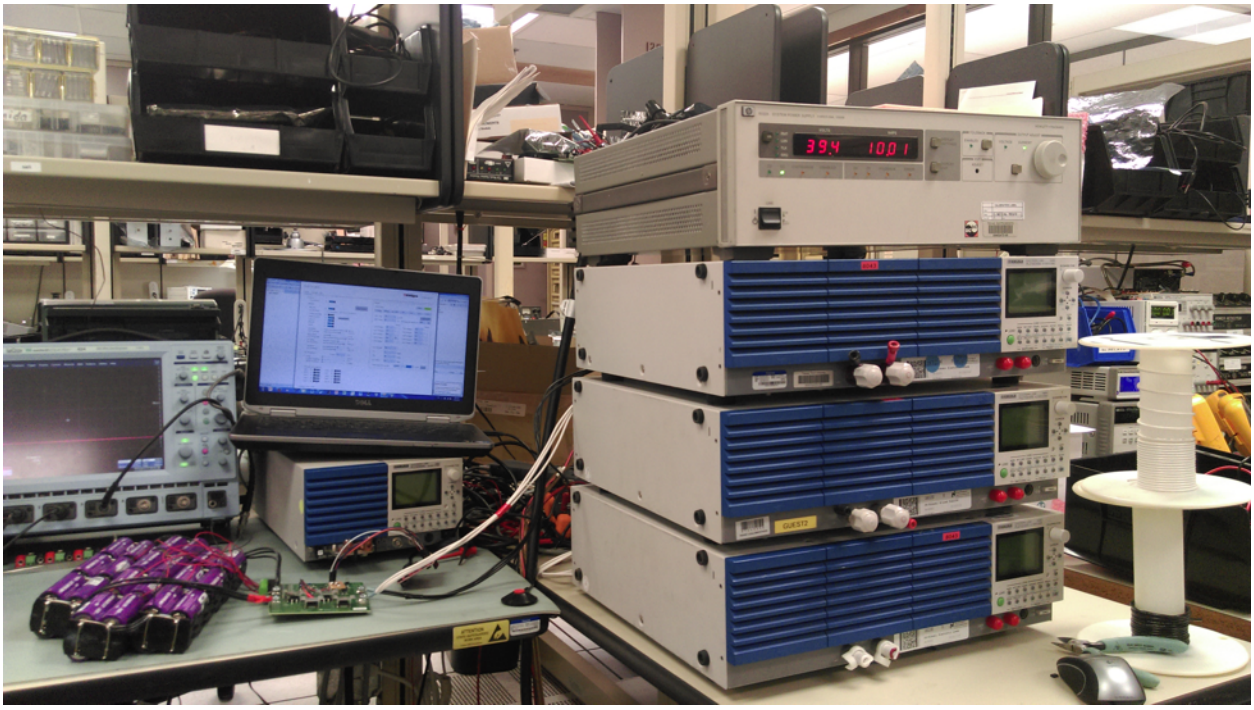


Figure 10. Test Setup for TIDA-00449 for Charge and Discharge

Table 5. Test Equipment

TEST EQUIPMENT	PART NUMBER
Oscilloscope	LeCroy WaveSurfer 424
Electronic load	Kikusui PLZ1004W
Thermal camera	ICI Duracam XT
Power supply	HP Agilent 6032A
TTL-to-USB serial converter	TTL-232R-3V3
Battery cell	IMR 2015 P26650 4200 mAh V1
MSP430 programmer	MSP430 LaunchPad™

For discharging, three Kikusui PLZ1004W electronic loads were installed in parallel.

For charging, the HP Agilent 6032A power supply was used. By setting the current limit at the desired charging current, the power supply emulate the behavior of a Li-ion battery charger, which is constant current until the desired cell voltage is reached (usually 4.2 V), then switch to constant voltage. The power supply is then switch off once the charging current drop below the taper current.

The TTL-232R-3V3, TTL-to-USB Serial Converter connects the UART connector of the TIDA-00449 to the computer.

The MSP430 LaunchPad is connected to the Spy-Bi-Wire connector to program the MSP430.

10.2 Test Results

10.2.1 Thermal

10.2.1.1 Full Discharge Cycle at 40-A Discharge Current

Figure 11 shows the end of a full discharge cycle at a 40-A continuous discharge current.

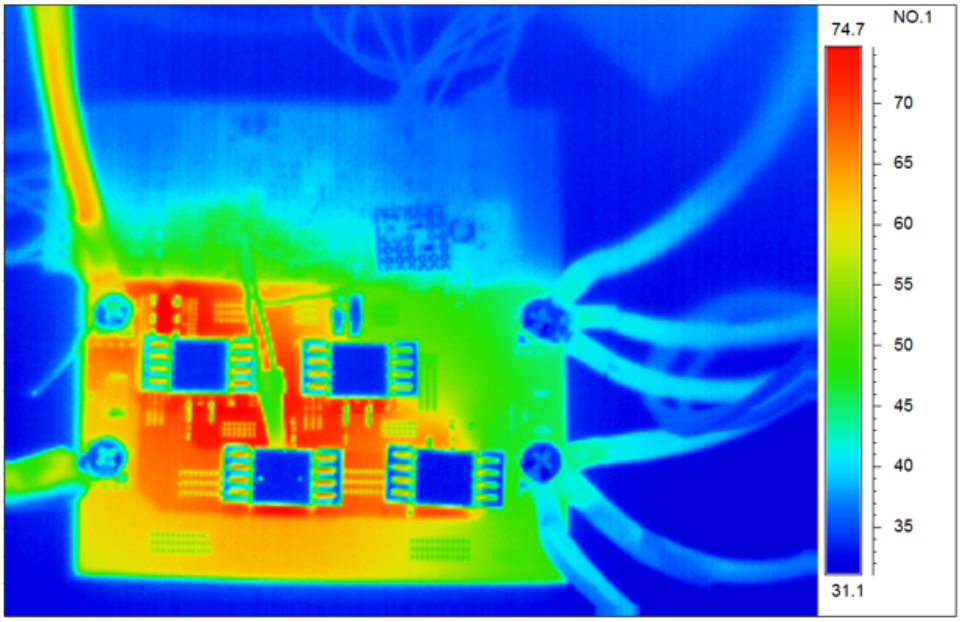


Figure 11. Thermal Picture at 40-A Discharge Current

10.2.1.2 End of Charge During Cell Balancing

Figure 12 shows the end of the charge, with the charger being in constant voltage mode with two cells (cells 4 and 6) being balanced.

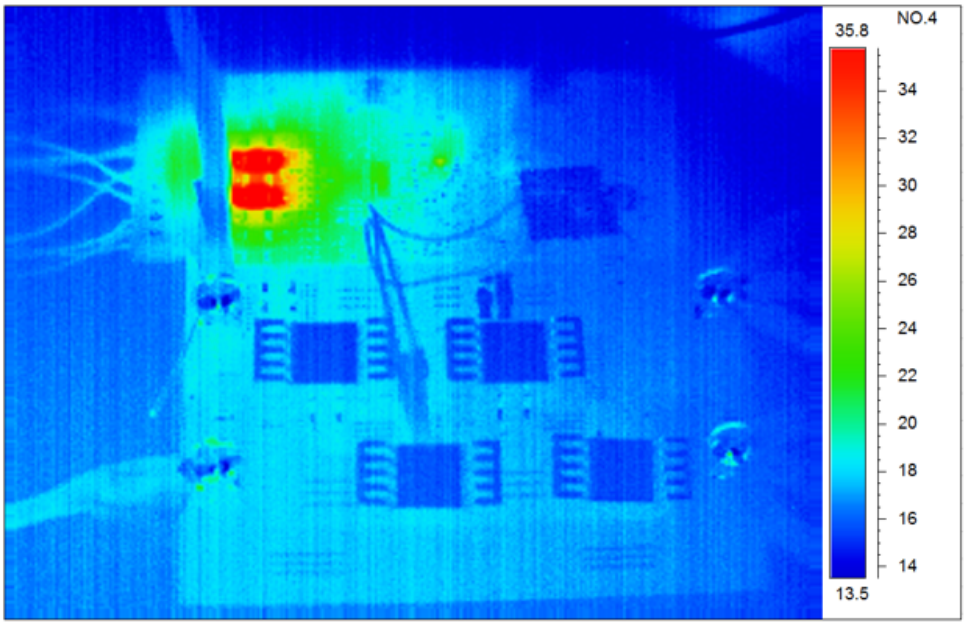


Figure 12. Thermal Picture at End of Charge During Cell Balancing

10.2.2 Discharge and Charge Cycle

Figure 13 shows the discharge and charge cycle with a 40-A continuous discharging current and 9-A charging current.

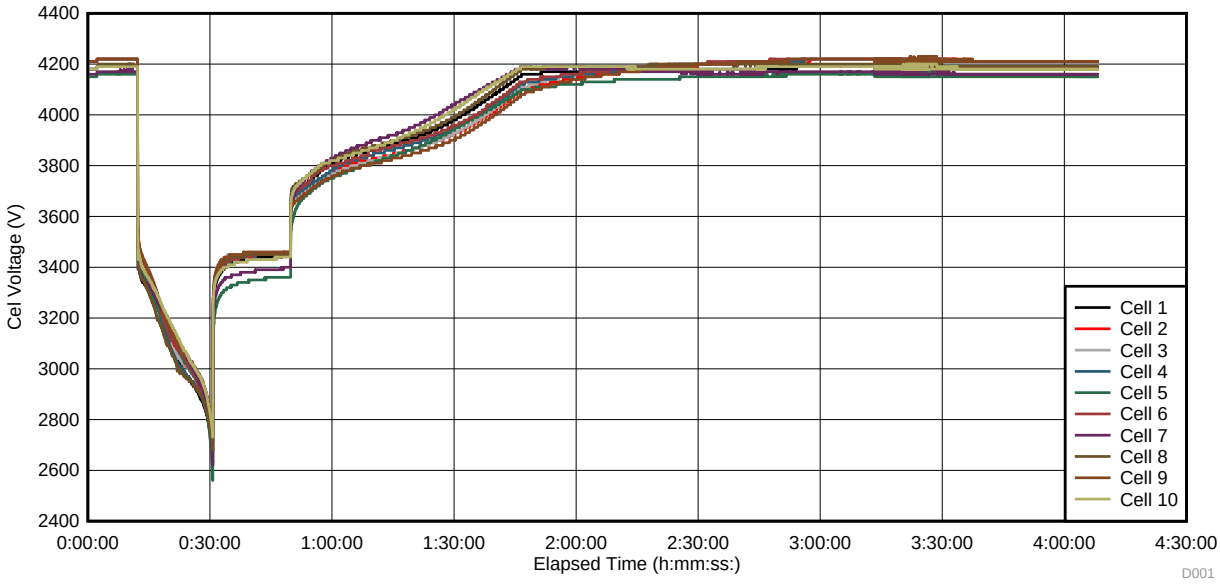


Figure 13. Discharge and Charge Cycle

10.2.3 Protection FETs

10.2.3.1 DSG FETs

Figure 14 and Figure 15 display the gate voltage of the DSG FETs while they are being turned on and off.

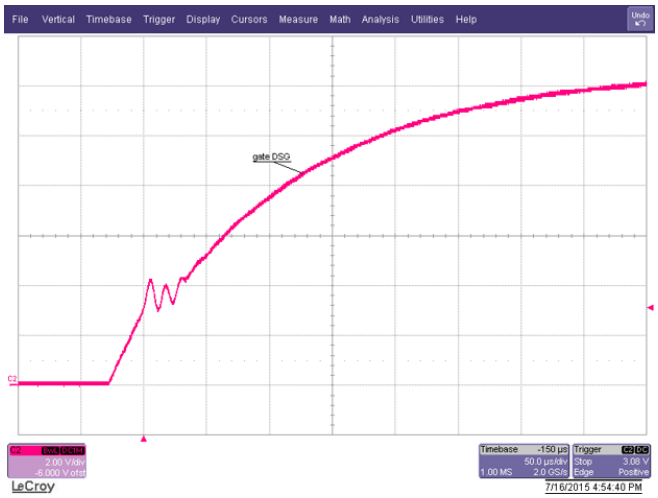


Figure 14. Gate Voltage of DSG FETs While Closing

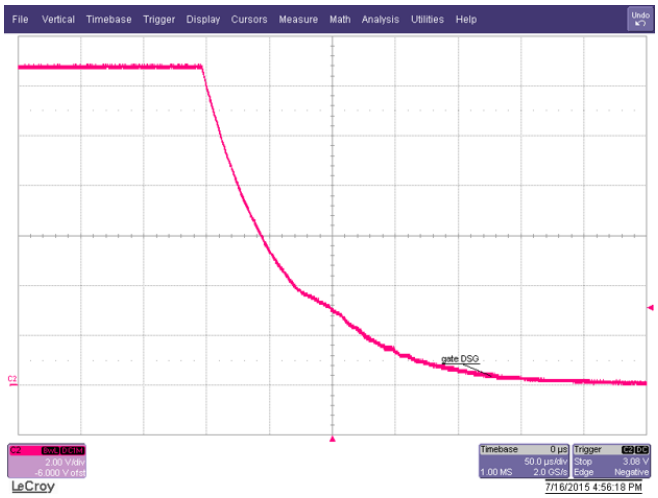


Figure 15. Gate Voltage of DSG FETs While Opening

10.2.3.2 CHG FETs

Figure 16 and Figure 17 display the gate voltage of the CHG FETs while they are being turned on and off.

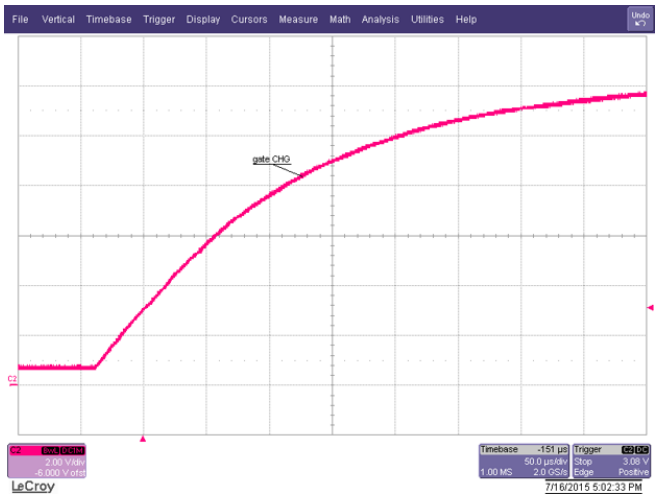


Figure 16. Gate Voltage of CHG FETs While Closing

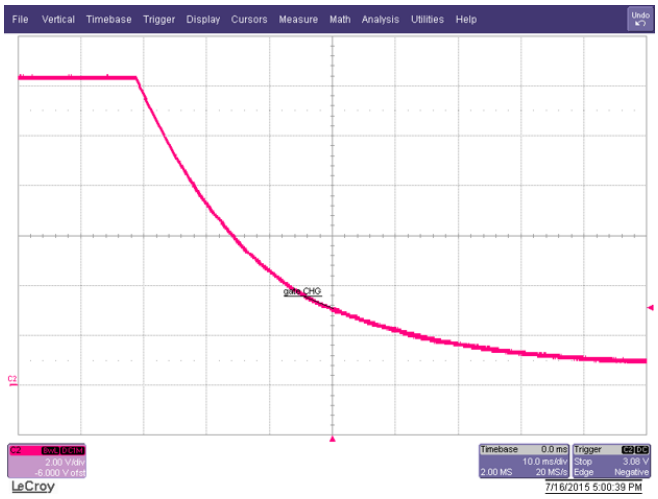


Figure 17. Gate Voltage of CHG FETs While Opening

10.2.4 Short Circuit Protection

Figure 18 shows the short circuit protection when a short circuit is applied between Pack– and Pack+. Channel 1 is the DSG FETs gate voltage, channel 2 is the voltage across the sense resistors, and channel 3 is the voltage between Batt– and Pack–.

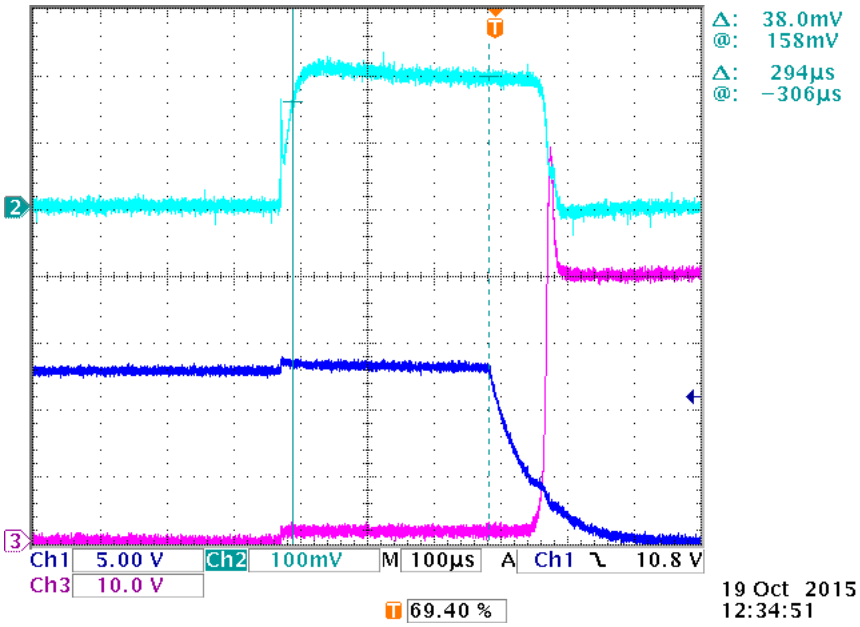


Figure 18. Short Circuit Protection

11 Design Files

11.1 Schematics

To download the schematics, see the design files at TIDA-00449.

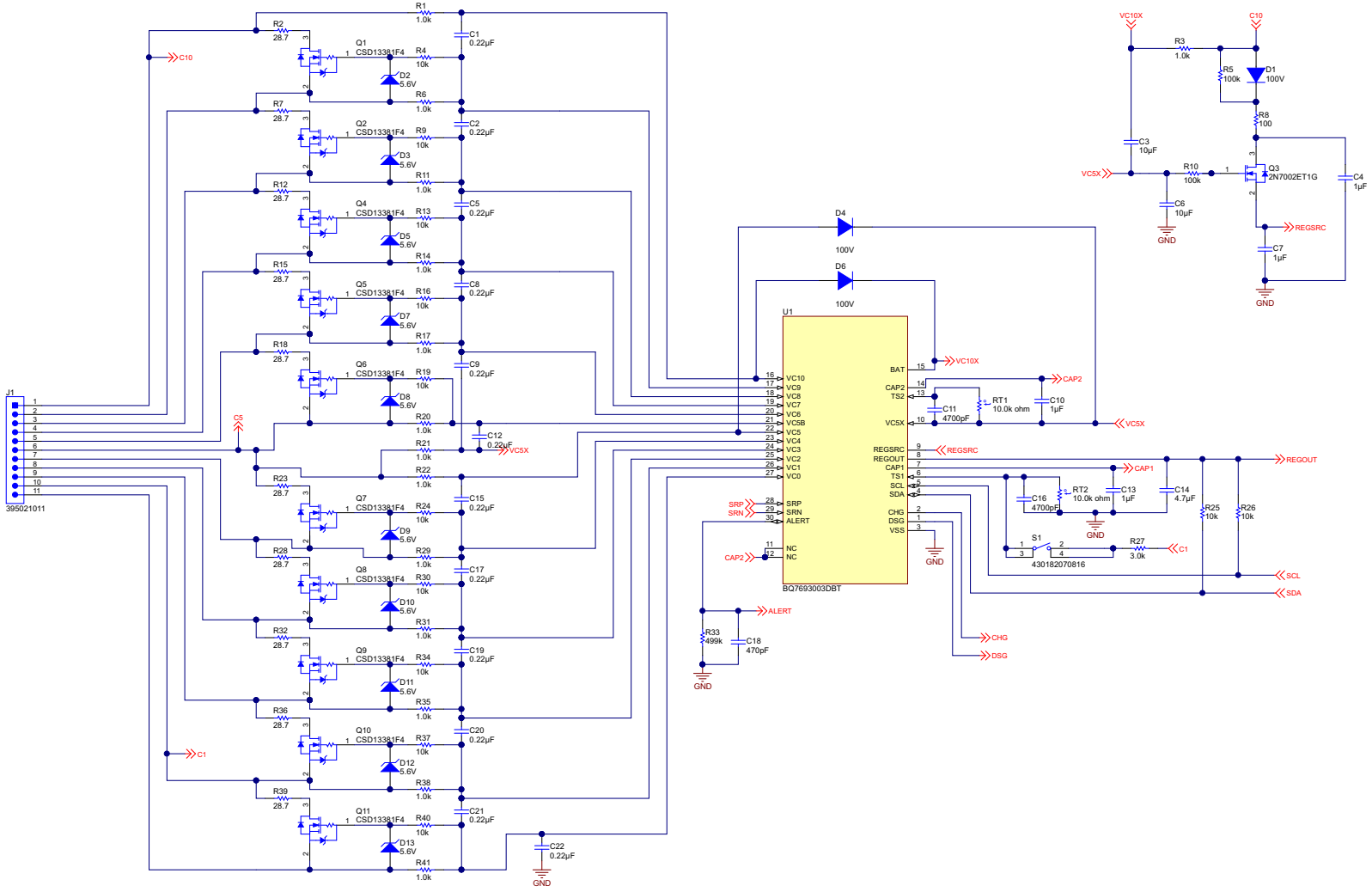


Figure 19. AFE Schematic

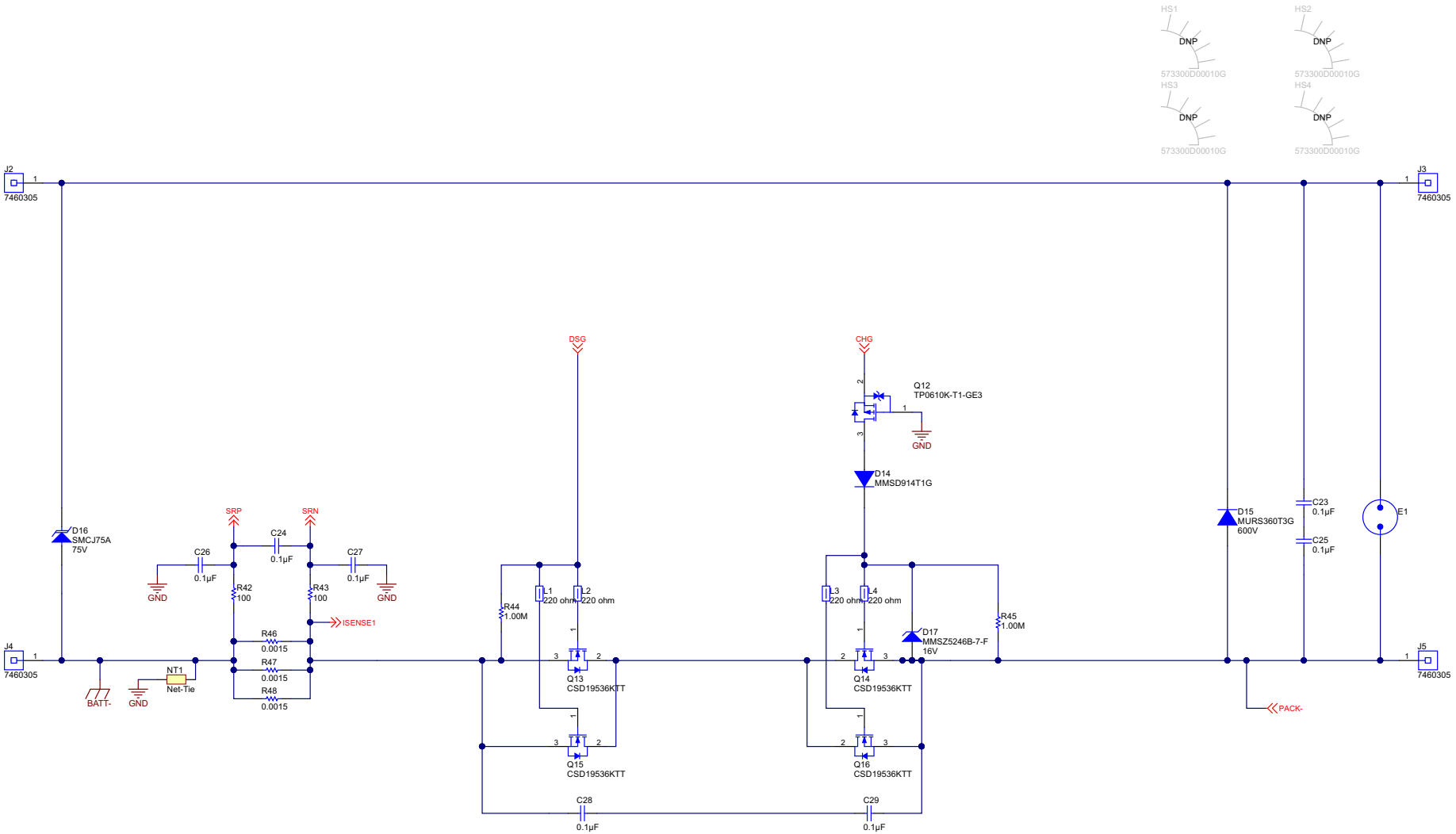


Figure 20. Sense Resistor and Protection FETs Schematic

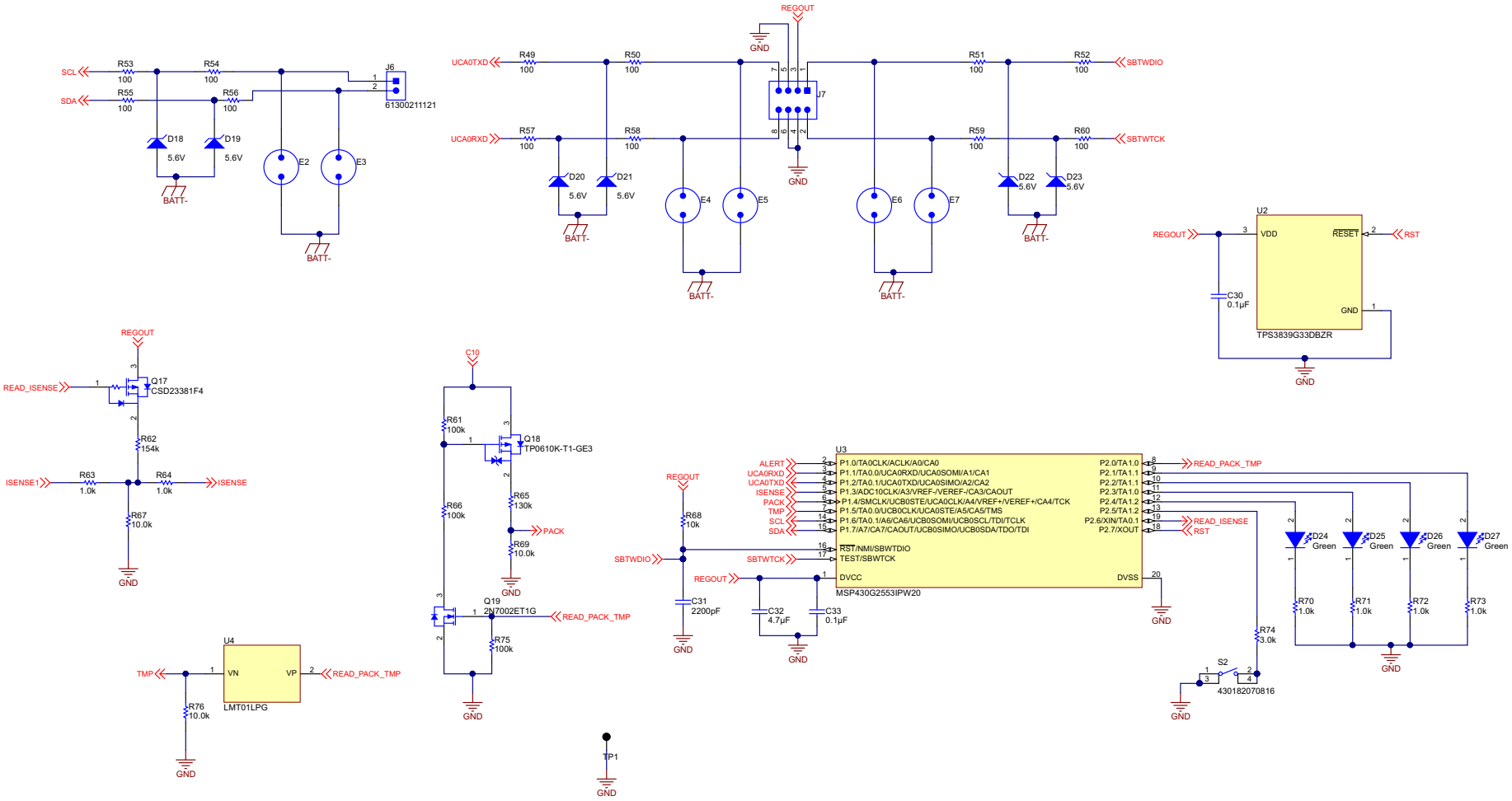


Figure 21. Battery Management Controller Schematic

11.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00449.

Table 6. BOM

ITEM	QTY	REFERENCE	VALUE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT
1	1	!PCB1		Printed Circuit Board	Any	TIDA-00449	
2	12	C1, C2, C5, C8, C9, C12, C15, C17, C19, C20, C21, C22	0.22uF	CAP, CERM, 0.22 µF, 16 V, +/- 10%, X7R, 0603_095	Wurth Elektronik	885012206048	0603_095
3	2	C3, C6	10uF	CAP, CERM, 10uF, 35V, +/-10%, X7R, 1210	MuRata	GRM32ER7YA106KA12L	1210
4	2	C4, C7	1uF	CAP, CERM, 1 µF, 50 V, +/- 10%, X7R, 0805	MuRata	GRM21BR71H105KA12L	0805
5	2	C10, C13	1uF	CAP, CERM, 1 µF, 16 V, +/- 10%, X7R, 0603_095	Wurth Elektronik	885012206052	0603_095
6	2	C11, C16	4700pF	CAP, CERM, 4700 pF, 50 V, +/- 10%, X7R, 0603_095	Wurth Elektronik	885012206087	0603_095
7	2	C14, C32	4.7uF	CAP, CERM, 4.7 µF, 10 V, +/- 10%, X7R, 0805	Wurth Elektronik	885012207025	0805
8	1	C18	470pF	CAP, CERM, 470 pF, 50 V, +/- 10%, X7R, 0603_095	Wurth Elektronik	885012206081	0603_095
9	4	C23, C25, C28, C29	0.1uF	CAP, CERM, 0.1uF, 100V, +/-10%, X7R, 0603	MuRata	GRM188R72A104KA35D	0603
10	3	C24, C26, C27	0.1uF	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603_095	Wurth Elektronik	885012206095	0603_095
11	2	C30, C33	0.1uF	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603_095	Wurth Elektronik	885012206046	0603_095
12	1	C31	2200pF	CAP, CERM, 2200 pF, 16 V, +/- 10%, X7R, 0603_095	Wurth Elektronik	885012206036	0603_095
13	3	D1, D4, D6	100V	Diode, Ultrafast, 100V, 0.15A, SOD-123	Diodes Inc.	1N4148W-7-F	SOD-123
14	16	D2, D3, D5, D7, D8, D9, D10, D11, D12, D13, D18, D19, D20, D21, D22, D23	5.6V	Diode, Zener, 5.6V, 200mW, SOD-323	Diodes Inc.	MMSZ5232BS-7-F	SOD-323
15	1	D14	100V	Diode, Switching, 100 V, 0.2 A, SOD-123	ON Semiconductor	MMSD914T1G	SOD-123
16	1	D15	600V	Diode, Ultrafast, 600V, 3A, SMC	ON Semiconductor	MURS360T3G	SMC
17	1	D16	75V	Diode, TVS, Uni, 75V, 1500W, SMC	Fairchild Semiconductor	SMCJ75A	SMC
18	1	D17	16V	Diode, Zener, 16V, 500mW, SOD-123	Diodes Inc.	MMSZ5246B-7-F	SOD-123
19	4	D24, D25, D26, D27	Green	LED, Green, SMD	Wurth Elektronik	150060GS75000	LED_0603

Table 6. BOM (continued)

ITEM	QTY	REFERENCE	VALUE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT
20	3	FID1, FID2, FID3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	Fiducial
21	4	H1, H2, H3, H4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)	Transparent Bumpon
22	4	HS1, HS2, HS3, HS4		Heatsink, DDPAK/TO-263, SMT	Aavid	573300D00010G	Heatsink, DDPAk
23	1	J1		Terminal block, 3.5mm, 11x1, R/A, TH	Molex	395021011	39.90x7.03x9.33 mm
24	4	J2, J3, J4, J5		Power Element Bush, M5, 4x2	Wurth Elektronik	7460305	Power Bush
25	1	J6		Header, 2.54 mm, 2x1, Gold, TH	Wurth Elektronik	61300211121	Header, 2.54mm, 2x1, TH
26	1	J7		Header, 100mil, 4x2, Tin, TH	Sullins Connector Solutions	PEC04DAAN	Header, 4x2, 100mil, Tin
27	4	L1, L2, L3, L4	220 ohm	Ferrite Bead, 220 ohm @ 100 MHz, 2.5 A, 0603	MuRata	BLM18SG221TN1D	0603
28	10	Q1, Q2, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11	12V	MOSFET, N/P-CH, 12 V, 2.1 A, 1.0x0.35x0.6mm	Texas Instruments	CSD13381F4	1.0x0.35x0.6mm
29	2	Q3, Q19	60V	MOSFET, N-CH, 60 V, 0.26 A, SOT-23	ON Semiconductor	2N7002ET1G	SOT-23
30	2	Q12, Q18	-60V	MOSFET, P-CH, -60 V, -0.185 A, SOT-23	Vishay-Siliconix	TP0610K-T1-GE3	SOT-23
31	4	Q13, Q14, Q15, Q16	100V	MOSFET, N-CH, 100 V, 200 A,	Texas Instruments	CSD19536KTT	
32	1	Q17	-12V	MOSFET, P-CH, -12 V, -2.3 A,	Texas Instruments	CSD23381F4	
33	20	R1, R3, R6, R11, R14, R17, R20, R21, R22, R29, R31, R35, R38, R41, R63, R64, R70, R71, R72, R73	1.0k	RES, 1.0 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00JNEA	0603
34	10	R2, R7, R12, R15, R18, R23, R28, R32, R36, R39	28.7	RES, 28.7, 1%, 0.75 W, 2010	Vishay-Dale	CRCW201028R7FKEF	2010
35	13	R4, R9, R13, R16, R19, R24, R25, R26, R30, R34, R37, R40, R68	10k	RES, 10 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0JNEA	0603
36	2	R5, R10	100k	RES, 100k ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW0805100KFKEA	0805
37	15	R8, R42, R43, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60	100	RES, 100 ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW0805100RFKEA	0805
38	2	R27, R74	3.0k	RES, 3.0 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06033K00JNEA	0603
39	1	R33	499k	RES, 499 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603499KFKEA	0603
40	2	R44, R45	1.00Meg	RES, 1.00 M, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031M00FKEA	0603

Table 6. BOM (continued)

ITEM	QTY	REFERENCE	VALUE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT
41	3	R46, R47, R48	0.0015	RES, 0.0015, 1%, 2 W, AEC-Q200 Grade 0, 2512	TT Electronics/IRC	ULRB22512R0015FLFSLT	2512
42	3	R61, R66, R75	100k	RES, 100 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603100KJNEA	0603
43	1	R62	154k	RES, 154 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603154KFKEA	0603
44	1	R65	130k	RES, 130 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603130KFKEA	0603
45	3	R67, R69, R76	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0FKEA	0603
46	2	RT1, RT2	10.0k ohm	Thermistor NTC, 10.0k ohm, 1%, Disc, 5x8.4 mm	SEMITEC Corporation	103AT-2	Disc, 5x8.4 mm
47	2	S1, S2		Switch, SPST-NO, Off-Mom, 1 Pos, 0.05A, 12 VDC, SMT	Wurth Elektronik	430182070816	6.2x6.2mm
48	1	TP1	Black	Test Point, Miniature, Black, TH	Keystone	5001	Black Miniature Testpoint
49	1	U1		Battery Monitor for Lithium-Ion and Phosphate Battery Packs, DBT0030A	Texas Instruments	BQ7693003DBT	DBT0030A
50	1	U2		Ultralow Power, Supply Voltage Supervisor, DBZ0003A	Texas Instruments	TPS3839G33DBZR	DBZ0003A
51	1	U3		16 MHz Mixed Signal Microcontroller with 16 KB Flash, 512 B SRAM and 24 GPIOs, -40 to 85 degC, 20-pin SOP (PW), Green (RoHS & no Sb/Br)	Texas Instruments	MSP430G2553IPW20	PW0020A
52	1	U4		0.5°C Accurate 2-Pin Digital NTC or PTC Thermistor Replacement, LPG0002A	Texas Instruments	LMT01LPG	LPG0002A

11.3 PCB Layer Plots

To download the layer plots, see the design files at TIDA-00449.

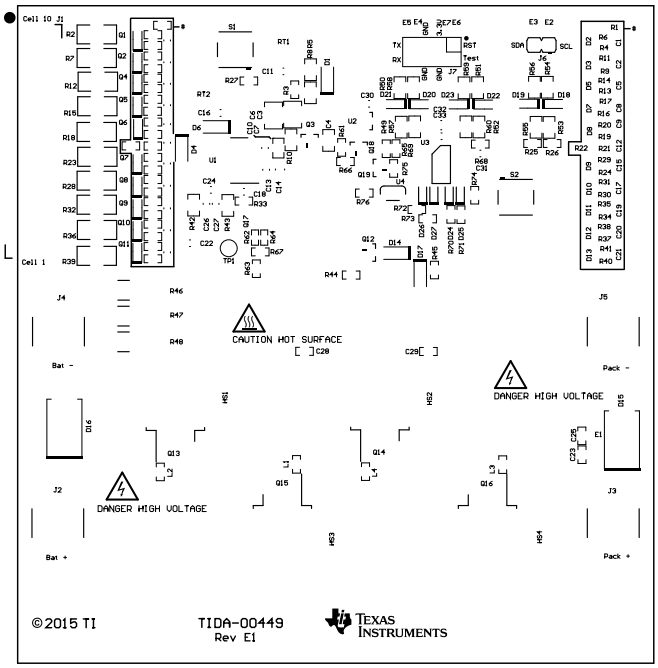


Figure 22. Top Overlay

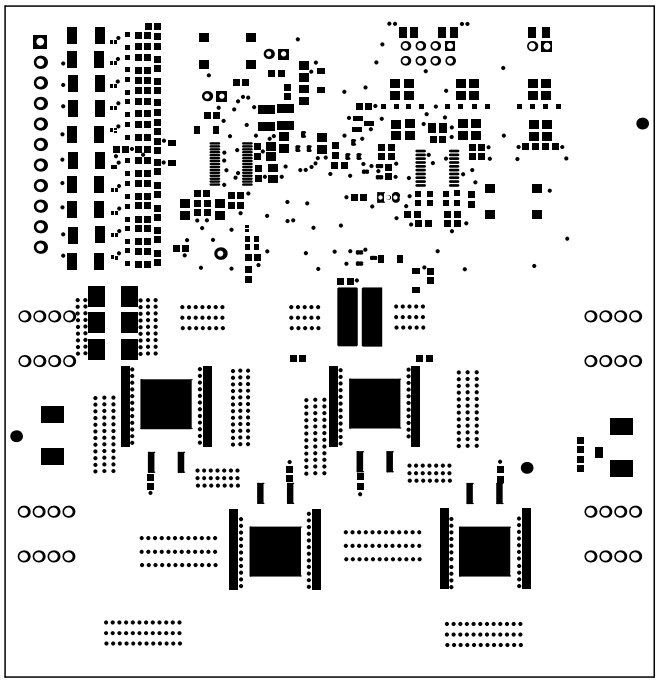


Figure 23. Top Solder Mask

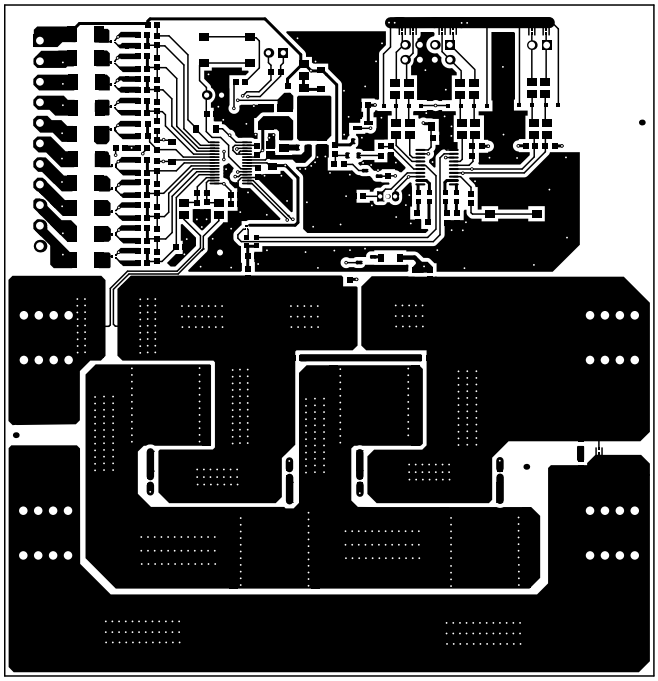


Figure 24. Top Layer

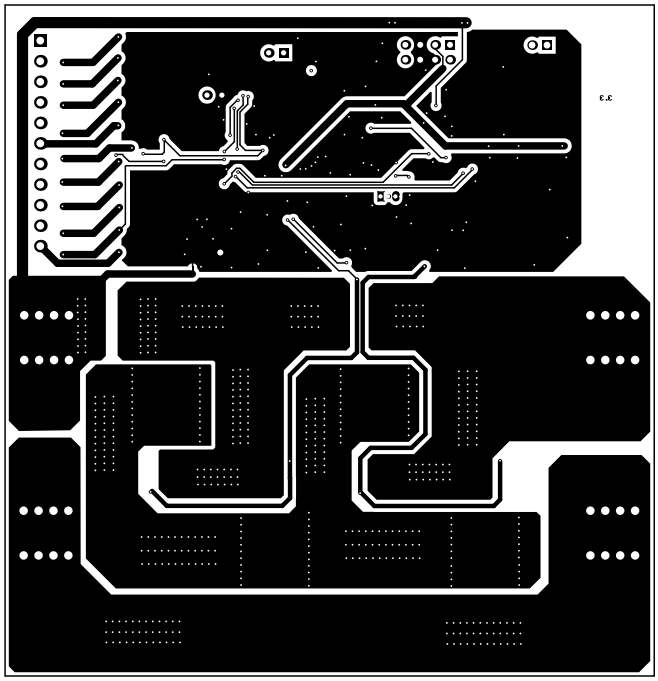


Figure 25. Bottom Layer

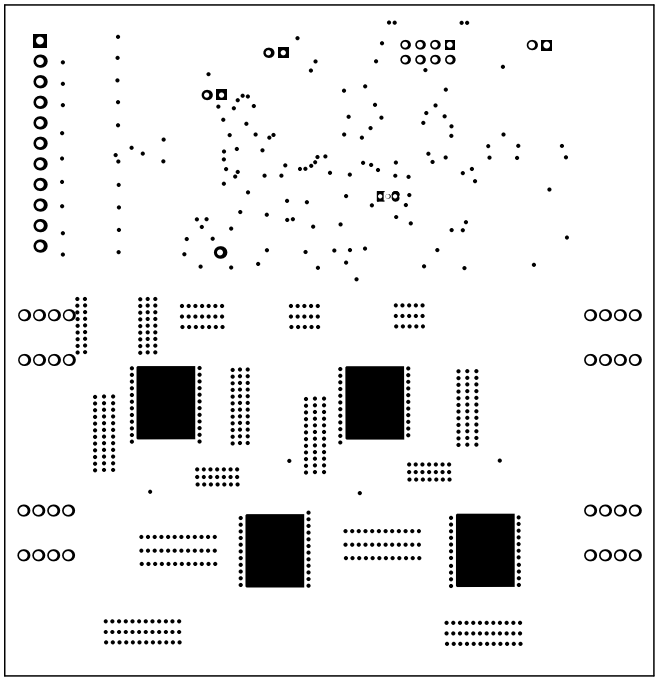


Figure 26. Bottom Solder Mask

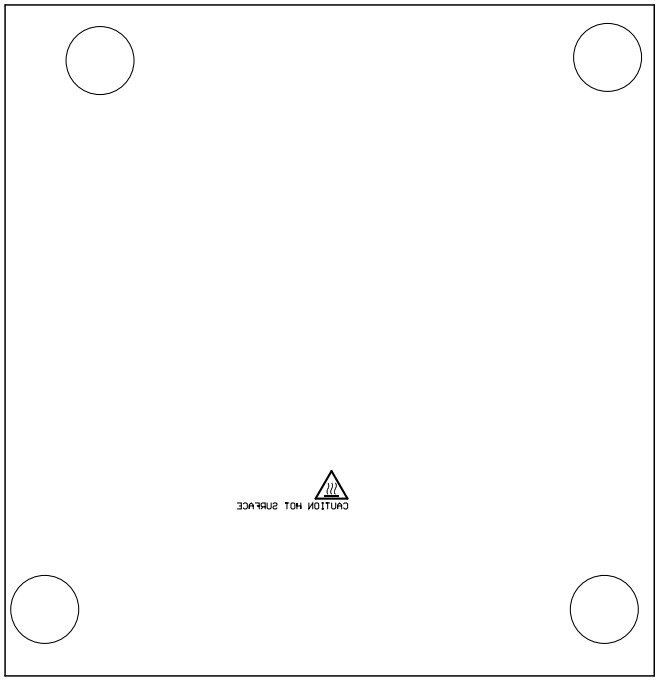
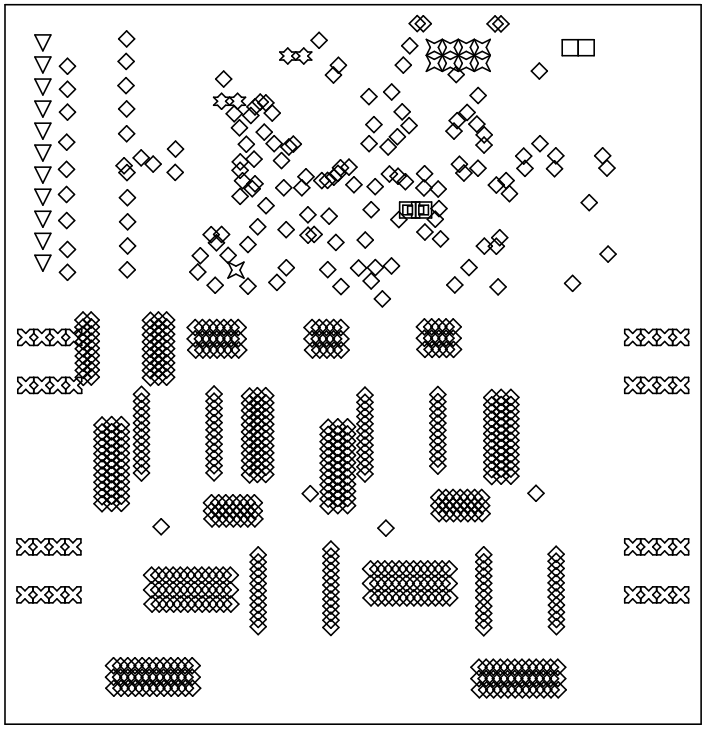


Figure 27. Bottom Overlay



Symbol	Quantity	Finished Hole Size	Plated	Hole Type
○	1	29.53mil (0.750mm)	NPTH	Round
◇	665	12.00mil (0.305mm)	PTH	Round
◘	2	29.53mil (0.750mm)	PTH	Round
✡	4	35.00mil (0.889mm)	PTH	Round
✖	9	40.00mil (1.016mm)	PTH	Round
□	2	45.28mil (1.150mm)	PTH	Round
▽	11	52.00mil (1.321mm)	PTH	Round
⊠	32	57.09mil (1.450mm)	PTH	Round
	726 Total			

Figure 28. Drill Drawing

11.4 Layout Guidelines

The first decision concerning the layout was to only populate components on the top layer because of cost as well as to facilitate integrating a battery pack. The decision was made to use a dual-layer board with copper 2 oz thick. The dual layer is a good compromise between cost and routing complexity, and the 2-oz thick copper helps with the high current of the application.

The layout of the TIDA-00449 contains two blocks:

- The FETs block, which handles the high current, consisting of the sense resistors, the protection FETs, and the high current connectors
- The control block, which only handles low current, consisting of the rest of the components (balancing circuit, AFE, MCU)

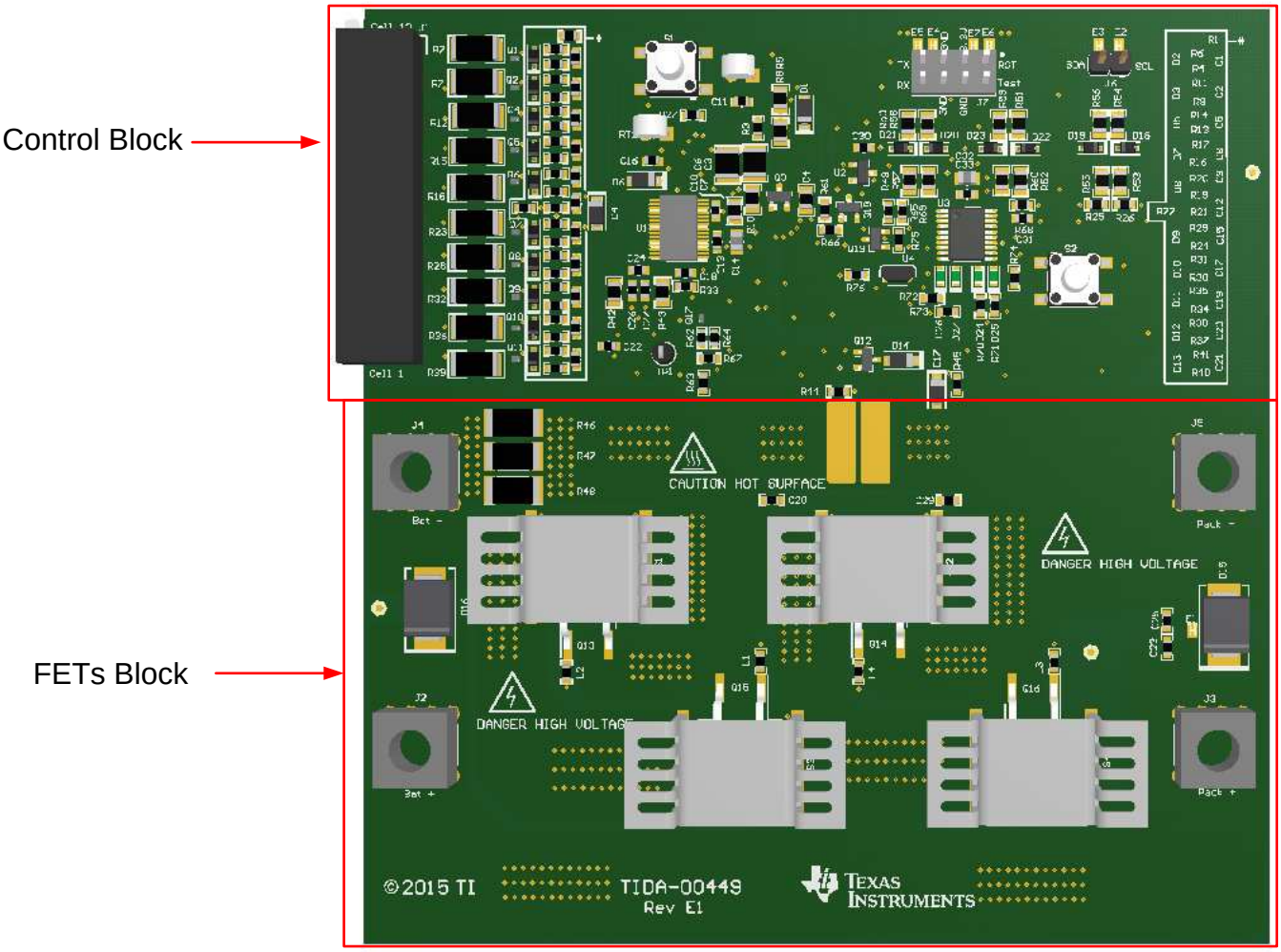


Figure 29. Layout Blocks

11.4.1 FETs Block

The main consideration for the layout of this section is the heat generated by the high current passing through the sense resistors and the protection FETs. In addition to the 2-oz thick copper, wide traces (>350-mil wide) are used for the routing between Bat– and Pack– and between Bat+ and Pack+ on both top and bottom layers with a fair number of vias to link the two layers.

A pad added on the bottom layer under each of the four protection FETs allows the possibility to add a heat sink on the bottom layer.

In some applications, protections FETs are not used; for this reason, two pads were added to bypass the protection FETs.

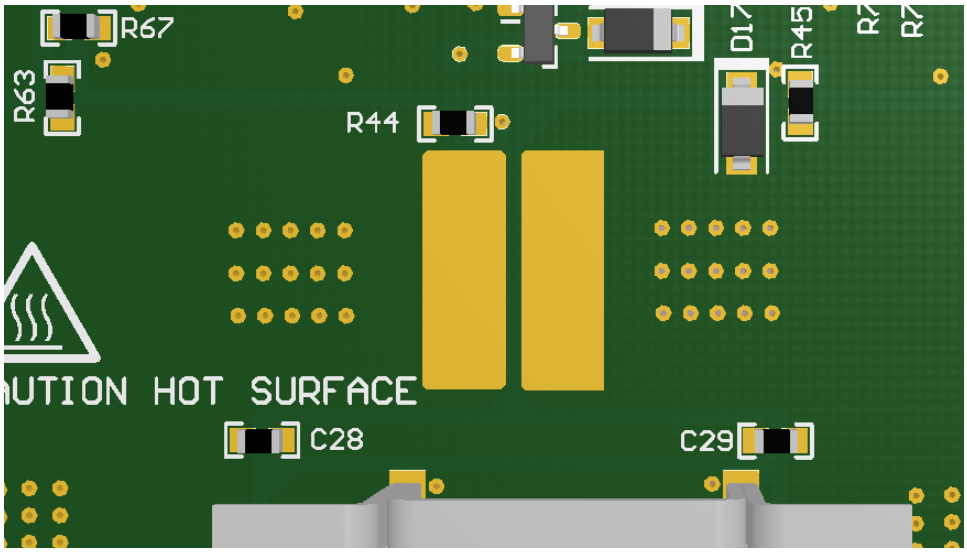


Figure 30. Protection FETs Bypass Option

11.4.2 Control Block

To decrease the parasitic PCB impedance, the grounding of the control block is connected to the high current, Bat– trace through a net tie.

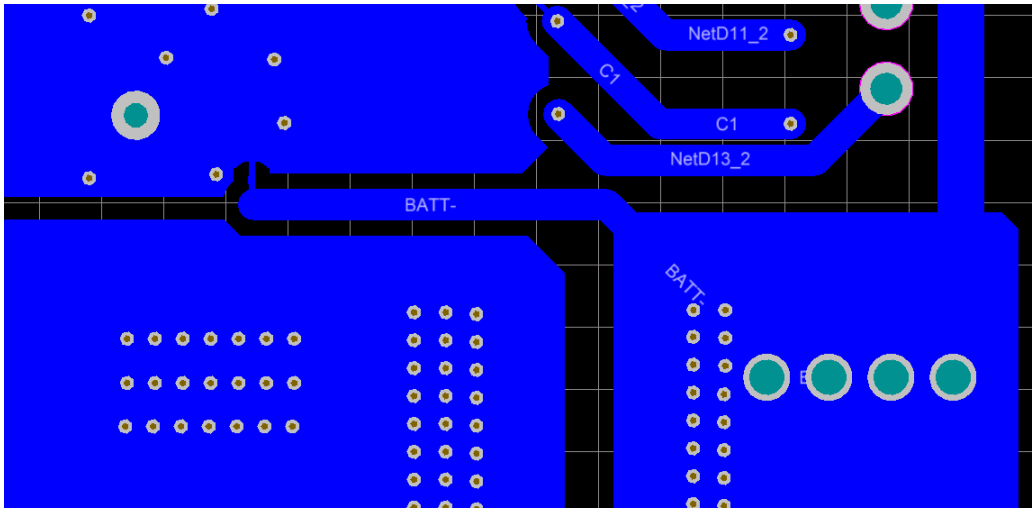


Figure 31. Ground Connection Through Net Tie

Some spark gaps (E1 through E7) were added on the connectors that are going out of the battery pack (UART, SBW, Pack– and Pack+) to help the pack withstand ESD.

11.5 Altium Project

To download the Altium project files, see the design files at TIDA-00449.

11.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00449.

11.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00449.

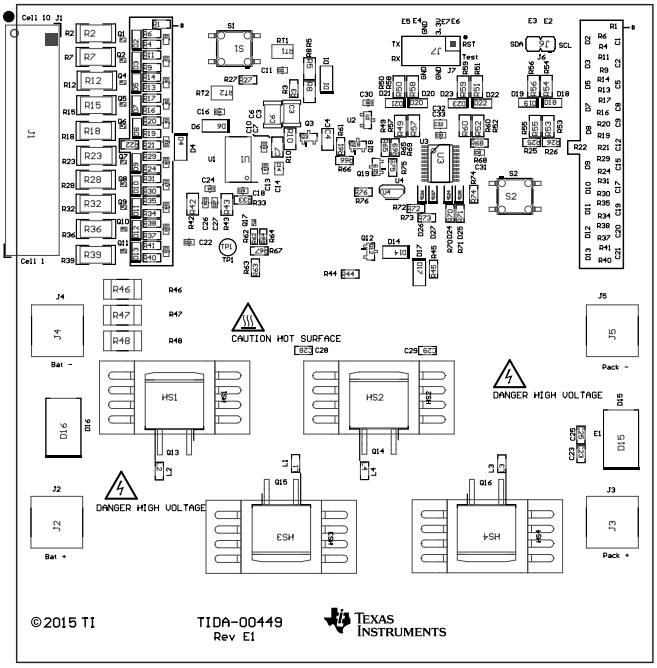


Figure 32. Top Assembly Drawing

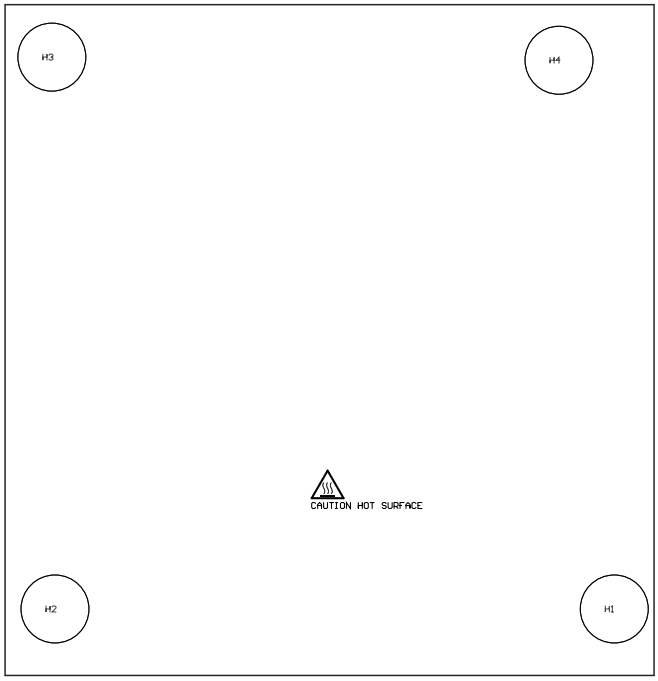


Figure 33. Bottom Assembly Drawing

12 Related Documentation

1. Texas Instruments, *bq769x0 Family Top 10 Design Considerations*, Application Report (SLUA749)
2. Texas Instruments, *bq76930 and bq76940 Evaluation Module*, User's Guide (SLVU925)
3. Texas Instruments, *bq76920, bq76930, bq76940 AFE FAQ*, User's Guide (SLUUB41)
4. Texas Instruments, *I^2C Communication Sample Code for the bq76940 with a CRC Option Based on the MSP430G2553*, Application Report (SLVA626)
5. Texas Instruments, *PCB Layout Guidelines for Fuel Gauge Design*, Video (https://training.ti.com/pcb-layout-guidelines-fuel-gauge-design)

12.1 Trademarks

13 About the Author

KEVIN STAUDER is a System Engineer in the Industrial Systems–Motor Drive team at Texas Instruments, who is responsible for developing reference designs for industrial drives.

RENTON MA is a System Engineer in the Industrial Systems–Motor Drive team at Texas Instruments, who is responsible for developing reference designs for industrial drives.

Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (October 2015) to B Revision	Page
• Changed title	1

Revision A History

Changes from Original (September 2015) to A Revision	Page
• Changed from preview page	1

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