Version: 1.0

Technical Specification

MODEL NO: 7.3inch e-Paper (F)

The content of this information is subject to be changed without notice. Please contact Waveshare

Revision History

Rev.	Issued Date	Revised Contents
0.1	2021.09.10	Tentative
1.0	2021.11.29	Final

TECHNICAL SPECIFICATION

CONTENTS

1. Application

This is a reflective electrophoretic E Ink® technology display module on an active matrix TFT substrate. The diagonal length of the active area is 7.3” and contains 800 x 480 pixels. The panel is capable of displaying 7-colors of black, white, red, yellow, blue, green, and orange images depending on the associated lookup table used. The circuitry on the panel includes an integrated gate and source driver, timing controller, oscillator, DC-DC boost circuit, and memory to store the frame buffer and lookup tables, and additional circuitry to control VCOM and BORDER settings.

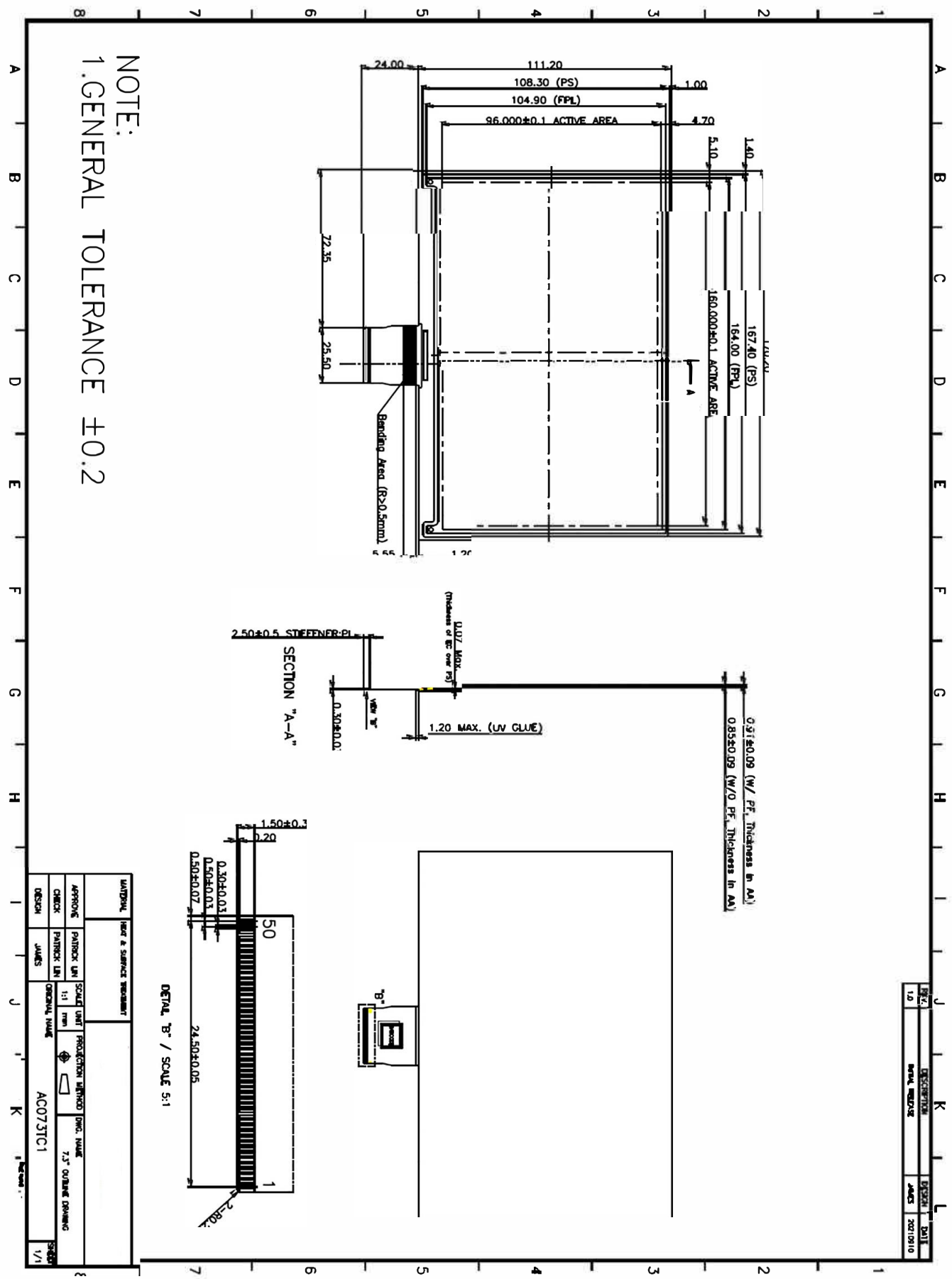
2. Features

- E Ink Gallery Palette™ display
- High contrast TFT electrophoretic
- 800 x 480 display
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Low current sleep mode
- On chip display RAM
- Serial Peripheral Interface
- External SPI flash/eeprom for waveform
- On-chip oscillator
- On-chip booster and regulator control for generating Vcom, Gate and Source driving voltage
- I2C Signal Master Interface to read external temperature sensor
- Operational temperature range (15 ~ 35℃)

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	7.3	Inch	
Display Resolution	800 (H) × 480 (V)	Pixel	127 PPI
Active Area	160 (H) × 96 (V)	mm	
Pixel Pitch	200 (H) × 200 (V)	um	
Outline Dimension	170.2 (H) × 111.2 (V) × 0.91 (D)	mm	With protective film
Module Weight	33.0±3.3 g	g	

4. Mechanical Drawing of EPD Module



5. Input/Output Interface

5-1) Recommended Connector Type of Panel

FH34SRJ-50S-0.5SH(50)

5-2) Pin Assignment of Panel

Pin #	Type	Single	Description	Remark
1		NC	No connection and do not connect with other NC pins	
2	P	TFT_VCOM	TFT_VCOM driving voltage	
3	P	FPL_VCOM	FPL_VCOM driving voltage	
4		NC	NC	
5	I/O	GDRH	N-Channel MOSFET Gate Drive Control	
6	I/O	RESEH	Current Sense Input for the Control Loop	
7		GDRL	Reserved	
8	P	GND	Ground	
9	I/O	GDRC	P-Channel MOSFET Gate Drive Control	
10	I/O	RESEC	Current Sense Input for the Control Loop	
11	P	VPC	VPC driving voltage	
12	P	GND	Ground	
13	P	VGL	Negative Gate driving voltage	
14	P	VPH	VPH driving voltage	
15	P	VSH	Positive Source driving voltage	
16	P	VSH_LV	Positive Source driving voltage	
17	P	VSH_LV2	Positive Source driving voltage	
18	P	VSL	Negative Source driving voltage	
19	P	VSL_LV	Negative Source driving voltage	
20	P	VSL_LV2	Negative Source driving voltage	
21	P	GNDA	Ground ; Connect to GND	
22		REFN	Reserved	
23		REFP	Reserved	
24	O	TSCL	I2C Interface to digital temperature sensor Clock pin	
25	I/O	TSDA	I2C Interface to digital temperature sensor Data pin	
26	I	BS0	Bus selection pin; L: 4-wire IF. **H: 3-wire IF. (Default)**	
27	I	BS1	Bus selection pin; L: refer to BS0. (Default) H: Standard 4-wire SPI/dual SPI/quad SPI	
28	I	RES#	Reset	
29	O	BUSY_N	Busy state output pin	
30	I	D/C#	Data /Command control pin (D/C)	
31	I	CS#	Chip Select input pin (CSB)	
32	I	SCL	Serial clock pin (SPI)	
33	I/O	SI0	serial data pin (SPI)	
34	I/O	SI1	serial data pin ; Reserved	
35	I/O	SI2	serial data pin ; Reserved	
36	I/O	SI3	serial data pin ; Reserved	
37	P	VDDDO	Core logic power pin; Connect to VDDD	

38	P	VDD	Supply voltage	
39	P	GND	Ground; Connect to GNDA	
40	P	VDDIO	Supply voltage	
41	P	VCP2	Charge Pump Pin	
42	P	CP2N	Charge Pump Pin	
43	P	CP2P	Charge Pump Pin	
44	P	VCP1	Charge Pump Pin	
45	P	CP1N	Charge Pump Pin	
46	P	CP1P	Charge Pump Pin	
47		CGH1N	Charge Pump Pin; Reserved	
48		CGH1P	Charge Pump Pin; Reserved	
49	P	VGH	Positive Gate driving voltage	
50	P	VCOMBD	VCOMBD driving voltage	

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active Low.

Note 5-4: This pin (BUSY_N) is Busy state output pin. When Busy is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:

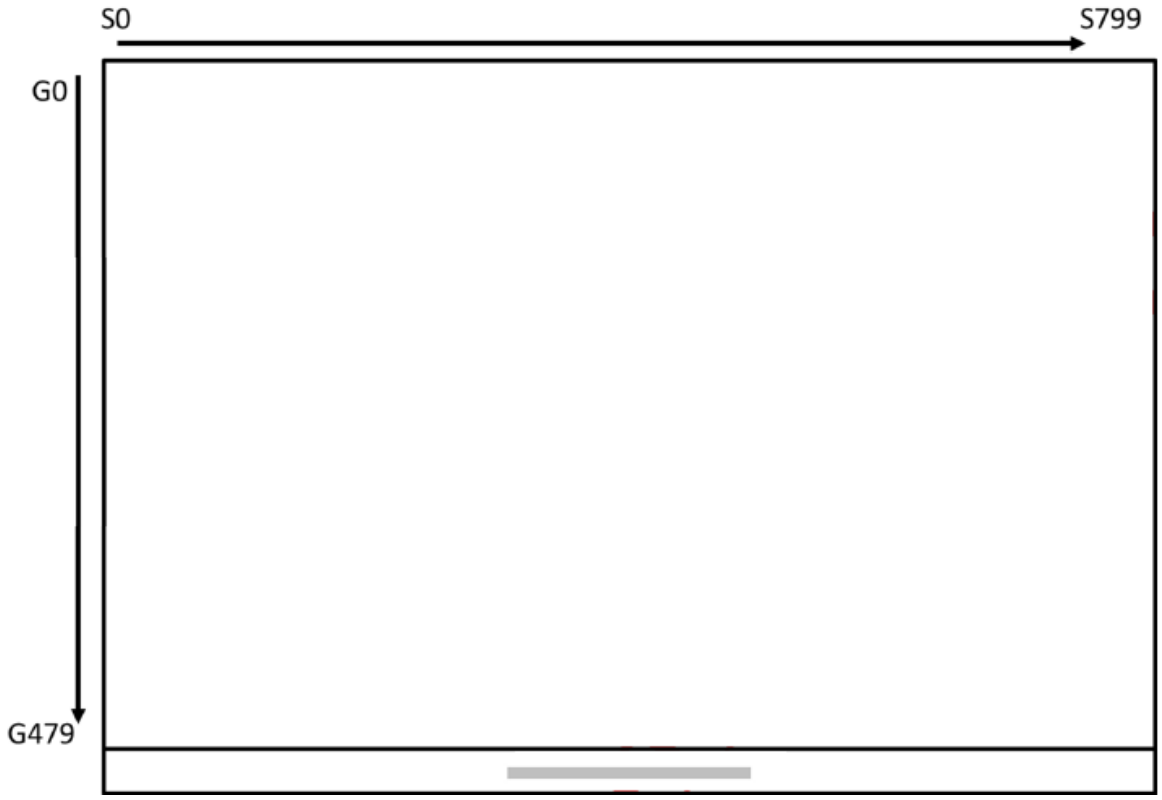
- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-5: This pin (BS0) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS1	**MPU Interface**
L	**4-lines serial peripheral interface (SPI)**
H	**3-lines serial peripheral interface (SPI) – 9 bits SPI**

5-3) Panel Scan direction



6. Command Table

6-1) Register Definition

W/R: 0: Write cycle 1: Read cycle C/D: 0: Command 1: Data D7~D0: -: Don't care

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Setting
1	Power OFF	0	0	0	0	0	0	0	0	1	0		02h
		0	1	0	0	0	0	0	0	0	0		00h
2	Power ON	0	0	0	0	0	0	0	1	0	0		04h
3	Deep Sleep	0	0	0	0	0	0	0	1	1	1		07h
		0	1	1	0	1	0	0	1	0	1		A5h
4	Data Start transmission	0	0	0	0	0	1	0	0	0	0		10h
		0	1	#	#	#	#	#	#	#	#		--
		0	1	..	..	..	..	..	..	..	..		--
		0	1	#	#	#	#	#	#	#	#		--
5	Data Refresh	0	0	0	0	0	1	0	0	1	0		12h
		0	1	0	0	0	0	0	0	0	1		01h

6-1-1) R02H : Power OFF Command

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0
	0	1	0	0	0	0	0	0	0	0

6-1-2) R04H : Power ON Command

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the power	0	0	0	0	0	0	0	1	0	0

6.1.1 6-1-3) R07H : Deep sleep

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver.

6.1.2 6-1-4) R10H : Data Start Transmission

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Data Start transmission	0	0	0	0	0	1	0	0	0	0
	0	1	#	#	#	#	#	#	#	#
	0	1	..	..	..	..	..	..	..	..
	0	1	#	#	#	#	#	#	#	#

After this command, data entries will be written into the RAM until another command is written.

6.1.3 6-1-5) R12H : Data Refresh

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Data Start transmission	0	0	0	0	0	1	0	0	1	0
	0	1	0	0	0	0	0	0	0	1

When this command is received. IC will start the refresh process. BUSY_N will become "0". After the refresh process is finished, BUSY_N will become "1".

7. Electrical Characteristics

7-1) Absolute Maximum Ratings:

Item	Symbol	Min	Max	Unit
Logic Supply Voltage	VDD	-0.5	+3.6	V
Tst	Storage Temperature	-25	60	℃
Tot	Operating Temperature	15	35	℃

Note: Maximum ratings are those values beyond which damages to the device may occur.
Functional operation should be restricted to the limits in the Electrical Characteristics chapter.
Suggested operation temperature range between 17~31℃ for better optical performance.

7-2) Panel DC characteristics

The following specifications apply for: VDD = 3.3V, VDD_1.8 = 1.8V, TA = 25℃

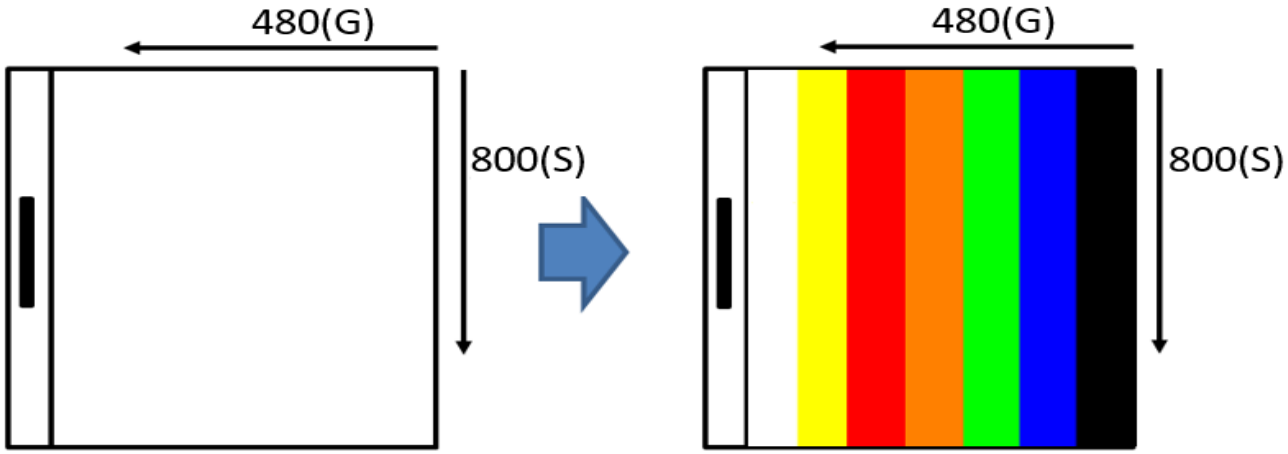
DIGITAL DC CHARACTERISTICS						
Symbol	**Parameter**	**Conditions**	**MIN.**	**TYP.**	**MAX.**	**Unit**
VDD	Logic supply voltage		2.4	3.3	3.6	V
VGH	Positive Gate driving voltage		19	20.0	21	V
VGL	Negative Gate driving voltage		-21	-20.0	-19	V
VSH	Positive source driving voltage		14.5	15.0	15.5	V
VSL	Negative source driving voltage		-15.5	-15.0	-14.5	V
VCOM_DC	VCOM_DC output voltage		-4.0	Adjusted	-0.3	V
VCOM_AC	VCOM_AC output voltage		VSL+ VCOM_DC	--	VSH+ VCOM_DC	V
VIL	Low level input voltage	Digital input pins	0	--	0.2xVDD	V
VIH	High level input voltage	Digital input pins	0.8xVDD	--	VDD	V
VOH	High level output voltage	Digital input pins, IOH= 8 mA	0.8xVDD	--	--	V
VOL	Low level output voltage	Digital input pins, IOL= 8 mA	0	--	0.2xVDD	V
IMSTB	Module stand-by current	Stand-by mode	--	48	--	uA
IMDS	Module deep sleep current	Deep sleep mode	--	1	--	uA
Inc	Inrush Current	High Loading Pattern	--	123	174.2	mA
IMOPR	Module operating current	TYP Loading Pattern	--	14.8	25.8	mA
		High Loading Pattern	--	43.3	59.6	mA
P	Operation Power Dissipation	TYP Loading Pattern VDD=3.3V with DC-DC	--	48.58	84.9	mW

		High Loading Pattern VDD=3.3V with DC-DC		142.7	196.7	mW
PSTBY	Standby Power Dissipation	VDD=3.3V	--	158.4	--	uW

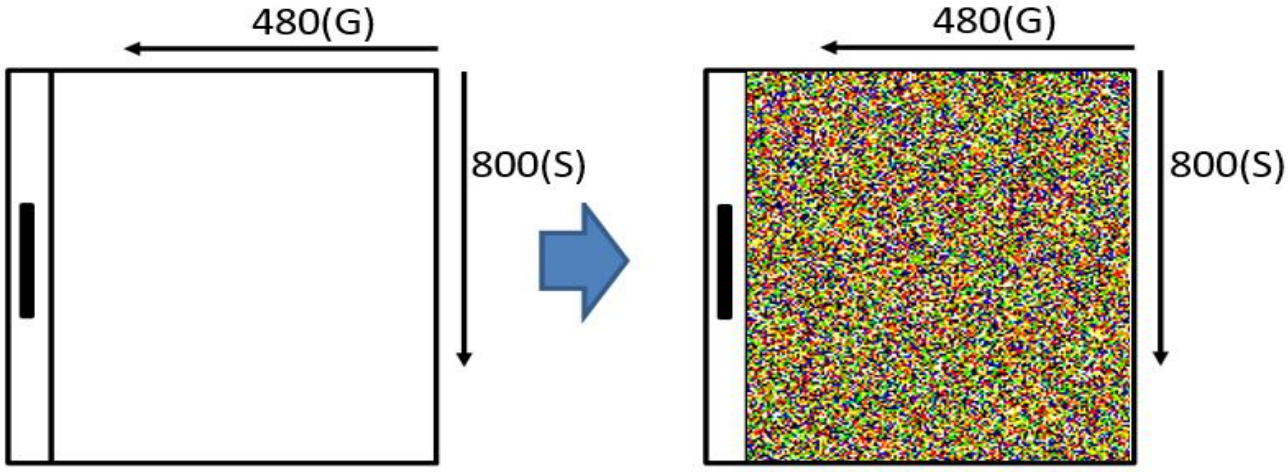
Note: The Module operating current data is measured by using Oscilloscope, and extract the Mean value.

- The typical power consumption is measured using associated 24C waveform with following pattern transition: from full white pattern to color stripe pattern. (Note 7-1)
- The high loading power consumption is measured using associated 24C waveform with following pattern transition: from full white pattern to noise pattern (including random scattering of 7 colors) (Note 7-2)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Waveshare
- Vcom value has been set in the IC on the panel.

Note 7-1
The typical power consumption



Note 7-2
The high loading power consumption



7-3) Panel AC characteristics

7-3-1 MCU Interface

7-3-1-1 MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS0 pins. When it is “High”, 4-wire SPI is selected. When it is “Low”, 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
SPI4	SDIN	SCLK	CS#	D/C#	RES#
SPI3	SDIN	SCLK	CS#	L	RES#

Table 7-1: MCU interface assignment under different bus interface mode

Note 7-3: L is connected to GND

Note 7-4: H is connected to VDD

7-3-1-2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDA, D/C#, CS#.

Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write data	L	H	↑

Table 7-2: Control pins of 4-wire Serial Peripheral interface

Note 7-5: ↑stands for rising edge of signal

SDA is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

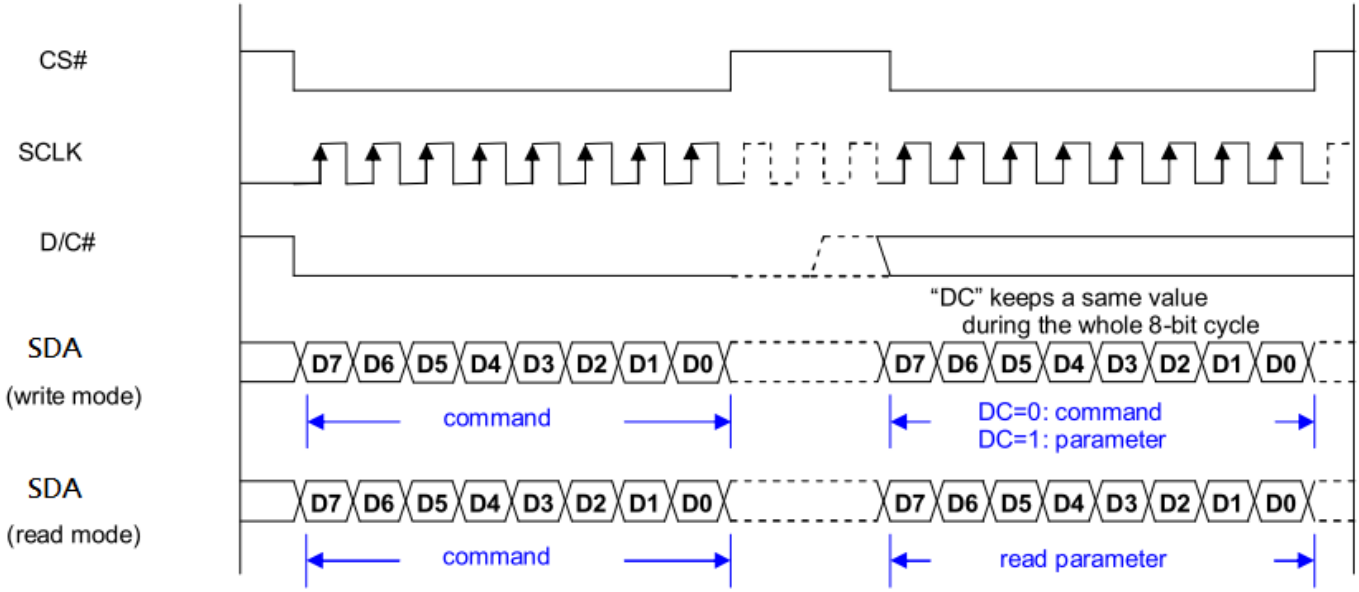


Figure 7-1: Write procedure in 4-wire Serial Peripheral Interface mode

7-3-1-3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDA and CS#.
In 3-wire SPI mode, the pin D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Table 7-3: Control pins of 3-wire Serial Peripheral Interface

Note 7-6: ↑stands for rising edge of signal

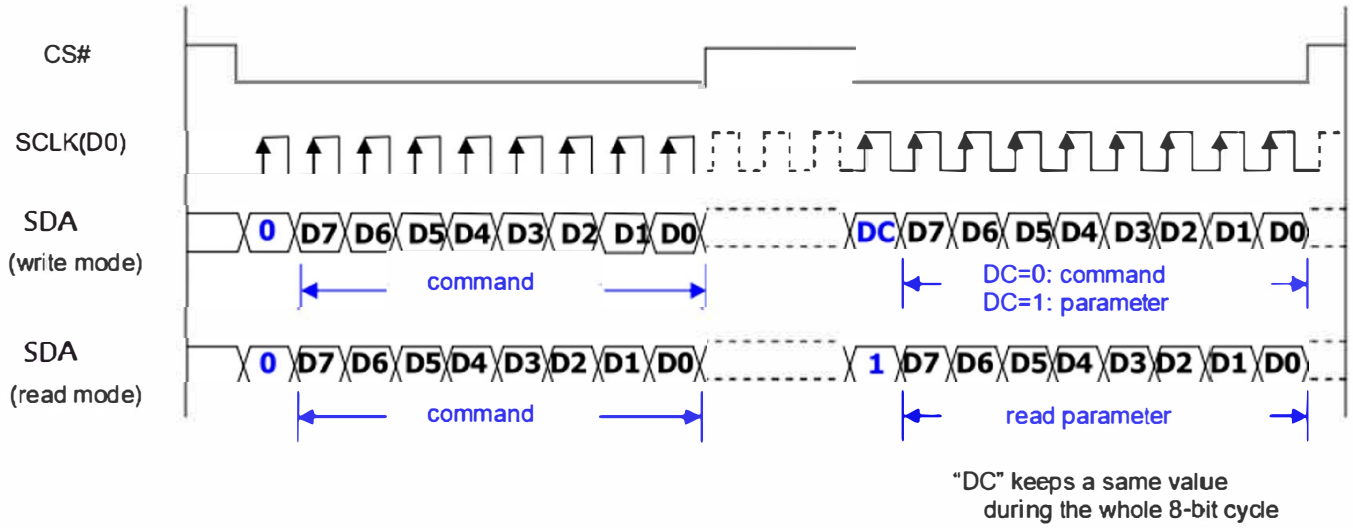


Figure 7-2: Write procedure in 3-wire Serial Peripheral Interface mode

7-3-2 Timing Characteristics of Series Interface

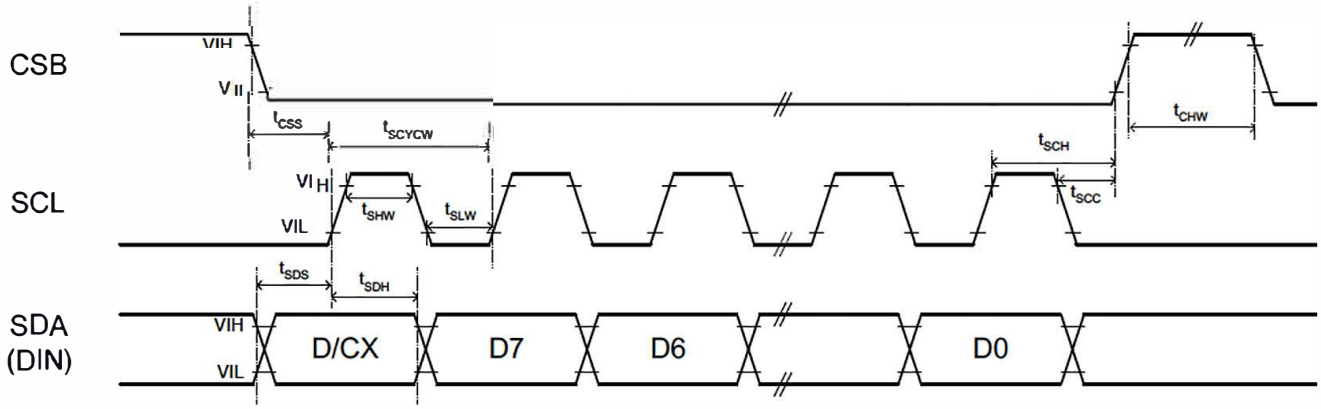
The following specifications apply for: VDDIO - GND = 2.4V to 3.6V, TOPR = 25°C, CL=20pF
Serial Peripheral Interface Timing Characteristics

SYMBOL	SIGNAL			MIN.	TYP.	MAX.	UNIT
tCSS	C/S# (CSB)	Chip select setup time		60			ns
tCSH		Chip select hold time		65			ns
tSCC		Chip select setup time		20			ns
tCHW		Chip select setup time		40			ns
tSCYCW	SCL	Serial clock cycle (Write)		50			ns
tSHW		SCL "H" pulse width (Write)		25			ns

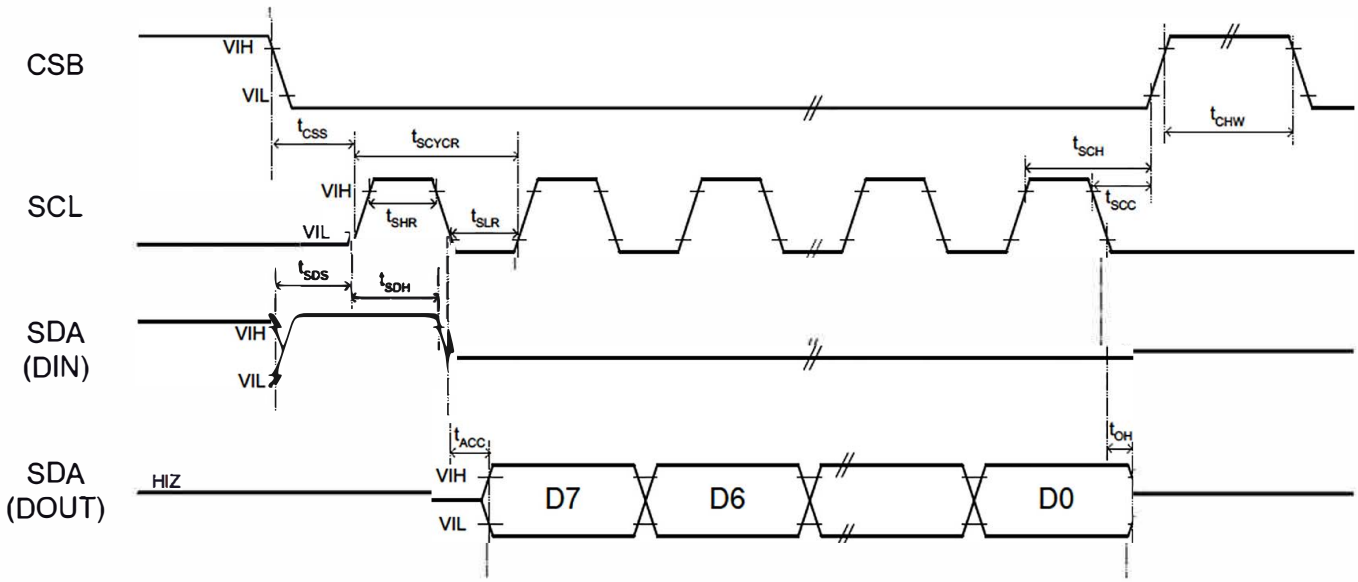
SYMBOL	SIGNAL			MIN.	TYP.	MAX.	UNIT
tSLW		SCL "L" pulse width (Write)		25			ns
tSCYCR		Serial clock cycle (Read)		150			ns
tSHR		SCL "H" pulse width (Read)		60			ns
tSLR		SCL "L" pulse width (Read)		60			ns
tSDS		Data setup time		30			ns
tSDH	SDA (DIN)	Data hold time		30			ns
tACC	(DOUT)	Access time				75	ns
tOH		Output disable time		10			ns

Note: All timings are based on 20% to 80% of VDDIO-GND

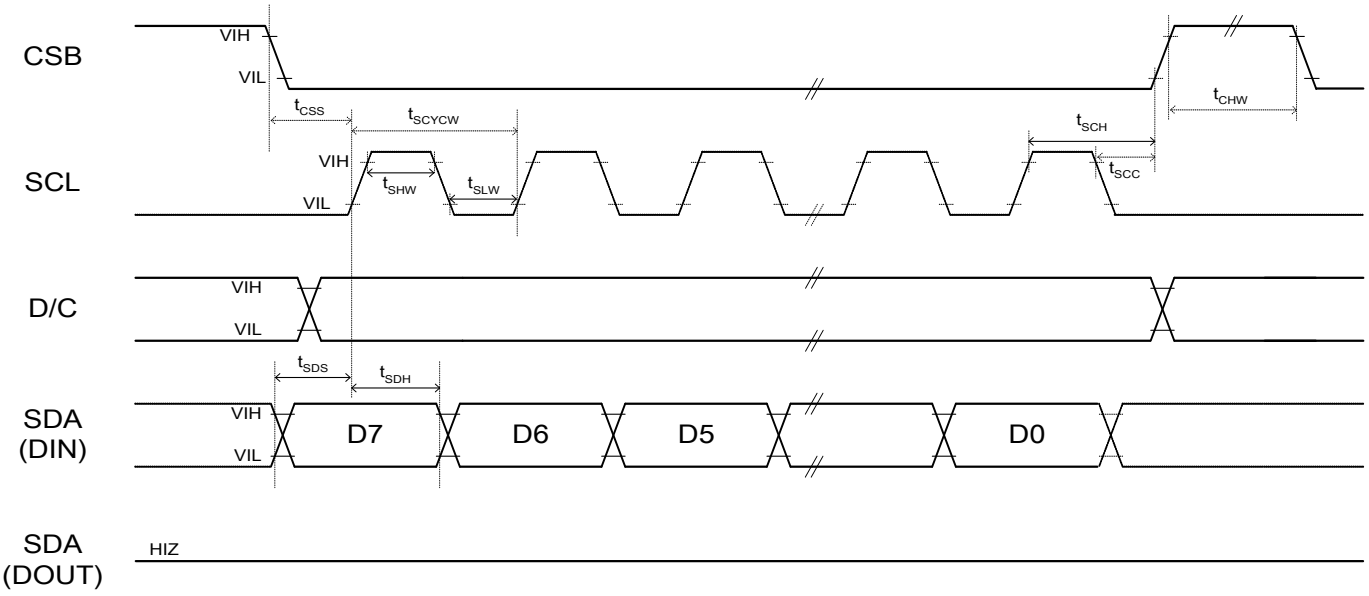
Note 7-3. 3 pin serial interface characteristics (write mode)



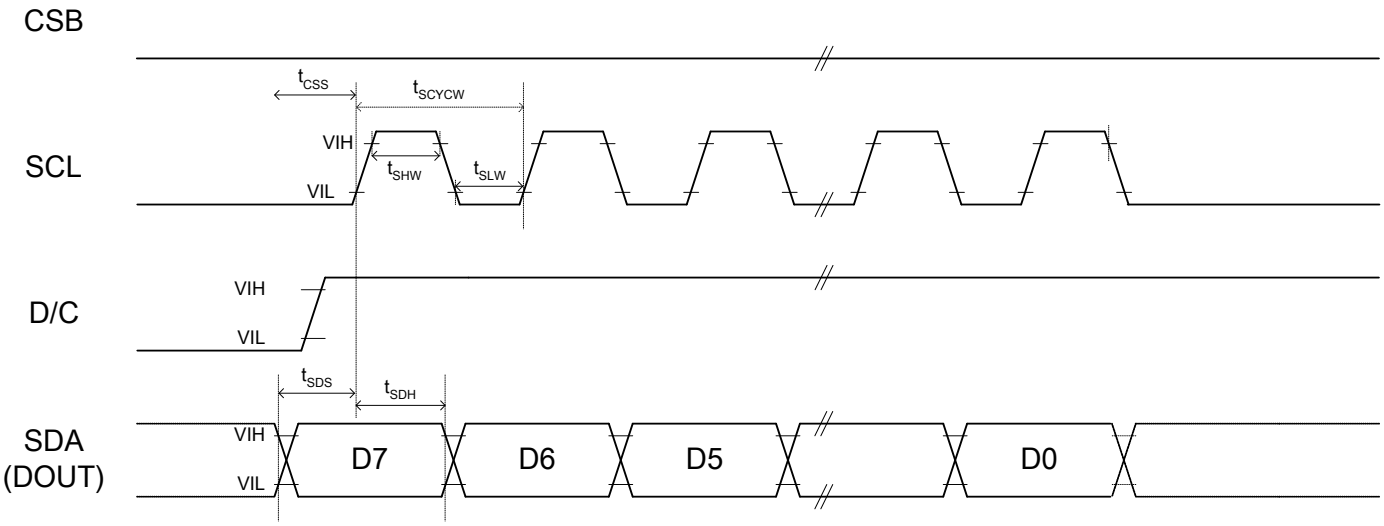
Note 7-4. 3 pin serial interface characteristics (read mode)



Note 7-5. 4 pin serial interface characteristics (write mode)

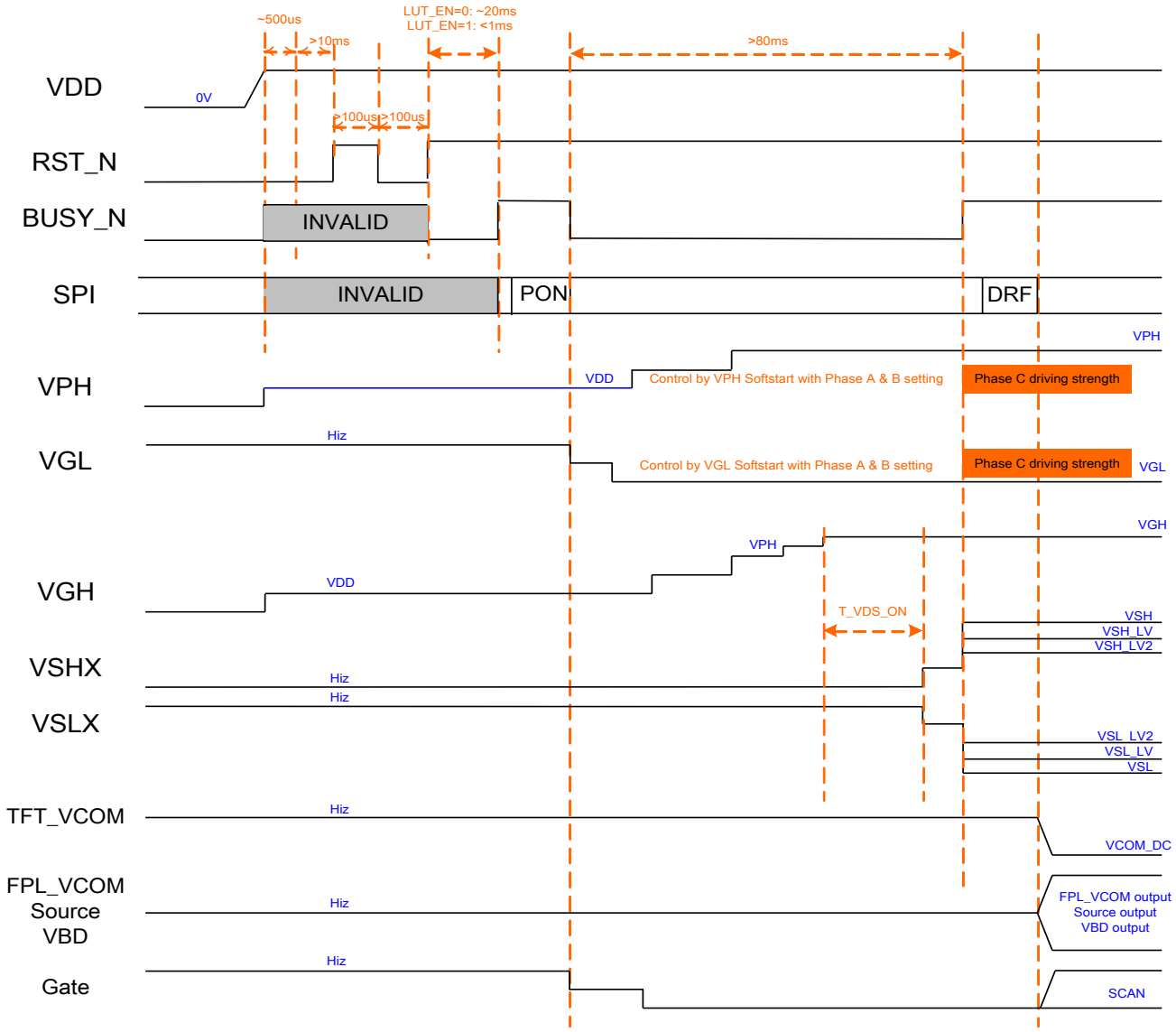


Note 7-6. 4 pin serial interface characteristics (read mode)

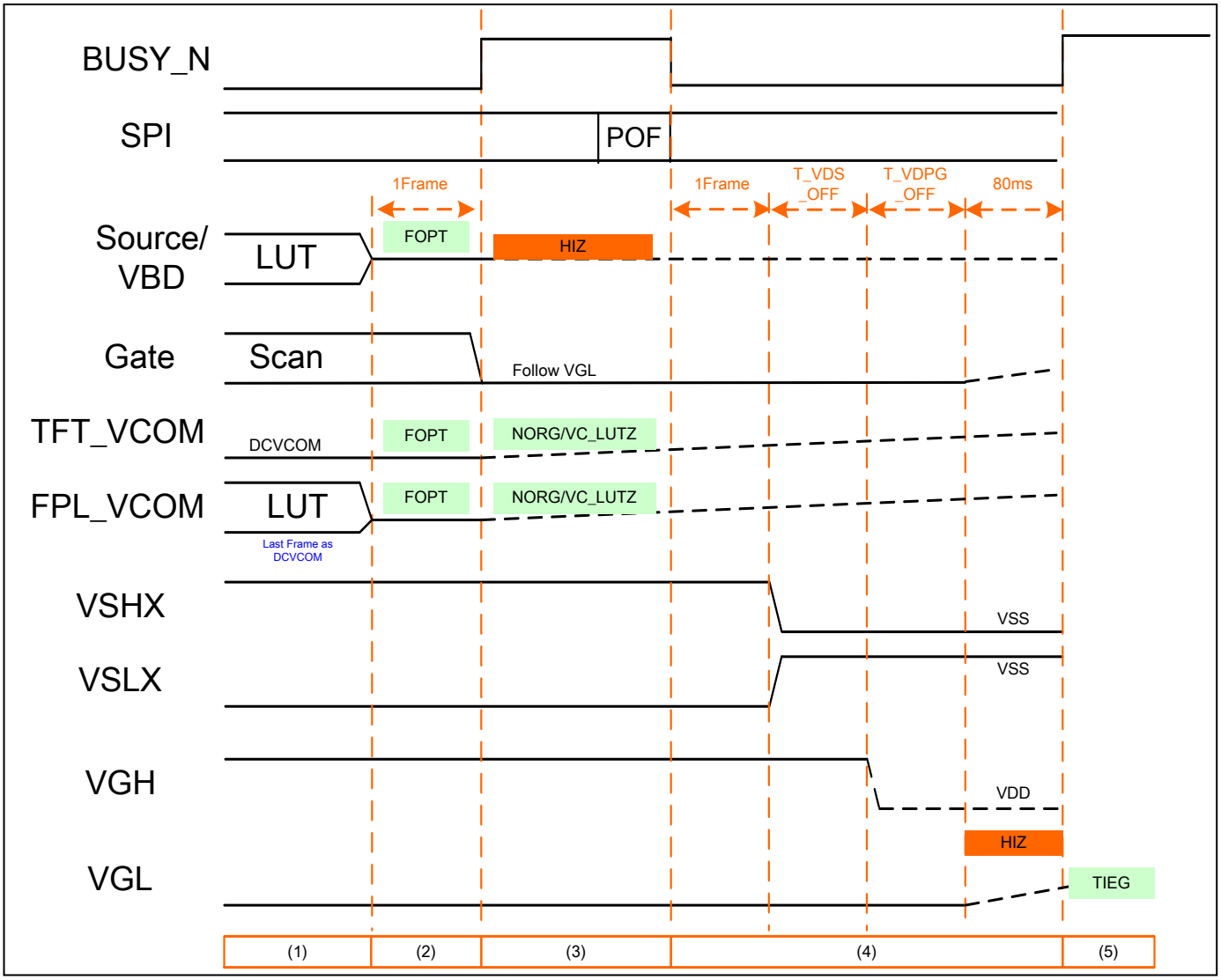


7-3-3) Power On/Off Characteristics

Power ON Sequence



Power OFF Sequence



8. Optical Characteristics

8-1)Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T = 24℃

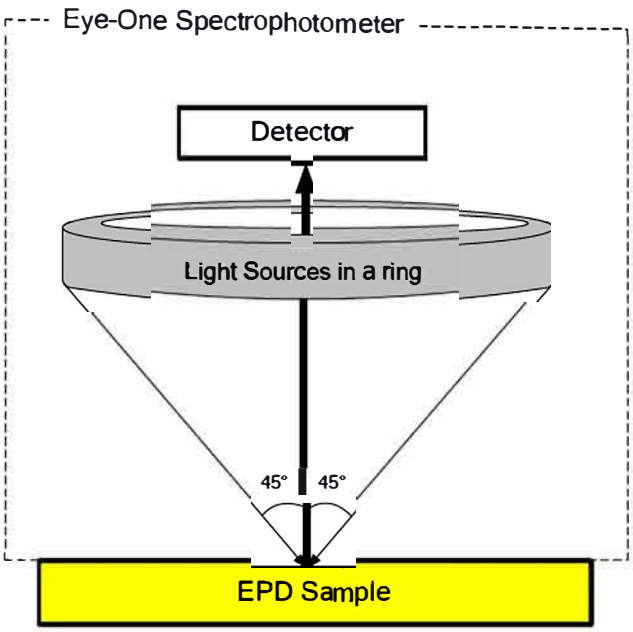
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	Unit
R	Reflectance	White		41		%
CR	Contrast Ratio		9	12		
T_{update}	Update time			30		sec
SYMBOL	Color coordinates		L*_TYP	a*_TYP	b*_TYP	dE2000_Max
DS	Dark state		17.6	8.3	-8.9	7
WS	White state		70.6	-0.4	2.4	4
BS	Blue state		28.0	9.2	-25.0	7
GS	Green state		38.3	-26.0	13.4	7
RS	Red state		37.6	35.9	17.4	5
YS	Yellow state		65.5	-6.7	46.4	4
OS	Orange state		44.4	30.0	24.9	7

*Color performance measured with Konica Minolta CM-25cG
*Image Transition: White → Black →White →Picture

8-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in x

CR = Rl/Rd



8-3) Reflection Ratio

The reflection ratio is expressed as：

R = Reflectance $Factor_{white\ board}$ x (L_{center} / $L_{white\ board}$)

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{white\ board}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. Handling, Safety and Environmental Requirements and Remark

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	This data sheet contains final product specifications.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Long Term Storage

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.

REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

10. Reliability Test

	TEST	CONDITION	REMARK
1	High Temperature Storage	Ta= 60°C 40% RH, 240hrs	(Test in White Pattern)
2	Low Temperature Storage	Ta= -25°C, 240hrs	(Test in White Pattern)
3	High Temperature Operation	Ta= 35°C 35% RH, 240hrs	
4	Low Temperature Operation	Ta= 15°C 35% RH, , 240hrs	
5	High Temperature, High Humidity Operation test	Ta= 35°C 80% RH, 240hrs	
6	High Temperature, High Humidity Storage test	Ta= 50°C 80% RH, 240hrs	(Test in White Pattern)
7	Thermal cycles	-25°C(30min) ~60°C (30min), 50 cycle, 1hr/cycle	(Test in White Pattern)
8	Electrostatic Discharge	(Machine model) +/- 200V 0Ω , 200pF	Non-operation

Actual EMC level to be measured on customer application.
Note：The protective film must be removed before temperature test.

< Criteria >

In the standard conditions, there is not display function NG issue occurred.
All the cosmetic specification is judged before the reliability stress.

11. Block Diagram