Charles Hong

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Education

University of California, Berkeley 2021 – Present
Ph.D., Electrical Engineering and Computer Science *Berkeley, CA*
M.S., Electrical Engineering and Computer Science

University of California, Berkeley 2017 – 2021
B.S., Electrical Engineering and Computer Science *Berkeley, CA*

Publications

Learning A Continuous and Reconstructible Latent Space for Hardware Accelerator Design
Qijing Huang, Charles Hong, John Wawrzynek, Mahesh Subedar, Yakun Sophia Shao
International Symposium on Performance Analysis of Systems and Software (ISPASS), May 2022

Honors

Master's Scholarship in Integrated Systems – University of California, Berkeley | Apple 2021
High Honors at Graduation – University of California, Berkeley 2021
EECS 151 Design Award – University of California, Berkeley | Apple 2019
Eta Kappa Nu Honor Society – IEEE 2018

Experience

University of California, Berkeley June 2020 – Present
Undergraduate/Graduate Student Researcher *Berkeley, CA*

- Researcher at ADEPT and SLICE computer architecture labs, advised by Professor Sophia Shao
- Areas of focus include deep learning accelerators, hardware/software co-design, and ML for systems (see publications and projects for details)

University of California, Berkeley August 2018 – Present
Undergraduate/Graduate Student Instructor *Berkeley, CA*

- Six-time (U)GSI for CS 61A (programming fundamentals), CS 61C (computer architecture), and EECS 151 (digital design, FPGAs)

Intel Labs May 2022 - December 2022
Research Intern *Hillsboro, OR*

- Investigating methods for ML/DL-based accelerator design space exploration

Apple May 2021 – August 2021
Hardware Technology Intern *Cupertino, CA*

- Developed CPU Emulation Flow 2.0, which enhances support for internal emulation users, increases test throughput, and reduces runtime of common queries

NVIDIA May 2020 – August 2020
System Architect Intern *Santa Clara, CA*

- Applied machine learning to CPU networking workload analysis, predicting costs to within 15% accuracy

NVIDIA May 2019 – August 2019
System Architect Intern *Santa Clara, CA*

- Modeled power data of SoC use cases based on task scheduling and per-IP workload parameters
- Still in use as of following internship

Oski Technology June 2018 – August 2018
Formal Verification Intern *San Jose, CA*

- Verified an interconnect bridge design and prototyped Chisel FV flow

Projects

Modeling DNN Layer Performance Across Accelerators (Paper) (Poster) 2021

- Compares accuracy and interpretability of learned models for layer schedule performance
- Presented at *ACM Student Research Competition, MICRO 2021*

Fast Thread Migration in a Heterogeneous ISA System (Paper) (Poster) 2021

- Devises a mechanism for automatic firmware-level migration of programs to appropriate heterogeneous core

Enhancing Yelp Rating Predictions (Paper) 2021

- Applies novel ensembling and multi-head approaches to improve the classification accuracy of BERT

Monte Carlo Tree Search for Query Optimization 2020

- Implements database join order optimization using Monte Carlo tree search and reinforcement learning

A Chipyard Comparison of NVDLA and Gemmini (Paper) 2020

- Integrates NVDLA into RISC-V SoC environment and compares its performance to Gemmini's

Technical Skills

Languages: Python, C/C++, RISC-V, Verilog, Chisel, Java, Golang, HTML/CSS, JavaScript, SQL
Developer Tools: Git, Perforce, SVN
Python/ML Libraries: PyTorch, TensorFlow/Keras, NumPy, Pandas, Matplotlib, Hugging Face, W&B
Parallel Programming Libraries: CUDA, OpenMP/MPI
CAD Tools: Vivado, Quartus, JasperGold

Volunteering

Pioneers in Engineering September 2017 – Present
Advisor, Director of Engineering, Project Manager, Software Developer *Berkeley, CA*

- Various roles helping run robotics competition for local underserved high schools
- Two years as project manager; one year as engineering director, managing 30+
- Lead developer of robot simulator web app (pimulator.pierobotics.org)