Charles Hong

charleshong@berkeley.edu | charleshong3.github.io | linkedin.com/in/charleshong3

Education

University of California, Berkeley 2021 – Present
Ph.D., Electrical Engineering and Computer Science *Berkeley, CA*
M.S., Electrical Engineering and Computer Science

University of California, Berkeley 2017 – 2021
B.S., Electrical Engineering and Computer Science *Berkeley, CA*

Honors/Awards

Master's Scholarship in Integrated Systems – University of California, Berkeley | Apple 2021

High Honors at Graduation – University of California, Berkeley 2021

Eta Kappa Nu Honor Society – IEEE 2018

Conference Publications

DOSA: Differentiable Model-Based One-Loop Search for DNN Accelerators (Paper)
Charles Hong, Qijing Huang, Grace Dinh, Mahesh Subedar, Yakun Sophia Shao
56th IEEE/ACM International Symposium on Microarchitecture (MICRO), October 2023

Learning A Continuous and Reconstructible Latent Space for Hardware Accelerator Design (Paper) (Slides)
Qijing Huang, Charles Hong, John Wawrzynek, Mahesh Subedar, Yakun Sophia Shao
International Symposium on Performance Analysis of Systems and Software (ISPASS), May 2022

Workshop Publications

Sample-Efficient Mapspace Optimization for DNN Accelerators with Bayesian Learning (Paper)
Grace Dinh, Iniyaal Kannan Jegadesan Valsala, Hengrui Luo, Charles Hong, Younghyun Cho, James Demmel, Sherry Li, Yang Liu
ML for Computer Architecture and Systems Workshop (MLArchSys), co-located with ISCA, June 2023

Modeling DNN Layer Performance Across Accelerators (Poster)
Charles Hong, Yakun Sophia Shao
MICRO ACM Student Research Competition, October 2021

Experience

University of California, Berkeley June 2020 – Present
Undergraduate/Graduate Student Researcher *Berkeley, CA*

- Researcher at ADEPT and SLICE computer architecture labs, advised by Professor Sophia Shao.
- Areas of focus include deep learning accelerators, hardware/software co-design, and ML for systems (see publications and projects for details).

University of California, Berkeley August 2018 – August 2023
Undergraduate/Graduate Student Instructor *Berkeley, CA*

- Six-time (U)GSI for CS 61A (programming fundamentals), CS 61C (computer architecture), and EECS 151 (digital design, FPGAs).
- Lecturer for CS 61C in Summer 2023.

Intel Labs May 2022 - December 2022
AI Research Intern *Remote*

- Developed methods for ML/DL-based optimization of deep learning accelerator hardware and software.
- Progress towards Intel FPGA-based platform for SoC evaluation.

Apple May 2021 – August 2021
Hardware Technology Intern *Cupertino, CA*

- Intern in CPU DV. Developed CPU Emulation Flow 2.0, which enhances support for internal emulation users, increases test throughput, and reduces runtime of common tasks.

NVIDIA May 2020 – August 2020
System Architect Intern *Santa Clara, CA*

- Applied machine learning to CPU networking workload analysis, predicting costs to within 15% accuracy.

NVIDIA May 2019 – August 2019
System Architect Intern *Santa Clara, CA*

- Built tool to model power data of SoC use cases based on task scheduling and per-IP workload parameters.
- Enabled estimation of power variation over time and sped up evaluation by several times.

Oski Technology June 2018 – August 2018
Formal Verification Intern *San Jose, CA*

- Verified an interconnect bridge design and prototyped Chisel FV flow.

Projects

Fast Thread Migration in a Heterogeneous ISA System (Paper) (Poster) 2021

- Devises a mechanism for automatic firmware-level migration of programs to appropriate heterogeneous core.

Enhancing Yelp Rating Predictions (Paper) 2021

- Applies novel ensembling and multi-head approaches to improve the classification accuracy of BERT.

A Chipyard Comparison of NVDLA and Gemmini (Paper) 2020

- Integrates NVDLA into Chipyard RISC-V SoC environment and compares its performance to Gemmini's.

Technical Skills

Languages: Python, Java, C/C++, Golang, RISC-V, Verilog, HTML/CSS, JavaScript, SQL
Developer Tools: Git, Perforce, SVN
Python/ML Libraries: PyTorch, TensorFlow/Keras, NumPy, Pandas, Matplotlib, W&B
Parallel Programming Libraries: CUDA, OpenMP, MPI
CAD Tools: Vivado, Quartus, JasperGold

Volunteering

Pioneers in Engineering September 2017 – Present
Advisor, Director of Engineering, Project Manager, Software Developer *Berkeley, CA*

- Various roles helping run robotics competition for local underserved high schools.
- Two years as project manager; one year as engineering director, managing 30+.
- Developed robot simulator web app (pimulator.pierobotics.org).