

Charles Hong

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EDUCATION

University of California, Berkeley <i>Ph.D., Electrical Engineering and Computer Science</i>	Ongoing
University of California, Berkeley <i>M.S., Electrical Engineering and Computer Science</i>	2025
University of California, Berkeley <i>B.S., Electrical Engineering and Computer Science</i>	2021

HONORS/AWARDS

Master's Scholarship in Integrated Systems – Apple	2021
High Honors at Graduation – University of California, Berkeley	2021
Eta Kappa Nu Honor Society – IEEE	2018
Edward Kraft Award for Freshmen – University of California, Berkeley	2017

CONFERENCE PUBLICATIONS

DOSA: Differentiable Model-Based One-Loop Search for DNN Accelerators (Paper) (Slides) (GitHub) Charles Hong, Qijing Huang, Grace Dinh, Mahesh Subedar, Yakun Sophia Shao <i>56th IEEE/ACM International Symposium on Microarchitecture (MICRO), October 2023</i>
Learning A Continuous and Reconstructible Latent Space for Hardware Accelerator Design (Paper) (Slides) (GitHub) Qijing Huang, Charles Hong, John Wawrzynek, Mahesh Subedar, Yakun Sophia Shao <i>International Symposium on Performance Analysis of Systems and Software (ISPASS), May 2022</i>

PREPRINTS

hdl2v: A Code Translation Dataset for Enhanced LLM Verilog Generation (Paper) Charles Hong, Brendan Roberts, Huijia An, Alex Um, Advay Ratan, Yakun Sophia Shao <i>arXiv, June 2025</i>
Autocomp: LLM-Driven Code Optimization for Tensor Accelerators (Paper) (GitHub) Charles Hong, Sahil Bhatia, Alvin Cheung, Yakun Sophia Shao <i>arXiv, May 2025</i>
Polaris: Multi-Fidelity Design Space Exploration of Deep Learning Accelerators (Paper) Chirag Sakhuja, Charles Hong , Calvin Lin <i>arXiv, December 2024</i>

WORKSHOPS AND RESEARCH COMPETITIONS

LLM-Aided Compilation for Tensor Accelerators (Paper) Charles Hong, Sahil Bhatia, Altan Haan, Shengjun Kris Dong, Dima Nikiforov, Alvin Cheung, Yakun Sophia Shao <i>The First IEEE International Workshop on LLM-Aided Design (LAD'24), June 2024</i>
Sample-Efficient Mapspace Optimization for DNN Accelerators with Bayesian Learning (Paper) Grace Dinh, Iniyaal Kannan, Hengrui Luo, Charles Hong, Younghyun Cho, James Demmel, Sherry Li, Yang Liu <i>ML for Computer Architecture and Systems Workshop (MLArchSys), co-located with ISCA, June 2023</i>
Modeling DNN Layer Performance Across Accelerators (Poster) Charles Hong, Yakun Sophia Shao <i>MICRO ACM Student Research Competition, October 2021</i>

EXPERIENCE

University of California, Berkeley

June 2020 – Present

Undergraduate/Graduate Student Researcher

Berkeley, CA

- Researcher at ADEPT and SLICE computer architecture labs, advised by Professor Sophia Shao.
- Areas of focus include deep learning accelerators, hardware/software co-design, and ML for systems (see publications and projects for details).

Siemens EDA

May 2024 - August 2024

HLS Intern

Wilsonville, OR

- Improved tool flow for Catapult HLS-generated machine learning acceleration and demonstrated results via FPGA prototype-based demo.

University of California, Berkeley

August 2018 – August 2023

Undergraduate/Graduate Student Instructor

Berkeley, CA

- Six-time (U)GSI for CS 61A (programming fundamentals), CS 61C (computer architecture), and EECS 151 (digital design, FPGAs).
- Lecturer for CS 61C in Summer 2023.

Intel Labs

May 2022 - December 2022

AI Research Intern

Remote

- Developed methods for ML/DL-based optimization of deep learning accelerator hardware and software.
- Prototyped an Intel FPGA-based platform for SoC evaluation.

Apple

May 2021 – August 2021

Hardware Technology Intern

Cupertino, CA

- Intern in CPU DV. Developed CPU Emulation Flow 2.0, which enhances support for internal emulation users, increases test throughput, and reduces runtime of common tasks.

NVIDIA

May 2020 – August 2020

System Architect Intern

Santa Clara, CA

- Profiled CPU networking workloads and built a machine learning-based cost model, predicting cycle counts to within 15% accuracy.

NVIDIA

May 2019 – August 2019

System Architect Intern

Santa Clara, CA

- Built tool to model power data of SoC workloads based on hardware configuration and task scheduling across various IPs.
- Enabled estimation of power variation over time and sped up evaluation by several times.

Oski Technology

June 2018 – August 2018

Formal Verification Intern

San Jose, CA

- Verified an interconnect bridge design and prototyped Chisel FV flow.

OTHER PROJECTS

Fast Thread Migration in a Heterogeneous ISA System ([Paper](#)) ([Poster](#))

2021

Enhancing Yelp Rating Predictions ([Paper](#))

2021

Monte Carlo Tree Search for Query Optimization

2020

A Chippyard Comparison of NVDLA and Gemmini ([Paper](#))

2020

TECHNICAL SKILLS

Software Engineering: Experienced in building large software projects in Python, Java, and C/C++. Familiar with web programming in HTML/CSS/JavaScript.

Hardware and Systems Engineering: Expert in computer architecture, especially domain-specific architectures for machine learning. Experienced in hardware design in Verilog/SystemVerilog and low-level programming in RISC-V assembly.

Machine Learning/Data Science: Experienced in model training at all levels, from sklearn to PyTorch to HuggingFace Transformers (including LLM fine-tuning). Highly experienced in data analysis and visualization with NumPy, Pandas, Matplotlib.

EDA Tools: Significant FPGA prototyping experience with both Xilinx Vivado and Altera Quartus. Familiar with Cadence Joules for RTL-level power estimation.

Formal Methods: Familiar with Rosette and Z3 for program synthesis and verification, as well as JasperGold for RTL FV.

VOLUNTEERING

Pioneers in Engineering

Advisor, Director of Engineering, Project Manager, Software Developer

September 2017 – Present

Berkeley, CA

- Various roles helping run robotics competition for local underserved high schools.
- Two years as project manager; one year as engineering director, managing 30+.
- Developed robot simulator web app (pimulator.pierobotics.org).