Charles Babu M

Curriculum Vitae

Research Interests

· To design techniques and build tools to formally verify software systems
· Formal methods and machine learning
· Static analysis and abstract interpretation

Education

2020–2024 **Ph.D. in Computer Science**, *Atomic Energy Commission (CEA Paris-Saclay)*.

2015–2017 **M.Sc. in Theoretical Computer Science**, *Chennai Mathematical Institute (CMI)*.

2010–2014 **B.Tech. in Computer Science and Engineering**, *Rajiv Gandhi University of Knowledge Technologies, Nuzvid (RGUIIIT)*.

Graduate Courses

Mathematical Logic, Graduate Logic, Proofs and Types, Concurrency theory, Model-checking and Systems Verification, Software Verification using SMT Solvers, Logic Automata and Games, Topics in Verification.

Master's Thesis

Title *Improving Precision of Loop Acceleration for C Programs*

Supervisor Prof. Mandayam Srivas (CMI)

Abstract The transitive closure of Flat Linear Counter Systems with finite monoid transformations is Presburger definable. We develop techniques to verify this subclass of counter systems using SMT solvers. We implement our technique in Veriabs, a portfolio software verifier, improving the precision of the tool.

Research Experiences

Aug'18 – present **Chennai Mathematical Institute.** Research assistant.

Project: 2LS: Disjunctive Invariant Synthesis using Max-Strategy Iteration.

Max-strategy iteration (Max-SI) accelerate fixpoint computation without a need for widening operators on template linear constraint domains. We develop techniques to synthesize disjunctive invariants using Max-SI and classical completeness properties of abstract interpretation. We implement our techniques in 2LS tool.

Supervised by Prof. Mandayam Srivas, Peter Schrammel (Diffblue, Oxford).

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Aug'17 – Jul'18 **Chennai Mathematical Institute & Tata Research Design and Development Center** Research assistant.

Project: Acceleration in Symbolic Model-Checking

We develop exact acceleration and abstract acceleration techniques for linear counter systems. We implement our techniques in Veriabs, to improve the precision of the tool.
(Gold in ReachSafety Category in both SV-Comp 2019, 2020)

Supervised by Prof. Mandayam Srivas, Prof. Praveen M (CMI)

May'16 – Aug'16 **Tata Research Development and Design Center.** Summer Intern.

Project: Improving Precision of Abstract Loop Acceleration for C Programs.

Achievements

2015 **Cleared CMI national entrance exam to pursue master's in theoretical computer science**.

2017-2020 **Recipient of TCS-Research scholarship**.

Computer Skills

PL	Java, C++, Python, Haskell	Type Setting	LaTeX, Microsoft Office
Familiar With	Racket, Ocaml	OS	Linux, Unix, Microsoft Windows
IDE	Vim, Eclipse, Visual Studio	Database	MySQL

Summer Schools and Relevant Talks

Jul 1-5, 2019 **UniGR Summer School on Verification Technology, Systems & Applications, VTSA 2019**, *University of Luxembourg, Luxembourg*.

Jul 7-11, 2019 **International Conference on Theory and Applications of Satisfiability Testing, SAT 2019**, *University of Lisbon*.

Dec 6-8, 2017 **The Second Indian SAT+SMT School - Infosys Mysore**, *Improving Precision of Loop Acceleration for C Programs*, Student talk.

2017 **Tata Research Development and Design Center**, *Improving Precision of Loop Acceleration for C Programs*, Research talk.

Dec 11-15, 2016 **36th IARCS Annual Conference on Foundations of Software Technology and Theoretical Computer Science**, *Chennai Mathematical Institute, India*.

Publications

1. VeriAbs: Verification by Abstraction and Test Generation.

TACAS-2020 M Afzal, Avriti Chauhan, Supratik Chakraborty, B Chimdyalwar, P Darke, Ashutosh Gupta, S Kumar, Charles B M, D Unadkat, and Venkatesh R (**Tool paper**)

2. VeriAbs: Verification by Abstraction and Test Generation.

ASV-2020 Accepted R. Venkatesh, Priyanka Darke, B Chimdyalwar, Shrawan Kumar, Avriti Chauhan, Advaita Datar, M Afzal, A. Asia, D Unadkat, Charles Babu M, Supratik Chakraborty, Ashutosh Gupta (**Book Chapter**)

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