Charles Liu

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Objective: **Master's Degree in Data Science and Information Technology**

EDUCATION

Aug. 2014 – Jul. 2018	**Major in Electronic Engineering in Tsinghua University**
	● **Theoretical Basis:**
	Digital Image Processing, Statistical Signal Processing, Media and Cognition, Stochastic Process(91/100), Database (96/100), MATLAB Application(97/100), Internet Techniques(98/100)
	● **Scholarship:**
	• National Encouragement Scholarship
	• Scholarship for Academic Progress
	• Outstanding Volunteer Scholarship
Aug. 2016 – Jul. 2018	**Minor in Statistics in Tsinghua University**
	● **Theoretical Basis:**
	Probability Theory, Machine Learning & Data Mining, Statistical Inference, Applied Linear Regression, Multivariate Statistics

SKILLS & CERTIFICATES

Programming	C++, R, MATLAB, Python, SQL, Verilog, Git
English	CET-6: 556 CET-6: 604 TEPT: 96.75/120

RESEARCH EXPERIENCES

Mar. 2017 – present	**Mobile Big Data Mining based on Deep Learning** **Python**
	● Build an Spatial-Temporary RNN model based on Tensorflow platform to process the trajectory data from both time and space dimension, trying to find the pattern of users' behavior and predict where the users would be in the future.
Mar. 2017 – May 2017	**Continuous Speech Recognition** **Python**
	● The project is mainly based on Kaldi. The monophone and triphone models are trained by thsch30 dataset. After the models trained, a concise and friendly GUI is developed using PyQt. It can be used both online and offline.
Jan. 2017 – Feb. 2017	**Data Analysis and Exploration of Bay Area Shared Bicycle** **R**
	● Use Machine Learning algorithms, including linear regression and LASSO regression, to analyze the data, and reveal the hidden patterns. Besides, a shiny app was designed using R Shiny.
Jun. 2016 – Aug. 2016	**Speech Synthesis and Image Processing** **MATLAB**
	● Analyze speech signals, make linear predication. Implement JPEG algorithm, compared the results of information hiding in both spatial and DCT domain. Face detection based on RGB color histogram model.
Jun. 2016 – Jul. 2016	**MIPS CPU Design and Implementation** **Verilog**
	● Participate in the design and implementation of a single-cycle CPU, along with the pipeline and UART. The software includes Modelsim for simulation and Vivado for synthesis.