本文介绍IR压降分析的基础，解释同集成电路封装和印刷电路板相关的IR压降的意义，并展示典型的IR压降模拟，以帮助确定有问题的配电。根据欧姆定律，IR压降为同电阻（R）和电流（I）相关的压降。IR压降分析对于大型复杂电路板特别重要，这些电路板常常要求配电系统横穿数英尺的层板和迹线，才能到达远端装置。因此，远端装置承受的压降常常比靠近稳压器模块的装置大。

IR DROP in High-Speed IC Packages and PCBs

Neckdowns, low-weight copper and Swiss cheese effects are conspiring to wreak havoc on your high-speed design. Get the drop on them. **by SAM CHITWOOD and JI ZHENG**

Today's low-voltage, high-current designs require DC IR drop analysis for off-chip power distribution systems in order to optimize end-to-end voltage margins for every device on the distribution. This article will introduce the basics of IR drop analysis, exemplify the significance of IR drop associated with IC packages and PCBs, and demonstrate typical IR drop simulations for the identification of problematic power distributions.

As system complexity and operational speeds increase, the power consumption of integrated circuits increases dramatically. Additionally, the IC supply voltage continues to drop with the inevitable scaling of VLSI technology. With the switch to 90 nm technologies from 130 nm technology, supply voltages have shrunk to 1.2 V and below. According to the International Technology Roadmap for Semiconductors,[1] this trend is expected to continue. See **FIGURE 1**.

Reducing the nominal supply voltage is accompanied by a reduction in device noise margins, making components more vulnerable to power supply noise. This noise consists of the dynamic AC voltage fluctuation due to the frequency-dependent distributed parasitics inherent in today's power distribution systems, and the DC voltage drop (i.e., "IR" drop, according to Ohm's Law V=I*R, where R is the equivalent path DC resistance between the source location and the device location and I is the average current the chip draws from the supply).

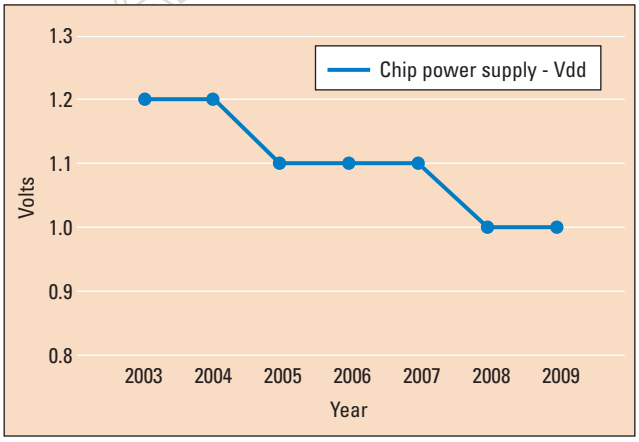

FIGURE 1. ITRS projects the core IC supply voltages by year.

IR Drop Basics

As illustrated in **FIGURE 2**, Ohm's Law relates conduction current to voltage drop, and at DC, the relation coefficient is a constant representing the resistance of the conductor. Conductors also dissipate power due to their resistance. Both voltage drop and power dissipation are proportional to the resistance of the conductor.

Resistance is determined by a metal's conductivity and the path geometry of the conduction current. Conductivity (σ) is the measure of a metal's capability to conduct current and is an intrinsic property of the material. The most common metal used in IC packages and PCBs is copper, whose conductivity is approximately 5.8 X 10^7 siemens per meter.

DC resistance can be found analytically for conductors of simple geometries, such as the metal bar of uniform cross-section shown in **FIGURE 3**. The sheet resistance concept is introduced in **FIGURE 4** as plane structures are widely used in IC package and PCB power distribution systems. Finally, the closed formula for plane resistance between two via contacts is given in **FIGURE 5**.

Various kinds of metal structures including planes, vias and traces constitute the power distribution system between the supply source and one or more IC components. The supply source is typically implemented as a DC-DC converter and referred to as a voltage regulator module (VRM).

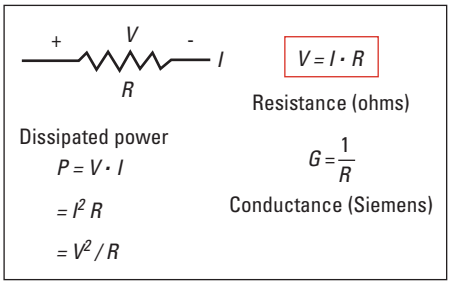

FIGURE 2. Ohm's Law and power dissipation equations are shown.

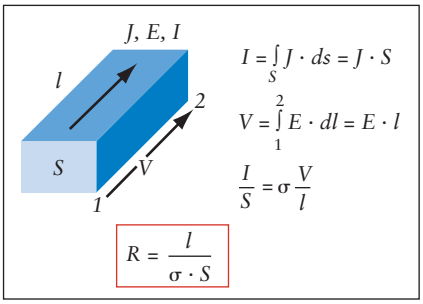

FIGURE 3. Example details the resistance of a metal bar of uniform cross-section.

The resistance Rs of a plane conductor for a unit length and unit width is called the **surface resistivity** (ohms per square).

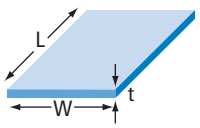

FIGURE 4. The basics of sheet resistance are useful when determining IR drop for IC package and PCB structures that contain planes.

Assuming the current requirements are met, the IR drop is determined by the effective path resistance between the VRM and the IC components. In a microelectronic system, the system's IR drop may be budgeted into three portions: on-chip, package and board.

On-chip IR drop has been extensively studied because the resistive loss is severe due to the fine feature-size (a few microns and below) of the on-die power grid. On the other hand, package and board-level IR drop have not been given much attention due to their much smaller contribution to the overall path resistance and hence voltage drop. However, due to increased current requirements and reduced supply voltage noise margins, package and board IR drop (in the range of tens to hundreds of millivolts) now can have a significant impact on the operation of high-speed devices.

Several factors contribute to increased off-chip path resistances. In multilayer IC packages such as BGAs, for example, the power distribution usually traverses multiple layers from the balls to the controlled collapse chip connect (C4) bumps, as shown in **FIGURE 6**. These paths are much shorter than those on the board; however, package power and ground planes usually require much more irregular shapes to accommodate the chip I/O breakout and usually are not allowed to fill an entire plane. Many packages also contain a number of power domains, but a very limited number of layers are available for their distribution. Therefore, it is very common for power distributions to contain complex shapes such as neckdowns (small copper widths for short lengths) and other non-ideal routing.

Printed circuit boards have their own share of issues as well. In large, complex PCBs the power distribution system may have to traverse several feet of planes and traces to reach the far-end devices. Therefore, far-end devices will see a larger voltage drop compared to devices closer to the VRM. The ICs themselves also contribute to the board designers' problems. Higher-density, high-pin-count components have large via fields and their associated anti-pads create a "Swiss cheese" effect in the power distribution layers of both IC packages and PCBs. See **FIGURE 7** and **FIGURE 8**. This Swiss cheese effectively creates a smaller equivalent conductor of higher resistance. Finally, the situation has been further exacerbated by material suppliers who have reduced their copper weights (thickness) to the IPC standard minimums.

Because of the long distribution paths, neckdowns, low weight copper, and Swiss cheese effects, it is possible for designs to deliver insufficient voltage to some devices. Therefore, for high-current and low-voltage designs, it is becoming critically important to include package and board IR drop into the total noise budget of the system.

IR Drop Simulation

Unfortunately, calculating the IR drop of modern power distributions is a formidable task. The amount of information required is not overwhelming, but the complexity of the distribution's geometry is daunting. To accu-

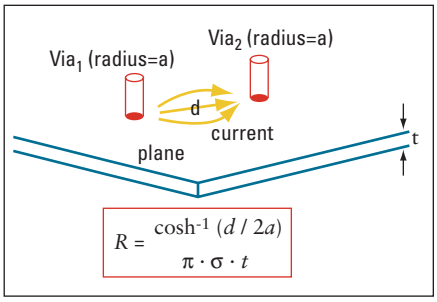

FIGURE 5. Plane resistance is depicted between two via contacts.

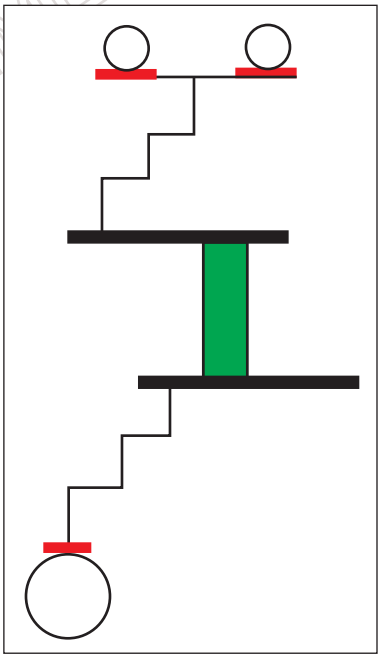

FIGURE 6. This cross-section shows a view of BGA package power distribution from bumps to balls.

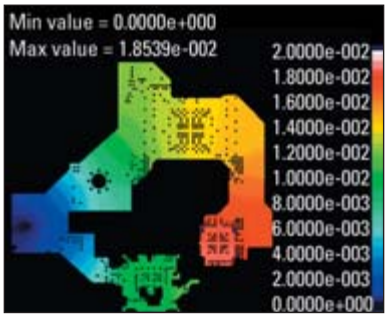

FIGURE 7. IR drop (in volts) is depicted for a typical PCB distribution.

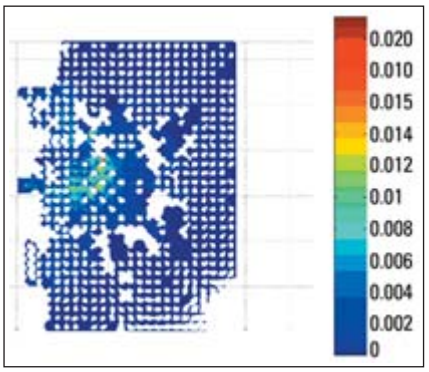

FIGURE 8. Current distribution is shown in a typical IC package layer.

rately analyze package and board IR drop, the actual geometry of the distribution must be properly modeled and simulated.

Let us investigate the single-layer distribution example shown in **FIGURE 7**. Three large ASICs draw current from this rail; two devices are on the upper portion of the distribution and the third device is on the bottom. The VRM is located on the left side of the board. In addition to the layout, the device currents, the stackup and the metal's conductivity must be known.

Figure 7 shows the IR drop at every location along the distribution. The results indicate that the ASIC farthest from the VRM will see 18.5 mV of IR drop, while the other ASICs have drops of 11 mV and 14 mV. If the nominal voltage of this rail is 3.3 V, the IR drop is 0.5% of nominal. However, if the rail's nominal is 1.2 V, the IR drop is 1.5% of nominal. For systems with noise budgets of +/- 5%, IR drop must be allocated 30% of this budget, leaving only 70% for AC noise.

IR drop is not the only DC property of interest. Current produces a heating effect in the planes and for some package designs, it must be accounted for in the system's thermal budget. If too much current passes through a small path, a potential hot spot can develop. Neighboring planes may act as heatsinks, but Swiss cheese limits this effect as well. The effects of hot spots can range from insignificant to melted dielectrics.

In addition to IR drop, simulation calculates the current distribution on the planes as well (see **FIGURE 8**). These distributions quickly identify potential hot spots and the results can be imported by system-level thermal analysis tools.

DC analysis for off-chip power distribution systems is becoming mandatory for high-current, low-voltage designs. Simulation allows adjustment of VRM nominals, strategic placement of sense lines and early identification of problematic distributions. Budgeting for AC noise and system-level IR drop will optimize the voltage margins for every device on the distribution. **PCD&M**

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REFERENCES

1. International Technology Roadmap for Semiconductors Web site: http://public.itrs.net.