μPD71611

CMOS Clock Generator

Preliminary Information

September 1986

Description

The μPD71611 is a high performance CMOS clock generator/driver for the μPD70616 (V60) microprocessor. The μPD71611 contains a crystal oscillator for use with a fundamental mode crystal. An external clock source can also be used if it is necessary to synchronize the μPD70616 to an external clock.

Reset logic with a Schmitt-trigger input is also included to synchronize a power-on reset signal to the system clock and be used as a system-wide reset signal. The μPD71611 also contains wait state logic for generation of 0 to 7 wait states in any bus cycle.

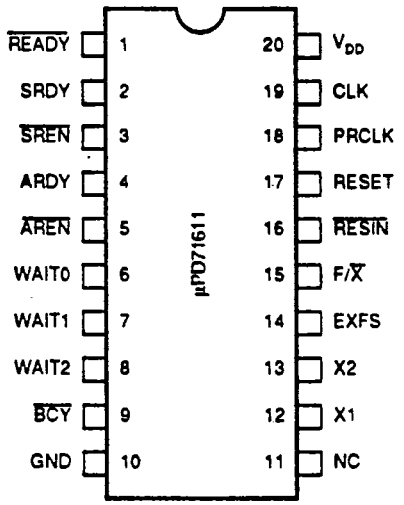
Features

- μPD70616 system clock generator/driver
- 16 MHz system clock (32MHz input divided by two)
- Programmable wait state generator
- Schmitt-trigger reset logic
- Low power CMOS technology
- 20-pin plastic DIP

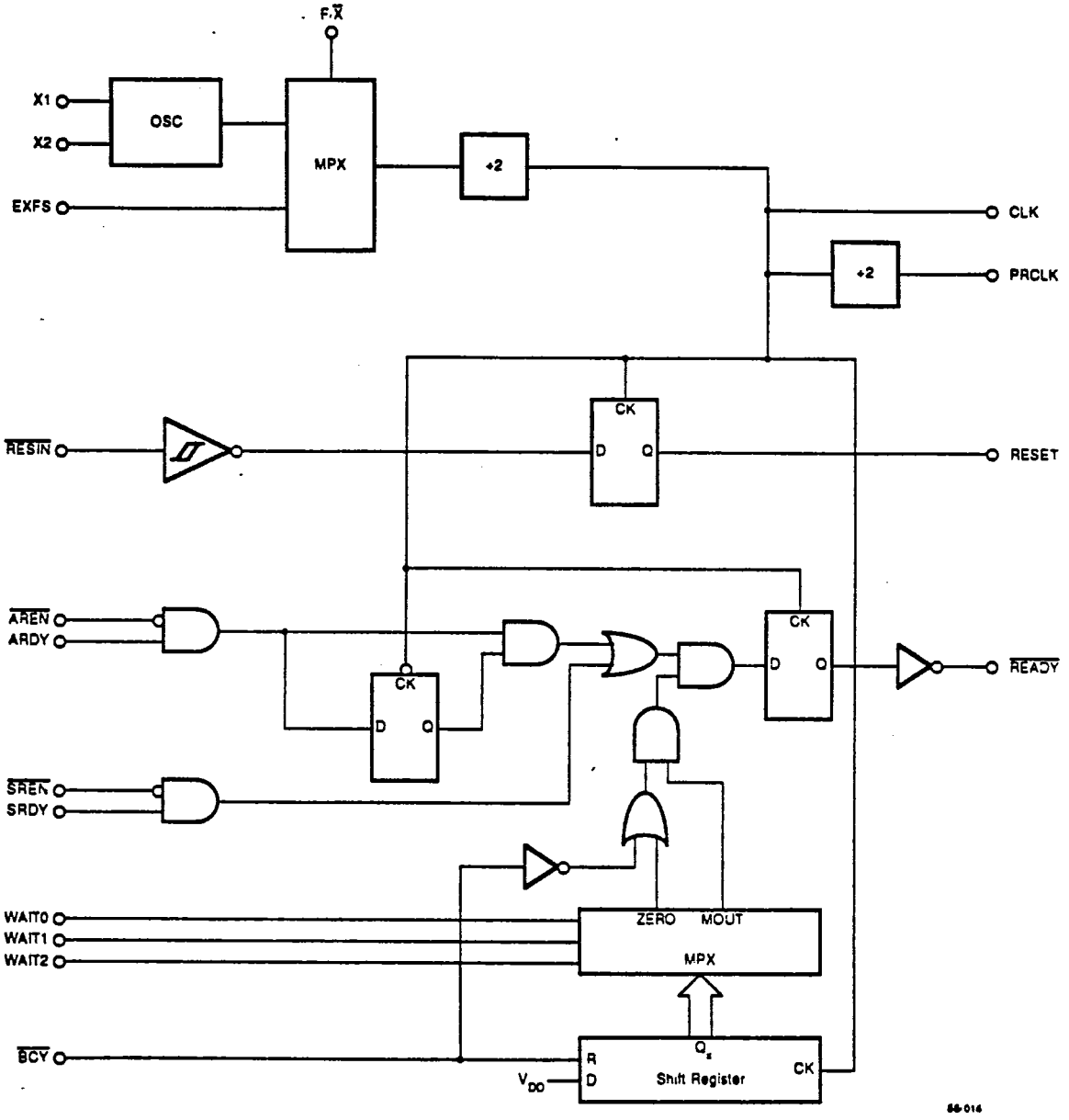
Ordering Information

Part Number	Package	Maximum Frequency
μPD71611C	20-pin plastic DIP	16 MHz

Pin Configuration



Block Diagram



Pin Identification

Symbol		I/O	Function
X1, X2	Crystal Inputs	I/O	I/O terminals for crystal, twice the μPD70616 frequency
EXFS	External Clock Source	In	External clock input pin, twice the μPD70616 frequency
F/X*	Frequency/Crystal Select	In	Clock source multiplexer control
CLK	Clock	Out	μPD70616 system clock, 1/2 the input clock frequency
PRCLK	Peripheral Clock	Out	Peripheral clock, 1/4 the input clock frequency
RESIN*	Reset Input	In	Schmitt trigger reset input
RESET	Reset Out	Out	μPD70616 and system reset output
ARDY	Asynchronous Ready	In	Asynchronous ready input
AREN*	Asynchronous Ready Enable	In	Enable input for ARDY
SRDY	Synchronous Ready	In	Synchronous ready input
SREN*	Synchronous Ready Enable	In	Enable input for SRDY
BCY*	Bus Cycle	In	μPD70616 bus cycle output
WAIT0 WAIT1 WAIT2	Wait State Controls	In	Wait state inputs to add 0 to 7 wait states to a bus cycle
READY*	Ready	Out	Ready output to the μPD70616

Pin Functions

This section describes the operation of the μPD71611 I/O terminals. Inputs and outputs are considered at a logic "0" level when a low level signal is present. Likewise, a logic "1" is represented by a high level signal. Bus states are defined and measured from the rising edge of the clock to the rising edge of the next clock.

X1, X2 [Crystal Inputs] ..... inputs/outputs
The X1 and X2 inputs are used to connect a fundamental mode crystal to the internal oscillator circuitry. The crystal is selected to oscillate at a frequency twice the μPD70616 operating frequency.

EXFS [External Frequency Source] ..... input
The EXFS pin allows an external TTL-level clock source twice the desired operating frequency to be used as the input clock.

F/X* [Frequency/Crystal Select] ..... input
The F/X* input selects either the internal crystal oscillator or an external clock oscillator as the clock source for the μPD70616 and other devices.

CLK [Clock] ..... output
CLK is the μPD70616 processor clock output. The CLK output has additional drive capabilities matched to the requirements of the μPD70616 and associated microprocessors.

PRCLK [Peripheral Clock] ..... output
CLK is the μPD70616 system clock output available for use by peripheral devices.

RESIN* [Reset Input] ..... input
RESIN* is a Schmitt-trigger input used to synchronize the asynchronous reset input to the rising edge of the processor clock before use by the rest of the system.

RESET [Reset Output] ..... output
RESET is an active high synchronized reset signal for the μPD70616 and peripheral devices.

ARDY [Asynchronous Ready Input] ..... input
The ARDY input is used by ready signals which are not synchronized to the μPD70616 clock. This input is internally applied to a synchronizer before being used as a ready output to the processor.

AREN* [Asynchronous Ready Enable] ..... input
AREN* is an enable for the ARDY input. If ARDY is not used in a system, AREN* can be pulled up to the positive power supply to disable the asynchronous ready logic.

SRDY [Synchronous Ready Input] ..... input
The SRDY input is used by ready signals which are synchronized to the μPD70616 clock.

SREN* [Synchronous Ready Enable] ..... input
SREN* is an enable for the SRDY input. If SRDY is not used in a system, SREN* can be pulled up to the positive power supply to disable the synchronous ready logic.

BCY* [Bus Cycle] ..... input
The μPD70616 indicates the start of a new bus cycle by asserting the BCY* output. The μPD71611 uses BCY* to control the operation of the wait state logic.

WAIT2–0 [Wait State Mode Inputs] ..... inputs
The WAIT2–0 inputs are decoded to determine the number of wait states the μPD71611 should automatically insert into the bus cycle. These inputs can be dynamically changed on a bus cycle basis to insert from 0 to 7 seven wait states into a bus cycle.

READY* [Ready Output] ..... output
READY* is an active low output used by slow memory and peripheral devices to insert wait states into a μPD70616 bus cycle.

V_{DD} [Power Supply]
The V_{DD} pin supplies +5 Volt power to the μPD71611.

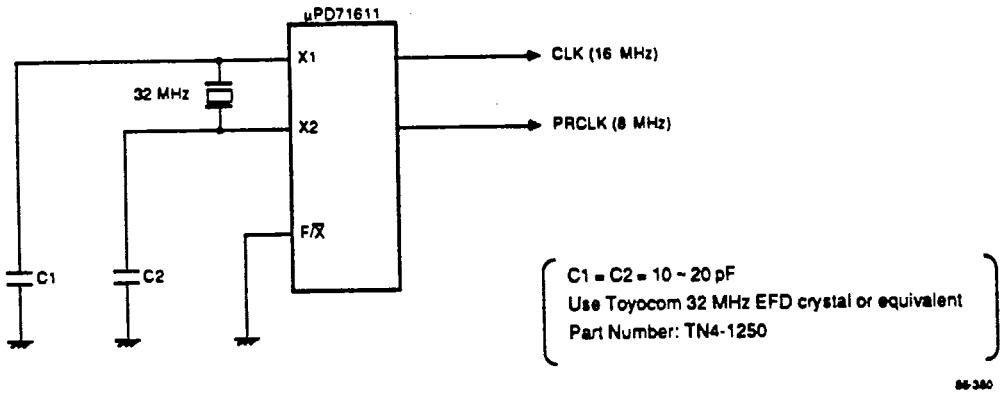
GND [Ground]
The GND pin is the power supply return.

Operational Description

The μPD71611 serves as the system clock generator/driver for the μPD70616 (V60) microprocessor. The primary clock source can be selected from an internal crystal oscillator and fundamental mode crystal or from an external TTL-level clock. The source clock is then divided by two to generate the μPD70616 clock (CLK) and by four to generate the peripheral clock (PRCLK).

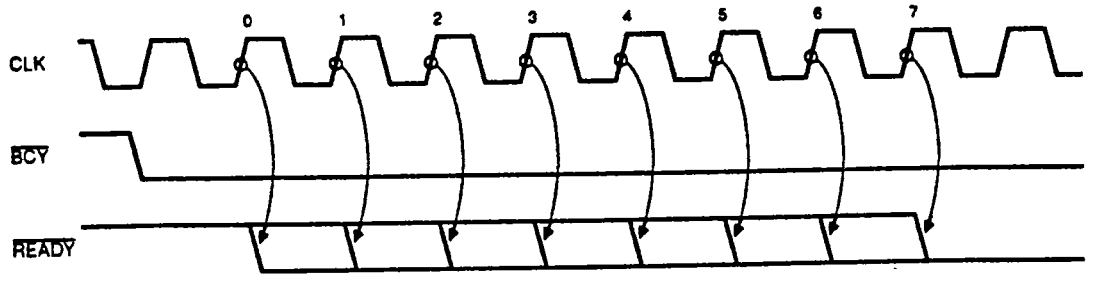
The μPD71611 contains additional logic for synchronization of a reset input and the generation of processor wait states. Figure 1 shows a typical μPD71611 design example using the on-chip clock oscillator logic.

Figure 1. Crystal Oscillator Example



Three different types of wait states are accommodated by the μPD71611. Both synchronous and asynchronous wait ready inputs are available, each with a corresponding enable input. Zero to seven wait states can also be automatically inserted into a bus cycle using the WAIT2–0 inputs.

Figure 2. WAIT2–0 and READY* Timing



WAIT2	0	0	0	0	1	1	1	1
WAIT1	0	0	1	1	0	0	1	1
WAIT0	0	1	0	1	0	1	0	1
Wait States	0	1	2	3	4	5	6	7

μPD71611

Absolute Maximum Ratings

T_A = +25°C

Power Supply Voltage, V_{DD}	−0.5 V to +7.0 V
Input Voltage, V_I	−1.0 V to V_{DD} + 1.0 V
Output Voltage, V_O	−0.5 V to V_{DD} + 0.5 V
Operating Temperature, T_{OPT}	−40°C to +85°C
Storage Temperature, T_{STG}	−65°C to +150°C
Power Dissipation, P_D	500mW

Comment: Exposing the device to stresses above those listed in the Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = +25°C, V_{DD} = 0 V

		Limits			
Parameter	Symbol	Min	Max	Unit	Conditions
Input Capacitance	C_I		10	pf	f = 1 MHz

DC Characteristics

T_A = −40°C to +85°C, V_{DD} = +5 V ±5%

		Limits			
Parameter	Symbol	Min	Max	Unit	Conditions
Input Voltage Low	V_{IL}		0.8	V	
Input Voltage High	V_{IH}	2.2		V	except RESIN*
		2.6		V	RESIN* input
Output Voltage Low	V_{OL}		0.45	V	I_{OL} = 4mA
Output Voltage High	V_{OH}	V_{DD} − 0.4		V	CLK output, I_{OH} = −4mA
		V_{DD} − 0.8		V	except CLK, I_{OH} = −4mA
Input Current	I_I	−1.0	1.0	μA	
RESIN* Hysteresis		0.25		V	
Supply Current (Static)	I_{DD}		200	μA	
Supply Current (Dynamic)	I_{DDdyn}		50	mA	f_{in} = 32 MHz, outputs open

AC Characteristics

T_A = −40°C to +85°C, V_{DD} = +5 V ±5%

		Limits			
Parameter	Symbol	Min	Max	Unit	Conditions
EXFS Cycle Time	t_{CYFS}	28		ns	
EXFS Pulse Width High	t_{PWFSH}	10		ns	2.2 V measurement point
EXFS Pulse Width Low	t_{PWFSL}	10		ns	0.8 V measurement point
OSC Cycle Time	f_{OSC}		32	MHz	
CLK Cycle Time	t_{CYCK}	60		ns	
CLK Pulse Width High	t_{PWCKH}	25		ns	3.0 V measurement point
CLK Pulse Width Low	t_{PWCKL}	25		ns	1.5 V measurement point
CLK Rise Time	t_{LHCK}		5	ns	1.5 V → 3.0 V
CLK Fall Time	t_{HLCK}		5	ns	3.0 V → 1.5 V
CLK Delay from EXFS↓	t_{DCKH}	0	20	ns	CLK↑
CLK Delay from EXFS↓	t_{DCKL}	0	20	ns	CLK↑

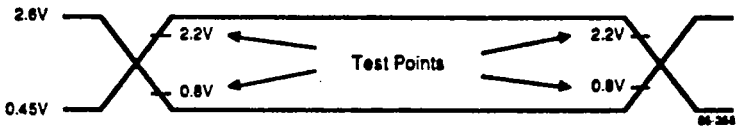
AC Characteristics (cont)

T_A = −40°C to +85°C, V_{DD} = +5 V ±5%

Parameter	Symbol	Limits Min	Limits Max	Unit	Conditions
PRCLK Cycle Time	t_{CYPRK}	120		ns	
PRCLK Pulse Width High	t_{PWPRKH}	t_{CYCK} − 15		ns	
PRCLK Pulse Width Low	t_{PWPRKL}	t_{CYCK} − 15		ns	
PRCLK↑ Delay from CLK↓	t_{DPRKH}		20	ns	
PRCLK↓ Delay from CLK↓	t_{DPRKL}		20	ns	
RESIN* Setup to CLK↓	t_{SRICK}	20		ns	
RESIN* Hold from CLK↓	t_{HCKRI}	0		ns	
RESET* Delay from CLK↓	t_{DCKRS}		10	ns	
SREN* Setup to CLK↑	t_{SSRECK}	20		ns	
SREN* Hold from CLK↑	t_{HCKSRE}	0		ns	
SRDY Setup to CLK↑	t_{SSRYCK}	20		ns	
SRDY Hold from CLK↑	t_{HCKSRY}	0		ns	
AREN* Setup to CLK↓	t_{SARECK}	20		ns	
AREN* Hold from CLK↓	t_{HCKARE}	0		ns	
ARDY Setup to CLK↓	t_{SARYCK}	20		ns	
ARDY Hold from CLK↓	t_{HCKARY}	0		ns	
READY* Output Delay from CLK↑	t_{DCKRDY}		10	ns	READY*↑
			8	ns	READY*↓
BCY* Setup to CLK↑	t_{SBCCK}	15		ns	
BCY* Hold from CLK↑	t_{HCKRE}	5		ns	
WAIT0, 1, 2 Setup to CLK↑	t_{SRYCK}	15		ns	
WAIT0, 1, 2 Hold from CLK↑	t_{HCKRY}	5		ns	
Input Rise Time	t_{RI}		15	ns	0.8 V → 2.2 V
Input Fall Time	t_{FI}		8	ns	2.2 V → 0.8 V
Output Rise Time	t_{RO}		10	ns	0.8 V → 2.2 V
Output Fall Time	t_{FO}		6	ns	2.2 V → 0.8 V

Timing Waveforms

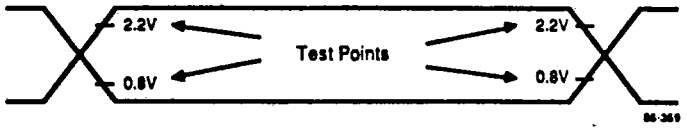
AC Test Input (except RESIN*)



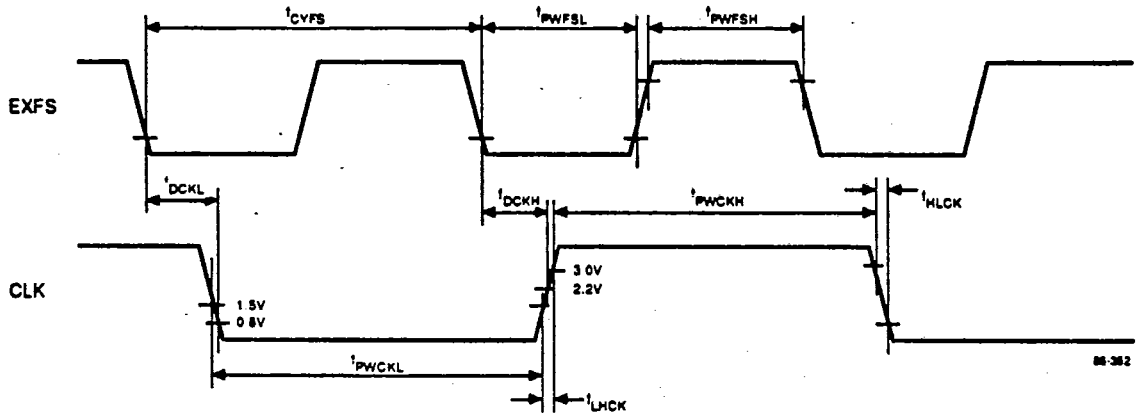
(When $\overline{RESIN}$: Input high level is 3.0V, low level is 0.45V
High level test point is 2.6V, low level test point is 0.8V)

Timing Waveforms (cont)

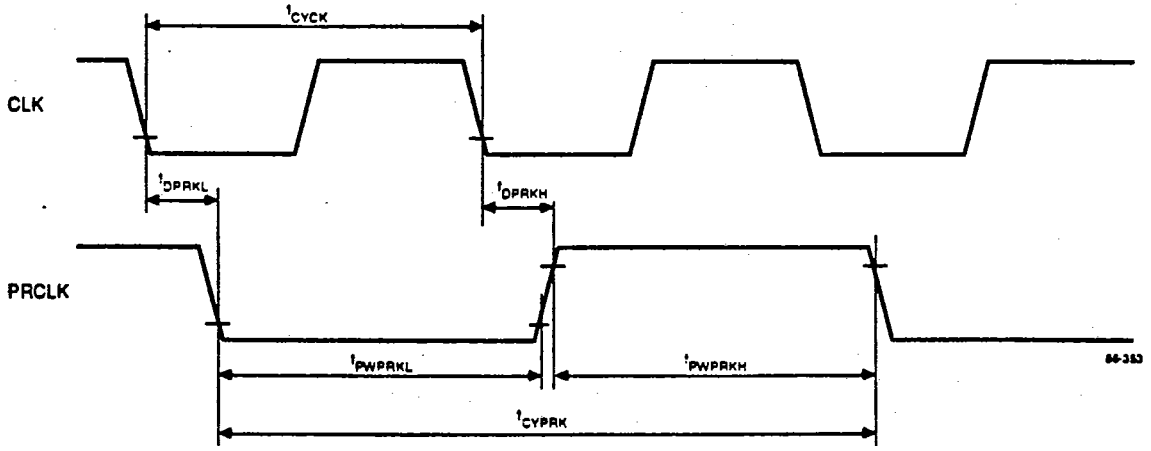
AC Test Output (except CLK)



Clock (CLK) Timing

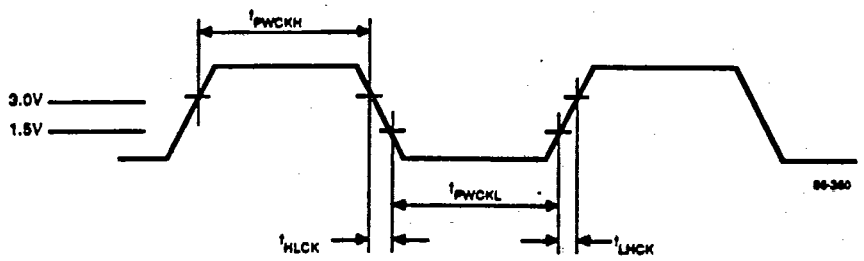


Peripheral Clock (PRCLK) Timing

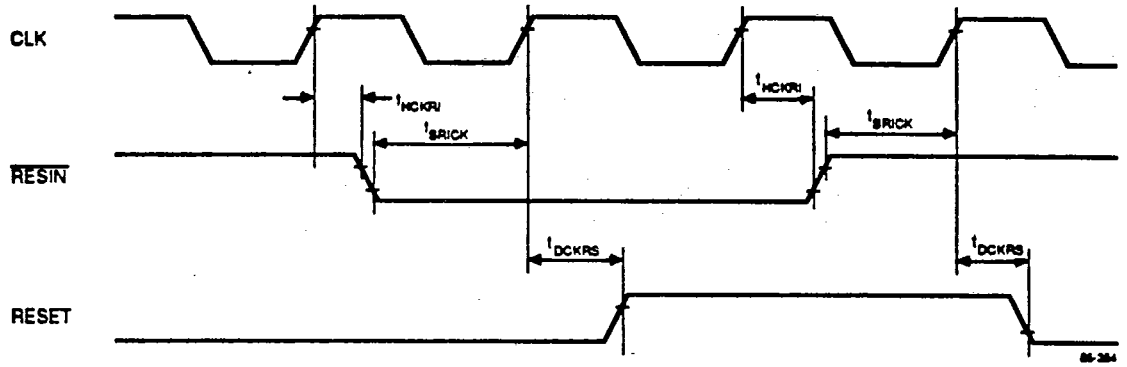


Timing Waveforms (cont)

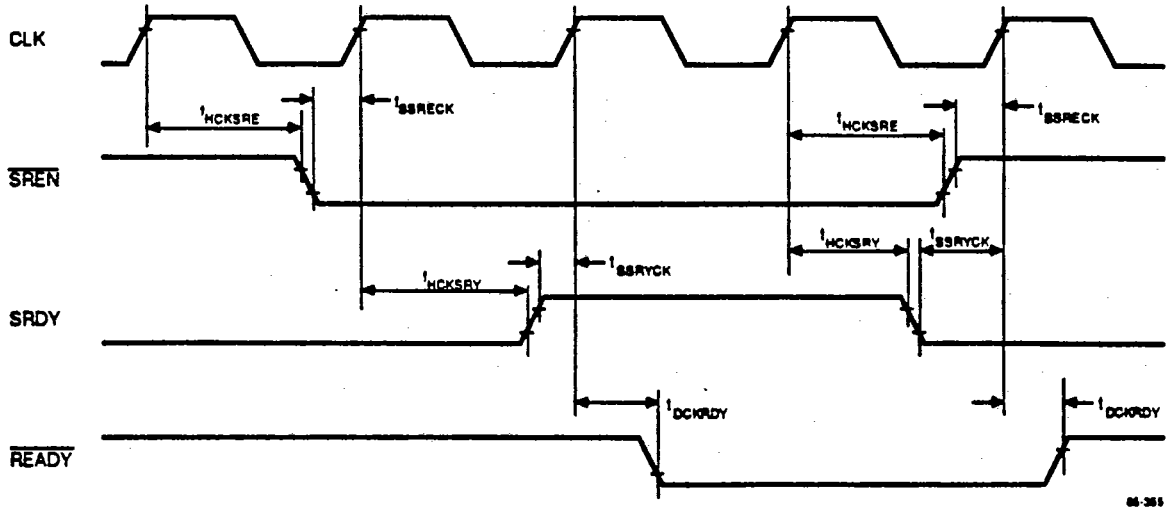
Clock (CLK) Output Timing



Reset Timing

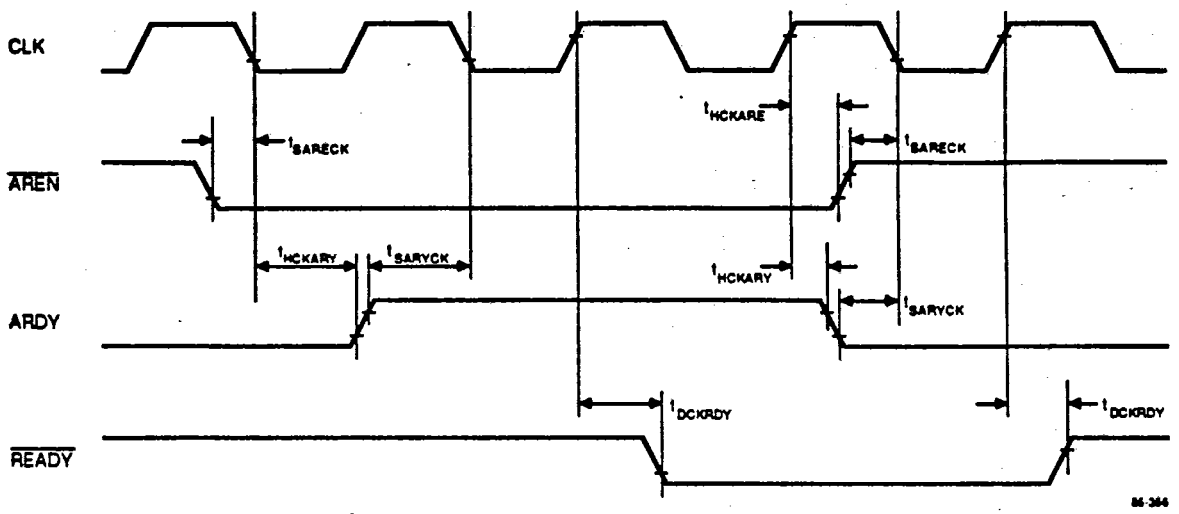


Synchronous Ready Timing

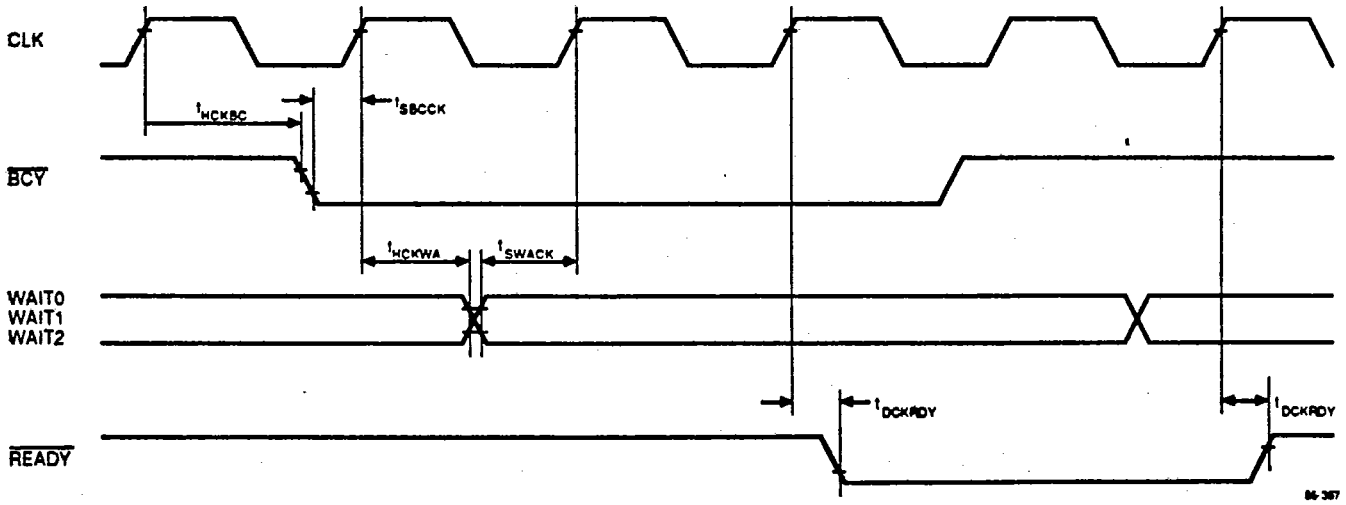


Timing Waveforms (cont)

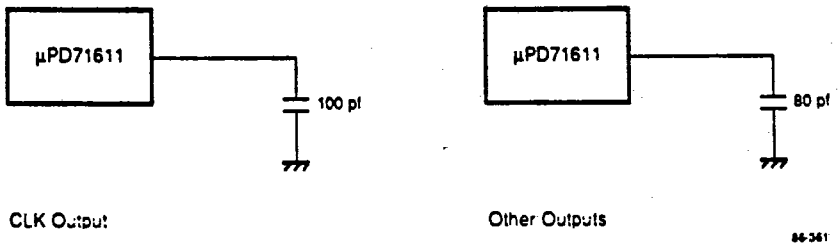
Asynchronous Ready Timing



Wait State Timing

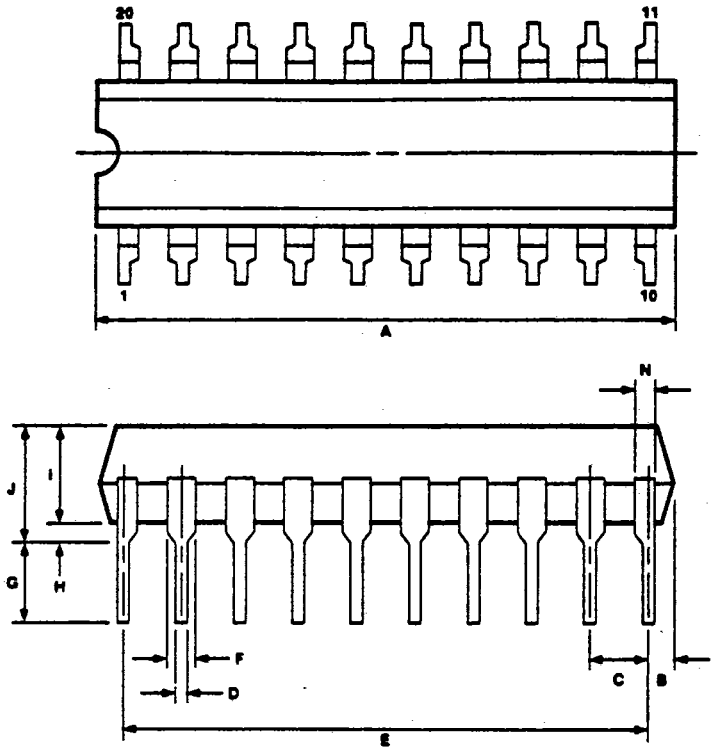


Loading Circuits



Packaging Information

20-Pin Plastic DIP Package (300 mil)



Item	Millimeters	Inches
A	25.40 max	1.0 max
B	1.27 max	.05 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	22.86	.9
F	1.1 min	.043 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.08 max	.2 max
K	7.62 [TP]	.3 [TP]
L	6.4	.252
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$
N	.5 min	.635 min

Notes: 1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

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