μPD70632 (V70) 32-Bit, High-Integration CMOS Microprocessor

NEC Electronics Inc.

T-49-17-32

Description

The μPD70632 (V70™) is the second implementation of NEC's 32-bit V-Series architecture. Like its predecessor, the μPD70616 (V60™), the V70 is a second-generation microprocessor designed for a wide range of applications including personal computers, engineering workstations, office workstations, and industrial controllers. Combining mainframe computer design concepts with NEC's advanced CMOS technology, the 32-bit V-Series architecture's performance is limited only by IC technology. As ICs grow faster, the 32-bit V-Series architecture will permit dramatic increases in performance. All members of this family are upward and downward compatible, allowing a broad spectrum of 16- and 32-bit applications to share a single unified architecture.

The V70 is a 32-bit multitasking virtual memory processor implemented with 385 K transistors in 1.5 μCMOS with AL interconnect. A six-stage pipeline and a synchronous two-clock bus cycle help realize a peak performance of 6 MIPS at 20 MHz. Like the V60, the V70 offers thirty-two 32-bit general-purpose registers and a powerful instruction set optimized for high-level languages and operating systems such as UNIX™ and MS-DOS®. The on-chip demand paged memory management and floating point further increase performance. Functional Redundancy Mode (FRM) addresses fault tolerant applications.

To provide a clean upgrade path from existing 16-bit applications, the V70 can execute V20®/V30® object code in an emulation mode. V30 segmentation is supported in both real and virtual modes, and multiple virtual V30 tasks are possible.

Support for software development and debugging is provided by instruction trace traps and breakpoints. In addition, two hardware address traps support real-time software debugging, a function normally provided only by in-circuit emulators.

Features

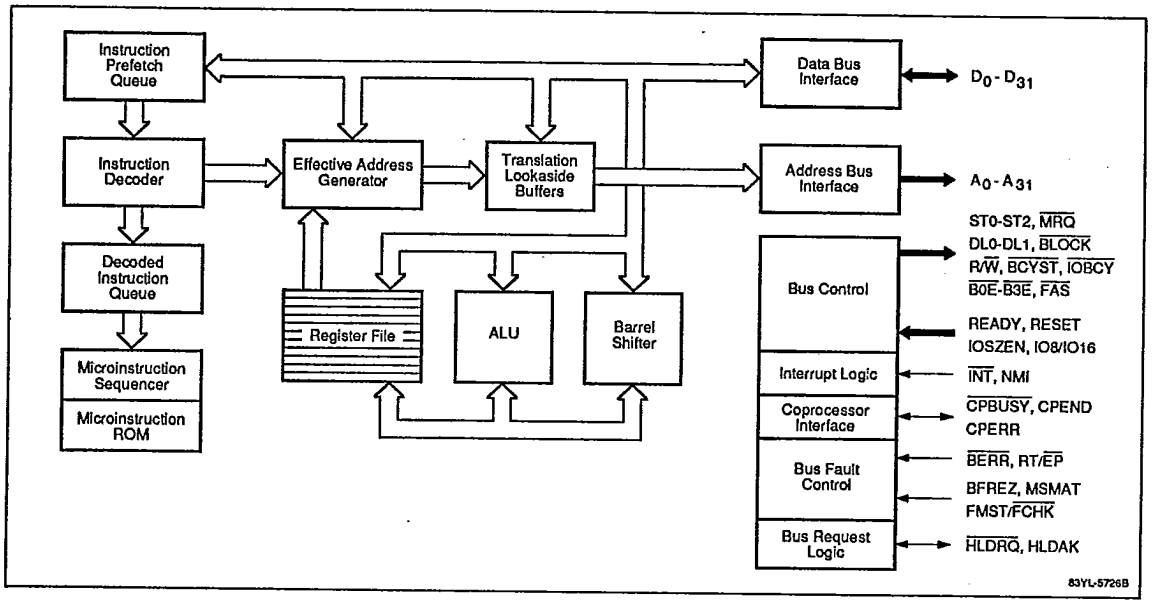
- Same instruction and register sets as V60
  - Thirty-two 32-bit general-purpose registers
  - Pitch orthogonal instruction set supports OS and HLL
  - 21-byte addressing modes and 18-bit addressing modes
- On-chip demand paged memory management unit
  - 4-gigabyte virtual and physical address spaces
  - Three level translation scheme (section/area/page)
  - Four levels of protection
  - Translation Look-aside Buffer (TLB)
- On-chip IEEE754 floating point support
- Supported data types include:
  - 8-, 16-, 32-, 64-bit integer, and 32-, 64-bit floating point
  - 8-, 16-bit characters
  - Bit, bit field and bit string data types
- V20/V30 emulation mode
- Functional Redundancy Monitor (FRM)
- Flexible hardware debugging support
  - Breakpoint trap, instruction trap, address traps
- Six-stage pipeline with multiple internal 32-bit buses
- Fast ALU with 16 scratch registers and 64-bit barrel shifter
- Separate 32-bit address and data buses
- Synchronous bus interface
  - Two-clock cycle data access for 40 Mb/s bandwidth
  - Cycle extendable on a clock-by-clock basis with READY
- Dynamic bus sizing for I/O bus cycles
- Coprocessor interface

Ordering Information

Part Number	Package	Maximum Frequency
μPD70632R	132-pin PGA	20 MHz

The V20 and V30 are registered trademarks of NEC Corporation.
The V60 and V70 are trademarks of NEC Corporation.
UNIX is a trademark of AT&T Bell Laboratories.
MS-DOS is a registered trademark of Microsoft Corporation.

Block Diagram



2