μPD71613

CMOS BUS CONTROLLER

PRELIMINARY INFORMATION

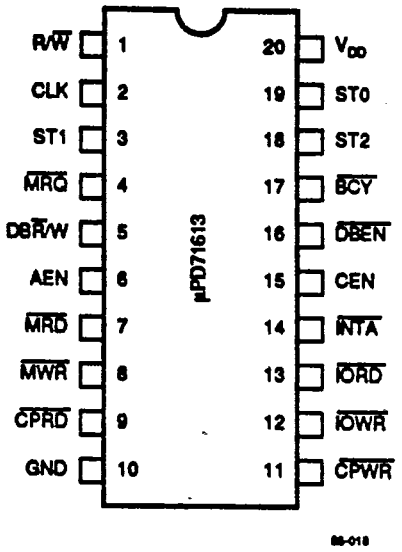
Description

The μPD71613 is a high performance CMOS bus controller for the μPD70616 (V60) microprocessor. The μPD71613 decodes the μPD70616 status outputs and generates the memory, I/O and coprocessor read/write strobes. A separate interrupt acknowledge output is also provided for interfacing to interrupt controllers.

Features

- High output drive (I_{OL} = 16 mA)
- Decodes μPD70616 bus status for
  - memory read/write
  - I/O read/write
  - coprocessor read/write
  - interrupt acknowledge
- 3-state command outputs
- CMOS technology
- 20-pin plastic DIP

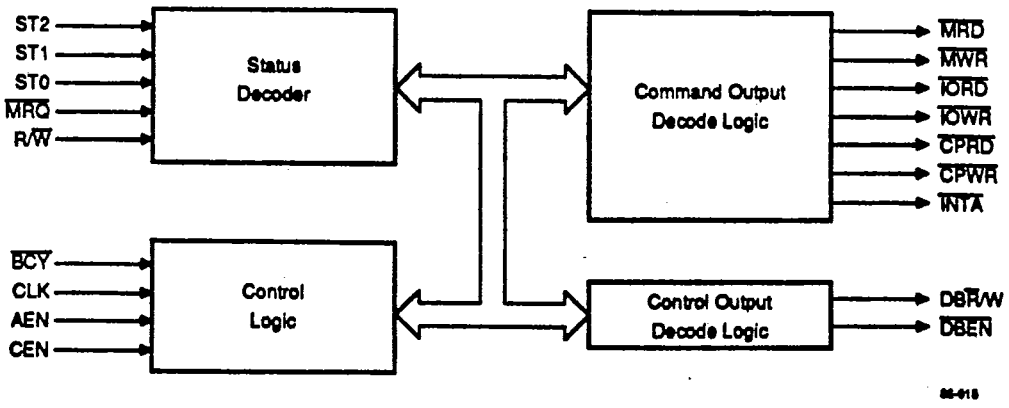
Pin Configuration



Ordering Information

Part Number	Package	Maximum Frequency
μPD71613C	20-pin plastic DIP	16 MHz

Block Diagram



μPD71613

Pin Identification

Symbol		I/O	Function
ST2-ST0	Bus Status	In	μPD70616 bus status inputs
CLK	Clock	In	μPD70616 clock input
MRQ*	Memory Request	In	μPD70616 memory request strobe
R/W*	Read/Write	In	μPD70616 bus cycle direction input
BCY*	Bus Cycle	In	μPD70616 bus cycle active input
AEN	Address Enable	In	Command output buffer control pin
CEN	Command Enable	In	Command output control pin
MRD*	Memory Read	3-state output	Memory read strobe output
MWR*	Memory Write	3-state output	Memory write strobe output
IORD*	I/O Read	3-state output	I/O read strobe output
IOWR*	I/O Write	3-state output	I/O write strobe output
CPRD*	Coprocessor Read	3-state output	Coprocessor read strobe output
CPWR*	Coprocessor Write	3-state output	Coprocessor write strobe output
INTA*	Interrupt Acknowledge	Out	Interrupt acknowledge output
DBEN*	Data Bus Enable	Out	External data bus buffer enable output
DBR*/W	Data Buffer Read/Write	Out	Data bus buffer direction output

Pin Functions

This section describes the operation of the μPD71613 terminals. Inputs and outputs are considered at a logic "0" level when a low level signal is present. Likewise, a logic "1" is represented by a high level signal. Bus states are defined and measured from the rising edge of the clock to the rising edge of the next clock.

ST2-ST0 [Bus Status]..... inputs
The ST2–ST0 inputs are connected to the encoded CPU bus status outputs. The bus status inputs are decoded into the command and control outputs for timing control.

CLK [Clock]..... input
CLK is the μPD70616 system clock from the μPD71611 clock generator.

BCY* [Bus Cycle]..... input
The μPD70616 indicates the start of a new bus cycle by asserting the BCY* output. The μPD71613 uses BCY* to generate the timing for all command and control outputs.

MRQ* [Memory Request]..... input
MRQ* is a μPD70616 output which indicates whether or not the bus cycle is in the memory address space or in some other address space.

R/W* [Read/Write]..... input
R/W* is the bus cycle direction status from the μPD70616.

AEN [Address Enable]..... input
The AEN input is the three-state control for the command output buffers. When AEN is high, all output buffers are enabled and the decoded command is determined by the input status. When AEN is low, all command output buffers are in the high impedance state.

CEN [Command Enable]..... input
CEN controls the DBEN* and all command outputs. When CEN is high, all outputs are enabled and controlled by the status inputs. When CEN is low, DBEN* and the command outputs are forced to the inactive state.

MRD* [Memory Read]..... output
MRD* is an active low three-state output strobe used to read data from memory.

MWR* [Memory Write]..... output
MWR* is an active low three-state output strobe used to write data to memory.

IORD* [I/O Read]..... output
IORD* is an active low three-state output strobe used to read data from a peripheral device.

IOWR* [I/O Write]..... output
IOWR* is an active low three-state output strobe used to write data to a peripheral device.

CPRD* [Coprocessor Read]..... output
CPRD* is an active low three-state output strobe used to read data from a coprocessor device.

CPWR* [Coprocessor Write]..... output
CPWR* is an active low three-state output strobe used to write data to a coprocessor.

INTA* [Interrupt Acknowledge]..... output
The INTA* output is used to indicate to interrupt controllers that an interrupt acknowledge bus cycle is taking place. The selected interrupt controller is responsible for supplying the interrupt vector.

DBEN* [Data Buffer Enable]..... output
DBEN* is used to enable the three-state output buffers of the data bus transceivers. This output is only asserted during valid μPD70616 bus cycles.

DBR*/W [Data Buffer Read/Write]..... output
This output controls the direction of the external data bus transceivers. When DBR*/W is high, data will be transferred from the μPD70616 local bus to an I/O or memory location. When DBR*/W is low, data will be transferred from memory or I/O peripherals to the μPD70616 local bus.

V_{DD} [Power Supply]
The V_{DD} pin supplies +5 Volt power to the μPD71613.

GND [Ground]
The GND pin is the power supply return.

Operational Description

The μPD71613 serves as the system bus controller for the μPD70616 (V60) microprocessor. The μPD71613 monitors the μPD70616 status (ST2–ST0), memory request (MRQ*) and read/write (R/W*) outputs and during valid bus cycles (determined by the μPD70616 BCY* output), drives the command and control outputs. Command outputs consist of the memory, I/O, coprocessor and interrupt acknowledge strobe signals. Control outputs are the data buffer enable and data buffer direction signals.

Figure 1 depicts a typical μPD70616 system design using both the μPD71613 and the μPD71611 clock generator. Table 1 contains a state table of the command and control outputs.

Figure 1. Basic System Configuration

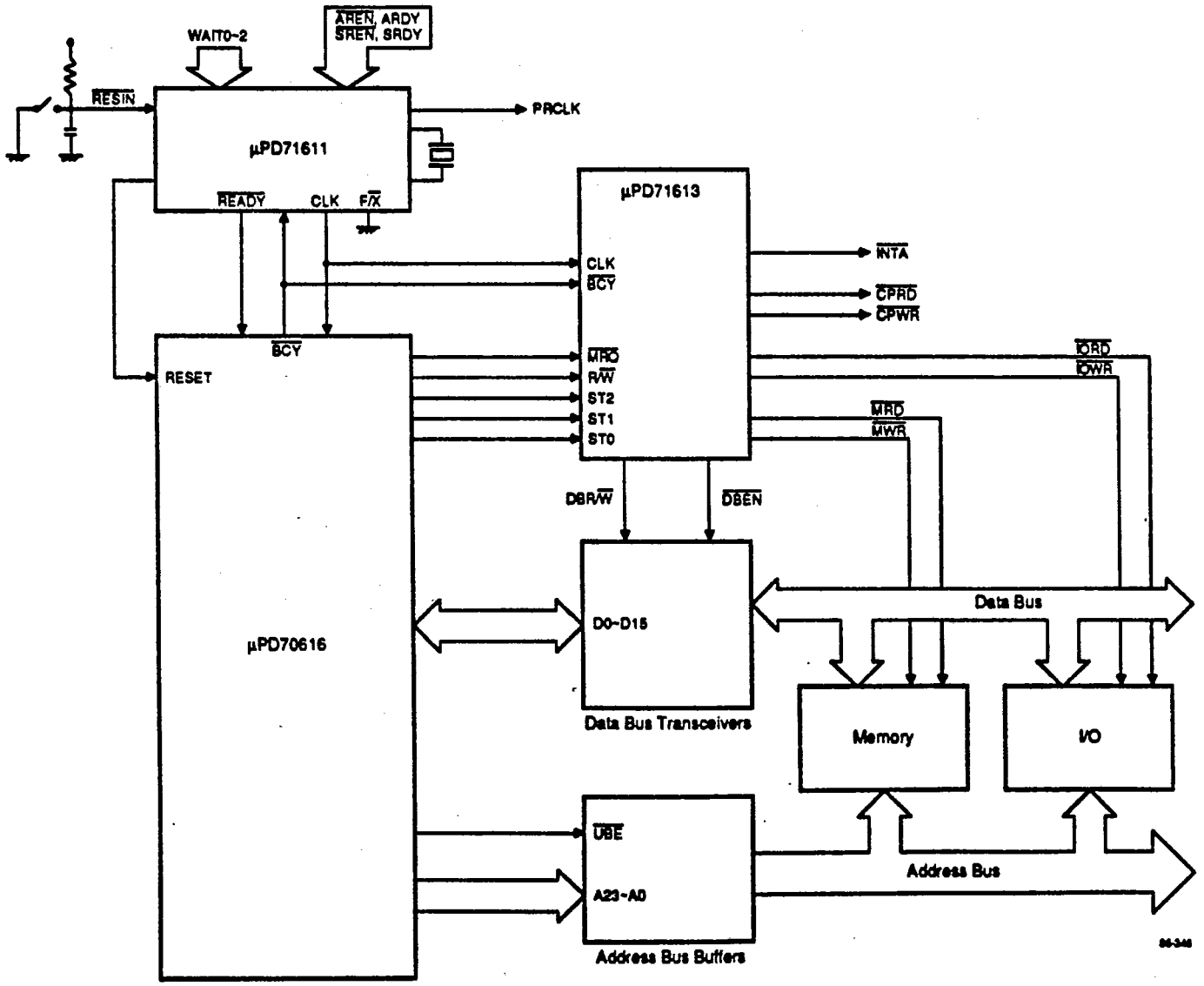


Table 1. Command and Control Output State Table

$\overline{MRQ}$	R/$\overline{W}$	Status			Bus Cycle	Command Outputs	Control Outputs	
		ST2	ST0	ST1			$\overline{DBEN}$	DB$\overline{R}$/W
0	0	0	0	0	Coprocessor Memory Write	$\overline{MWR}$, $\overline{CPRD}$	0	1
		0	0	1	String Mode Memory Write	$\overline{MWR}$	0	1
		0	1	0	Memory Write with Short Pass	$\overline{MWR}$	0	1
		0	1	1	Single Mode Memory Write	$\overline{MWR}$	0	1
		1	0	0	Single Mode Memory Write	$\overline{MWR}$	0	1
		1	0	1	Translation Table Memory Write	$\overline{MWR}$	0	1
		1	1	0	Translation Table Memory Write	$\overline{MWR}$	0	1
		1	1	1	Translation Table Memory Write	$\overline{MWR}$	0	1
	1	0	0	0	Coprocessor Memory Read	$\overline{MRD}$, $\overline{CPWR}$	0	0
		0	0	1	String Mode Memory Read	$\overline{MRD}$	0	0
		0	1	0	String Mode Memory Read	$\overline{MRD}$	0	0
		0	1	1	Single Mode Memory Read	$\overline{MRD}$	0	0
		1	0	0	System Base Table Access	$\overline{MRD}$	0	0
		1	0	1	Translation Table Access	$\overline{MRD}$	0	0
		1	1	0	Demand Mode Instruction Fetch	$\overline{MRD}$	0	0
		1	1	1	Instruction Prefetch	$\overline{MRD}$	0	0
1	0	0	0	0	Coprocessor Write	$\overline{CPWR}$	0	1
		0	0	1	String Mode I/O Write	$\overline{IOWR}$	0	1
		0	1	0	Reserved	–	0	1
		0	1	1	Single Mode I/O Write	$\overline{IOWR}$	0	1
		1	0	0	Halt Acknowledge	–	1	1
		1	0	1	Halt Acknowledge	–	1	1
		1	1	0	None	–	0	1
		1	1	1	Reserved	–	0	1
	1	0	0	0	Coprocessor Read	$\overline{CPRD}$	0	0
		0	0	1	String Mode I/O Read	$\overline{IORD}$	0	0
		0	1	0	Reserved	–	0	0
		0	1	1	Single Mode I/O Read	$\overline{IORD}$	0	0
		1	0	0	Halt Acknowledge	–	1	0
		1	0	1	Halt Acknowledge	–	1	0
		1	1	0	Interrupt Acknowledge	$\overline{INTA}$	0	0
		1	1	1	Reserved	–	0	0

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"0" is a logic low level, "1" is a logic high level

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Absolute Maximum Ratings

T_A = +25°C

Power Supply Voltage, V_{DD}	–0.5 V to +7.0 V
Input Voltage, V_I	–1.0 V to V_{DD} + 1.0 V
Output Voltage, V_O	–0.5 V to V_{DD} + 0.5 V
Operating Temperature, T_{OPT}	–40°C to +85°C
Storage Temperature, T_{STG}	–65°C to +150°C
Power Dissipation, P_D	500 mW

Comment: Exposing the device to stresses above those listed in the Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = +25°C, V_{DD} = 0 V

		Limits			
Parameter	Symbol	Min	Max	Unit	Conditions
Input Capacitance	C_I		12	pf	f = 16 MHz

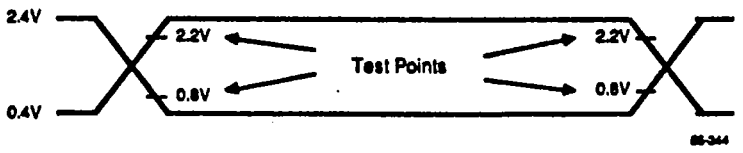
DC Characteristics

T_A = –40°C to +85°C, V_{DD} = +5 V ±10%

		Limits			
Parameter	Symbol	Min	Max	Unit	Conditions
Input Voltage High	V_{IH}	2.2		V	
Input Voltage Low	V_{IL}		0.8	V	
Output Voltage High	V_{OH}	V_{DD} – 0.8		V	Command outputs, I_{OH} = –4mA
		V_{DD} – 0.8		V	Control outputs, I_{OH} = –4mA
Output Voltage Low	V_{OL}		0.45	V	Command outputs, I_{OL} = 16mA
			0.45	V	Control outputs, I_{OL} = 8mA
Input Current	I_I	–1.0	1.0	μA	V_I = V_{DD}, V_{SS}
3-state Output Leakage Current	I_{OFF}	–10	10	μA	
Static Supply Current	I_{DD}		80	μA	V_I = V_{DD}, V_{SS}
Dynamic Supply Current	I_{DDdyn}		30	mA	f_{in} = 16 MHz

Timing Waveforms

AC Input/Output Test



AC Characteristics

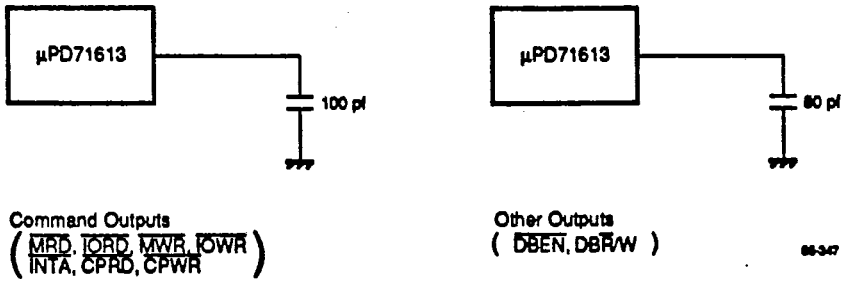
T_A = −40°C to +85°C, V_{DD} = +5 V ±10%

Output Pin Load Capacitance: 100 pf

Parameter	Symbol	Limits Min	Limits Max	Unit	Conditions
CLK Cycle Time	t_{CYCK}	60		ns	
CLK Pulse Width High	t_{PWCKH}	25		ns	
CLK Pulse Width Low	t_{PWCKL}	25		ns	
ST2-ST0, MRQ*, R/W* Setup to CLK↑	t_{SSTCK}	15		ns	
ST2-ST0, MRQ*, R/W* Hold from CLK↑	t_{HCKST}	5		ns	
BCY* Setup to CLK↑	t_{SBYCK}	15		ns	
BCY* Hold from CLK↑	t_{HCKBY}	5		ns	
Command Active Delay from CLK↑	t_{DCKCML}	3	15	ns	
Command Inactive Delay from CLK↓	t_{DCKCMH}	3	15	ns	
Command Inactive Delay from BCY*↑	t_{DBYCMH}	3	15	ns	
Command Output On Delay from AEN↑	t_{DAECM}	3	15	ns	
Command Active Delay from AEN↑	t_{DAECML}	80	160	ns	
Command Output Float Delay from AEN↓	t_{FAECM}		40	ns	
Command Active Delay from CEN↑	t_{DCECML}	3	15	ns	
Command Inactive Delay from CEN↓	t_{DCECMH}	3	15	ns	
DBEN* Inactive Delay from CLK↑	t_{DCKDE}	3	15	ns	
DBEN* Active Delay from AEN↑	t_{DAEDE}	3	15	ns	
DBEN* Active Delay from CEN↑	t_{DCEDEL}	3	15	ns	
DBEN* Inactive Delay from CEN↓	t_{DCEDEH}	3	15	ns	
DBR*/W↑ Delay from CLK↑	t_{DCKDM}	3	15	ns	
DBR*/W↓ Delay from R/W*	t_{DRWDM}	3	15	ns	
Input Rise Time	t_{RI}		12	ns	0.8 V → 2.2 V
Input Fall Time	t_{FI}		8	ns	2.2 V → 0.8 V
Output Rise Time	t_{RO}		10	ns	0.8 V → 2.2 V
Output Fall Time	t_{FO}		6	ns	2.2 V → 0.8 V

Timing Waveforms (cont)

Loading Circuits

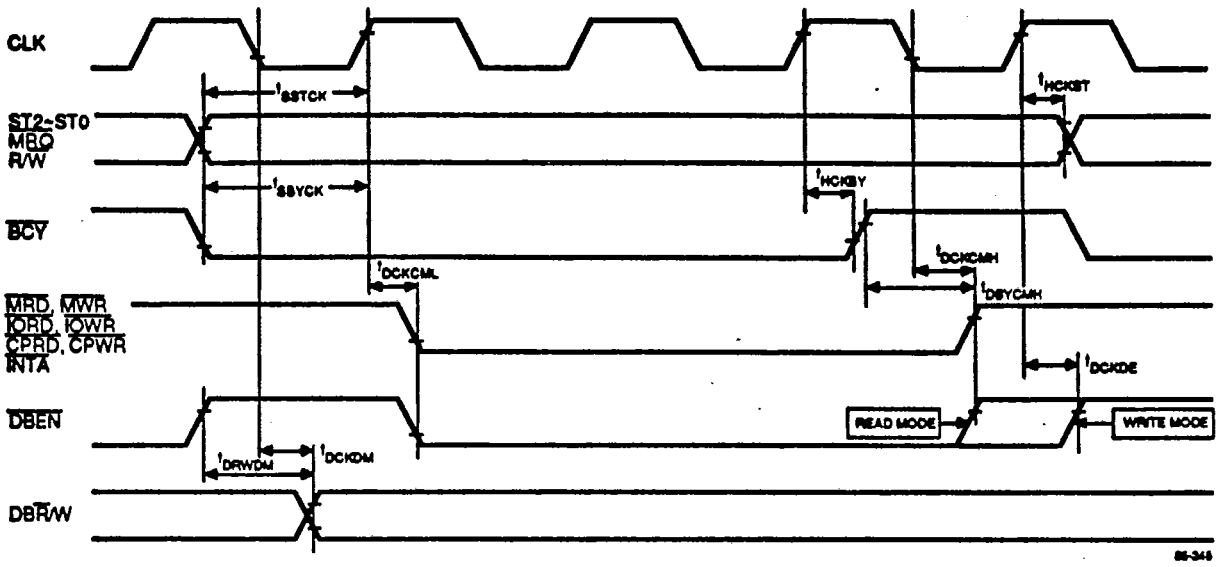


Command Outputs
($\overline{MRD}$, $\overline{IORD}$, $\overline{MWR}$, $\overline{IOWR}$ $\overline{INTA}$, $\overline{CPRD}$, $\overline{CPWR}$)

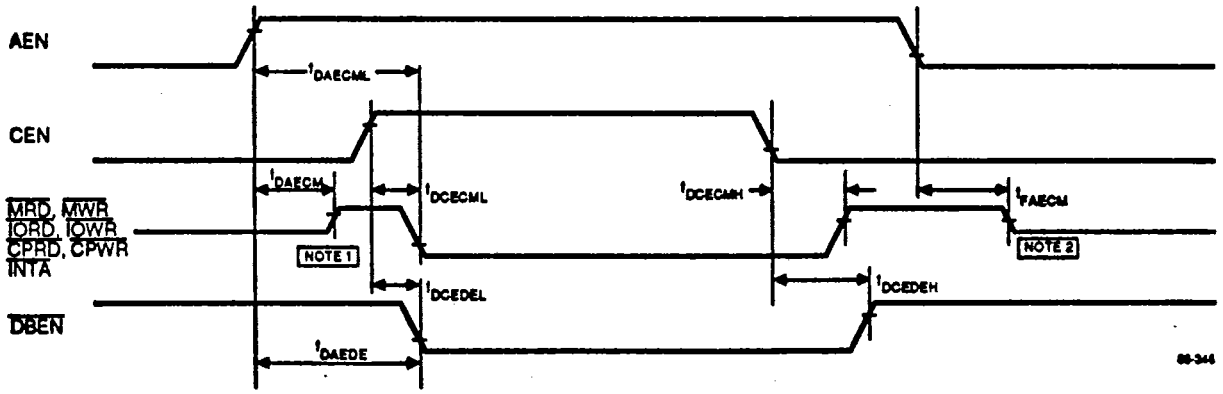
Other Outputs
($\overline{DBEN}$, DB$\overline{R/W}$)

Timing Waveforms (cont)

Command/Control Output Timing



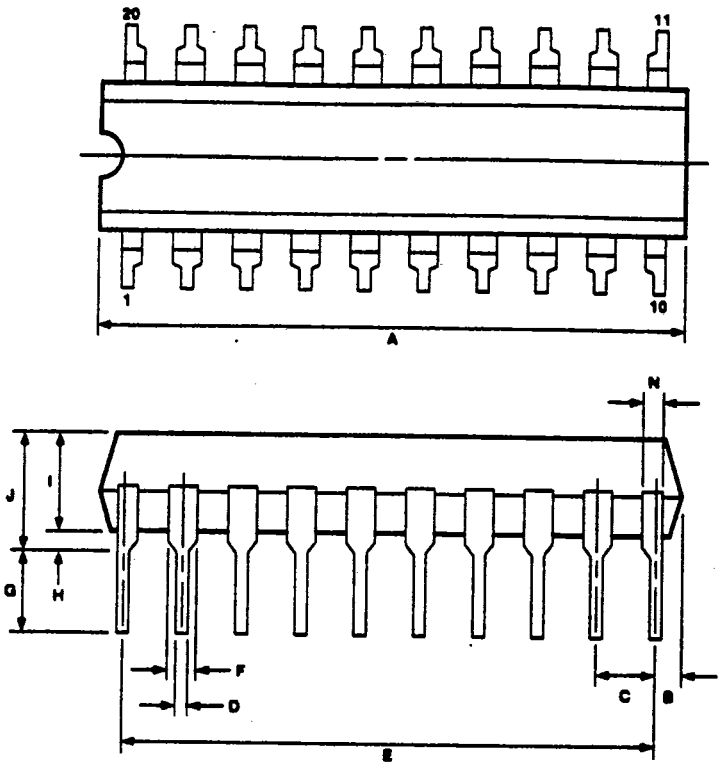
Command Output Timing

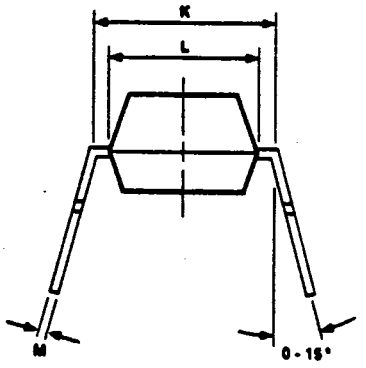


Note 1. This measurement point is 0.1V above the float voltage.
Note 2. This measurement point is 0.1V below the high level output voltage. For a low level output,, the measurement point is 0.1V above the low level output voltage.

Packaging Information

20-Pin Plastic DIP Package (300 mil)





Item	Millimeters	Inches
A	25.46 max	1.0 max
B	1.27 max	.05 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	22.86	.9
F	1.1 min	.043 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.08 max	.2 max
K	7.62 [TP]	.3 [TP]
L	6.4	.252
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$
N	.9 min	.035 min

Notes: 1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

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